

# PI3DPX1202A

## Low power DisplayPort 1.2 Redriver with DDC/AUX CH Switch

### Description

PI3DPX1202A is DisplayPort 1.2 standard compliant, very low power DP Redriver.

The device can read the Aux-channel Link Training (LT) Swing and Pre-emphasis data between Transmitter and Receiver, configure the output swing / Pre-emphasis, and automatically calculates EQ based on Swing/Pre-emphasis LT values through the built-in Aux listener. EQ can program by the I2C serial interface.

The device can reduce signal jitter caused by transmission line effects, and compensate for the PCB-related frequency and switching-related loss to provide optimum DP performance between the link.

### Features

- ➔ Dual mode DisplayPort Redriver, DP 1.2 Specification compliant
- ➔ Support all 1.62 / 2.7 / 5.4 Gbps data rate with DDC/ Aux signal switching
- ➔ High speed inputs with internal 50 Ohm pull-down
- ➔ Ultra Low-power design
- ➔ Dual mode DisplayPort Input/Output with TMDS clock Frequencies up to 340 MHz
- ➔ Aux Listener support link training and configure output level, pre-emphasis setting during link initialization. Aux Listener supports "sink Request test mode"
- ➔ Pseudo-adaptive equalization based on signal level and pre-emphasis setting in Aux register
- ➔ CNTRL provides pin control EQ, Output Voltage Swing and Pre-Emphasis
- ➔ DP and TMDS output mode selection with Cable Detection pins
- ➔ Support Hot Plug Detect and Cable Detect function
- ➔ Individual lane power down automatically when no DP signal present
- ➔ DP redriver enter power down state to reduce current consumption when sink device deserted
- ➔ Power Supply : 3.3V

- ➔ ESD HBM protection 2kV
- ➔ Package: 48-pin TQFN (7x7mm)

### Typical Applications

- ➔ Notebook, AIO and Desktop PCs
- ➔ Graphic Cards

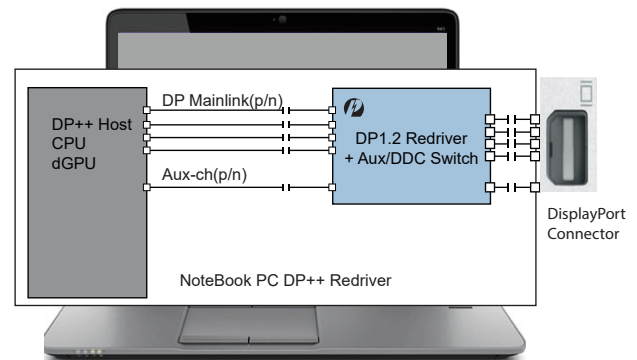


Figure: NB Application Block Diagram

### Ordering Information

| Ordering Code      | Package Code | Package Type   |
|--------------------|--------------|--|
| PI3DPX1202A2 ZBEX  | ZB           | 3.3V only power, Pb-free & Green, 48-pin TQFN, Tape/Reel                         |
| PI3DPX1202A2 ZBIEX | ZB           | Industrial Temperature, 3.3V only power, Pb-free & Green, 48-pin TQFN, Tape/Reel |
| PI3DPX1202A1 ZBEX  | ZB           | 3.3V only power, Pb-free & Green, 48-pin TQFN, Tape/Reel                         |
| PI3DPX1202A1 ZBIEX | ZB           | Industrial Temperature, 3.3V only power, Pb-free & Green, 48-pin TQFN, Tape/Reel |

Suffix: I = Industrial Temperature, E = Pb-free and Green, X = Tape/Reel.

## 2. General Information

### 2.1 Revision History

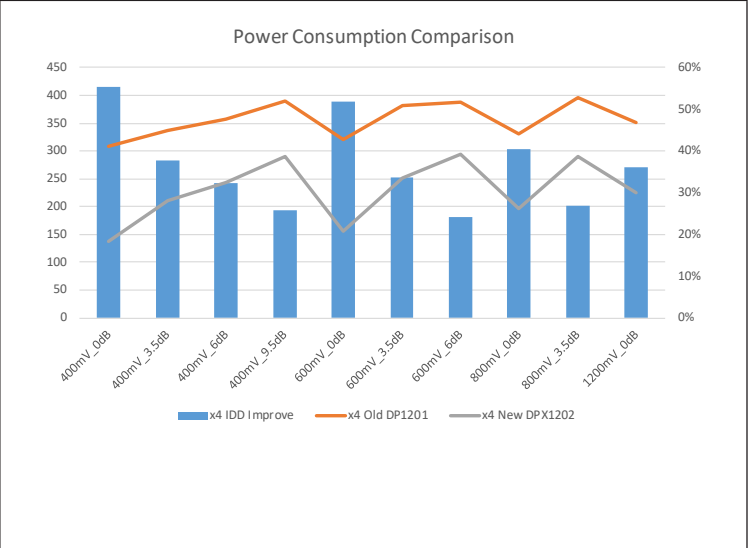
| Revision | Changes   |
|----------|---|
| Mar 2017 | Release. Always Automatic EQ control through Aux channel listener or I2C programmable control mode support  |
| Apr 2017 | Ch3: Functional description to simplify.<br>Ch4: Min temp changed 0 to -40 deg C for I-temp support. ICC measurement data updated with different Pre-emphasis and Voltage swing setting condition.<br>Ch5: Add Aux-listener redriver latency information & power mW comparison data |
| May 2017 | Ch3: Improved Functional description  |
| Jun 2017 | Power-up / Reset timing added in functional session<br>Eye waveforms by Pre channel length added in application session   |
| Oct 2017 | I-temp ordering part number added (p1), IIL Min changed -0.6 from GND(p31)  |

### 2.2 Similar Products Selection Guide

|                | PI3DPX1202A2  | PI3DPX1202A1   | PI3EQXDP1201   | PI3DPX1203B  |
|----------------|---|--|--|--|
| Version        | DP 1.2, DP++ 1.2  | DP 1.2, DP++1.2  | DP 1.2, DP++1.2  | DP 1.4, DP++ 1.4   |
| Recommendation | New DP 1.2 Design Power, BOM sensitive system   | PI3EQXDP1201 Pin-to-pin replacement  | Not recommend  | Variable Frame Rate application, latency critical system<br>DP1.4 Data Rate system |
| Redriver Type  | Limiting-type Redriver, Depend Aux listener for automatic Device setting control  | Same as PI3DPX1202A1   | Same as PI3DPX1202A1                                   | Linear-type Redriver<br>No need Aux listener for Automatic Device setting control  |
| EQ mode        | Auto, I2C and Fixed EQ setting  | Auto EQ, I2C setting only  | Auto, I2C and Fixed EQ setting                         | EQ setting 4-bit with Pin or I2C mode.   |
| Auto_EQ pin    | Auto EQ pin: Tri-state mode to control Auto EQ/ Fixed EQ and I2C mode<br>0: Disable<br>1: Enable<br>M: Pin-control EQ mode        | No Auto EQ pin control pin. Internally Pull-Up to VDD for always for Pin-to-Pin with PI-3EQXDP1201 | Internal 100kΩ pull up.<br>0 = Fixed EQ<br>1 = Auto EQ | None   |
| New Features   | Low-power design 136mA @ 400mV, 0dB setting.<br>Increase Aux Listener FIFO size.<br>Drop-in Pin out compatible with PI3EQXDP1201. |  | 300mA @ 400mV, 0dB setting                             | Latency Free, Not blocking linked channels and boost Receiver DFE performance      |
| Availability   | Production  | Production   | EOL  | Production   |

### 2.3 Power Consumption Comparison

| Swing, Preemph setting       | x4 IDD Improve | x4 Old DP1201 | x4 New DPX1202 | Units     |
|------------------------------|----------------|---------------|----------------|-----------|
| 400mV_0dB                    | 55%            | 309           | 138            | mA        |
| 400mV_3.5dB                  | 38%            | 338           | 211            | mA        |
| 400mV_6dB                    | 32%            | 358           | 242            | mA        |
| 400mV_9.5dB                  | 26%            | 390           | 289            | mA        |
| 600mV_0dB                    | 52%            | 321           | 155            | mA        |
| 600mV_3.5dB                  | 34%            | 381           | 252            | mA        |
| 600mV_6dB                    | 24%            | 388           | 294            | mA        |
| 800mV_0dB                    | 40%            | 332           | 197            | mA        |
| 800mV_3.5dB                  | 27%            | 396           | 289            | mA        |
| 1200mV_0dB                   | 36%            | 351           | 225            | mA        |
| <b>Average Total Current</b> | <b>36%</b>     | <b>356</b>    | <b>229</b>     | <b>mA</b> |
| <b>Average Total Power</b>   | <b>36%</b>     | <b>1175</b>   | <b>756</b>     | <b>mW</b> |



### 2.4 Output Eye Waveforms with different Pre-channel length

Output Eye Opening with Input Equalization, 5.4 Gbps, Vdd=3.3V, 25C with PRBS 2<sup>7</sup>-1 pattern, Input/Output Swing=800mVd

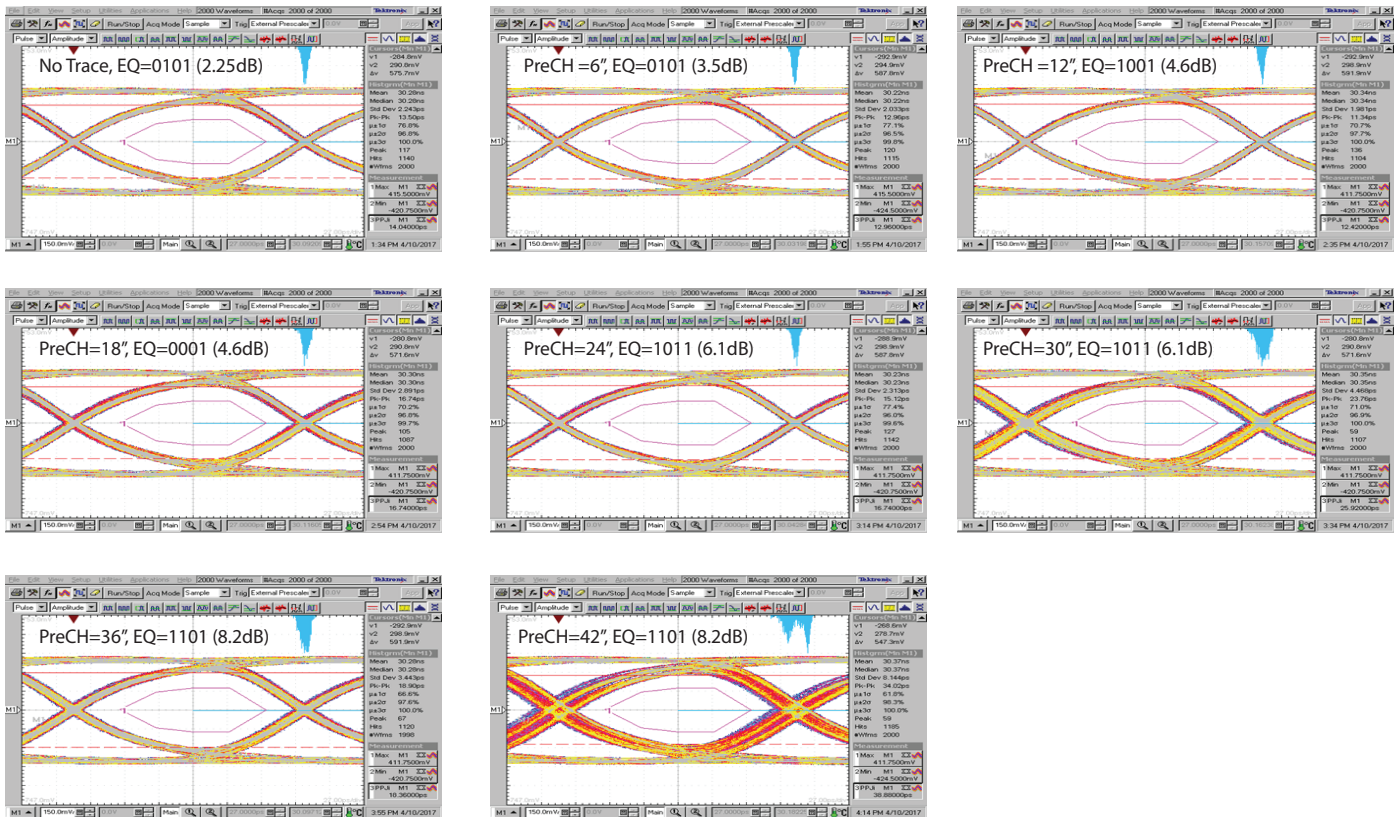


Figure 2-1: Pre-channel length/insertion loss and EQ compensation

## 2.5 Related Products

| Part Numbers                | Products Description  |
|-----------------------------|---|
| Retimers / Jitter Cleaner   |   |
| PI3HDX2711B                 | HDMI 2.0 and DP++ Retimer (Jitter Cleaner)  |
| PI3HDX711B                  | HDMI 1.4 and DP++ ReTimer (Jitter Cleaner)  |
| Redrivers                   |   |
| PI3DPX1203B                 | DisplayPort 1.4 Redriver for Source/Sink/Cable Application, Linear-type                         |
| PI3HDX1204B1                | HDMI 2.0 Redriver (DP++ Level Shifter), High EQ, place near to the source-side, Limiting type   |
| PI3HDX1204E                 | HDMI 2.0 Linear Redriver (DP++ Level Shifter) , Link transparent, place near to the sink-side   |
| PI3DPX1207B                 | DisplayPort 1.4 Alt Type-C Redriver, 8.1 Gbps and USB3.1 10 Gbps, Link Transparent              |
| PI3DPX1202A                 | Low Power DisplayPort 1.2 Redriver with built-in AUX Listener, Limiting-type                    |
| PI3HDX511F                  | High EQ HDMI 1.4b Redriver and DP++ Level Shifter for Sink/Source Application, Limiting-type    |
| Active Switches & Splitters |   |
| PI3DPX1205A                 | DisplayPort 1.4 Alt Type-C Mux Redriver, 8.1 Gbps and USB3.1 10 Gbps, Link Transparent          |
| PI3HDX231                   | HDMI 2.0 3:1 ports Mux Redriver, Linear-type  |
| PI3HDX414                   | HDMI 1.4b 1:4 Demux Redriver & Splitter for 3.4 Gbps Application, Limiting-type                 |
| PI3HDX412BD                 | HDMI 1.4b 1:2 Demux Redriver & Splitter for 3.4 Gbps Application, Limiting-type                 |
| PI3HDX621                   | HDMI 1.4 Redriver 2:1 Active Switch with built-in ARC and Fast Switching support, Limiting-type |

## 2.6 Product Status Definition

| Product Status               |                     | Definition  |
|------------------------------|---------------------|---|
| 0 - Advanced Information     | In Design           | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.   |
| 1 - Preliminary              | Engineering Samples | Datasheet contains preliminary data; supplementary data will be published at a later date. Diodes Incorporated reserves the right to make changes at any time without notice to improve design. |
| 2 - No Identification Needed | Full Production     | Datasheet contains final specifications. Diodes Incorporated reserves the right to make changes at any time without notice to improve the design.   |
| 3 - Obsolete                 | Not In Production   | Datasheet contains specifications on a product that is discontinued by Diodes Incorporated. The datasheet is for reference information only.  |

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### 3. Package Pin-out Information

#### 3.1 Package Pin-out

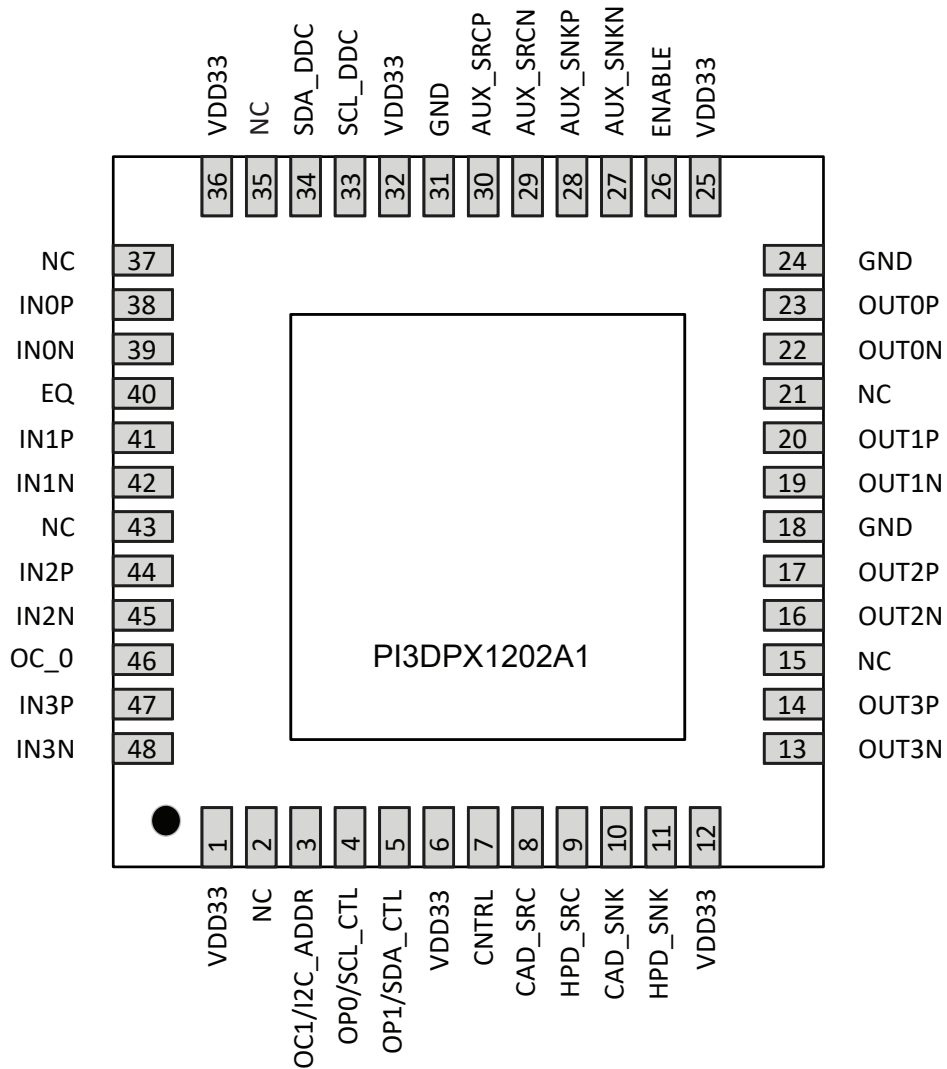


Figure 3-1: PI3DPX1202A1 Package Pin-out



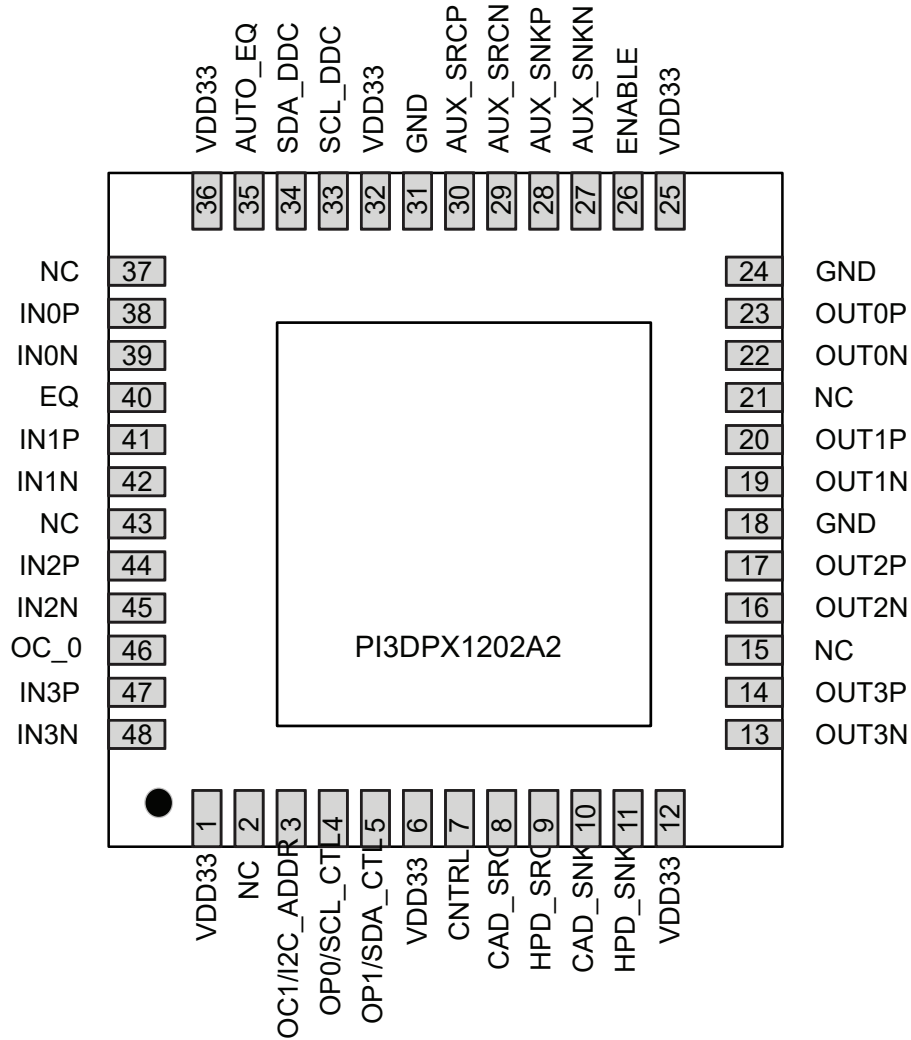


Figure 3-2: PI3DPX1202A2 Package Pin-out

### 3.2 Pin Description

| Pin # | Pin Name                  | I/O    | Description   |
|-------|---------------------------|--------|---|
| 35    | AUTO_EQ<br>(PI3DPX1202A2) | Input  | Auto EQ Selection pin. Auto EQ has 3 modes. EQ (Pin 40) can select one of the Auto EQ modes. This pin is internally biased to 50% of VDD33 ( $M = VDD/2$ ).<br>"1": Enable<br>"0": Disable<br>"M": Please refer to the Functional Truth table |
| 35    | NC<br>(PI3DPX1202A1)      | NC     | Non connection pin. Internally Pull-up tied to 3.3V VDD. This pin does not bond-out to package.   |
| 1     | VDD33                     | Power  | 3.3V power supply   |
| 2     | NC                        | NC     | Do Not Connect. Leave this pin floating.  |
| 3     | OC1/I2C_ADDR              | Shared | Shared pin. Pulled-up internally with 100 k $\Omega$<br>"I2C_ADDR": SMBus control address pin<br>"OC1": Voltage Swing control bit 1   |
| 4     | OP0/SCL_CTL               | Shared | Shared pin. Internally pulled-up with 100 k $\Omega$<br>"SCL_CTL": SMBus Clock<br>"OP0": Pre-emphasis control bit 1   |
| 5     | OP1/SDA_CTL               | Shared | Shared pin. Internally pulled-up with 100 k $\Omega$<br>"SDA_CTL": SMBus Data<br>"OP1": Pre-emphasis control bit 0  |
| 6     | VDD33                     | Power  | 3.3V power supply   |
| 7     | CNTRL                     | Input  | Primary Control Pin for Auto-configuration or Fine-tuning boost mode<br>"0": SMBus mode<br>"M": Aux listener mode (Default)<br>"1": Pin strap mode.   |
| 8     | CAD_SRC                   | Output | Cable Adapter Detection pin from source side<br>"0": no cable adapter; enable DP redriver mode with AUX listening and link training active<br>"1": Installed cable adapter; enable TMDS redriver mode and disable AUX interception            |
| 9     | HPD_SRC                   | Output | Hot Plug detect pin to source-side. 3.3V CMOS output. Active High   |
| 10    | CAD_SNK                   | Input  | Cable detect pin from sink-side. 1M $\Omega$ pull-down resistor must be connected for proper cable detection  |
| 11    | HPD_SNK                   | Input  | Hot Plug Detect pin from the sink-side.<br>Internally 200 k $\Omega$ Pull-down.   |
| 12    | VDD33                     | Power  | 3.3V power supply   |
| 13    | OUT3N                     | Output | Main Link 3 data 100 $\Omega$ Differential negative output.   |
| 14    | OUT3P                     | Output | Main Link 3 data 100 $\Omega$ Differential positive output  |
| 15    | NC                        | NC     | Do Not Connect  |
| 16    | OUT2N                     | Output | Main Link 2 data 100 $\Omega$ Differential negative output  |
| 17    | OUT2P                     | Output | Main Link 2 data 100 $\Omega$ Differential positive output  |
| 18    | GND                       | Ground | Ground  |
| 19    | OUT1N                     | Output | Main Link 1 data 100 $\Omega$ Differential negative output  |

| Pin # | Pin Name | I/O    | Description  |
|-------|----------|--------|--|
| 20    | OUT1P    | Output | Main Link 1 data 100 $\Omega$ Differential positive output   |
| 21    | NC       | NC     | Do Not Connect   |
| 22    | OUT0N    | Output | Main Link 0 data 100 $\Omega$ Differential negative output   |
| 23    | OUT0P    | Output | Main Link 0 data 100 $\Omega$ Differential positive output   |
| 24    | GND      | Ground | Ground   |
| 25    | VDD33    | Power  | 3.3V power supply  |
| 26    | ENABLE   | Input  | Enable pin. Pulled-up internally with 100 k $\Omega$<br>"0"= Power down<br>"1"= Enable. Normal operation                             |
| 27    | AUX_SKNK | I/O    | AUX negative channel connected to DP sink device   |
| 28    | AUX_SNKP | I/O    | AUX positive channel connected to DP sink device   |
| 29    | AUX_SRCN | I/O    | AUX negative channel connected to DP source device   |
| 30    | AUX_SRCN | I/O    | AUX positive channel connected to DP source device   |
| 31    | GND      | Ground | Ground   |
| 32    | VDD33    | Power  | 3.3V power supply  |
| 33    | SCL_DDC  | I/O    | DDC clock channel from source-side when CAD_SNK=1  |
| 34    | SDA_DDC  | I/O    | DDC Data channel from source-side when CAD_SNK=1   |
| 36    | VDD33    | Power  | 3.3V power supply  |
| 37    | NC       | NC     | Do Not Connect   |
| 38    | IN0P     | Input  | Main Link 0 data 100 $\Omega$ Differential positive input  |
| 39    | IN0N     | Input  | Main Link 0 data 100 $\Omega$ Differential negative input  |
| 40    | EQ       | Input  | EQ selection pin. This pin is internally biased to 50% of VDD33.<br>When AUTO_EQ pin = 0, EQ pin can adjust EQ in the fixed pin mode |
| 41    | IN1P     | Input  | Main Link 1 data 100 $\Omega$ differential positive input  |
| 42    | IN1N     | Input  | Main Link 1 data 100 $\Omega$ differential negative input  |
| 43    | NC       | NC     | NC   |
| 44    | IN2P     | Input  | Main Link 2 data 100 $\Omega$ differentia positive input   |
| 45    | IN2N     | Input  | Main Link 2 data 100 $\Omega$ differentia negative input   |
| 46    | OC0      | Input  | Output Voltage Swing Control pin.<br>Internally pull-up with 100 k $\Omega$  |
| 47    | IN3P     | Input  | Main Link 3 data 100 $\Omega$ differential positive input  |
| 48    | IN3N     | Input  | Main Link 3 data 100 $\Omega$ differential negative input  |
| EPAD  | EPAD     | Ground | Tied to Ground   |

## 4. Functional Description

### 4.1 Block Diagram

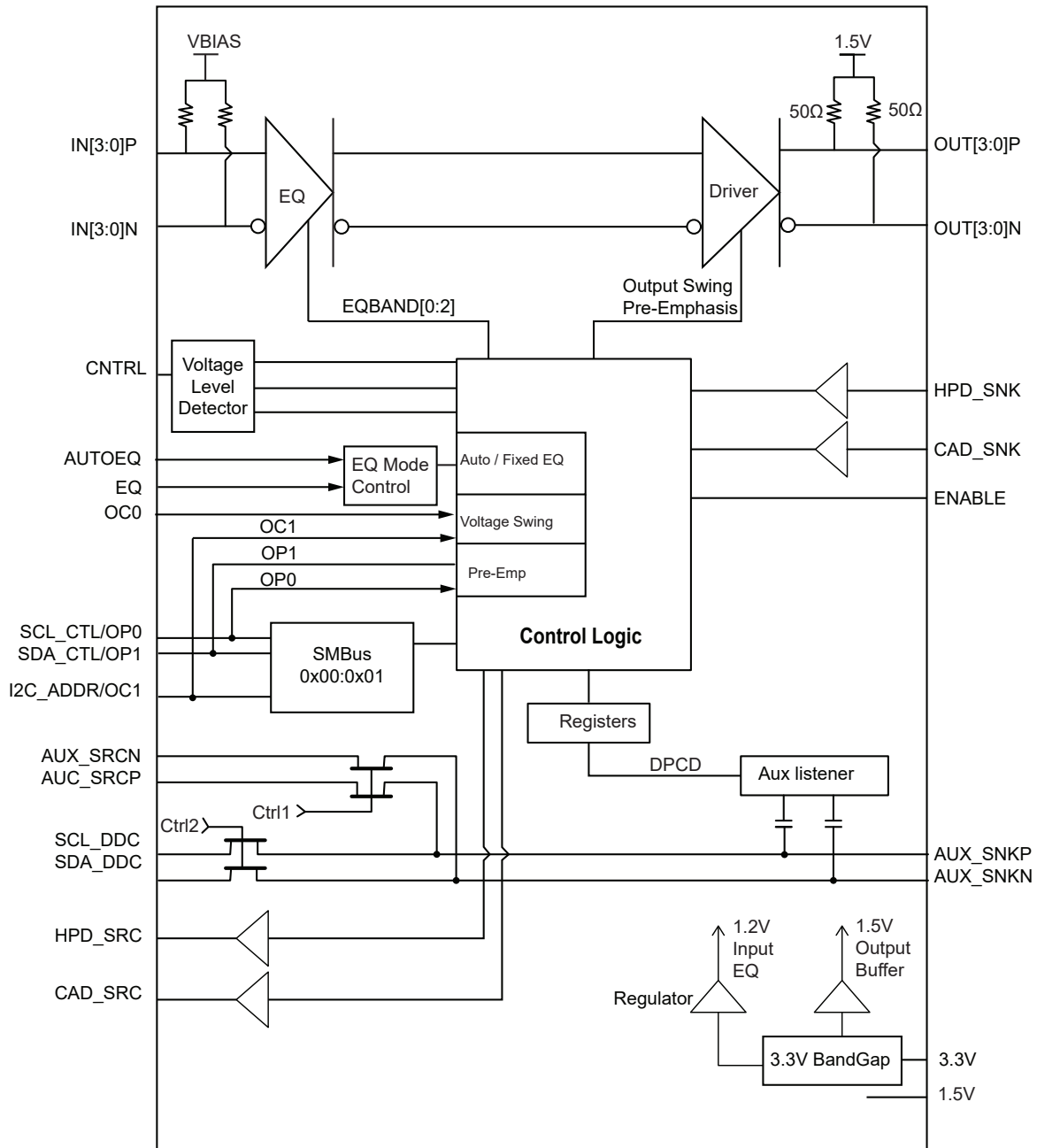
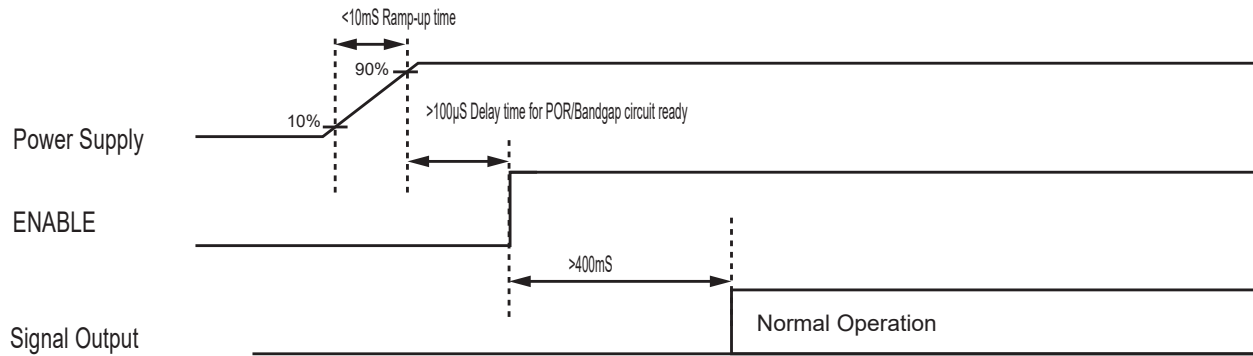


Figure 4-1: Functional Block Diagram

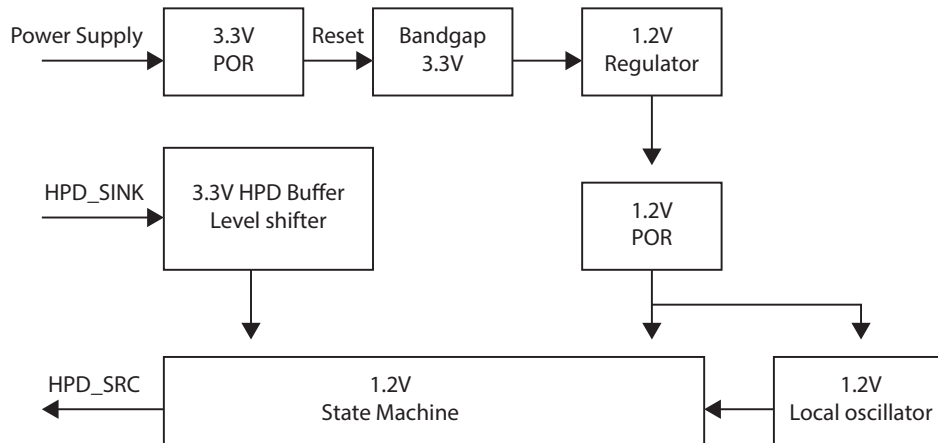
## 4.2 Function Description

### Power up operation Timing

After ENABLE signal is properly set, power up timing sequence complete. ENABLE signal from controller must be LOW until power supply become stable.



**Figure 4-2: Power up timing Sequence**

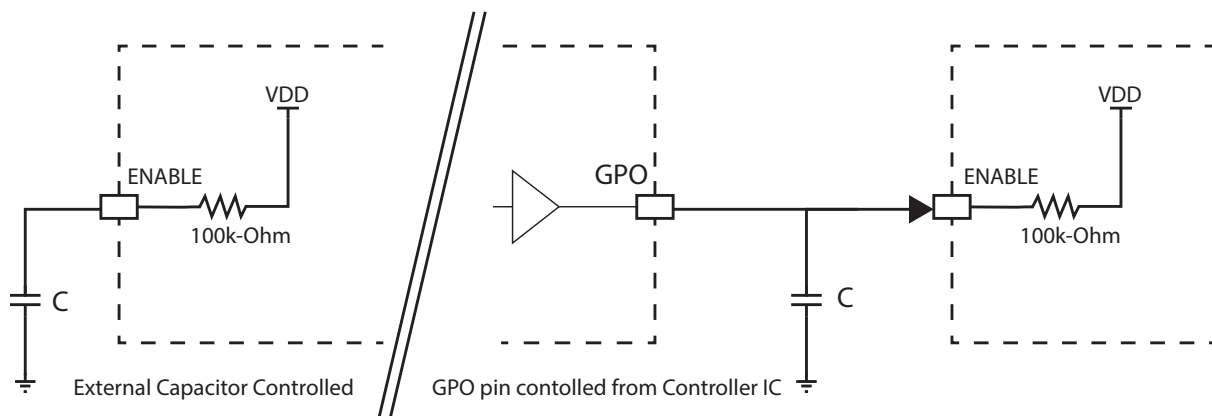


**Figure 4-3: Internal power up timing sequence**

**Reset Implementation**

When ENABLE is Low, the device is power-down mode and output are high impedance. It is critical to transition the ENABLE after the power supply VDD has reached the minimum recommended operation voltage. This can be achieved by the control signal GPO or by an external capacitor connected to GND.

To insure properly Reset, the ENABLE pin must be de-asserted for at least 100µS before asserted, and must be reprogrammed in I2C programming mode. When using external capacitor, the size of the cap value depends on the power up VDD supply ramp. Larger value results in a slower ramp-up time. Consider 0.1µF capacitor as a reasonable first estimate.



**Figure 4-4: Reset control from External Capacitor or GPO pin**

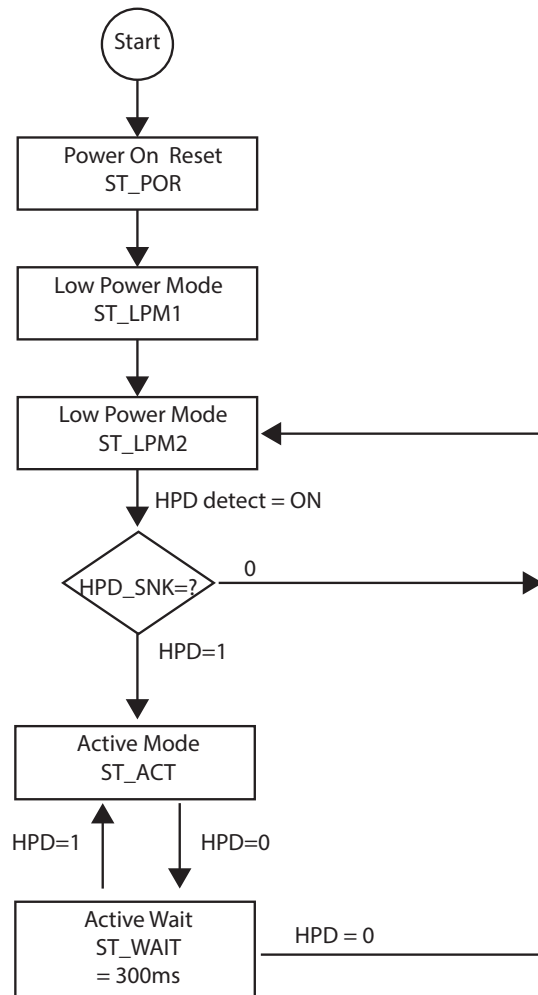
**Power-up/down and Hot Plug Detect (HPD)**

Following power on, state machine enter Reset State. Chip is powered down. HPD startup oscillator and Bandgap and Digital VDD regulator is on.

After Power-On-Reset (POR) de-asserted, state machine enter "Low Power Mode 1" and then 2-ms later enter "Low Power Mode 2" and monitor HPD\_SINK.

When HPD\_SINK is asserted, the state will change from "Low Power State 2" to "Active state". In Active stage, 1.2V regulator is turned on. When 1.2V POR detects valid voltage, RX and TX section of the channel will power on.

In Active state, if HPD\_SINK=0, then it will go to wait state and initiate debounce timer, if HPD\_SINK is still=0 after 300ms, this signal a HPD reset and the state machine goes to the "Low Power mode 2" state. If HPD\_SINK reverts back to 1 (High) within 300ms, then the controller will return active state. All circuits blocks are active in both active and wait state.



**Figure 4-5: Power up sequence flow chart**



### Intelligent Power Management

The device intelligent signal detection scheme allows portions, or all of the IC, to be disabled for power savings. In DP mode, if only one or two lanes are active, the other lanes will be automatically powered off. If there is no input video signal the entire IC will be powered down. If there is no monitor detected, it can also automatically power down the IC. The power-down mode can also be entered using hard pin ENABLE, or through DPCD register (AUX link training).

**Table 4-1: DP Channel Power down State**

| State POR | State POR Description | External Pins |          | Internal Signal | 3.3-1.2V active channel regulator(1) | Active channel |
|-----------|-----------------------|---------------|----------|-----------------|--------------------------------------|----------------|
|           |                       | HPD           | CAD _SNK | DPCD CS decode  |                                      |                |
| ST_POR    | Power On Reset        | X             | X        | 0               | Powered down                         | Powered down   |
| ST_LPM1   | Low Power Mode 1      | X             | X        | 0               | Powered down                         | Powered down   |
| ST_LPM2   | Low Power Mode 2      | X             | X        | 0               | Powered down                         | Powered down   |
| ST_ACT    | Active Mode           | 1             | 0        | 1               | Active                               | Active         |
| ST_ACT    | Active Mode           | 1             | 0        | 0               | Powered down                         | Powered down   |
| ST_WAIT   | Active Wait           | 1             | 0        | 1               | Active                               | Active         |
| ST_WAIT   | Active Wait           | 1             | 0        | 0               | Powered down                         | Powered down   |
| ST_POR    | Power On Reset        | X             | 1        | X               | Powered down                         | Powered down   |
| ST_LPM1   | Low Power Mode 1      | X             | 1        | X               | Powered down                         | Powered down   |
| ST_LPM2   | Low Power Mode 2      | X             | 1        | X               | Powered down                         | Powered down   |
| ST_ACT    | Active Mode           | 1             | 1        | 1               | Active                               | * Note (1)     |
| ST_WAIT   | Active Wait           | 1             | 1        | 1               | Active                               | * Note (1)     |

Note:

(1) Inactive channel are always powered down.

**Equalization/Swing/Pre-emphasis mode settings**

**Table 4-2: EQBAND and EQ[2:0] Setting**

| EQBAND, EQ[2:0]<br>BYTE0 bit4, bit[7:5] | Gain@1.6Gbps<br>dB | Gain @2.7Gbps<br>dB | Gain@5.4Gbps<br>dB |
|---|--------------------|---------------------|--------------------|
| 0000 (Default)                          | -0.384             | -0.9281             | -2.0054            |
| 0001                                    | -0.3443            | -0.849              | -1.8155            |
| 0010                                    | -0.2832            | -0.7256             | -1.5318            |
| 0011                                    | -0.1959            | -0.5518             | -1.1537            |
| 0100                                    | -0.1217            | -0.4054             | -0.8518            |
| 0101                                    | -0.0347            | -0.2355             | -0.5169            |
| 0110                                    | -0.0841            | -0.00704            | -0.0866            |
| 0111                                    | 0.2295             | 0.2698              | 0.4153             |
| 1000                                    | 0.3045             | 0.5198              | 0.8871             |
| 1001                                    | 0.4452             | 0.7885              | 1.4147             |
| 1010                                    | 0.6993             | 1.2611              | 2.2531             |
| 1011                                    | 1.1651             | 2.0748              | 3.5315             |
| 1100                                    | 1.67               | 2.8963              | 4.6837             |
| 1101                                    | 2.4082             | 4.0103              | 6.1106             |
| 1110                                    | 3.7438             | 5.8413              | 8.2595             |
| 1111                                    | 6.0652             | 8.6898              | 11.3532            |

**Table 4-3: EQ Setting**

when Auto\_EQ = 1 (Refer to Table 4-2)

| Pre-emphasis<br>OP[1:0]<br>Byte0 bit[3:2] | Pre-emphasis | Auto EQ mode 0<br>EQ = 0<br>Byte1 bit[3:2] = 00<br>EQBAND, EQ[2:0] | Auto EQ mode 1<br>EQ = M<br>Byte1 bit[3:2] = 01<br>EQBAND, EQ[2:0] | Auto EQ mode 2<br>EQ = 1<br>Byte1 bit[3:2] = 11<br>EQBAND, EQ[2:0] |
|---|--------------|--|--|--|
| 0 0                                       | 3.5dB        | 1010   | 1101   | 1111   |
| 0 1                                       | 6 dB         | 0111   | 1010   | 1101   |
| 1 0                                       | 9 dB         | 0011   | 0111   | 1011   |
| 1 1                                       | 0 dB         | 0000   | 0011   | 1001   |

**Table 4-4: EQ Setting**

when Auto\_EQ = 0 (Refer to Table 4-2)

| EQ | EQBAND, EQ[2:0] |         |         |
|----|-----------------|---------|---------|
|    | 1.62Gbps        | 2.7Gbps | 5.4Gbps |
| 0  | 0000            | 0000    | 0000    |
| M  | 1100            | 1100    | 1100    |
| 1  | 1111            | 1111    | 1111    |

**Table 4-5: EQ Setting**

when Auto\_EQ = M and CNTRL = M

| CNTRL | EQBAND = OC0         | EQ0 = OC1 | EQ1 = OP0 | EQ2 = OP1 |
|-------|----------------------|-----------|-----------|-----------|
| M     | (Refer to Table 4-2) |           |           |           |

**Table 4-6: Output Swing Setting**

in Register Programming Mode when CNTRL = 0 or in Pin Control Mode when CNTRL = 1

| CNTRL | OC[1:0]<br>Byte0 bit[1:0] | Output Swing     | Comments   |
|-------|---------------------------|------------------|--|
| 0/1   | 0 0                       | 400mV            | See Table 3-9: SMBUS Register 0x00 & 0x01 Definition |
| 0/1   | 0 1                       | 600mV            |  |
| 0/1   | 1 0                       | 1200mV (Default) |  |
| 0/1   | 1 1                       | 800mV            |  |

**Table 4-7: Output Swing Setting**

when CNTRL = M

| CNTRL | CAD_SNK | Output Swing        | Comments  |
|-------|---------|---------------------|-----------|
| M     | 0       | Follow AUX listener | DP Mode   |
| M     | 1       | 800mV               | TMDS Mode |

**Table 4-8: Output Pre-emphasis Setting**

in Register Programming Mode when CNTRL = 0 or in Pin Control Mode when CNTRL = 1

| CNTRL | OP[1:0]<br>Byte0 bit[3:2] | Output Pre-emphasis |  |
|-------|---------------------------|---------------------|--|
| 0 / 1 | 0 0                       | 3.5dB               | See Table 3-9: SMBUS Register 0x00 & 0x01 Definition |
| 0 / 1 | 0 1                       | 6dB (Default)       |  |
| 0 / 1 | 1 0                       | 9dB                 |  |
| 0 / 1 | 1 1                       | 0dB                 |  |

**Table 4-9: Output Pre-emphasis Setting**

when CNTRL = M

| CNTRL | CAD_SNK | Output Swing        | Comments  |
|-------|---------|---------------------|-----------|
| M     | 0       | Follow AUX listener | DP Mode   |
| M     | 1       | 0 dB                | TMDS Mode |

### 4.3 SMBus Registers

The AUX register can be read/write using the SMBus input. When in AUX mode, the control of the registers is passed to AUX, writing the SMBUS as the same time should be avoided.

In TMDS mode setting (CAD\_DET) = 1, external source can use SMBus to set the Equalization settings. EQ table can also be set by programming SMBus register 1.

SMBus is set to auto EQ mode 1 by default. ie. Reg0x01=00001101.

**Table 4-10: SMBUS Register 0x00 & 0x01 Definition**

| SMBus Registers | Description  | Default value | SMBus Access |
|-----------------|--|---------------|--------------|
| 0x00            | EQ Control Select, when CNTRL= 0 with SMBus_reg 0x01 bit [1:0]<br><br>bit[7]: EQ2<br>bit[6]: EQ1<br>bit[5]: EQ0<br>bit[4]: EQBAND is EQ group control register. Please refer Gain(dB) Control table<br><br>Pre-emphasis control<br>bit[3]: Control OP1 pin<br>bit[2]: Control OP0 pin<br><br>Swing control<br>bit[1]: Control OC1 pin<br>bit[0]: Control OC0 pin | 06h           | R/W          |
| 0x01            | bit [7:4] Reserved<br>bit [3:2] EQ control<br>00: EQ pin set Low<br>01: EQ pin set Middle<br>11: EQ pin set High<br>bit [1:0] AUTO_EQ control<br>00: AUTO_EQ pin set Low<br>01: AUTO_EQ pin set Middle<br>11: AUTO_EQ pin set High   | 00h           | R/W          |
| 0x02: 0x14      | Reserved   | 00h           | R/W          |

#### 4.4 DisplayPort AUX Listener

DP AUX listener supports Native AUX CH Syntax. Mapping of SMBus onto AUX CH Syntax is not supported.

AUX listener monitor AUX communication from requester and replier for transactions and stored AUX communication , related to the link settings.

In AUX read/write request cycle, the AUX address compares with the following registers' address. When the addresses matches, data shall extract and store into the respective AUX Listener registers. Below registers will set during the link training sequence after the hot plug detection.

00100h Data Rate Register  
 00101h LANE\_COUNT\_SET  
 00103h - 00106h TRAINING\_LANE0/1/2/3\_SET  
 00260h Sink Test request response  
 00600h Power Down

The AUX listener supports Sink request Test sequence. After HPD IRQ event and DP source read 00201h AUX register and if bit 1 is high, the DP source will enter a Sink request test mode and initiate a sequence of AUX read request cycle. During the read cycle, data matching the following registers address are stored in the listener.

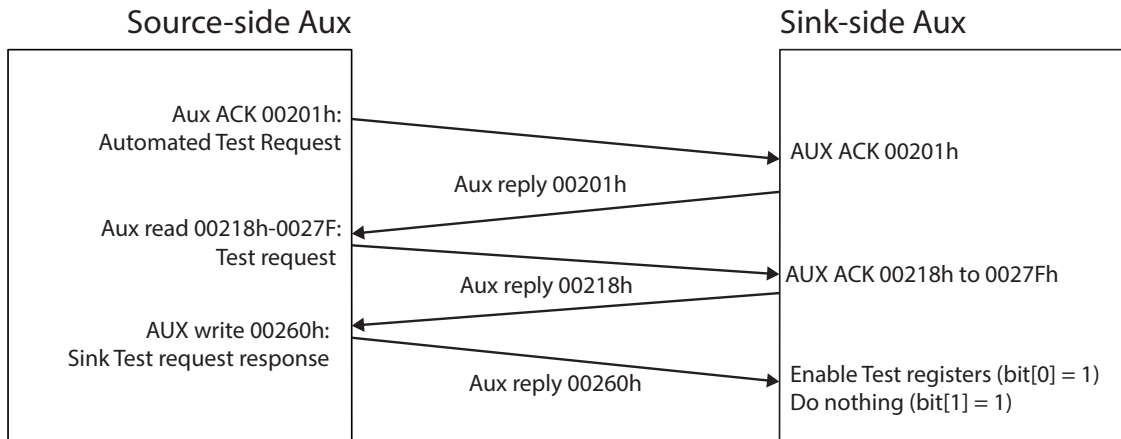
00206h ADJUST\_REQUEST\_LANE0\_1  
 00207h ADJUST\_REQUEST\_LANE2\_3  
 00218h Test Request  
 00219h Test link rate  
 00220h Test Lane count

After the read request cycle, the DP source will write 1 to Bit 0 register 00260h if the DP source enters sink request mode, or 1 to Bit 1 of register 00260h if the source declined the sink test request. The data stored in registers 002xx above will override the value set in 00101h to 00106h registers when the sink entered the Sink Test mode.

**Table 4-11: Sink Test Request Acknowledgement**

**Table 4-12:**

| 00260h    | Mode                    | Buffer configuration outputs  |
|-----------|-------------------------|---|
| xxxxxx00b | No action               | 00100 : 00106h  |
| xxxxxx01b | Sink Test mode          | 00206h,00207h,00219h,00220h Override 00100,1,3,4,5,6h register settings |
| xxxxxx10b | Sink test mode declined | 00100h : 00106h   |
| xxxxxx11b | Not Legal code          | 00100h : 00106h   |



**Figure 4-6: Sink Test Request Transaction in Aux Link Training**

A complete two way AUX transaction is defined as one of the following

**AUX write and Sink issue ACK reply:**

From Source

|      |                     |                |                |
|------|---------------------|----------------|----------------|
| Sync | Start/Start Pattern | 4-bit cmd 1000 | 20-bit address |
|------|---------------------|----------------|----------------|

From Sink ACK

|      |           |          |      |
|------|-----------|----------|------|
| Sync | Start bit | 00000000 | Stop |
|------|-----------|----------|------|

**AUX write and Sink issue NACK reply:**

A data byte “M” must follow AUX NACK, “M” indicates the number of data bytes successfully written. When a Source Device is writing a DPCD address not supported by the Sink Device, the Sink Device shall reply with AUX NACK and “M” equal to zero.

From Source

|      |           |                |            |              |      |      |
|------|-----------|----------------|------------|--------------|------|------|
| Sync | Start bit | 4-bit cmd 1000 | 20-bit adr | 8-bit length | Data | Stop |
|------|-----------|----------------|------------|--------------|------|------|

From Sink NACK

|      |           |          |                   |      |
|------|-----------|----------|-------------------|------|
| Sync | Start bit | 00010000 | 8-bit data byte M | Stop |
|------|-----------|----------|-------------------|------|

**AUX Read and Sink issue ACK reply:**

Ready to reply to Read request with data following. DisplayPort receiver may assert a STOP condition before transmitting the total number of requested data bytes when not all the bytes are available.

From Source

|      |           |                |                |              |      |
|------|-----------|----------------|----------------|--------------|------|
| Sync | Start bit | 4-bit cmd 1001 | 20-bit address | 8-bit length | Stop |
|------|-----------|----------------|----------------|--------------|------|

From sink ACK

|      |           |          |      |      |
|------|-----------|----------|------|------|
| Sync | Start bit | 00000000 | Data | Stop |
|------|-----------|----------|------|------|

**AUX Read and Sink issue NACK reply:**

A Sink Device receiving a Native AUX CH read request for an unsupported DPCD address must reply with an AUX ACK and read data set equal to zero instead of replying with AUX NACK.

From Source

|      |           |                |                |              |      |
|------|-----------|----------------|----------------|--------------|------|
| Sync | Start bit | 4-bit cmd 1001 | 20-bit address | 8-bit length | Stop |
|------|-----------|----------------|----------------|--------------|------|

From Sink NACK

|      |           |          |          |      |
|------|-----------|----------|----------|------|
| Sync | Start bit | 00001000 | data = 0 | Stop |
|------|-----------|----------|----------|------|



## 4.5 DPCD Aux Registers

### DPCD Aux Register Definitions

| SMBus Registers | AUX Registers                                       | Description   | Default value | DP Access |
|-----------------|---|---|---------------|-----------|
| 0x02            | Link initialization field<br>AUX operation : 00100h | <p>LINK_BW_SET : Main Link Bandwidth Setting=Value x 0.27Gbps per lane</p> <p>Bits 7:0 = LINK_BW_SET<br/>For DisplayPort version 1, revision 1a, only three values are supported. All other values are reserved.</p> <p>06h = 1.62 Gbps per lane<br/>0Ah = 2.7 Gbps per lane<br/>14h = 5.4 Gbps per lane</p> <p>The Source may choose any of the three link bandwidths as long as it does not exceed the capability of DisplayPort receiver as indicated in the receiver capability field.</p>  | 14h           | R/W       |
| 0x03            | Link initialization field<br>AUX operation : 00101h | <p>LANE_COUNT_SET : Main Link Lane Count = Value</p> <p>Bits 4:0 = LANE_COUNT_SET<br/>For DisplayPort version 1 revision 1a, only the following three values are supported. All other values are reserved.</p> <p>1h = One lane<br/>2h = Two lanes<br/>4h = Four lanes</p> <p>For one-lane configuration, Lane0 is used. For 2-lane configuration, Lane0 and Lane1 are used. The source may choose any lane count as long as it does not exceed the capability of the DisplayPort receiver as indicated in the receiver capability field.</p> <p>For DPCD Ver.1.0:<br/>Bits 7:5 = RESERVED. Read all 0's.</p> <p>For DPCD Ver.1.1:<br/>Bits 6:5 = RESERVED. Read all 0's.<br/>Bit 7 = ENHANCED_FRAME_EN<br/>0 = Enhanced Framing symbol sequence is not enabled.<br/>1 = Enhanced Framing symbol sequence for BS, SR, CPBS, and CPSR is enabled. Applicable to SST mode only. A uPacket TX must set this bit to 1 when the uPacket RX has the ENHANCED_FRAME_CAP bit (Bit 7 of DPCD 00002h) set to 1 (with the exception of eDP operation).</p> | 04h           | R/W       |

| SMBus Registers | AUX Registers                                 | Description  | Default value | DP Access |
|-----------------|---|--|---------------|-----------|
| 0x04            | DPCD Lane 0 status<br>Aux operation<br>00103h | <p>TRAINING_LANE0_SET<br/>Link Training Control_Lane0</p> <p>Bits1:0 = DRIVE_CURRENT_SET<br/>00 – Training Pattern 1 w/ drive current level 1<br/>01 – Training Pattern 1 w/ drive current level 2<br/>10 – Training Pattern 1 w/ drive current level 3<br/>11 – Training Pattern 1 w/ drive current level 4</p> <p>Bit2 = MAX_CURRENT_REACHED<br/>Set to 1 when the maximum driven current setting is reached.</p> <p>Note: Support of programmable drive current is optional. For example if there is only 1 level, then program Bits2:0 to 100 to indicate to the receiver that Level 1 is the maximum drive current. Support of independent drive current control for each lane is also optional.</p> <p>Bit4:3 = PRE-EMPHASIS_SET<br/>00 = Training Pattern 2 w/o pre-emphasis<br/>01 = Training Pattern 2 w/ pre-emphasis level 1<br/>10 = Training Pattern 2 w/ pre-emphasis level 2<br/>11 = Training Pattern 2 w/ pre-emphasis level 3</p> <p>Bit5 = MAX_PRE-EMPHASIS_REACHED</p> | 00h           | R/W       |
| 0x05            | DPCD Lane 1 status<br>Aux operation<br>00104h | <p>Lane setting for lane 1.<br/>The definition is the same as lane 0</p>   | 00h           | R/W       |
| 0x06            | DPCD Lane 2 status<br>Aux operation<br>00105h | <p>Lane setting for lane 2.<br/>The definition is the same as lane 0</p>   | 00h           | R/W       |
| 0x07            | DPCD Lane 3 status<br>Aux operation<br>00106h | <p>Lane setting for lane 3.<br/>The definition is the same as lane 0</p>   | 00h           | R/W       |
| 0x08            | 00107h  | <p>DOWNSPREAD_CTRL : Down-spreading control</p> <p>Bit 3:0 = RESERVED. Read all 0's</p> <p>Bits 4 = SPREAD_AMP Spreading amplitude<br/>0 = No downspread<br/>1 = Equal to or less than 0.5% down spread</p> <p>Bit 7:5 = RESERVED. Read all 0's.</p> <p>Note: Write 00h to declare to the receiver that there is no down-spreading. The modulation frequency must be in the range of 30kHz ~ 33kHz</p>   | 00h           | R/W       |

| SMBus Registers | AUX Registers | Description  | Default value | DP Access  |
|-----------------|---------------|--|---------------|--|
| 0x09            | 00201h        | <p>DEVICE_SERVICE_IRQ_VECTOR</p> <p>Bit 0 = RESERVED for EMOTE_CONTROL_COMMAND_PENDING<br/>When this bit is set to 1, the Source Device must read the Device Services Field for REMOTE_CONTROL_COMMAND_PASS_THROUGH.</p> <p>Bit 1 = AUTOMATED_TEST_REQUEST<br/>When this bit is set to 1, the Source Device must read Addresses 00218h -0027Fh for the requested link test.</p> <p>Bit 2 = CP_IRQ<br/>This bit is used by an optional content protection system.</p> <p>Bit 3 = MCCS_IRQ<br/>This bit is used by an optional MCCS system in the Sink</p> <p>Bits 5:4 = RESERVED. Read all 0's.</p> <p>Bit 6 = SINK_SPECIFIC_IRQ<br/>Usage is vendor-specific.</p> <p>Bit 7 = RESERVED. Read 0.</p> | 00h           | Clearable read only. (Bit is cleared when '1' is written is written via an AUX CH write transaction. |
| 0x0A            | 00206h        | <p>ADJUST_REQUEST_LANE0_1 : Voltage Swing and Equalization Setting<br/>Adjust Request for Lane0 and Lane1</p> <p>Bits 1:0 = VOLTAGE_SWING_LANE0<br/>00 = Level 0<br/>01 = Level 1<br/>10 = Level 2<br/>11 = Level 3</p> <p>Bits 3:2 = PRE-EMPHASIS_LANE0<br/>00 = Level 0<br/>01 = Level 1<br/>10 = Level 2<br/>11 = Level 3</p>   | 00h           | R  |
| 0x0B            |               | <p>Bits 5:4 = VOLTAGE_SWING_LANE1<br/>00 = Level 0<br/>01 = Level 1<br/>10 = Level 2<br/>11 = Level 3</p> <p>Bits 7:6 = PRE-EMPHASIS_LANE1<br/>00 = Level 0<br/>01 = Level 1<br/>10 = Level 2<br/>11 = Level 3</p>   |               |  |

| SMBus Registers | AUX Registers | Description  | Default value | DP Access |
|-----------------|---------------|--|---------------|-----------|
|                 | 00207h        | ADJUST_REQUEST_LANE2_3<br>(Bit definitions as in ADJUST_REQUEST_LANE0_1)   | 00h           | R         |
| 0x0C            | 00218h        | <p>TEST_REQUEST: Test requested by the Sink Device. All other values reserved.</p> <p>Bit 0 = TEST_LINK_TRAINING<br/>0 = no link training test requested<br/>1 = link training test requested.<br/>See TEST_LINK_RATE and TEST_LANE_COUNT for link rate and linkwidth requested respectively.</p> <p>Bit 1 = TEST_PATTERN<br/>0 = no test pattern requested<br/>1 = test pattern requested</p> <p>Bit 2 = TEST_EDID_READ<br/>0 = no EDID read test requested<br/>1 = EDID read test requested.</p> <p>Checksum of the last EDID block read is written to TEST_EDID_CHECKSUM. The source will also send a color square test pattern.</p> <p>For DPCD version 1.0:<br/>Bits 7:3 = RESERVED. Read all 0's.<br/>For DPCD version 1.1:<br/>Bit 3 = PHY_TEST_PATTERN<br/>Set = 1 to request the PHY test pattern as specified at address 00248h.<br/>Bits 7:4 = Reserved. Read as zeros.</p> | 00h           |           |
| 0x0D            | 00219h        | <p>TEST_LINK_RATE<br/>Bits 7:0 = TEST_LINK_RATE<br/>06h = 1.62 Gbps<br/>0Ah = 2.7 Gbps<br/>14h = 5.4 Gbps</p>  | 00h           | R         |
| 0x0E            | 00220h        | <p>TEST_LANE_COUNT<br/>Bits 4:0 = TEST_LANE_COUNT<br/>1h = one lane<br/>2h = two lanes<br/>4h = four lanes<br/>All other values reserved.<br/>Bits 7:5 = RESERVED. Read all 0's.</p>   | 00h           | R         |

| SMBus Registers | AUX Registers | Description   | Default value | DP Access |
|-----------------|---------------|---|---------------|-----------|
| 0x0F            | 00260h        | <p>TEST_RESPONSE</p> <p>Bit 0 = TEST_ACK<br/>0 = writing zero has no effect on TEST_REQ state<br/>1 = positive acknowledgement of TEST_REQ. Clears TEST_REQ interrupt flag and indicates to the sink that the source has started requested test mode.</p> <p>Bit 1 = TEST_NAK<br/>0 = writing zero has no effect on TEST_REQ state<br/>1 = negative acknowledgement of TEST_REQ. Clears TEST_REQ interrupt flag and indicates to sink that source will not start requested test mode.</p> <p>Bit 2 = TEST_EDID_CHECKSUM_WRITE<br/>0 = no write to TEST_EDID_CHECKSUM<br/>1 = EDID checksum has been written to TEST_EDID_CHECKSUM</p> <p>Bits 7:3 = RESERVED. Read all 0's.</p> | 00h           | R/W       |
| 0x10            | 00600h        | <p>Bit 1, 0</p> <p>0 1 - normal mode<br/>1 0 - D3 power down state</p>  | 01h           | R/W       |

#### 4.6 SMBus Programming

SMBUS support Block Read, Block Write, Indexed Block Read and Indexed Block Write function. No Byte write function is supported. SMBUS has 20 internal registers. Only two registers are accessible by users.

SMBUS address is set to 0xAA or 0xA8 depending on the SMBUS\_ADDR pin setting.

##### SMBus Address:

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 (I2C_ADDR pin 1-bit)                   | Bit 0             |
|-------|-------|-------|-------|-------|-------|--|-------------------|
| 1     | 0     | 1     | 0     | 1     | 0     | 1'b=0 : 0xA8 address<br>1'b=1 : 0xAA address | R/ $\overline{W}$ |

##### SMBus Write Byte

###### Block Write

| S | slave address | Wr | A | Command Code | A | Byte Count = N | A | Date Byte 0 | A |
|---|---------------|----|---|--------------|---|----------------|---|-------------|---|
|   |               |    |   | Date Byte 1  | A | Date Byte 2    | A | Date Byte 3 | A |
|   |               |    |   | Date Byte 4  | A | Date Byte 5    | A | Date Byte 6 | A |
|   |               |    |   | Date Byte 7  | A | Date Byte 8    | A |             | P |

###### Index Block Write

| S | slave address | Wr | A | Command Code | A | Byte Count = N | A | Date Byte 0 | A |
|---|---------------|----|---|--------------|---|----------------|---|-------------|---|
|   |               |    |   | Date Byte 1  | A | Date Byte 2    | A | Date Byte 3 | A |
|   |               |    |   | Date Byte 4  | A | Date Byte 5    | A | Date Byte 6 | A |
|   |               |    |   | Date Byte 7  | A | Date Byte 8    | A |             | P |

###### Byte Write

| S | slave address | Wr | A | Command Code | A | Byte | A | P |
|---|---------------|----|---|--------------|---|------|---|---|
|   |               |    |   |              |   |      |   |   |

## 5. Electrical Specification

### 5.1 Absolute Maximum Ratings

|                                 |                      |
|---------------------------------|----------------------|
| Supply Voltage Range 3.3V ..... | -0.5V to 4.0V        |
| DC Signal Voltage.....          | -0.5V to VDD33 +0.5V |
| Output Current .....            | -25mA to +25mA       |
| Storage Temperature .....       | -65 to +150°C        |
| Junction Temperature .....      | 125°C                |
| ESD HBM .....                   | ±2000V               |
| ESD CDM.....                    | ±500V                |

Note:  
1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### 5.2 Recommended Operating Conditions

| Symbol                  | Parameters   | Min.                   | Typ. | Max.  | Units            |
|-------------------------|--|------------------------|------|-------|------------------|
| VDD33                   | 3.3V Power Supply  | 3.0                    | 3.3  | 3.6   | V                |
| T <sub>A</sub>          | Operating temperature  | Commercial Part Number | 0    | 70    | °C               |
|                         |  | Industrial Part Number | -40  | 85    |                  |
| T <sub>CASE</sub>       | Case temperature   |                        |      | 103.1 | °C               |
| V <sub>IH(HPD)</sub>    | High-level input voltage HPD_SNK   | 1.9                    |      | 5.5   | V                |
| V <sub>IH</sub>         | High-level input voltage for device control signals  |                        | 0.75 |       | V                |
| V <sub>IL</sub>         | Low-level input voltage for device control signals   | 0                      |      | 0.8   | V                |
| <b>Main Link</b>        |  |                        |      |       |                  |
| V <sub>ID</sub>         | Peak to Peak input differential voltage  | 0.3                    |      | 1.4   | V <sub>pp</sub>  |
| DR                      | Data Rate  |                        |      | 5.4   | Gbps             |
| C <sub>AC</sub>         | AC Coupling Capacitance  | 75                     |      | 200   | nF               |
| R <sub>DIFF</sub>       | Differential output termination resistor   | 75                     | 100  | 120   | Ω                |
| V <sub>O_TERM</sub>     | Output Termination Voltage   | 0                      |      | 2     | V                |
| t <sub>SKEW</sub>       | Inter-pair Skew at the 5.4 Gbps Input  |                        |      | 20    | ps               |
| <b>Aux Channel Data</b> |  |                        |      |       |                  |
| V <sub>ID</sub>         | Input Differential Voltage   | 300                    |      | 1400  | mV <sub>pp</sub> |
| DR <sub>AUX</sub>       | Data Rate Aux  | 0.8                    | 1    | 1.2   | Mbps             |
| DR <sub>FAUX</sub>      | Data rate Fast Aux   |                        | 720  |       | Mbps             |
| C <sub>AC</sub>         | Aux AC Coupling Capacitance  | 75                     |      | 200   | nF               |
| V <sub>CM_SRC</sub>     | Aux Source common mode voltage<br>CAD=VIL; measured on Aux source and sink before AC coupling caps | 0                      |      | 2000  | mV               |



### 5.3 Power Dissipation

| Symbol     | Parameters  | Condition   | Min | Typ | Max | Units |
|------------|---|---|-----|-----|-----|-------|
| $I_{DD33}$ | 3.3V Single supply<br>@5.4Gbps, CAD_SNK = 0,<br>HPD_SNK = 1 | 400 mV Swing, 0 dB Pre-emphasis                           |     | 140 |     | mA    |
|            |   | 400 mV Swing, 9.5 dB Pre-emphasis                         |     | 290 |     | mA    |
|            |   | 600 mV Swing, 0 dB Pre-emphasis                           |     | 150 |     | mA    |
|            |   | 600 mV Swing, 6 dB Pre-emphasis                           |     | 290 |     | mA    |
|            |   | 800 mV Swing, 0 dB Pre-emphasis                           |     | 200 |     | mA    |
|            |   | 800 mV Swing, 3.5 dB Pre-emphasis                         |     | 290 |     | mA    |
|            |   | 1200 mV Swing, 0 dB Pre-emphasis                          |     | 226 |     | mA    |
| $I_{SB}$   | 3.3V Power down current                                     | ENABLE pin Low (Turn off all function including band-gap) |     | 130 |     | uA    |

## 5.4 Electrical Characteristic

### Control Pin ENABLE

| Symbol   | Parameters               | Condition        | Min. | Typ. | Max.  | Units |
|----------|--------------------------|------------------|------|------|-------|-------|
| $V_{IH}$ | LVTTL input high voltage |                  | 2.4  |      | VDD33 | V     |
| $V_{IL}$ | LVTTL input low voltage  |                  | GND  |      | 0.8   | V     |
| $I_{IH}$ | Input High-level current | $V_{IH} = VDD33$ | -5   |      | 5     | uA    |
| $I_{IL}$ | Input Low-level current  | $V_{IL} = GND$   | -50  |      | -15   | uA    |

### HPD\_SRC and HPD\_SNK Pins

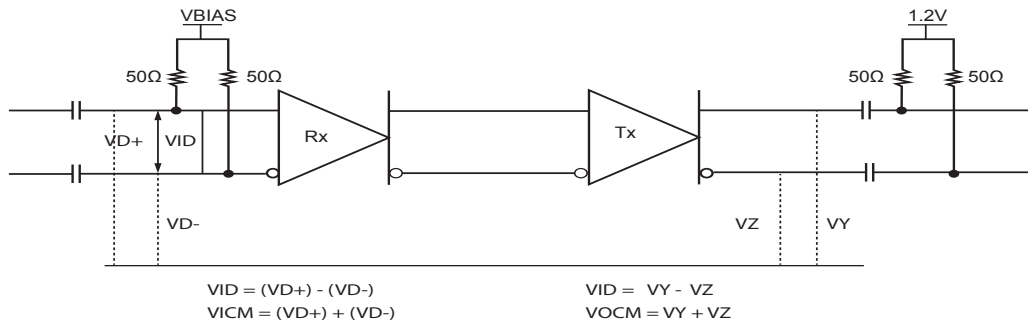
| Symbol   | Parameters                      | Condition        | Min.              | Typ. | Max.              | Units |
|----------|---------------------------------|------------------|-------------------|------|-------------------|-------|
| $V_{IH}$ | LVTTL input high voltage        |                  | 2.4               |      | VDD33             | V     |
| $V_{IL}$ | LVTTL input low voltage         |                  | $1/3 \cdot VDD33$ |      | $2/3 \cdot VDD33$ | V     |
| $I_{IH}$ | Input High-level current        | $V_{IH} = VDD33$ |                   |      | 40                | uA    |
| $I_{IL}$ | Input Low-level current         | $V_{IL} = GND$   | -0.6              |      | 0.6               | uA    |
| $V_{OH}$ | LVTTL high level output voltage | $I_{OH} = -8mA$  | 2.4               |      |                   | V     |
| $V_{OL}$ | LVTTL low level output voltage  | $I_{OL} = 8mA$   |                   |      | 0.4               | V     |

### SCL/SDA and AUX Pins

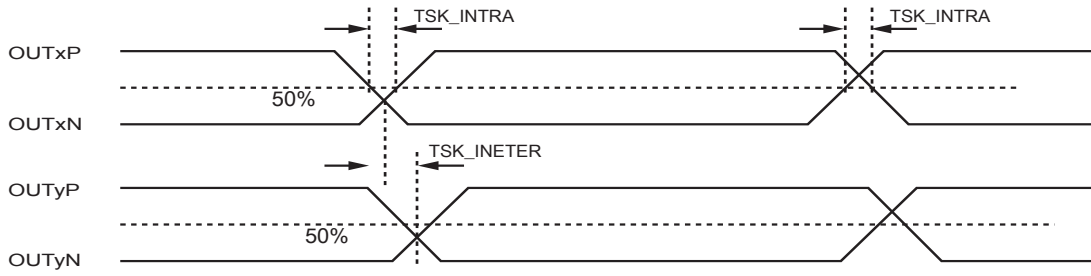
| Symbol                             | Parameters                        | Condition  | Min.            | Typ. | Max.            | Units    |
|------------------------------------|-----------------------------------|--|-----------------|------|-----------------|----------|
| When configure as SCL/SDA pins     |                                   |  |                 |      |                 |          |
| $V_{IH}$                           | LVTTL input high voltage          |  | $0.7 \cdot VDD$ |      | 5.5             | V        |
| $V_{IL}$                           | LVTTL input low voltage           |  | GND             |      | $0.3 \cdot VDD$ | V        |
| $I_{IH}$                           | Input High-level current          | $V_{IH} = VDD33$                                       | -1              |      | 1               | uA       |
| $I_{IL}$                           | Input Low-level current           | $V_{IL} = 0$   | -1              |      | 1               | uA       |
| $V_{OH}$                           | LVTTL high level output voltage   | $I_{OH} = -8mA$  | 2.4             |      |                 | V        |
| $V_{OL}$                           | LVTTL low level output voltage    | $I_{OL} = 8mA$   |                 |      | 0.4             | V        |
| When configure as Aux channel pins |                                   |  |                 |      |                 |          |
| $V_{CM}$                           | Common mode voltage               |  | 0               |      | 2.0             | V        |
| $V_{AUX(dif-pp)}$                  | Peak to peak differential voltage |  | 0.19            |      | 1.26            | V        |
| $R_{ON}$                           | On resistance                     | $V_{IN} = -0.3V \text{ to } +0.4V$<br>$I_{ON} = -40mA$ |                 | 11   | 20              | $\Omega$ |
| $BW_{3dB}$                         | 3dB Bandwidth                     |  |                 | 440  |                 | MHz      |

**DP Differential**

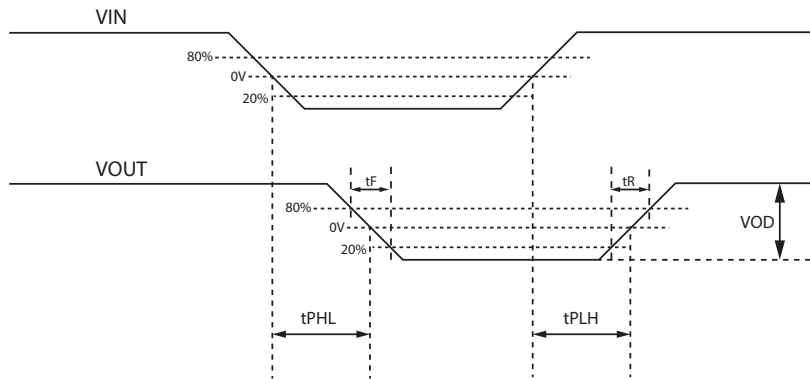
| Symbol  | Parameters                              | Condition   | Min. | Typ. | Max.      | Units |
|---|---|-------------|------|------|-----------|-------|
| <b>DP differential Input</b>  |   |             |      |      |           |       |
| V <sub>ID</sub>   | Peak to peak differential input voltage |             | 400  |      | 1200      | mV    |
| V <sub>ODO</sub>  | Differential overshoot voltage          |             |      |      | 15%*VDD33 | V     |
| V <sub>ODU</sub>  | Differential undershoot voltage         |             |      |      | 25%*VDD33 | V     |
| I <sub>OFF</sub>  | Single end standby current              |             |      |      | 10        | uA    |
| I <sub>SC</sub>   | Output short current                    |             |      |      | 60        | mA    |
| <b>DP differential Output</b>   |   |             |      |      |           |       |
| V <sub>tx diff-lev1</sub>   | Differential pk-pk level 1              |             | 340  | 400  | 460       | mV    |
| V <sub>tx diff-lev2</sub>   | Differential pk-pk level 2              |             | 510  | 600  | 680       | mV    |
| V <sub>tx diff-lev3</sub>   | Differential pk-pk level 3              |             | 690  | 800  | 920       | mV    |
| V <sub>tx diff-lev4</sub>   | Differential pk-pk level 4              |             | 1020 | 1200 | 1380      | mV    |
| <b>Pre-emphasis level</b>   |   |             |      |      |           |       |
| 0dB   | V <sub>tx diff</sub> = 1.2V             |             | 0    | 0    | 0         | dB    |
| 3.5dB (1.5x)  | V <sub>tx diff</sub> = 0.8V             |             | 2.8  | 3.5  | 4.2       | dB    |
| 6dB (2x)  | V <sub>tx diff</sub> = 0.6V             |             | 4.8  | 6    | 7.2       | dB    |
| 9.5dB (3x)  | V <sub>tx diff</sub> = 0.4V             |             | 7.6  | 9.5  | 11.4      | dB    |
| <b>DP differential output CML driver AC Switching Characteristics</b> |   |             |      |      |           |       |
| T <sub>rise</sub> / T <sub>fall</sub>                                 | Rise and Fall Time                      | 20% to 80 % | 80   | 115  | 150       | ps    |
| T <sub>sk(D)</sub>  | Intra-pair differential skew            |             |      |      | 50        | ps    |
| T <sub>sk(O)</sub>  | Intra-pair differential skew            |             |      |      | 50        | ps    |



**Figure 5-1: DisplayPort Main Link Test Circuit**



**Figure 5-2: DisplayPort Main Link Intra-Skew Measurement**



**Figure 5-3: Rising and Falling Time Definition**

## 6. Application

### Note

Information in the following applications sections is not part of the component specification, and does not warrant its accuracy or completeness. Customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 6.1 Application Circuit Diagrams

- SCL\_DDC and SDA\_DDC can be float, if unused.

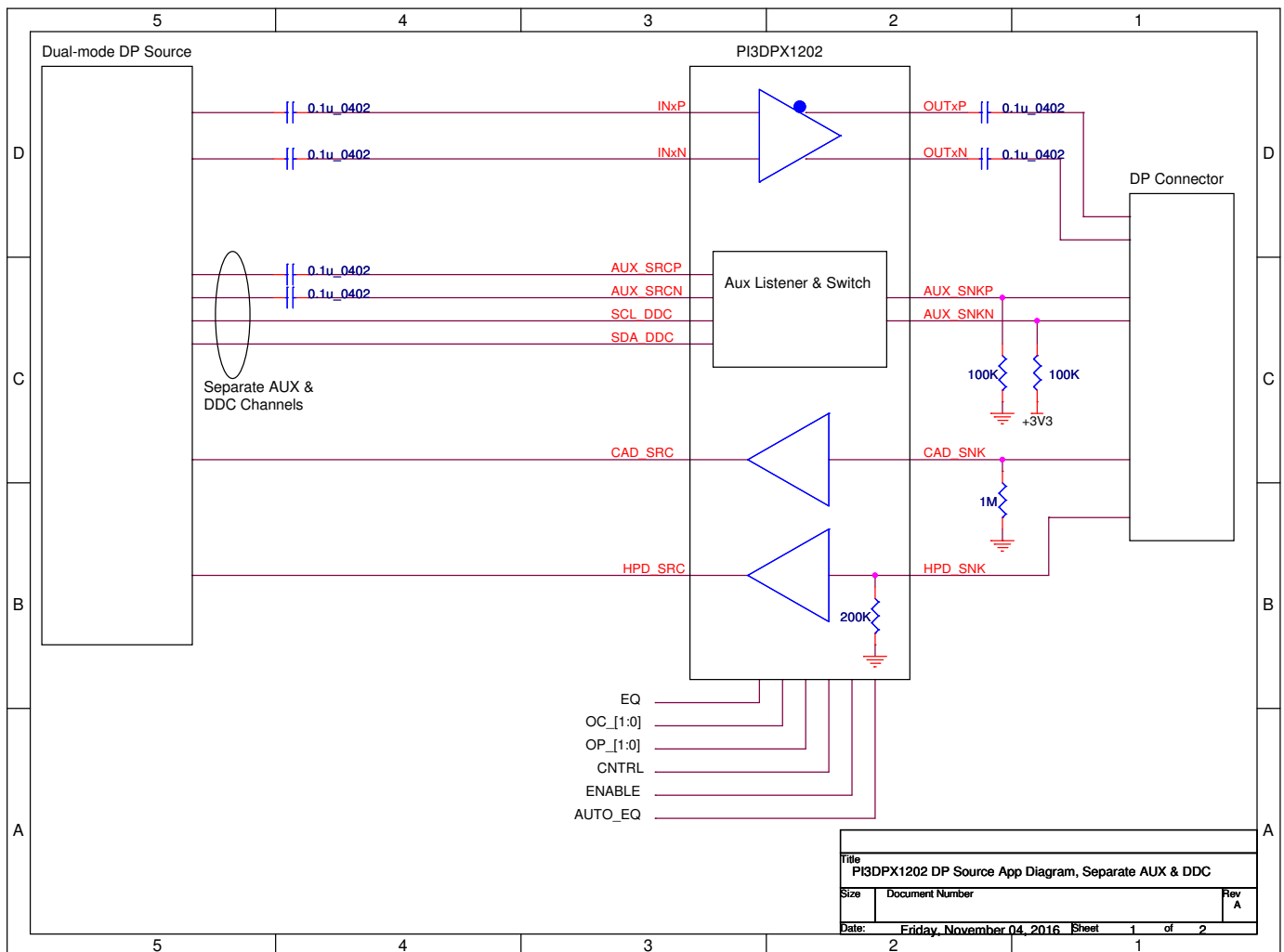


Figure 6-1: DP++ Source Application with combined Aux/DDC Channels

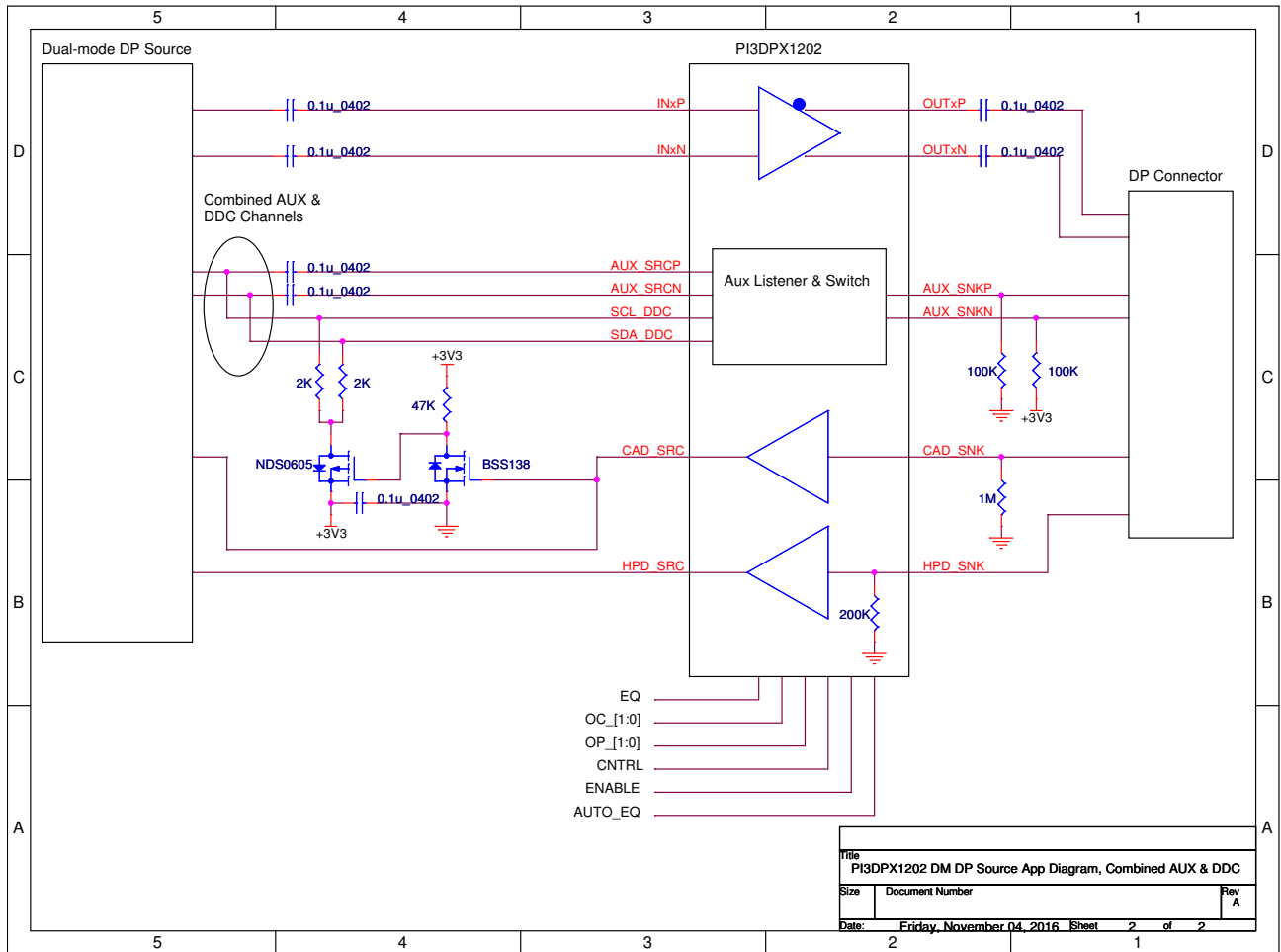


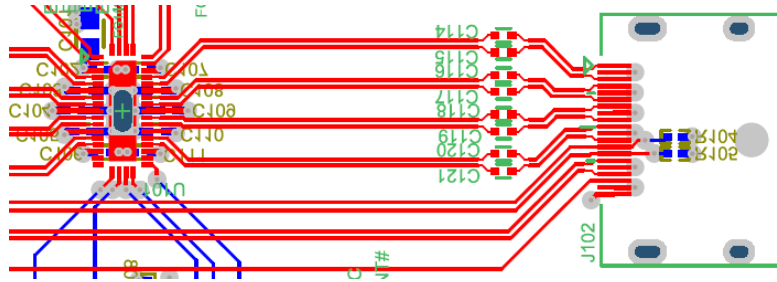
Figure 6-2: DP Source Application with separate Aux/DDC Channels

## 6.2 PCB Layout Guideline

As transmission data rate increases rapidly, any flaws and/or mis-matches on PCB layout are amplified in terms of signal integrity. Layout guideline for high-speed transmission is highlighted in this application note.

### AC coupling Capacitor

Below is an example of placing AC coupling capacitors on high-speed channels.

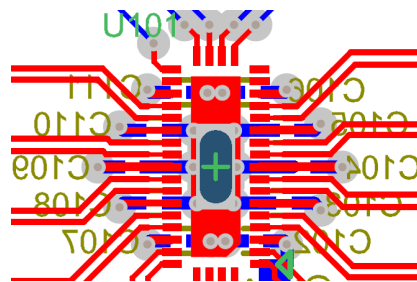


### Location

To wisely use the equalization selections offered by PI3DPX1202, it is recommended to place PI3DPX1202 at the end of the entire path. In short, PI3DPX1202 should be located close to the output DP connector in a source application. Below is the PI3DPX1202 placement on its evaluation board.

### Thermal Pad GND Via Recommendation

To wisely use the equalization selections offered by PI3DPX1202, it is recommended to place PI3DPX1202 at the end of the entire path. In short, PI3DPX1202 should be located close to the output DP connector in a source application. Below is the PI3DPX1202 placement on its evaluation board .

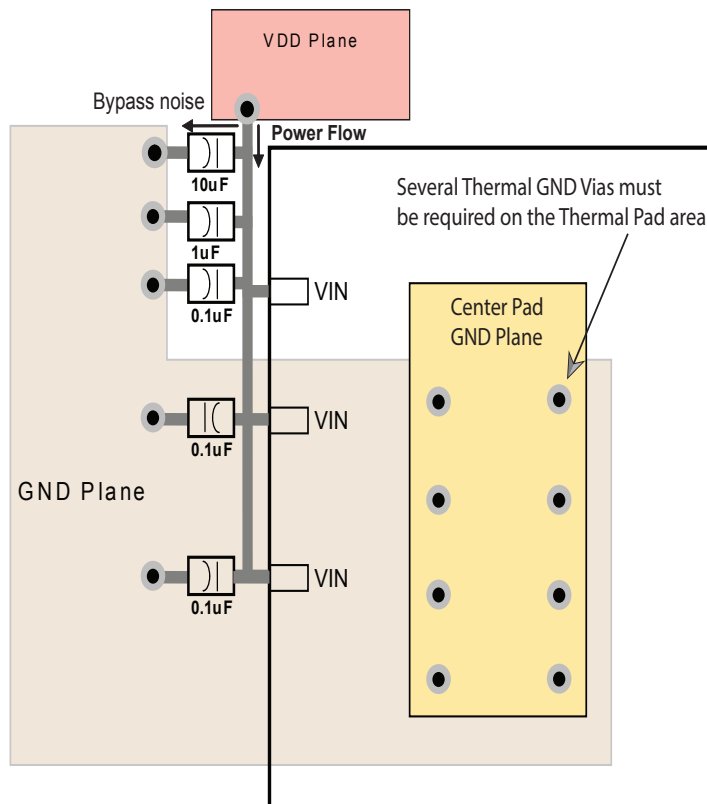


Several GND vias are the “must” requirement in thermal pad. The recommended Via size is 12/24 mil.

### General Power and Ground Guideline

To provide a clean power supply for Diodes high-speed device, few recommendations are listed below:

- Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly without passing through any resistor.
- The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- One low-ESR 0.1uF decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Capacitors of smaller body size, i.e. 0402 package, is more preferable as the insertion loss is lower. The capacitor should be placed next to the VDD pin.
- One capacitor with capacitance in the range of 4.7uF to 10uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- A ferrite bead for isolating the power supply for Diodes high-speed device from the power supplies for other parts on the printed circuit board should be implemented.
- Several thermal ground vias must be required on the thermal pad. 25-mil or less pad size and 14-mil or less finished hole are recommended.



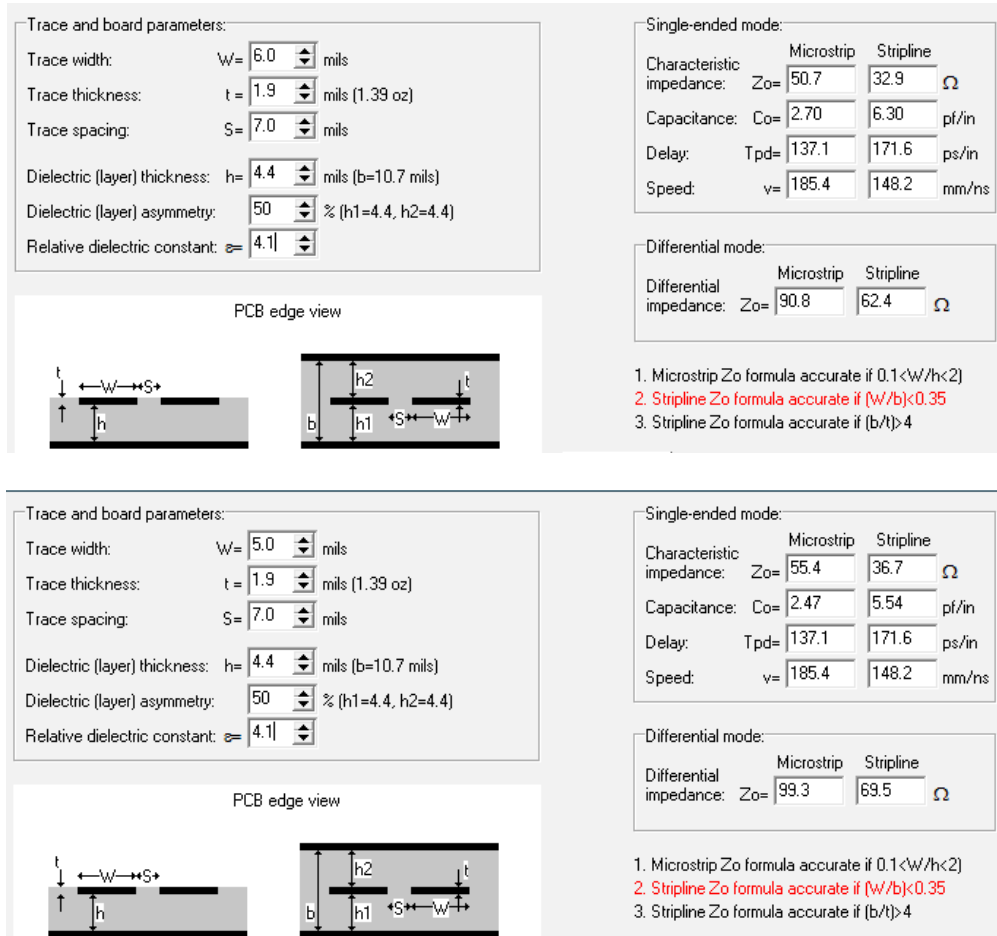
**Figure 6-3: Decoupling Capacitor Placement Diagram**



**High-speed signal Routing**

Well-designed layout is essential to prevent signal reflection:

- For 90Ω differential impedance, width-spacing-width micro-strip of 6-7-6 mils is recommended; for 100Ω differential impedance, width-spacing-width micro-strip of 5-7-5 mils is recommended.
- Differential impedance tolerance is targeted at ±15%.



**Figure 6-4: Trace Width and Clearance of Micro-strip and Strip-line**

- For micro-strip, using 1/2oz Cu is fine. For strip-line in 6+ PCB layers, 1oz Cu is more preferable.

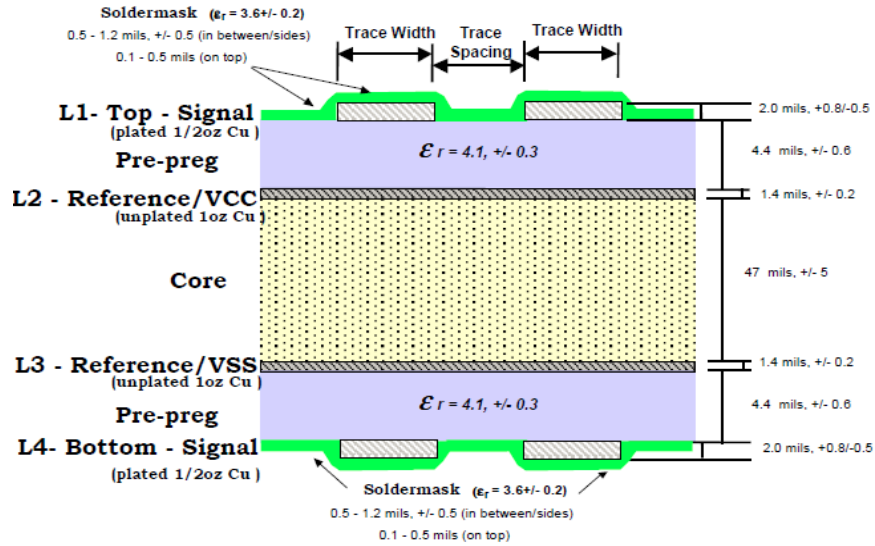


Figure 6-5: 4-Layer PCB Stack-up Example

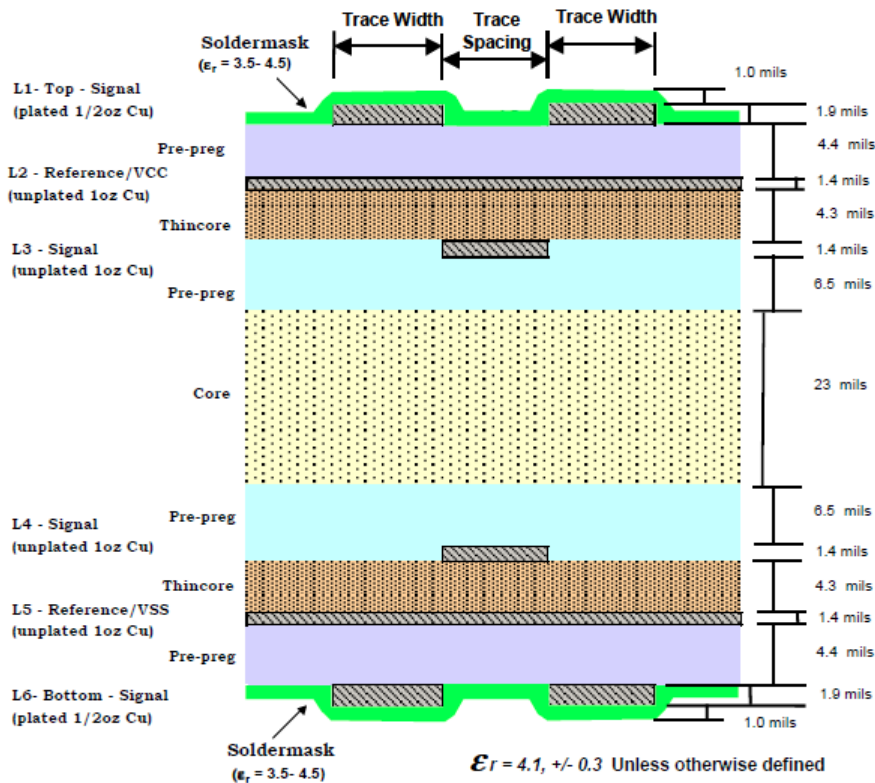


Figure 6-6: 6-Layer PCB Stack-up Example

- Ground referencing is highly recommended. If unavoidable, stitching capacitors of 0.1uF should be placed when reference plane is changed.

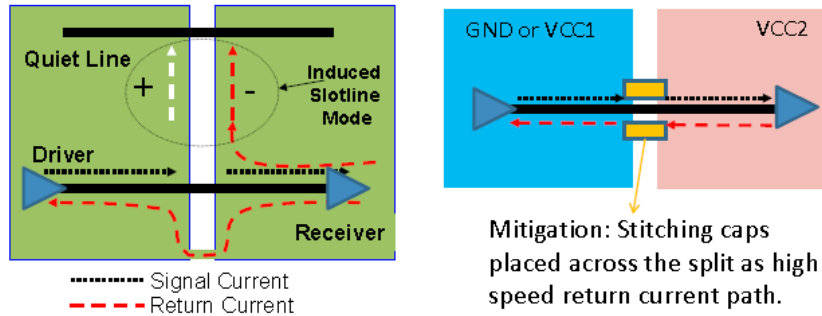


Figure 6-7: Stitching Capacitor Placement

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.
- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

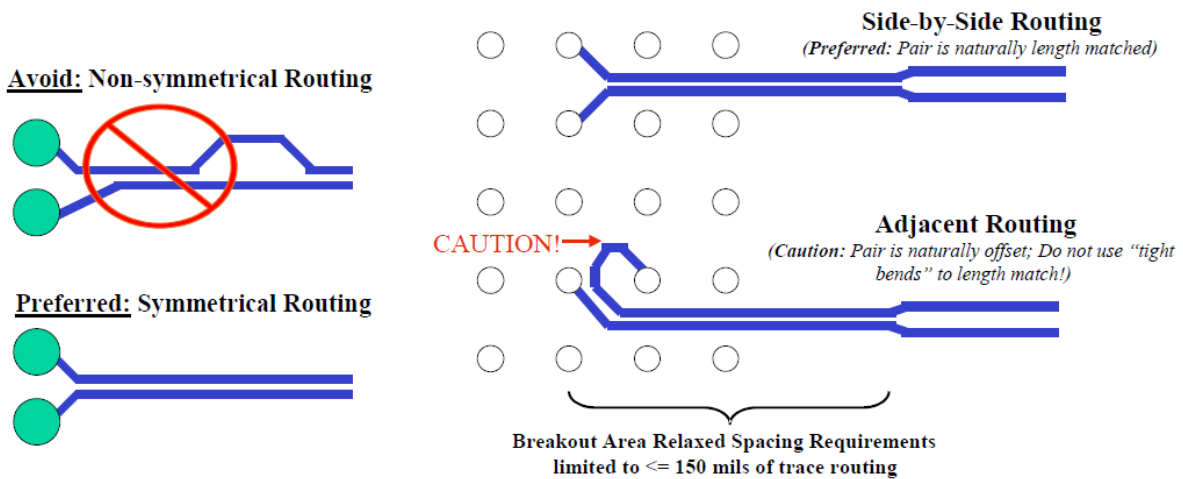


Figure 6-8: Layout Guidance of Matched Differential Pair

- For minimal crosstalk, inter-pair spacing between two differential micro-strip pairs should be at least 20 mils or 4 times the dielectric thickness of the PCB.
- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.

- To minimize signal loss and jitter, tight bend is not recommended. All angles  $\alpha$  should be at least 135 degrees. The inner air gap A should be at least 4 times the dielectric thickness of the PCB.

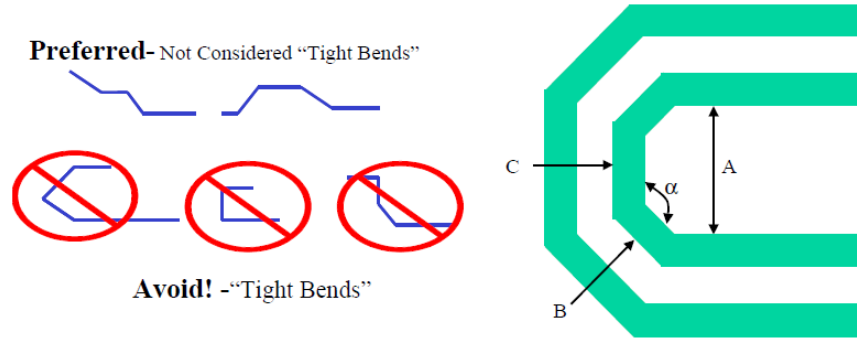


Figure 6-9: Layout Guidance of Bends

- Stub creation should be avoided when placing shunt components on a differential pair.

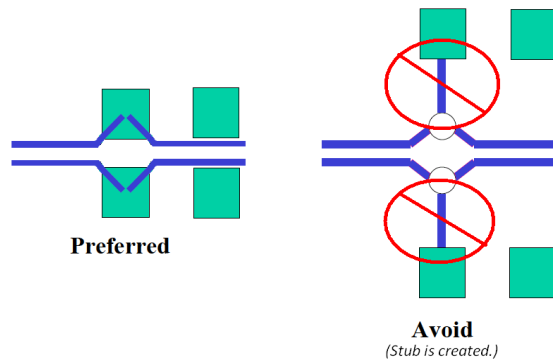


Figure 6-10: Layout Guidance of Shunt Component

- Placement of series components on a differential pair should be symmetrical.

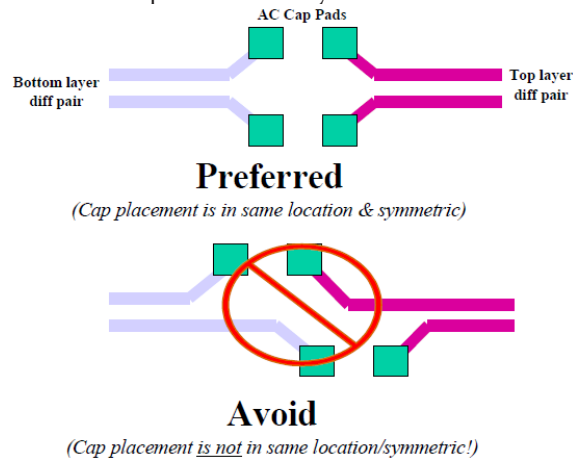


Figure 6-11: Layout Guidance of Series Component

- Stitching vias or test points must be used sparingly and placed symmetrically on a differential pair.

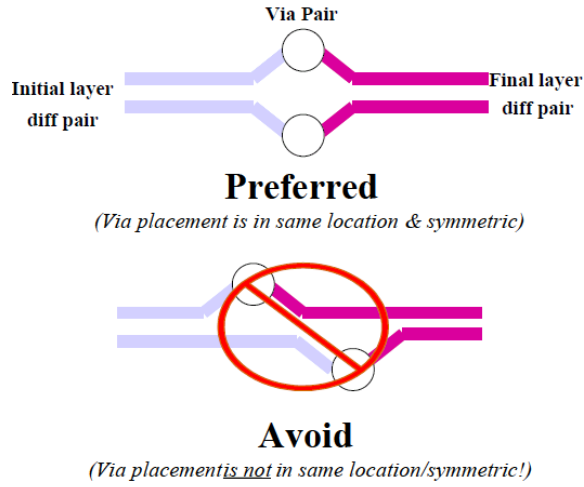


Figure 6-12: Layout Guidance of Stitching Via

### 6.3 DisplayPort 1.2 Test Report

Internal DisplayPort test setup is shown below for the reference.

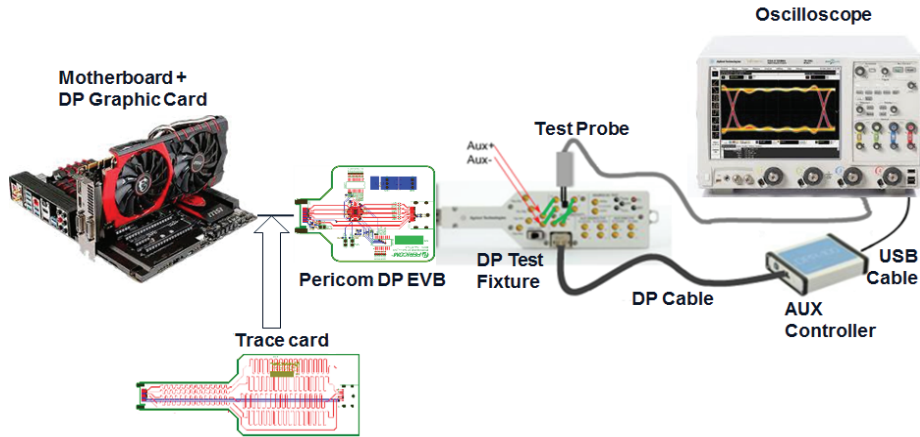


Figure 6-13: DisplayPort Test Set-up

Table 6-1: CTS Trace card insertion loss information

| DP FR4 trace             | 0 in     | 6 in     | 12 in    | 18 in     | 24 in     | 30 in     | 36 in     |
|--------------------------|----------|----------|----------|-----------|-----------|-----------|-----------|
| Insertion loss @ 5.4Gbps | -5.27 dB | -7.24 dB | -9.21 dB | -11.75 dB | -13.28 dB | -15.27 dB | -19.08 dB |

## DisplayPort Test Report

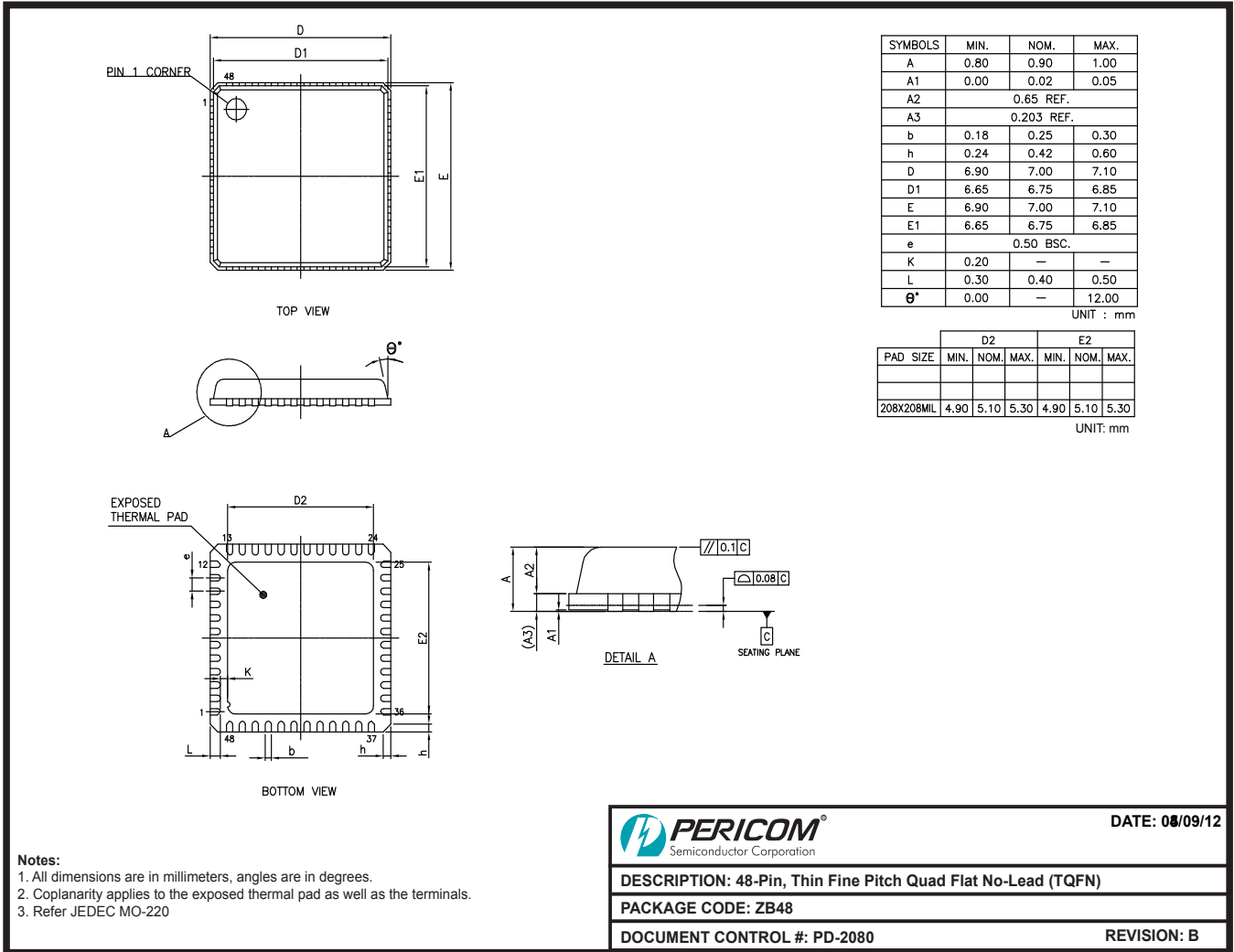
**Overall Result: PASS**

| Test Configuration Details |   |
|----------------------------|---|
| Device Description         |   |
| Test Specification         | 1.2b  |
| Test Session Details       |   |
| Fixture Type               | Agilent W2641B  |
| Infiniium SW Version       | 05.20.0013  |
| Infiniium Model Number     | DSOX92504A  |
| Infiniium Serial Number    | MY54410104  |
| Application SW Version     | 3.41  |
| Debug Mode Used            | No  |
| Probe (Channel 1)          | Model: N2801A<br>Serial: US54094067<br>Head: N5444A<br>Atten: Calibrated (18 FEB 2015 11:16:48), Using Cal Atten (5.7831E+000)<br>Skew: Calibrated (18 FEB 2015 11:16:56), Using Cal Skew |
| Probe (Channel 2)          | Model: N2801A<br>Serial: US54094054<br>Head: N5444A<br>Atten: Calibrated (18 FEB 2015 11:19:29), Using Cal Atten (5.5882E+000)<br>Skew: Calibrated (18 FEB 2015 11:13:57), Using Cal Skew |
| Probe (Channel 3)          | Model: N2801A<br>Serial: US54094059<br>Head: N5444A<br>Atten: Calibrated (18 FEB 2015 11:15:19), Using Cal Atten (5.7320E+000)<br>Skew: Calibrated (18 FEB 2015 11:15:29), Using Cal Skew |
| Probe (Channel 4)          | Model: N2801A<br>Serial: US54094057<br>Head: N5444A<br>Atten: Calibrated (18 FEB 2015 11:11:30), Using Cal Atten (5.5123E+000)<br>Skew: Calibrated (18 FEB 2015 11:12:12), Using Cal Skew |
| Last Test Date             | 2016-04-01 15:49:55 UTC +08:00  |

Figure 6-14: DisplayPort 1.2 Compliance Test Report

## 7. Mechanical/Packaging

### 7.1 Package Mechanical Outline



12-0459

Figure 7-1: Package TQFN-48 (ZB) Mechanical Outline Dimension



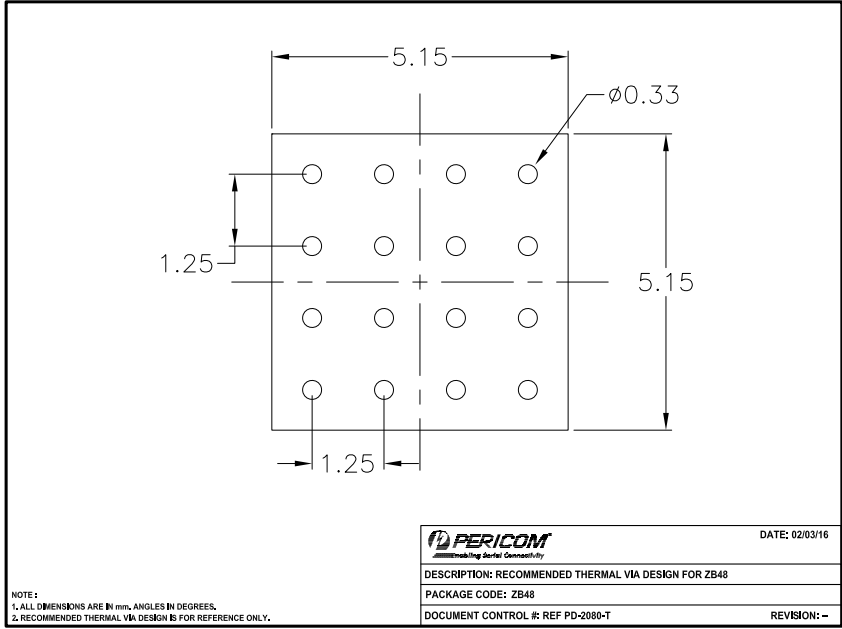


Figure 7-2: TQFN-48 (ZB) Thermal Via Pad Area

## 7.2 Part Marking Information

Our standard product mark follows our standard part number ordering information, except for those products with a speed letter code. The speed letter code mark is placed after the package code letter, rather than after the device number as it is ordered. After electrical test screening and speed binning has been completed, we then perform an “add mark” operation which places the speed code letter at the end of the complete part number.

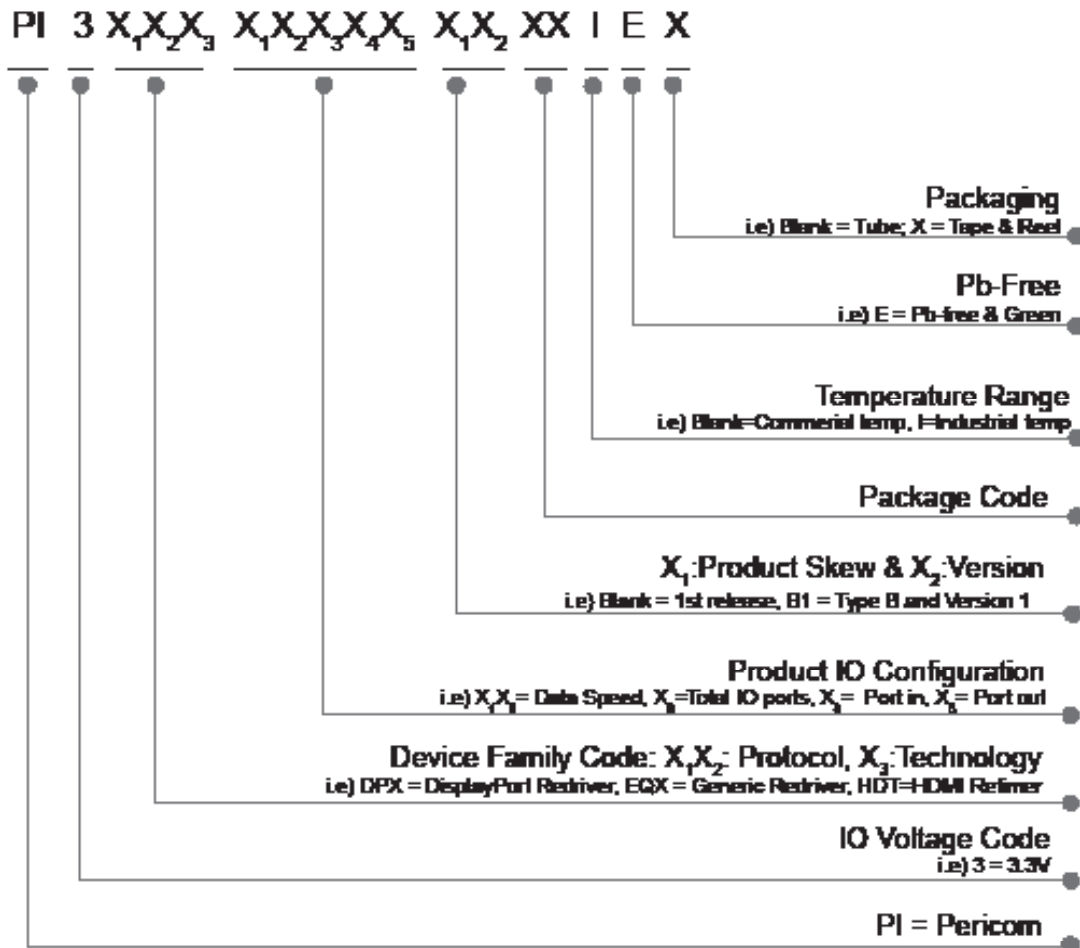


Figure 7-3: General Part marketing information

### 7.3 Tape & Reel Materials and Design

#### Carrier Tape

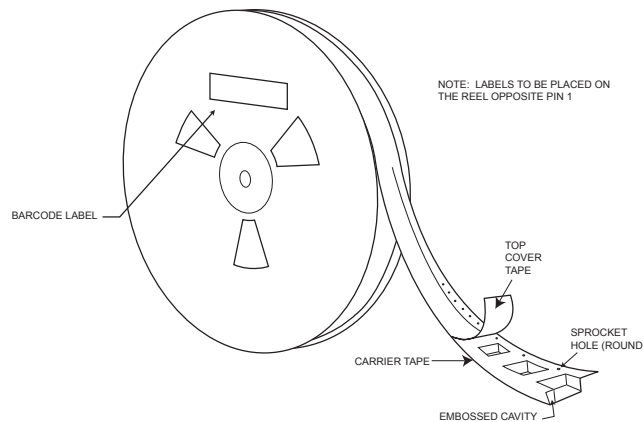
The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is  $10^6$  Ohm/sq. maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 3 and 4 for carrier tape dimensions.

#### Cover Tape

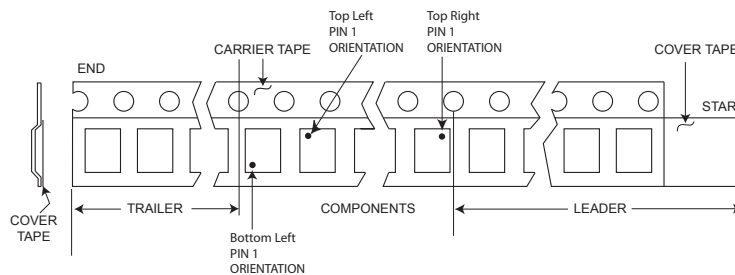
Cover tape is made of Anti-static Transparent Polyester film. The surface resistivity is  $10^7$  Ohm/Sq. Minimum to  $10^{11}$  Ohm sq. maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

#### Reel

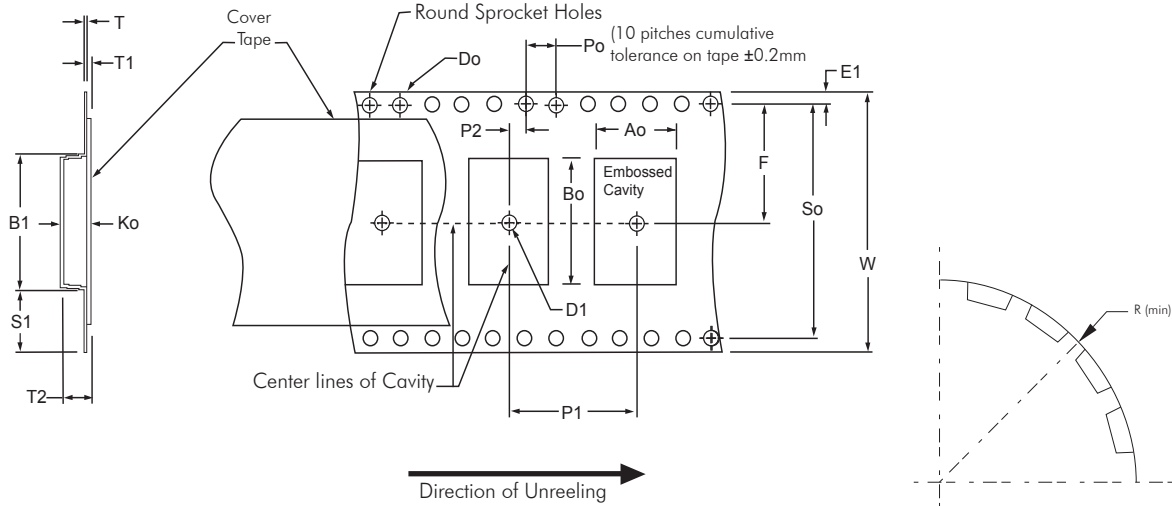
The device loading orientation is in compliance with EIA-481, current version (Figure 2). The loaded carrier tape is wound onto either a 13-inch reel, (Figure 4) or 7-inch reel. The reel is made of Anti-static High-Impact Polystyrene. The surface resistivity  $10^7$  Ohm/sq. minimum to  $10^{11}$  Ohm/sq. max.



**Figure 7-4: Tape & Reel label information**



**Figure 7-5: Tape leader and trailer pin 1 orientations**



**Figure 7-6: Standard embossed carrier tape dimensions**

**Table 7-1: Constant Dimensions**

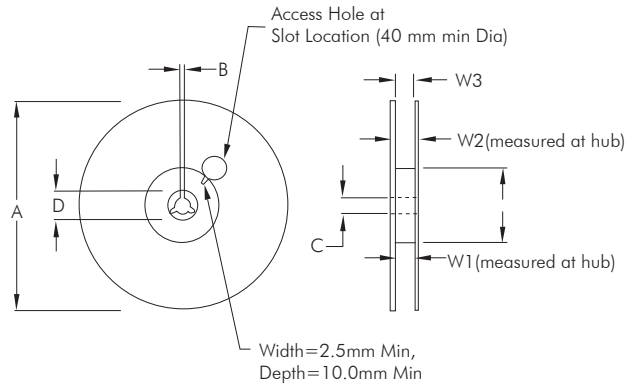
| Tape Size | D <sub>0</sub>   | D <sub>1</sub> (Min) | E <sub>1</sub> | P <sub>0</sub>      | P <sub>2</sub> | R(See Note 2) | S <sub>1</sub> (Min) | T (Max) | T <sub>1</sub> (Max) |                     |
|-----------|------------------|----------------------|----------------|---------------------|----------------|---------------|----------------------|---------|----------------------|---------------------|
| 8mm       | 1.5 +0.1<br>-0.0 | 1.0                  | 1.75 ± 0.1     | 4.0 ± 0.1           | 2.0 ± 0.05     | 25            | 0.6                  | 0.6     | 0.1                  |                     |
| 12mm      |                  | 1.5                  |                |                     | 2.0 ± 0.1      | 30            |                      |         |                      |                     |
| 16mm      |                  | 2.0                  |                |                     | 2.0 ± 0.1      | 50            |                      |         |                      | N/A<br>(See Note 3) |
| 24mm      |                  | 2.0                  |                |                     | 2.0 ± 0.15     |               |                      |         |                      |                     |
| 32mm      |                  | 2.0                  |                |                     | 2.0 ± 0.15     | 50            | N/A<br>(See Note 3)  |         |                      |                     |
| 44mm      | 2.0              | 2.0 ± 0.15           | 50             | N/A<br>(See Note 3) |                |               |                      |         |                      |                     |

**Table 7-2: Variable Dimensions**

| Tape Size | P <sub>1</sub>  | B <sub>1</sub> (Max) | E <sub>2</sub> (Min) | F           | So               | T <sub>2</sub> (Max.) | W (Max) | A <sub>0</sub> , B <sub>0</sub> , & K <sub>0</sub> |
|-----------|---|----------------------|----------------------|-------------|------------------|-----------------------|---------|--|
| 8mm       | Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information) | 4.35                 | 6.25                 | 3.5 ± 0.05  | N/A (see note 4) | 2.5                   | 8.3     | See Note 1   |
| 12mm      |   | 8.2                  | 10.25                | 5.5 ± 0.05  |                  | 6.5                   | 12.3    |  |
| 16mm      |   | 12.1                 | 14.25                | 7.5 ± 0.1   |                  | 8.0                   | 16.3    |  |
| 24mm      |   | 20.1                 | 22.25                | 11.5 ± 0.1  |                  | 12.0                  | 24.3    |  |
| 32mm      |   | 23.0                 | N/A                  | 14.2 ± 0.1  | 28.4 ± 0.1       | 32.3                  |         |  |
| 44mm      |   | 35.0                 | N/A                  | 20.2 ± 0.15 | 40.4 ± 0.1       | 44.3                  |         |  |

**NOTES:**

- A<sub>0</sub>, B<sub>0</sub>, and K<sub>0</sub> are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20° maximum for 8 and 12 mm carrier tapes and 10° maximum for 16 through 44mm.
- Tape and components will pass around reel with radius "R" without damage.
- S<sub>1</sub> does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where D<sub>0</sub> ≥ S<sub>1</sub>.
- So does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.



**Table 7-3: Reel dimensions by tape size**

| Tape Size | A                   | N (Min)<br>See Note A  | W1                | W2(Max) | W3  | B (Min) | C                 | D (Min) |
|-----------|---------------------|------------------------|-------------------|---------|---|---------|-------------------|---------|
| 8mm       | 178                 | 60 ±2.0mm or 100±2.0mm | 8.4 +1.5/-0.0 mm  | 14.4 mm | Shall Accommodate Tape Width Without Interference | 1.5mm   | 13.0 +0.5/-0.2 mm | 20.2mm  |
| 12mm      | ±2.0mm or 330±2.0mm |                        | 12.4 +2.0/-0.0 mm | 18.4 mm |   |         |                   |         |
| 16mm      | 330 ±2.0mm          | 100 ±2.0mm             | 16.4 +2.0/-0.0 mm | 22.4 mm |   |         |                   |         |
| 24mm      |                     |                        | 24.4 +2.0/-0.0 mm | 30.4 mm |   |         |                   |         |
| 32mm      |                     |                        | 32.4 +2.0/-0.0 mm | 38.4 mm |   |         |                   |         |
| 44mm      |                     |                        | 44.4 +2.0/-0.0 mm | 50.4 mm |   |         |                   |         |

**NOTE:**

A. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min)) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.

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## 8. Important Notice

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- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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## JONHON

«JONHON» (основан в 1970 г.)

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«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

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