DEMO CIRCUIT 1600
QUICK START GUIDE

LTC6412 and LTC2261-14
Low-Power, Direct-to-Digital
IF Receiver with Variable Gain

DESCRIPTION

The demonstration circuit 1600A supports the LTC6412 Analog-Controlled VGA driving LTC's family of 1.8V, 14/12 Bit, 80-125Msps ADC's. The 1600A derives from demonstration circuits 1369A and 1464A by combining the VGA and ADC functions with a suitable matching and anti-aliasing interface circuit to form a fully functional direct-to-digital IF receiver. Figure 1 shows a simplified schematic of DC1600A. The nominal WCDMA performance of this VGA+ADC combination is described and reported in LTC Design Note DN482. Full circuit schematics are included at the end of this document.

DC1600A supports the LTC2261 family's double-data rate (DDR) low-voltage differential signaling (LVDS) data output mode to the parallel data edge connector. This DDR LVDS output mode and edge connector is fully compatible with the LTC DC890 FastDAACs interface board and PScope data acquisition and analysis tools. Connection to these evaluation tools is further described in this guide.

Design files for this circuit board are available. Call the LTC factory.

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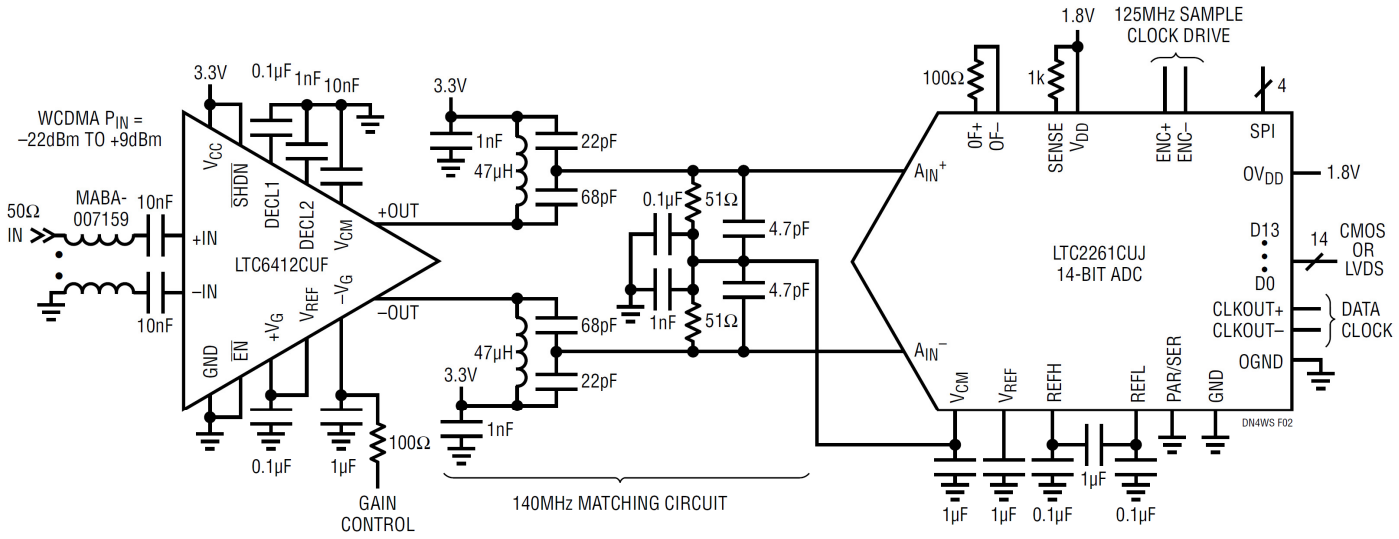


Figure 1. DC1600A Simplified Schematic

DEFAULT CONFIGURATION

Demonstration circuit 1600A is currently available in one default assembly configuration featuring the LTC6412 VGA and LTC2261-14 ADC with an interface circuit tuned for a wideband IF at 140MHz.

The default assembly includes the LTC2261-14, but the user can substitute and assemble any of the 14/12 Bit ADC's from the LTC2261 family of products including LTC2261-14, LTC2261-12, LTC2260-14, LTC2260-12, LTC2259-14, and LTC2259-12.

The input circuit to the VGA employs a balun to provide a single-ended 50 Ohm analog input impedance over a frequency range of 10MHz to 500MHz. Connections to the input balun can be reconfigured for 50 Ohm differential drive.

The encode clock is also configured for single-ended drive to a high impedance digital input. This clock signal requires proper filtering and termination to achieve the best ADC performance. These requirements are described further in this guide.

The interface circuit layout between the VGA and ADC is flexible to accommodate a variety of tuning and matching circuits over an intermediate frequency range of 70MHz to 240MHz. Several tuning options and component values are described further in this guide.

Table 1. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage – DC1600A	Depending on sampling rate and the ADC assembled, this supply must provide up to 250mA.	Optimized for 4.0V [4.0V ⇔6.0V min/max]
ADC Analog Input Range	Set by SENSE pin voltage from EXT REF turret. With no connection to EXT REF, the SENSE pin voltage pulls high to set the ADC analog input range to 2Vpp.	$1V_{PP}$ to $2V_{PP}$
Logic Input Voltages	Minimum Logic High	1.3V
	Maximum Logic Low	0.6V
Logic Output Voltages (differential)	Nominal Logic levels (100Ω load, 3.5mA Mode)	350mV/1.25V common mode
	Minimum Logic levels (100Ω load, 3.5mA Mode)	247mV/1.25V common mode
Sampling Frequency (Convert Clock Frequency)	LTC2261 LTC2260 LTC2259	125 Msps 105 Msps 80 Msps
Convert Clock Level	Single ended Encode Mode (ENC- tied to GND)	0–3.6V
Convert Clock Level	Differential Encode Mode (ENC- not tied to GND)	0.2V–3.6V
Resolution	LTC2261-14, LTC2260-14, LTC2259-14 LTC2261-12, LTC2260-12, LTC2259-12	14 Bits 12 Bits
Input frequency range	Default Assembly Configuration With Modified VGA/ADC Interface Tuning	100MHz – 180MHz 10MHz – 270MHz
ADC SFDR	See Applicable Data Sheet for ADC specifications	
ADC SNR	See Applicable Data Sheet for ADC specifications	

QUICK START PROCEDURE

Demonstration circuit 1600A is easy to set up to evaluate the performance of the LTC2261 A/D converters. Refer to Figure 2 for proper measurement equipment setup and follow the procedure below:

SETUP

If a DC890 FastDAACS Data Acquisition and Collection System was supplied with the DC1600 demonstration circuit, follow the DC890 Quick Start Guide to install the required software and connect the DC890 to both the DC1600 and a PC running Windows98, 2000 or XP.

CIRCUIT BOARD JUMPERS AND TURRETS

The DC1600 demonstration circuit board should have the following jumper settings as default positions: (as per Figure 2).

JP2: PAR/SER : Selects Parallel or Serial programming mode. (Default - Serial)

JP3: Duty Cycle Stabilizer: Enables/ Disable Duty Cycle Stabilizer. (Default - Enable)

JP4: SHDN: Enables and disables the LTC2261. (Default - Enable → Power UP).

Three turrets need supply and control for minimum operation. The balance of turrets can be left NC (not connected) for proper operation.

GND: Global PCB Ground. Redundant turrets are located around the top and left side of the board.

V+: DC Supply. 4-6V at approximately 250mA. On-board regulators supply the lower voltages as needed.

–VG: VGA Gain Control. Apply 0V–1.2V for Gmax to Gmin control. NC pulls pin low for Gmax.

CENTER FREQUENCY ADJUST

The analog input balun, VGA, and ADC are inherently broadband devices, but the interstage matching circuit is not. This matching circuit routes bias current to the VGA while performing a low-Q impedance transformation to the 100Ω differential load at the input of the ADC. The default assembly produces a tuned center frequency of 140MHz and a 1dB BW of 115-175MHz. Table 2 shows component values to achieve other common IF values with similar percentage bandwidths.

Table 2. Frequency Scaled Components of the VGA-to-ADC Tuned Matching Circuit

CENTER FREQUENCY	L7/L8 Coilcraft 0603CS	C9/C62 NPO/COG, 5%	C10/C63 NPO/COG, 5%	COMMENT
70 MHz	100 nH	150 pF	47 pF	
140 MHz	47 nH	68 pF	22 pF	DEFAULT ASSEMBLY
240 MHz	24 nH	39 pF	12 pF	

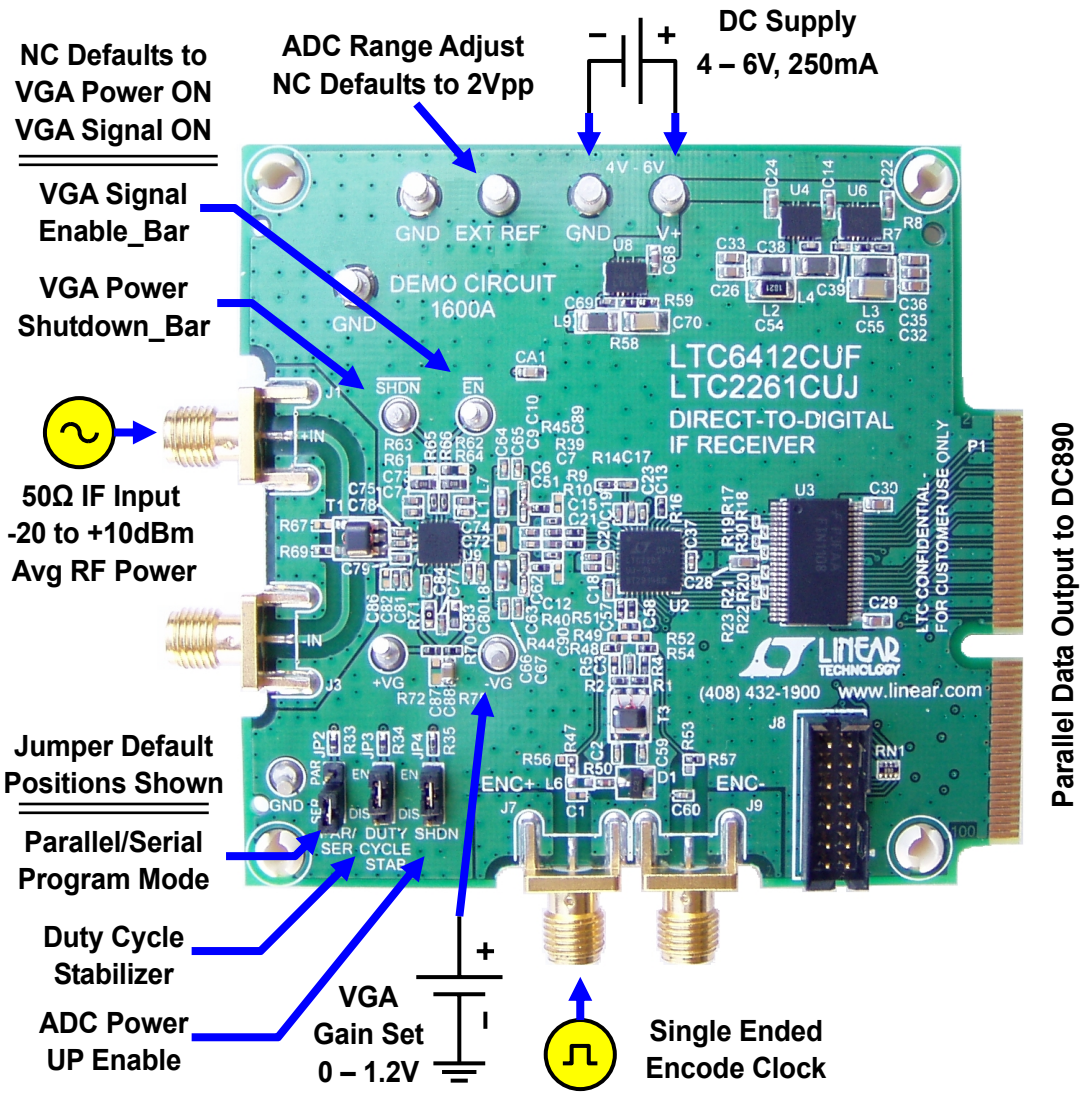


Figure 2. DC1600A Setup. The Minimum Hookup Requires DC Supply, Encode Clock, IF Input, and Connection to DC890.

APPLYING POWER AND SIGNALS TO THE DC1600 DEMONSTRATION CIRCUIT

If a DC890 is used to acquire data from the DC1600, the DC890 must FIRST be connected to a powered USB port or provided an external 6-9V BEFORE applying +4.0V to +6.0V across the pins marked "V+" and "GND" on the DC1600. DC1600 requires a minimum of 4.0V for proper operation. Regulators on the board produce the voltages required for the ADC and VGA. The DC1600 demonstration circuit requires up to 250mA depending on the sampling rate and the A/D converter installed.

The DC890 data collection board is powered by the USB cable. If the available USB port cannot support the required 700mA supply current, then the user must connect an external 6-9V supply on turrets G7(+) and G1(-) or the adjacent 2.1mm power jack.

ANALOG INPUT NETWORK

The 1:1 balun transformer connected from the LTC6412 VGA input to J1 provides a uniform 50 Ohm input impedance over the frequency range of 10MHz to 500MHz. The VGA and transformer effectively buffers and decouples the receiver input from the fluctuating impedance of the ADC input.

In most cases, filters are required on both the analog input and encode clock to provide datasheet performance. A SAW filter is often used to limit the input band of interest, and a band pass filter is connected to the input of the DC1075A clock shaping circuit. The DC1600 will function well without these filter embellishments, but the highest SNR, lowest spur and best phase noise performance requires careful filtering.

The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50 Ohm outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

If your generator cannot deliver full scale input signals without distortion, you may benefit from a high-OIP3, GaAs-based power amplifier prior to the final filter. A high order filter can be used before this final amplifier, and a relatively lower Q filter used between the amplifier and the demo circuit.

ENCODE CLOCK

NOTE: Apply an encode clock to the SMA connector on the DC1600 demonstration circuit board marked "J7". The DC1600 default assembly is populated to provide a single ended input.

For the best noise performance, the ENCODE INPUT must be driven with a very low jitter, square wave source. The amplitude should be large, up to 3Vpp or 13dBm. When using a sinusoidal signal generator a squaring circuit can be used. Linear Technology also provides demo board DC1075A to divide a high frequency sine wave by four, producing a low jitter square wave for best results with the LTC2261.

Using band pass filters on the clock and the analog input will improve the SNR performance by reducing the wideband noise power of the signals. A band pass filter on the clock line should be inserted just before the DC1075A. Datasheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non harmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used with TTE band pass filters for both the Clock input and the Analog input.

Apply the analog input signal of interest to the SMA connectors on the DC1600 demonstration circuit board marked "J1 +IN". In the default assembly configuration, this 50Ω single-ended input connects to a wideband balun which feeds the resulting differential signal to the VGA input.

At maximum VGA gain, a single tone input power of -10dBm at J1 will present a full scale signal to the ADC input at the IF center frequency. Signals with modulation require additional back-off of input power proportional to the Peak-to-Average (PAR) of the signal. For example, a signal with 8dB PAR would need -18dBm average input power to operate near the ADC full scale range.

An internally generated conversion clock output is available on the edge connector, P1. This signal can be collected via a logic analyzer, or other data collection system if populated with a SAMTEC MEC8-150 type connector or collected by the DC890 QuickEval-II Data Acquisition Board using PScope software.

SOFTWARE

The DC890B is controlled by the PScope System Software provided or downloaded from the Linear Technology website at http://www.linear.com/software/. If a DC890B was provided, follow the DC890 Quick Start Guide and the instructions below.

The data collection software can be started with or without the DC1600 connected. If "PScope.exe" is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

When the DC1600 demonstration circuit is properly connected to the DC890, PScope should automatically detect the DC1600 and configure itself identically to the

DC1369A-A demo board for the LTC2261-14. If necessary the procedure below explains how to manually configure PScope.

Under the "Configure" menu, go to "ADC Configuration...." Check the "Config Manually" box and use the following configuration options, see Figure 3.

Manual Configuration settings:

Bits: 14

Alignment: 14

FPGA Ld: DDR LVDS

Channs: 2

Bipolar: Not Checked

Positive-Edge Clk: Checked

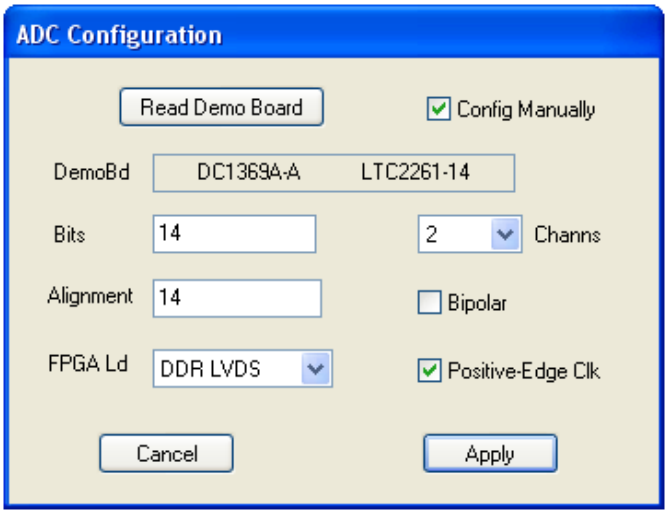


Figure 3. ADC Configuration

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the "Collect" button should produce time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC890B Quick Start Guide and in the online help available within the PScope program itself.

SERIAL PROGRAMMING

PScope can program the DC1600 ADC serially through the DC890. Several options available in the LTC2261 ADC family are available only through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the "Set Demo Bd Options" icon on the PScope toolbar (Figure 4). This will bring up the menu shown in figure 5.

Figure 4. PScope Toolbar

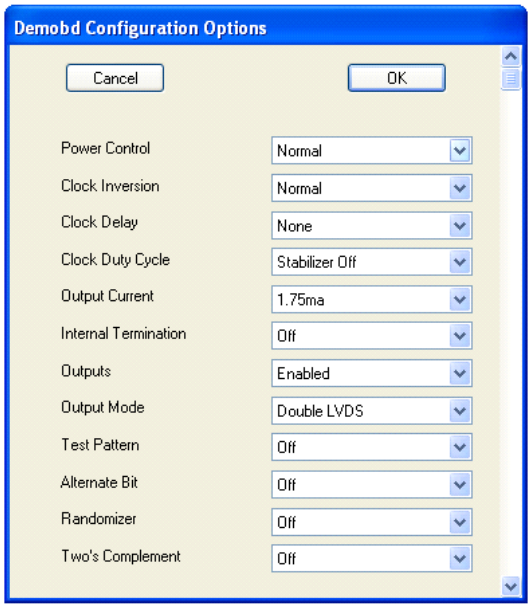


Figure 5. Demoboard Configuration Options

This menu allows any of the options available for the LTC2261 family to be programmed serially. Brief descriptions are given below. The LTC2261 program options are described more completely in the datasheet.

Power Control – Selects between normal operation, nap, and sleep modes:

- Normal (Default) – Entire ADC is powered, and active

- Nap – ADC core powers down, references stay active.

- Shutdown – The entire ADC is powered down.

Clock Inversion – Selects the polarity of the CLKOUT signal:

- Normal (Default) – Normal CLKOUT polarity
- Inverted – CLKOUT polarity is inverted

Clock Delay - Selects the phase delay of the CLKOUT signal:

- None (Default) – No CLKOUT delay
- 45 deg – CLKOUT delayed by 45 degrees
- 90 deg – CLKOUT delayed by 90 degrees
- 135 deg – CLKOUT delayed by 135 degrees

Clock Duty Cycle – Enable or disables Duty Cycle Stabilizer

- Stabilizer off (Default) –Duty Cycle Stabilizer Disabled
- Stabilizer on – Duty Cycle Stabilizer Enabled

Output Current – Selects the LVDS output drive current

- 1.75mA (Default) - LVDS output driver current
- 2.1mA - LVDS output driver current
- 2.5mA - LVDS output driver current
- 3.0mA - LVDS output driver current
- 3.5mA - LVDS output driver current
- 4.0mA - LVDS output driver current
- 4.5mA - LVDS output driver current

Internal Termination – Enables LVDS internal termination

- Off (Default) – Disables internal termination
- On – Enables internal termination

Outputs – Enables Digital Outputs

- Enabled (Default) – Enables digital outputs
- Disabled – Disables digital outputs

Output Mode – Selects Digital output mode

- Full Rate – Full rate CMOS output mode (This mode is not supported by the DC1600A to avoid digital feedback)
- Double LVDS (Default) – double data rate LVDS output mode
- Double CMOS – double data rate CMOS output mode (This mode is not supported by the DC1600A to avoid digital feedback)

Test Pattern – Selects Digital output test patterns

- Off (Default) – ADC data presented at output
- All out =1 – All digital outputs are 1
- All out = 0 – All digital outputs are 0
- Checkerboard - OF, and D13-D0 Alternate between 101 0101 1010 0101 and 010 1010 0101 1010 on alternating samples.
- Alternating – Digital outputs alternate between all 1's and all 0's on alternating samples.

Alternate Bit – Alternate Bit Polarity (ABP) Mode

- Off (Default) – Disables alternate bit polarity
- On – Enables alternate bit polarity (Before enabling ABP, be sure the part is in offset binary mode)

Randomizer – Enables Data Output Randomizer to help suppress digital feedback to the analog input.

- Off (Default) – Disables data output randomizer
- On – Enables data output randomizer

Two's Complement – Enables two's complement mode

- Off (Default) – Selects offset binary mode
- On – Selects two's complement mode

Once the desired settings are selected, hit OK and PScope will automatically update the register of the device on the DC1600A demo board.

ADDITIONAL INFORMATION

VGA SHUTDOWN AND ENABLE

The factory default configuration is set for a power-on and amplifier-enabled state ($\overline{SHDN}$=1, $\overline{EN}$=0). The $\overline{SHDN}$ pin is pulled high with a 1kΩ resistor to V_{CC}, and the $\overline{EN}$ pin is pulled low with a 1kΩ resistor to ground. The user can override these board-level defaults by applying voltages directly to the $\overline{SHDN}$ and $\overline{EN}$ turrets as needed.

VGA GAIN CONTROL

The default assembly configuration is set for negative gain control slope through the –VG turret. Gain decreases with an increasing –VG voltage. The –VG control turret is low-pass filtered to suppress noise from an unshielded connection and avoid AM up-conversion artifacts. When not connected, –VG pulls low, and the VGA assumes the maximum gain state.

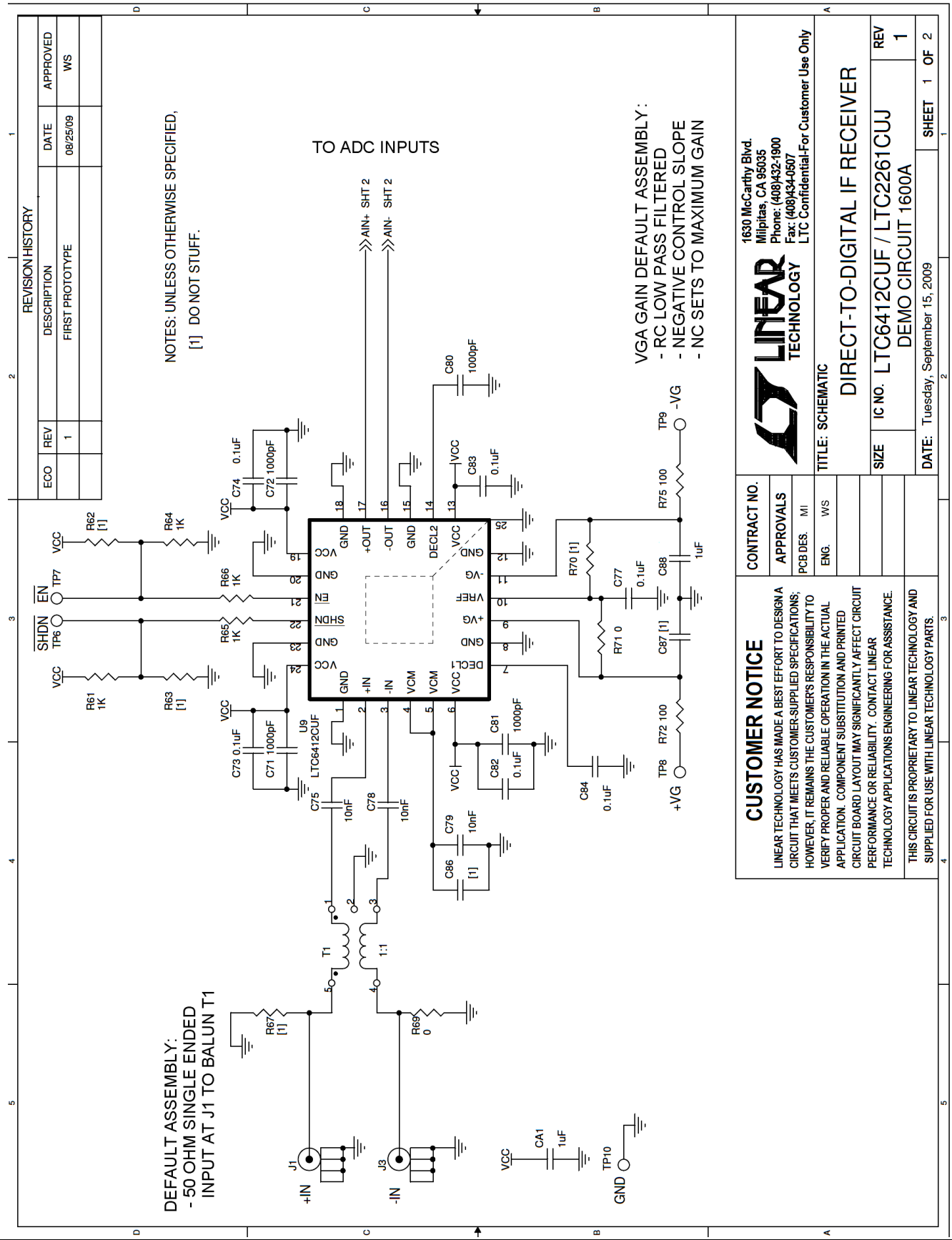
To change to a positive gain control slope configuration, swap the jumper from R71 to R70, and swap the LPF capacitor from C88 to C87. In this configuration, gain increases with an increasing +VG voltage. When not connected, +VG pulls low, and the VGA assumes the minimum gain state.

Removing the LPF capacitor enables the VGA to respond to sub-µsec control signals. When unfiltered, connection to the gain control turret should be shielded to avoid noise contamination of the gain control input.

DIFFERENTIAL ANALOG INPUTS

The analog input connectors J1 and J3 can be configured for differential drive. Remove the jumper at location R69 to enable 50-Ohm differential input drive. T1 effectively passes the intended differential mode signal while attenuating any common mode signal.

Alternatively, the input balun T1 can be removed completely and the ±IN signals at J1 and J3 routed directly to C75 and C78 using 0603 jumpers across the input balun pads. This last configuration closely resembles the board design of a fully differential signal path typical of LTC mixer, amplifier and ADC applications.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NOTES: UNLESS OTHERWISE SPECIFIED,
[1] DO NOT STUFF.
TO ADC INPUTS
VGA GAIN DEFAULT ASSEMBLY:
- RC LOW PASS FILTERED
- NEGATIVE CONTROL SLOPE
- NC SETS TO MAXIMUM GAIN
DEFAULT ASSEMBLY:
- 50 OHM SINGLE ENDED
INPUT AT J1 TO BALUN T1
U9
LTC6412CUF
T1
1:1
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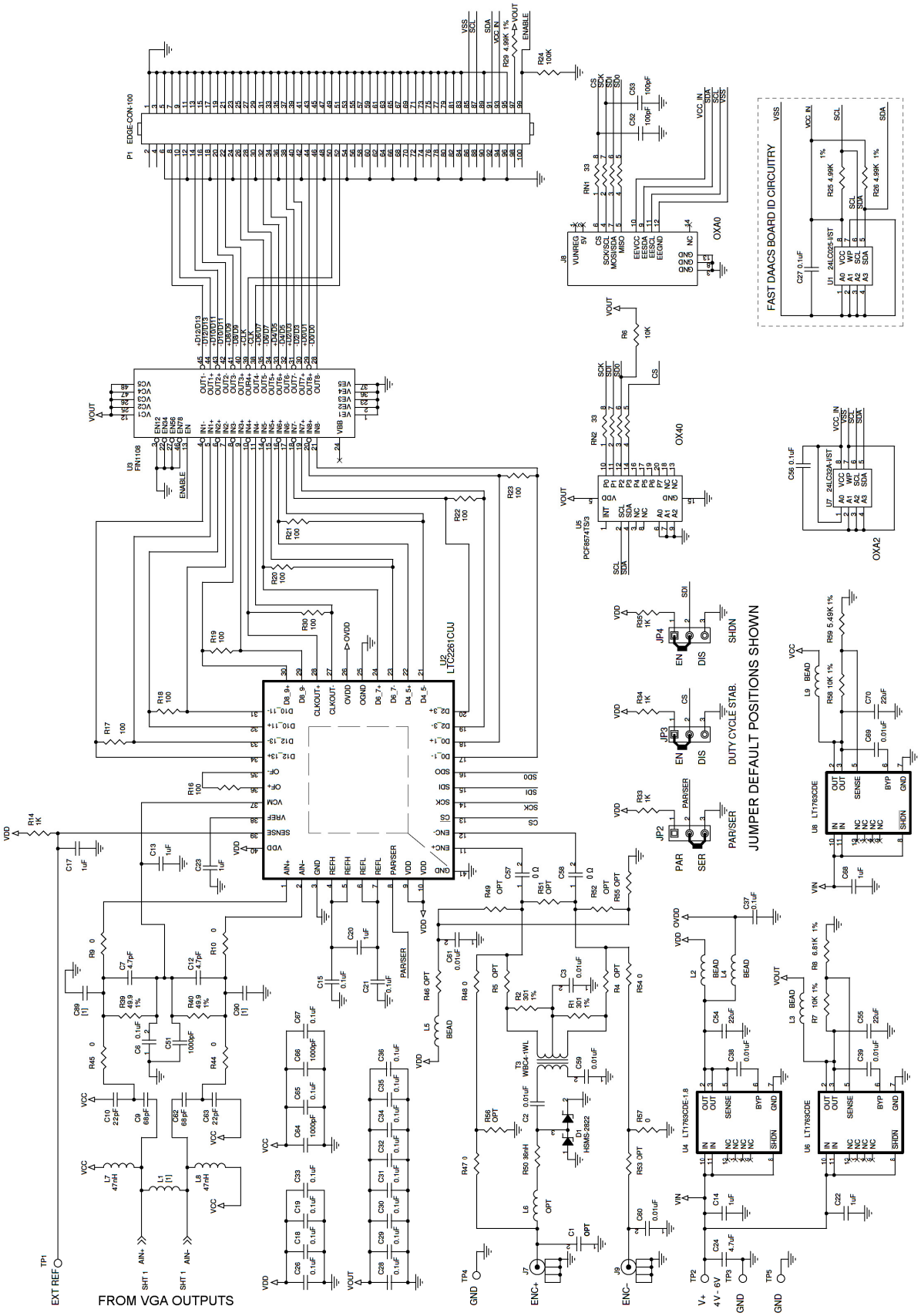
SIZE
IC NO. LTC6412CUF / LTC2261CUJ
DEMO CIRCUIT 1600A
REV 1
DATE: Tuesday, September 15, 2009
SHEET 1 OF 2


FROM VGA OUTPUTS
JUMPER DEFAULT POSITIONS SHOWN
FAST DAACS BOARD ID CIRCUITRY
EXT REF
ENC+
ENC-
GND
V+
4V - 6V
LTC2261CUJ
FIN1108
PCF8574TS/3
LT1763CDE
LT1763CDE-1.8
LT1763CDE
24LC025-I/ST
24LC32A-I/ST
EDGE-CON-100
OXA0
OXA2
OXA40
SHDN
DUTY CYCLE STAB.
PAR/SER
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