19-0941; Rev 3; 6/98

MAXIM

CMOS 12 Bit Multiplying D/A Converter

General Description

The MX7541A is high performance CMOS multiplying 12-bit digital-to-analog converter (DAC). Low power operation and 12 bit (0.012%) linearity make it suitable for a wide range of precision data acquisition and control applications.

Wafer level laser trimmed thin-film resistors and temperature compensated NMOS switches assure true 12-bit performance over the full operating temperature range. In addition, all digital inputs are compatible with both CMOS and TTL logic levels.

Maxim's MX7541A is electrically and pin compatible with the Analog Devices AD7541A and AD7541. Package types include 18-lead standard width DIP and Small Outline packages.

Applications

Machine and Motion Control Systems
Automatic Test Equipment
μP Controlled Calibration Circuitry
Programmable Gain Amplifiers
Digitally Controlled Filters
Programmable Power Supplies

Features

- **12 Bit Linearity (1/2 LSB)**
- **1 LSB Gain Accuracy**
- **Guaranteed Monotonic**
- **Low Power Consumption**
- **Four-Quadrant Multiplication**
- **TTL and CMOS Compatible**
- **Pin-For-Pin Second Source**

Ordering Information

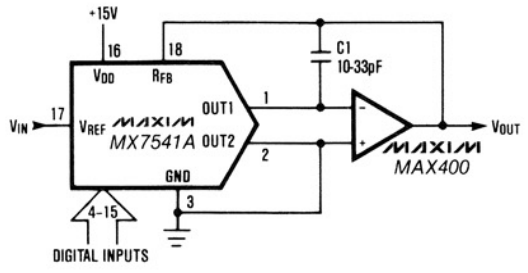
PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MX7541AJN	0°C to +70°C	18 Plastic DIP	1
MX7541AKN	0°C to +70°C	18 Plastic DIP	1/2
MX7541AJCWN	0°C to +70°C	18 SO	1
MX7541AKCWN	0°C to +70°C	18 SO	1/2
MX7541AJP	0°C to +70°C	18 PLCC	1
MX7541AKP	0°C to +70°C	18 PLCC	1/2
MX7541AJ/D	0°C to +70°C	Dice*	1

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

** *Maxim reserves the right to ship ceramic packages in lieu of CERDIP packages.*

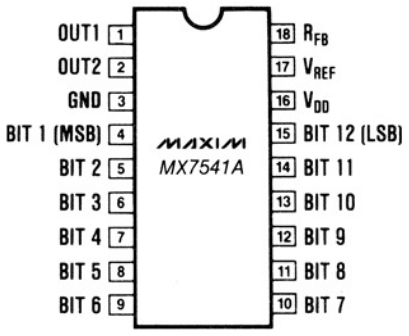
Typical Operating Circuit



Unipolar Operation

Pin Configuration

Top View



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

CMOS 12 Bit Multiplying D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) ..... -0.3V, V_{DD}
Power Dissipation (Derate 6mW/°C above +75°C) 450mW

Operating Temperature Range
Commercial MX7541AJ/AK..... 0° C to +70° C
Industrial MX7541AA/AB ..... -25° C to +85° C
Military MX7541AS/AT ..... -55° C to +125° C
Storage Temperature ..... -65° C to +150° C
Lead Temperature (Soldering 10 secs) ..... +300° C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +15V, V_{REF} = +10V, $V_{OUT1} = V_{OUT2}$ = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
DC ACCURACY (Note 3)							
Resolution				12			Bits
Relative Accuracy		1 LSB = 0.024% FSR 1/2 LSB = 0.012% FSR	MX7541AJ/AA/AS MX7541AK/AB/AT			±1 ±1/2	LSB
Differential Nonlinearity		12 Bit Monotonicity Guaranteed	MX7541AJ/AA/AS MX7541AK/AB/AT			±1 ±1/2	LSB
Gain Error (Note 3)		MX7541AJ/AA/AS MX7541AK/AB/AT	T_A = +25° C T_{MIN} to T_{MAX} T_A = +25° C T_{MIN} to T_{MAX}			±6 ±8 ±1 ±3	LSB
Gain Temperature Coefficient		(Note 2)			2	5	ppm/° C
Output Leakage Current (OUT1 with Digital Inputs = 0V, and OUT2 with Digital Inputs = V_{DD})		MX7541AJ/AK/AA/AB MX7541AS/AT	T_A = +25° C T_{MIN} to T_{MAX} T_A = +25° C T_{MIN} to T_{MAX}			±5 ±10 ±5 ±200	nA
Power Supply Rejection	PSRR	V_{DD} = 15V ±5%	T_A = +25° C T_{MIN} to T_{MAX}			±0.01 ±0.02	%/%V_{DD}
V_{REF} Input Resistance	R_{REF}			7	11	18	kΩ
V_{REF} Resistance Tempco					-300		ppm/° C
DIGITAL INPUTS							
Logic HIGH Threshold	V_{INH}			+2.4			V
Logic LOW Threshold	V_{INL}					+0.8	
Input Leakage Current	I_{IN}	Digital Inputs = 0V or V_{DD}	T_A = +25° C T_{MIN} to T_{MAX}		±0.001	±1	µA
Input Capacitance	C_{IN}	(Note 2)				8	pF
DYNAMIC PERFORMANCE (Note 2)							
Propagation Delay to 90% of Final Analog Output		Digital Input Change 0V to V_{DD} and V_{DD} to 0V, OUT1 Load = 100Ω, C_{EXT} = 13pF, T_A = +25° C			100		ns
Digital to Analog Glitch Impulse		V_{REF} = 0V, Dig. Inputs = 0V to V_{DD} or V_{DD} to 0V			1000		nV-sec
Multiplying Feedthrough Error		V_{REF} = ±10V, 10kHz Sinewave, T_A = +25° C			1		mVp-p
Output Current Settling Time to 0.01% of FSR		Digital Input Change 0V to V_{DD} and V_{DD} to 0V, OUT1 Load = 100Ω, C_{EXT} = 13pF, T_A = +25° C			600		ns
Output Capacitance	C_{OUT}	Digital Inputs = V_{INH} Digital Inputs = V_{INL}	OUT1 OUT2 OUT1 OUT2			200 70 70 200	pF

ELECTRICAL CHARACTERISTICS (continued)

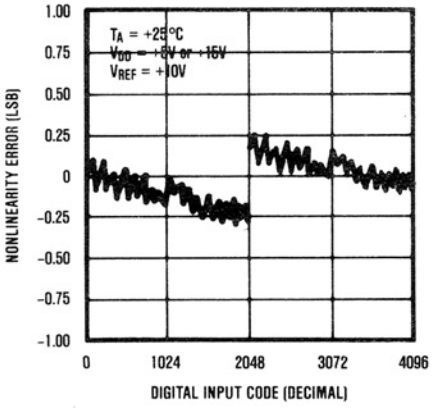
(T_A = T_{MIN} to T_{MAX}, V_{DD} = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
POWER REQUIREMENTS							
Operating Supply Range	V_{DD}	Accuracy Not Guaranteed		+5		+16	V
Power Supply Current	I_{DD}	Digital Inputs = V_{INH} or V_{INL}				2	mA
		Digital Inputs = 0V or V_{DD}	T_A = +25°C			100	μA
			T_{MIN} to T_{MAX}			500	

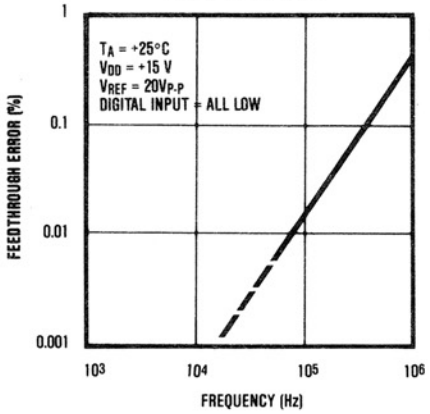
Note 1: $V_{OUT1,2}$ may exceed the Absolute Maximum Voltage rating if the current is limited to 30mA or less.
Note 2: Guaranteed by design but not 100% tested.
Note 3: Measured using internal R_{FB} and includes effect of Leakage Current and Gain Tempco. Gain Error can be trimmed to zero.

Typical Operating Characteristics

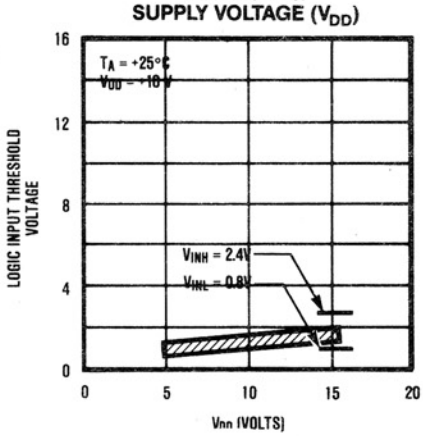
NONLINEARITY ERROR vs. DIGITAL CODE



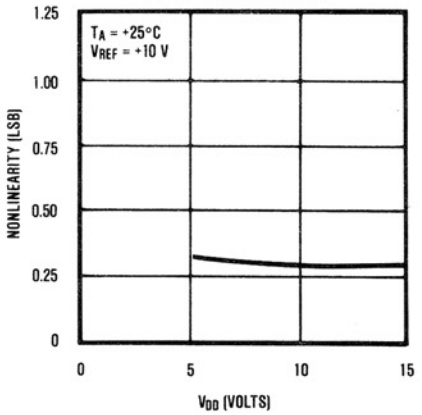
FEEDTHROUGH ERROR vs. FREQUENCY



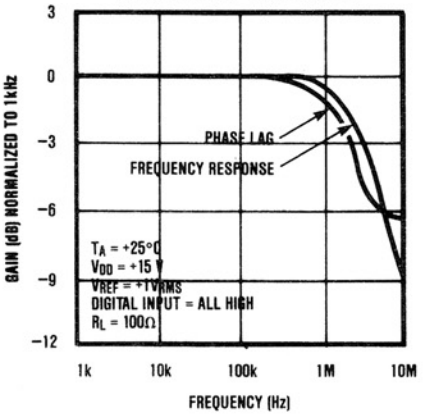
LOGIC INPUT THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE (V_{DD})



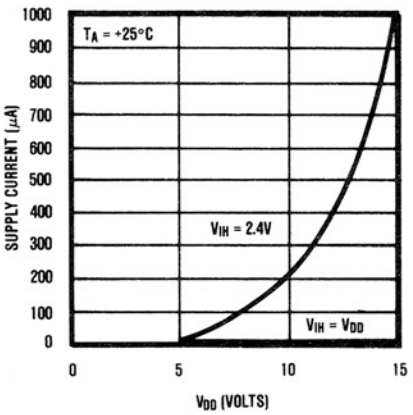
NONLINEARITY vs. SUPPLY VOLTAGE



V_{REF} PHASE LAG AND FREQUENCY RESPONSE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



CMOS 12 Bit Multiplying D/A Converter

Detailed Description

The basic MX7541A DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Although the current at OUT1 or OUT2 will depend on the digital input code, the sum of the two output currents is always equal to the input current at V_{REF} minus the termination resistor current (R_T).

Either current output can be converted into a voltage externally by adding an output amplifier (Figure 4). The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs. If a current source is used for the reference input, then a low temperature coefficient external resistor should be used for R_{FB} to minimize gain variation with temperature.

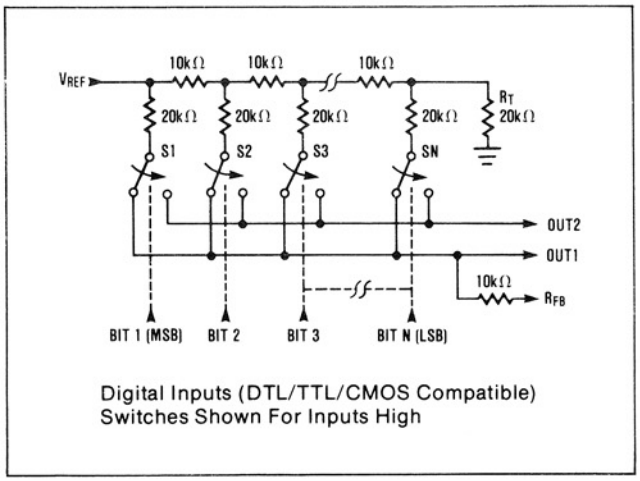


Figure 1. MX7541A Functional Diagram

Equivalent Circuit Analysis

Figures 2 and 3 show the equivalent circuits for the R-2R ladder when all digital inputs are LOW and HIGH respectively. The input resistance at V_{REF} is nominally 11kΩ and does not change with digital input code. The $I_{REF}/4096$ current source, which is actually the ladder termination resistor (R_T, Figure 1), results in an intentional 1-bit current loss to GND. The $I_{LEAKAGE}$ current sources represent junction and surface leakage currents.

Capacitors C_{OUT1} and C_{OUT2} represent the switches' ON and OFF capacitances respectively. When all inputs are switched from LOW to HIGH, the capacitance at OUT1 changes from approximately 70pF to 200pF. This capacitance is code-dependent and is a function of the number of ON switches that are connected to a specific output.

Circuit Configurations

Unipolar Operation

The most common configuration for the MX7541A is shown in Figure 4. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. The code table is given in Table 1. Note that the polarity of the output is the inverse of the reference input.

In many applications, gain adjustment of the MX7541A will not be necessary. In those cases, and also when gain is trimmed but only at the reference source, resistors R1 and R2 in Figure 4 can be omitted. However, if the trims are desired and the DAC is to operate over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used at R1 and R2.

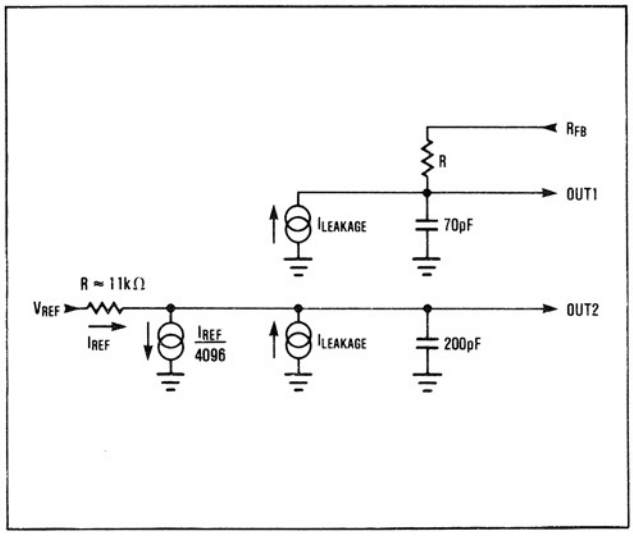


Figure 2. MX7541A DAC Equivalent Circuit, All Digital Inputs LOW

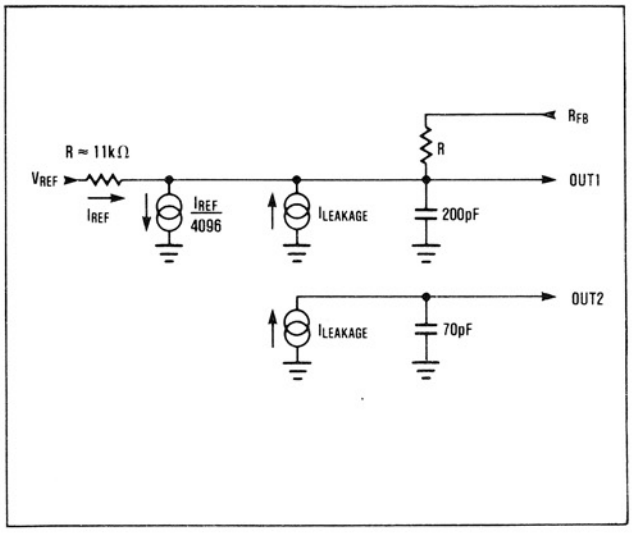
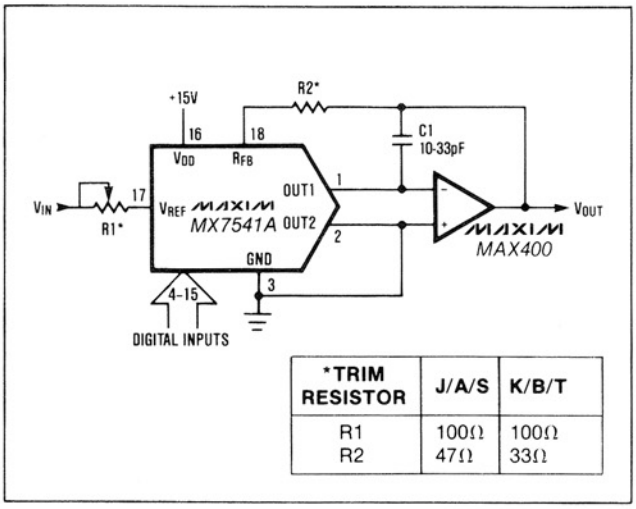
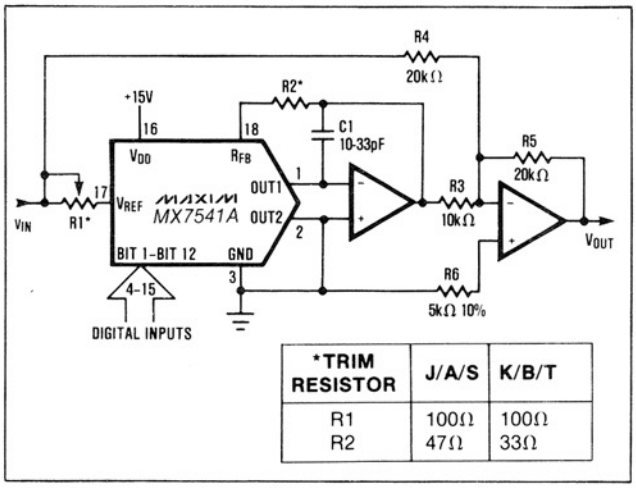


Figure 3. MX7541A DAC Equivalent Circuit, All Digital Inputs HIGH



*TRIM RESISTOR	J/A/S	K/B/T
R1	100Ω	100Ω
R2	47Ω	33Ω

Figure 4. Unipolar Binary Operation



*TRIM RESISTOR	J/A/S	K/B/T
R1	100Ω	100Ω
R2	47Ω	33Ω

Figure 5. Bipolar Operation (4-Quadrant Multiplication)

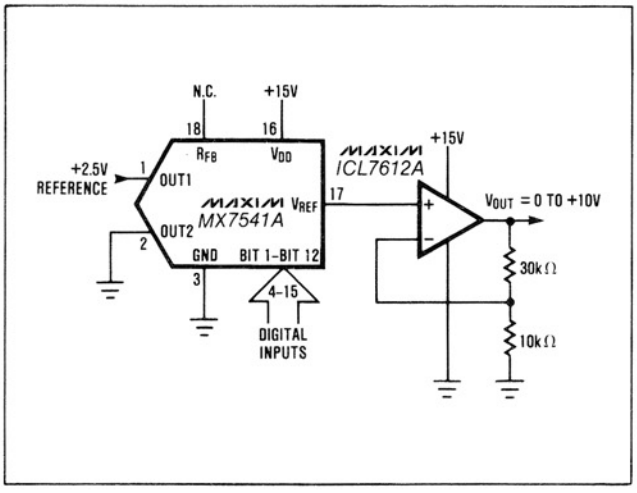


Figure 6. Single Supply Operation Using Voltage Mode

Table 1. Code Table — Unipolar Binary

DIGITAL INPUT MSB											LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{4095}{4096}\right)$
1	0	0	0	0	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2V_{REF}$
0	0	0	0	0	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{1}{4096}\right)$
0	0	0	0	0	0	0	0	0	0	0	0	0V

Table 2. Code Table — Bipolar (Offset Binary) Operation

DIGITAL INPUT MSB											LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{2047}{2048}\right)$
1	0	0	0	0	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{1}{2048}\right)$
1	0	0	0	0	0	0	0	0	0	0	0	0V
0	1	1	1	1	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{1}{2048}\right)$
0	0	0	0	0	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{2048}{2048}\right)$

Bipolar Operation

With the circuit configuration in Figure 5, the MX7541A operates in the bipolar, or four-quadrant multiplying mode. A second amplifier and three matched resistors are required. Matching to 0.01% is recommended for 12 bit performance. The code table for the output, which is "offset binary", is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control amplitude.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. If gain and offset trims are not required, R1 and R2 in Figure 5 can be omitted.

Voltage Mode (Single Supply)

The MX7541A is connected as a voltage output DAC in Figure 6. OUT1 is connected to the reference input and OUT2 is grounded. V_{REF}, now the DAC output, is a voltage source with a constant output resistance of R_{ladder} (nominally 10kΩ). This output is usually buffered with an op-amp.

Two advantages of voltage mode operation are single supply operation and that a negative reference is not required for a positive output. It should also be noted that the reference input (voltage at OUT1) must always be positive and is limited to no more than 2.5V when V_{DD} is 15V. If the reference voltage is greater than 2.5V or V_{DD} is reduced, resistance mismatches in the DAC's internal switches degrade linearity.

Application Information

Output Amplifier Offset

For best linearity, OUT1 and OUT2 should be terminated at exactly 0V. In most applications OUT1 is connected to the summing junction of an inverting op-amp. The amplifier's input offset voltage can degrade the linearity of the DAC by causing OUT1 to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}(1 + R_{FB}/R_O),$$

where V_{OS} is the op-amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code, and varies from approximately 10kΩ to 30kΩ. The error voltage range is then typically $4/3V_{OS}$ to $2V_{OS}$, a change of $2/3V_{OS}$. An amplifier with 3mV of offset will therefore degrade the linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10 of an LSB's value.

The output amplifier input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error. I_B should therefore be much less than the DAC output current for 1 LSB, typically 250nA with V_{REF}=10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier's noninverting input is grounded through a "bias current compensation resistor". This resistor adds to offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-!ead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

Compensation

A compensation capacitor, C1, may be needed when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. Its value depends on the type of op-amp used but typical values range from 10 to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized, and output settling performance improved, by keeping the PC board trace and stray capacitance at OUT1 as small as possible.

Grounding and Bypassing

Since OUT1, OUT2 and the output amp's noninverting input are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, very low resistance (less than 0.2Ω) path. The current at OUT1 and OUT2 varies with input code, creating a code dependent error if these terminals are connected to ground (or a virtual ground) through a resistive path.

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic cap, should be connected as close to the DAC's V_{DD} and GND pins as possible.

The MX7541A has high-impedance digital inputs. To minimize noise pick-up, they should be tied to either VDD or GND when not used. It is also good practice to connect active inputs to VDD or GND through high valued resistors (1MΩ) to prevent static charge accumulation if these pins are left floating, such as when a circuit card is left unconnected.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

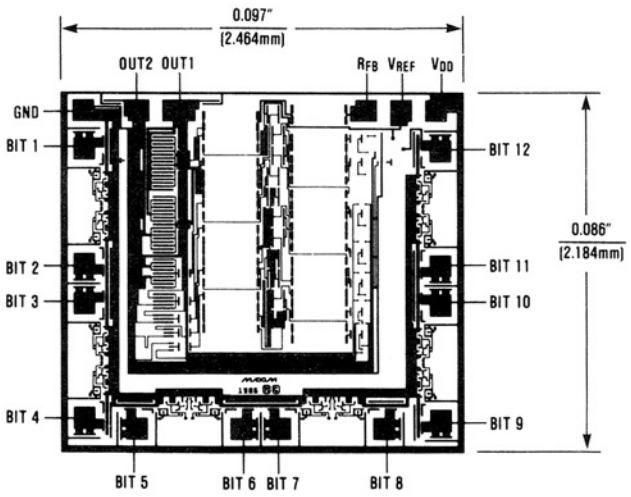
_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MX7541AJEWN	-40°C to +85°C	18 SO	1
MX7541AKEWN	-40°C to +85°C	18 SO	1/2
MX7541AAQ	-40°C to +85°C	18 CERDIP**	1
MX7541ABQ	-40°C to +85°C	18 CERDIP**	1/2
MX7541AAD	-40°C to +85°C	18 Ceramic SB	1
MX7541ABD	-40°C to +85°C	18 Ceramic SB	1/2
MX7541ASQ	-55°C to +125°C	18 CERDIP**	1
MX7541ATQ	-55°C to +125°C	18 CERDIP**	1/2
MX7541ASD	-55°C to +125°C	18 Ceramic SB	1
MX7541ATD	-55°C to +125°C	18 Ceramic SB	1/2

* *Contact factory for dice specifications.*

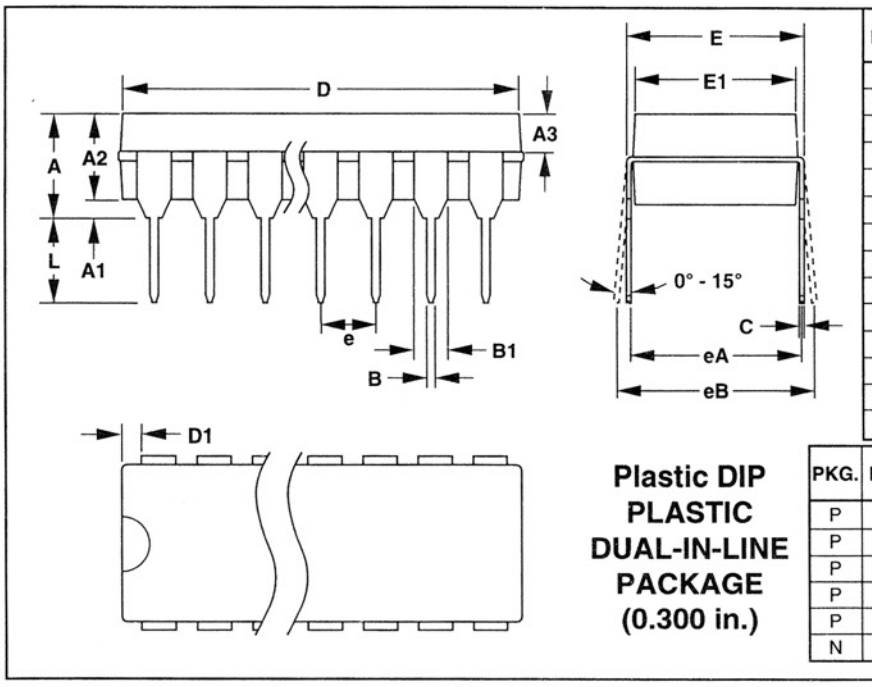
** *Maxim reserves the right to ship ceramic packages in lieu of CERDIP packages.*

Chip Topography



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

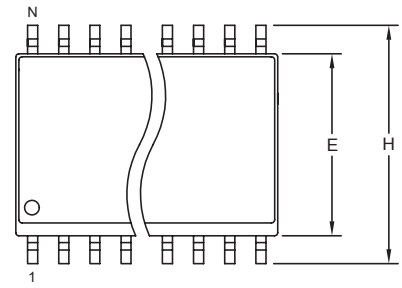
PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICW.EPS

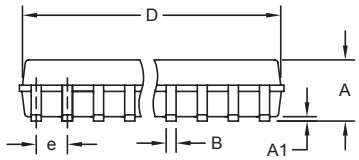


TOP VIEW

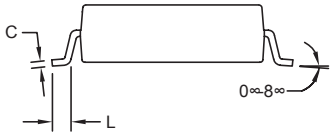
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

VARIATIONS:

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS013.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

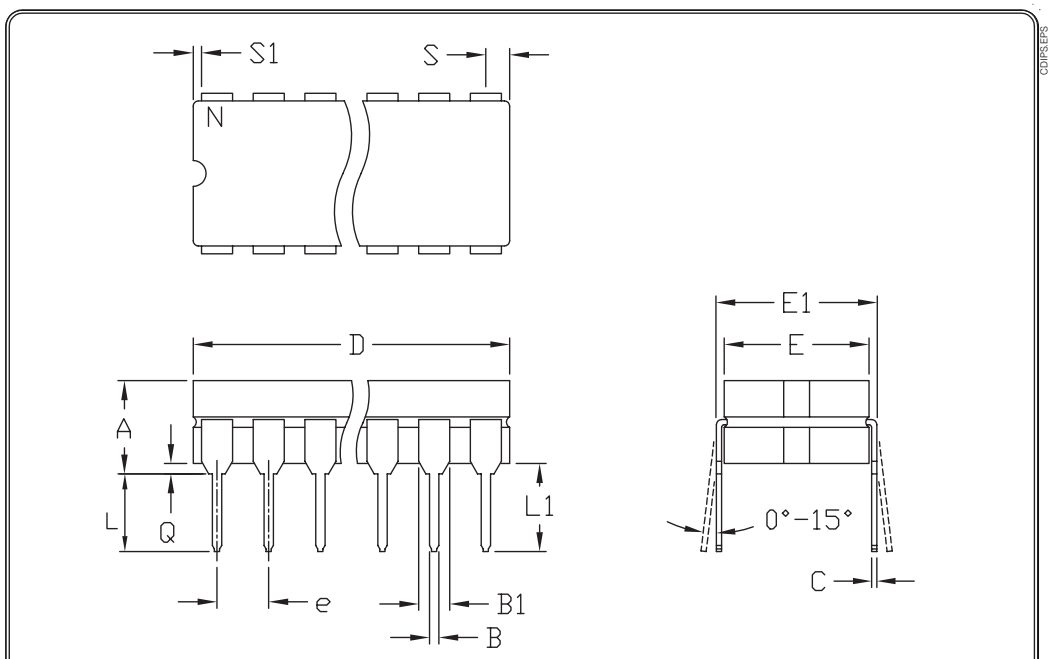
TITLE: PACKAGE OUTLINE, .300" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0042	B	1/1

CMOS 12 Bit Multiplying D/A Converter

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	---	0.00	---
Q	0.015	0.070	0.38	1.78
S	---	0.098	---	2.49
S1	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	0.405	---	10.29	8	P:D4
D	---	0.785	---	19.94	14	C:D1
D	---	0.840	---	21.34	16	E:D2
D	---	0.960	---	24.38	18	V:D6
D	---	1.060	---	26.92	20	R:D8
D	---	1.280	---	32.51	24	L:D9

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #1 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

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PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: CDIP .300" (TITLE)

1/1

21-0045 A (DOCUMENT CONTROL NUMBER REV)

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- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
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