MAX20317

Universal 3.5mmØ Accessory Management IC

General Description

The MAX20317 is an I²C controllable, universal 3.5mmØ accessory management IC. The device provides a universal jack interface solution, as well as a compact solution for the power management and interface control of a powered accessory, such as an active noise cancelling (ANC) headset.

The MAX20317 automatically measures headset impedance with a high precision, triple current source 8 bit ADC. After impedance detection, the device also detects when a headset is in a CTIA or OMTP configuration and automatically configures the SLEEVE and RING2 terminals to correctly connect the microphone and ground lines.

When a boost supply is applied, the MAX20317 can detect the presence of an ANC headset. When the ANC headset is detected and enabled, a button-press monitoring circuit activates and flags button presses by detecting the voltage drop across a sense resistor.

The MAX20317 provides a power line communication tool to a headset to exchange the data with the host device.

The MAX20317 has the two separate ground sense inputs from the SLEEVE and RING2 terminals of the connector to provide a high ground isolation to the audio codec.

The MAX20317 is available in a space-saving, 20-bump, 0.4mm pitch, 1.65mm x 2.05mm wafer-level package (WLP) and operates over the -40 $^{\circ}$ C to +85 $^{\circ}$ C extended temperature range.

Applications

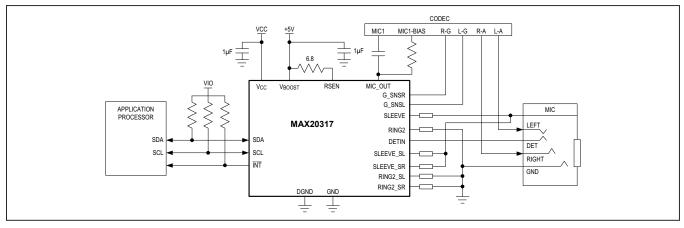
- Smart Phones
- Tablet PCs
- Phablet
- Notebook PCs

Benefits and Features

- Allows Wide Range of Applications by Supporting Universal 3.5mm Jack Types
 - · Auto-Configuration for CTIA and OMTP Headsets
 - Supports MEMS Microphone
 - 50mΩ Ground Switch
- Enables Long Utilization of Accessories by Supplying Power Through 3.5mm Jack
 - · Powered Accessory/Headset Detection
 - Bypass Switch to Power Accessories such as ANC Headsets
 - Programmable Button Detection in Powered Accessory Mode
- Empowers New Path in Data Communication to Accessories
 - Power Line Communication by 3.5mm Jack
 - Bidirectional Digital Data Communication in Power Mode
 - Allow Emergence of New Accessory Types
- Provides Comfortable Sounds by Introducing Automatic Volume Adjustment
 - Adaptive Volume Control Based on Precision Headset Impedance
 - · False Insertion Detection
- Saves Board Space with Small Form Factor
 - 1.65mm x 2.05mm 4 x 5 Array 20 Bump 0.4mm Pitch WLP

Ordering Information appears at end of data sheet.

Typical Application Circuit





Absolute Maximum Ratings

All voltages are referred to GND unless oth	erwise noted
V _{CC} , SCL, SDA, INT	0.3V to +6V
V _{BOOST} , RSEN	0.3V to +12V
MIC_OUT	$-0.3V$ to $V_{CC} + 0.3V$
DETIN	
SLEEVE, SLEEVE_SL, SLEEVE_SR,	
RING2, RING2_SL, RING2_SR	0.3V to +6V
G_SNSL, G_SNSR	0.3V to +0.3V
Continuous Current into V _{BOOST} , RSEN,	
MIC_OUT, RING2, SLEEVE	±200mA

Continuous Current into Any Other Terminal	±100mA
Continuous Power Dissipation (Multilayer Boa	rd)
(Derate 18.02mW/°C above +70°C)	1441.6mW
Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Soldering Temperature (Reflow)	+260°C

Package Thermal Characteristics (Note 1)

WLP

Junction-to-Ambient Thermal Resistance, Four Layer Board (θ_{JA})......55.49°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

 $(V_{CC}$ = +3.0V to +5.5V, V_{BOOST} = 0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V _{CC}						
Supply Voltage Range	V _{CC}		3		5.5	V
V _{CC} POR	V _{CCPOR}		0.9	1.7	2.45	V
		V _{CC} = +3.5V, DETIN = 1		2	5	
V _{CC} Supply Current	I _{VCC}	BYPASS (0x08[2]) = 0, DETIN = 0		10	15	μA
VCC Supply Sulfolic	1,000	V _{CC} = +3.5V, BYPASS (0x08[2]) = 1, DETIN = 0, I _{VBOOST} = 30mA		0.1	0.2	mA
Bypass Supply Voltage Range	V _{BOOST}				5.5	V
DETIN						
DETIN Pullup Current	I _{DETIN_PU}			4.5		μA
DETIN Detection Threshold			1/3 x V _{CC}	1/2 x V _{CC}	2/3 x V _{CC}	V
		SET_IDET (0x0B[5:4]) = 01	95	100	105	μA
DETIN Current Source	I _{DETIN}	SET_IDET (0x0B[5:4]) = 10	1.05	1.1	1.15	mA
		SET_IDET (0x0B[5:4]) = 11	5.25	5.5	5.75	IIIA

Electrical Characteristics (continued)

 $(V_{CC}$ = +3.0V to +5.5V, V_{BOOST} = 0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN TYP MAX		UNITS	
BYPASS SWITCH						
Output Shutdown R _{SEN} Drop	V _{SH}	V _{BOOST} = 5.0V	1.28	1.36	1.44	V
Bypass Switch R _{ON}	R _{BYPASS}	V_{CC} = 4.2V, V_{BOOST} = 5.0V, I_{BYPASS} = 150mA		1	1.5	Ω
Off Isolation to SLEEVE		$V_{RSEN} = 5V \pm 50$ mV, f = 20Hz to 20kHz		-90		dB
SLEEVE, RING2 (GND MU	X SWITCH)					
Ground MUX Switch RON	R _{GMP}	V _{CC} = 3.5V		50	85	mΩ
Ground MUX Switch Bandwidth		$R_{SOURCE} = R_{LOAD} = 50\Omega$		300		MHz
Ground Switch PSRR	PSRR _{GNDSW}	V _{CC} = 3.5V, R _{SOURCE} = 50Ω, f = 217Hz		-96		dB
Ground Bypass Switch THD		100mV _{Pk-Pk} , DC bias = 0V, f = 20Hz to 20KHz, R _{SOURCE} = R _{LOAD} = 50Ω		0.002		%
SLEEVE, RING2 (MIC MUX	SWITCH)					
MIC Switch Turn-On Time				5		μs
MIC Switch Turn-Off Time				4		μs
MIC Switch R _{ON}	R _{MIC}	V _{CC} = 3.5V, I = 10mA		1	2	Ω
MIC Switch Bandwidth		R _{SOURCE} = R _{LOAD} = 50Ω		25		MHz
MIC Switch PSRR		V_{CC} = 3.5V, R_{SOURCE} = 50Ω , f = 217Hz		-90		dB
MIC Switch Isolation				-90		dB
V _{BOOST} , RSEN (ANC DET	ECTION)					
ANC Headset Detection Accuracy		Using 6.8Ω External Sense for ANC detection, range from 1.5 to 5mA (ADC2_HL(0x0B[2])) = 1. Thresholds I ² C Programmable by HSDET_VAL	-3		+3	%
Button Press Current Measurement Accuracy		Using 6.8Ω External Sense, range from 5mA to 200mA (ADC2_HL(0x0B[2])) = 0. Thresholds I ² C Programmable by HSDET_VAL	-3		+3	%
		COM_THRS[1:0](0x08[1:0]) = 00	87	88	89	%V _{BOOST}
ANC Button Detection Interrupt Falling Edge	VCOM DET	COM_THRS[1:0] (0x08[1:0]) = 01	89	90	91	%V _{BOOST}
Threshold	V _{COM_DET}	COM_THRS[1:0] (0x08[1:0]) = 10	91	92	93	%V _{BOOST}
		COM_THRS[1:0] (0x08[1:0]) = 11	93	94	95	%V _{BOOST}
BOOST OVP OVLO Threshold	V _{BOOST_OVLO}	V _{BOOST} slew rate ≤ 1V/μs	5.6	5.75	5.94	V

Electrical Characteristics (continued)

 $(V_{CC}$ = +3.0V to +5.5V, V_{BOOST} = 0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GROUND SENSE SWITCH	(G_SNSR/G_SN	NSL)				
G_SNS Switch Turn-On Time				50		μs
G_SNS Switch Turn-Off Time				3		μs
G_SNS Switch R _{ON}		I _{LOAD} = 10mA		8.0	1.5	Ω
G_SNS Switch Bandwidth		$R_{SOURCE} = R_{LOAD} = 50\Omega,$ $C_{LOAD} = 10pF$		300		MHz
G_SNS Switch PSRR		V_{CC} = 3.3V, R_{SOURCE} = R_{LOAD} = 50 Ω , f = 217Hz, V_{IN} = 3.3V ±0.1V		-90		dB
G_SNS Switch Cross talk		V_{CC} = 3.3V, R_{SOURCE} = R_{LOAD} = 50 Ω , f = 20Hz to 20kHz, V_{MIC} = ±150mV		-90		dB
DIGITAL SIGNALS (SDA, S	CL, INT)					
Input Logic-High	V _{IH}		1.4			V
Input Logic-Low	V _{IL}				0.4	V
Input Leakage Current			-1		1	μA
Output Logic-High Leakage Current (Open-Drain)	loh_lkg	V _{IO} = 5V			1	μΑ
Output Logic-Low	V _{OL}	I _{SINK} = 4mA			0.4	V
POWER LINE COMMUNICATION	ATION					
PLC Logic-High		V _{BOOST} = 5V, Low is V _{RSENSE} below V _{COM_DET}			V _{COM_DET}	V
PLC Logic-Low		V _{BOOST} = 5V, High is V _{RSENSE} above V _{COM_DET}	V _{COM_DET}			V
Time Unit	t _{UNIT}	I ² C Programmable (24/30μs) Inferred from 1μs clock		24/30		μs
TX Logic 0	t _{TXLOGIC0}		90		110	% t _{UNIT}
TX Logic 1	tTXLOGIC1	Period for low and high	40		60	% t _{UNIT}
RX Logic 0	t _{RXLOGIC0}		85		115	% t _{UNIT}
RX Logic 1	t _{RXLOGIC1}	Period for low and high	35		65	% t _{UNIT}
DI O TV O	_	PLC_SINK (0x18[6]) = 0	90	100	110	mA
PLC TX Current Sink	I _{PLC}	PLC_SINK(0x18[6]) = 1	70	80	90	mA

Electrical Characteristics (continued)

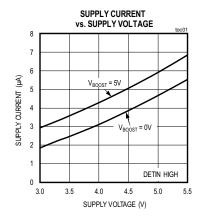
 $(V_{CC}$ = +3.0V to +5.5V, V_{BOOST} = 0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.5V, T_A = +25°C.) (Note 2)

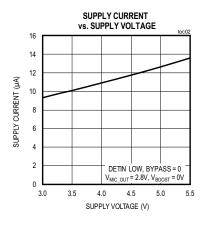
PARAMETER	SYMBOL	CONDITIONS MIN TYP MAX		UNITS	
DYNAMIC					
DETIN Dahawaa Tiraa		DETIN Falling Edge, DET_DEBOUNCE (0x08[6]) = 0	115		
DETIN Debounce Time	^t DIDEB	DETIN Falling Edge, DET_DEBOUNCE (0x08[6]) = 1	300		ms
SEND/END Debounce Time	^t SEDEB	I ² C selectable: 20/30/40/50ms	30		ms
I _{DETIN} Rise Time	t _{IDETINR}	Rising	50		ms
I _{DETIN} Fall Time	t _{IDETINF}	Falling	50		ms
I ² C TIMING					
I ² C Serial Clock Frequency	f _{SCL}		400		kHz
ESD PROTECTION					
DETIN		Human Body Model	±15		kV
SLEEVE, RING2, SLEEVE_SR, SLEEVE_ SL, RING2_SR, RING2_ SL		Human Body Model	±10		kV
All Other Pins		Human Body Model	±2		kV
THERMAL PROTECTION					
Thermal Shutdown	T _{SHDN}	Low to high	130		°C
Thermal Hysteresis	T _{HYST}	High to low	20		°C

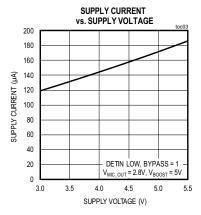
Note 2: All devices are 100% production tested at $T_A = +25$ °C. Limits over the operating temperature range are guaranteed by design.

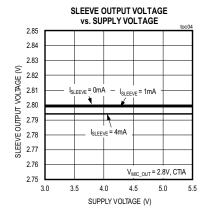
Typical Operating Characteristics

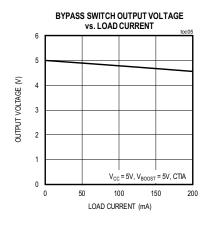
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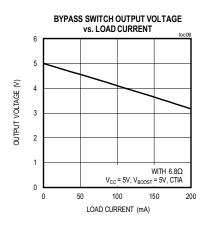


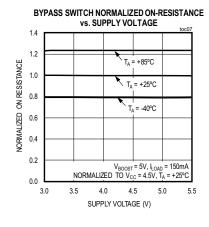


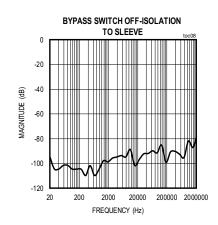






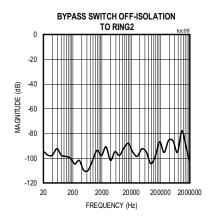


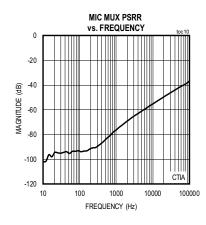


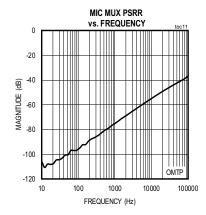


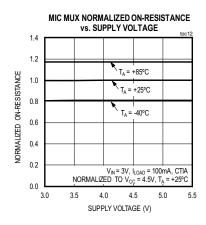
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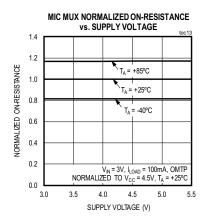
 $(V_{CC} = +3.5V, R_{SEN} = 6.8\Omega, T_A = +25^{\circ}C \text{ unless otherwise noted.})$

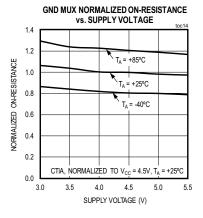


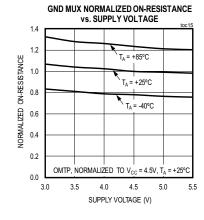


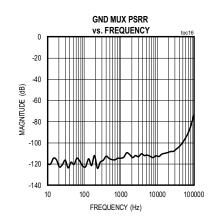






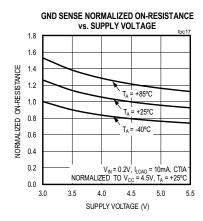


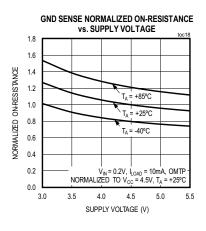


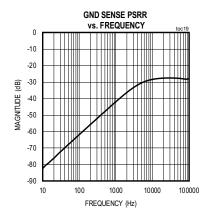


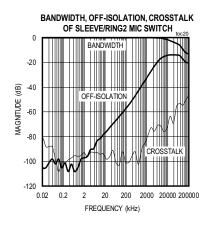
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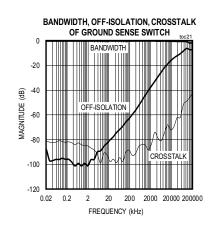
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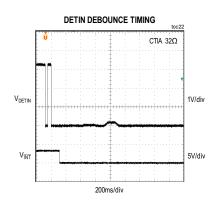


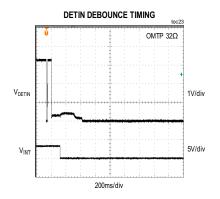


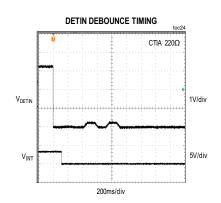






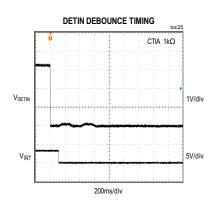


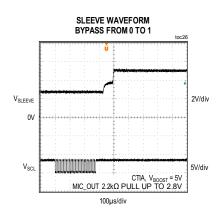


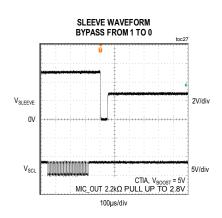


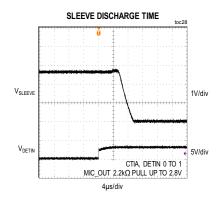
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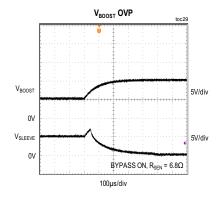
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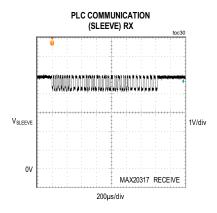


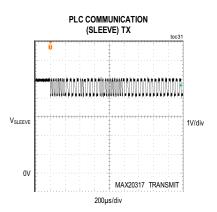




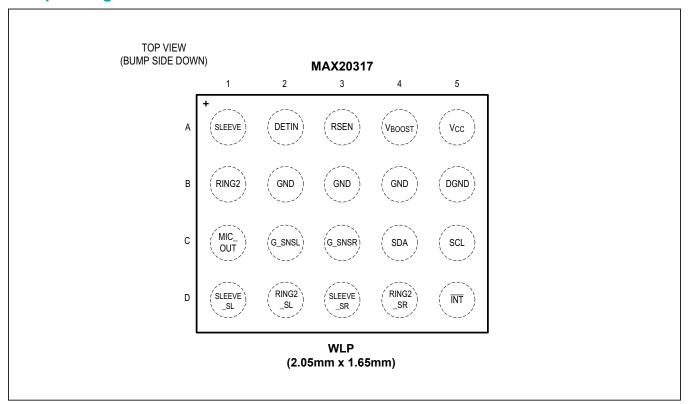








Bump Configuration



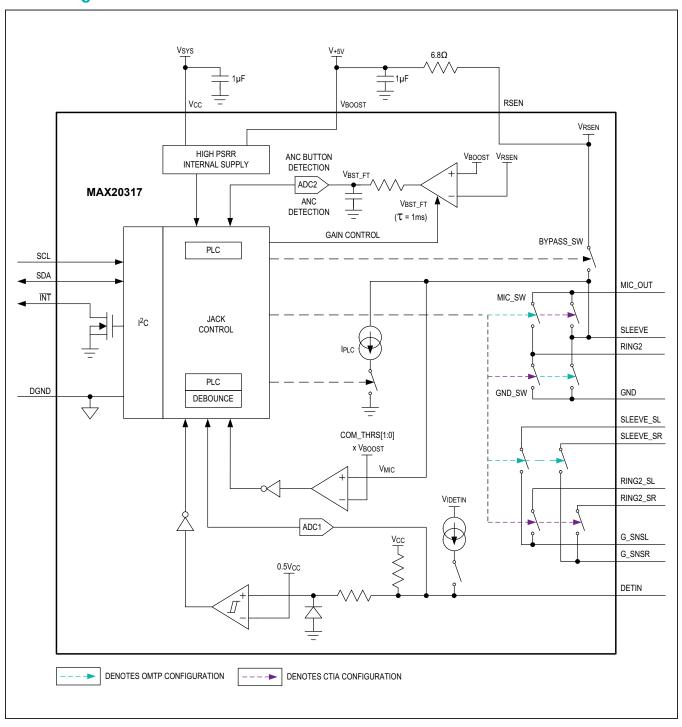
Bump Descriptions

BUMP	NAME	FUNCTION
A1	SLEEVE	Jack Sleeve Pin Contact
A2	DETIN	Jack Insertion Detection Input. An internal comparator monitors DETIN for jack insertion/ removal events.
A3	RSEN	RSEN connection for Bypass mode
A4	V _{BOOST}	Supply Voltage Input for Bypass Mode. Bypass V _{BOOST} to ground with a 1µF ceramic capacitor as close as possible to the device.
A5	V _{CC}	Supply Voltage Input. Bypass V_{CC} to ground with a $1\mu F$ decoupling capacitor as close as possible to the device.

Bump Descriptions (continued)

BUMP	NAME	FUNCTION
B1	RING2	Jack Ring2 Pin Connection
B2, B3, B4	GND	Ground. Connect all GND and DGND pins together.
B5	DGND	Digital Ground. Connect all GND and DGND pins together.
C1	MIC_OUT	Microphone to Phone Codec Output
C2	G_SNSL	Left Ground Reference Sense. G_SNSL is a ground reference prior to the ground switch to obtain a high ground isolation for the audio codec.
C3	G_SNSR	Right Ground Reference Sense. G_SNSL is a ground reference prior to the ground switch to obtain a high ground isolation for the audio codec.
C4	SDA	I ² C Data Line
C5	SCL	I ² C Clock
D1	SLEEVE_SL	Jack Sleeve Kelvin Pin Contact for Left Audio Line
D2	RING2_SL	Jack Ring2 Kelvin Pin Contact for Left Audio Line
D3	SLEEVE_SR	Jack Sleeve Kelvin Pin Contact for Right Audio Line
D4	RING2_SR	Jack Ring2 Kelvin Pin Contact for Right Audio Line
D5	ĪNT	I ² C Active-Low, Open-Drain Interrupt Output. Connect INT to an external pullup resistor.

Block Diagram



Detailed Description

The MAX20317 supports both CTIA and OMTP headsets. The advanced method used to detect the headset type provides error free connections to ground and the microphone line. Manual control allows for future expansion of accessory types and functions.

In addition to detecting the jack configuration, the MAX20317 also reliably detects ANC headsets and headset button press events. A built-in, low offset 8-bit ADC provides a precise method of detecting an ANC headset and button presses in ANC music mode. These functions are handled automatically by the device, but can also be controlled manually.

For both ANC and normal headsets, the MAX20317 measures the impedance of the speaker. High precision current sources and an 8-bit ADC permit high accuracy sensing of low impedance headsets, even distinguishing between 16Ω and 32Ω speakers. This is useful in dynamic volume scaling applications.

The MAX20317 features power-line communication (PLC) for accessories powered by the microphone line. Data transmits above audio frequencies to prevent interference with the audio signal to the headset. This permits accessories to communicate with the device while a system is in music mode.

After the startup process is complete and the DEVICE_READY bit (0x03[2]) is set, the MAX20317 enters normal operation. During this stage, an external controller and CODEC can confirm the jack type, either 3P or 4P, to enable or disable a MIC bias, detect the presence of an ANC headset, and communicate with accessories or use

the headset microphone. The full system flowchart is shown in <u>Figure 1</u>, while <u>Figure 2</u> details the jack detection process when a headset is connected.

Impedance Detection

When the MAX20317 detects the presence of a headset, it can measure the headset impedance. DETIN applies a current, I_{DETIN} , to the left channel of the 3.5mm jack and reads the resulting DC voltage with ADC1. This measurement occurs automatically when DET goes low after a DETIN debounce period or triggers manually upon receipt of an I^2C command while DET = 0. The start condition is set with ADC_CTRL[1:0] (0x0A[3:2]).

Automatic impedance measurements begin when a head-set insertion event forces DET low. The MIC and GND switches close in a CTIA configuration. If the OPEN_DETECT bit (0x09[4]) is HIGH, IDETIN is set to 100 μ A for a high-impedance measurement. If the voltage measured by ADC1 is less than the value saved in HIHS_VAL (register 0x0E), or if OPEN_DETECT is low, a low impedance measurement is performed with IDETIN = 1.1mA. If the voltage is still too low, the low-impedance measurement is repeated with IDETIN = 5.5mA. This automatic process is illustrated in Figure 3.

Alternatively, the MAX20317 can measure impedance only upon receipt of an I²C command. Setting ADC1_CTRL[1:0] to 01 or 10 causes the impedance measurement to trigger when FORCE_ADC1_START (0x0B[1]) goes high. The I_{DETIN} value for manual impedance measurements is set by SET_IDET[1:0] (0x0B[5:4]). After an automatic measurement, SET_IDET[1:0] equals the last I_{DETIN} value used in the impedance check, but it can be forced to any value for manual tests.

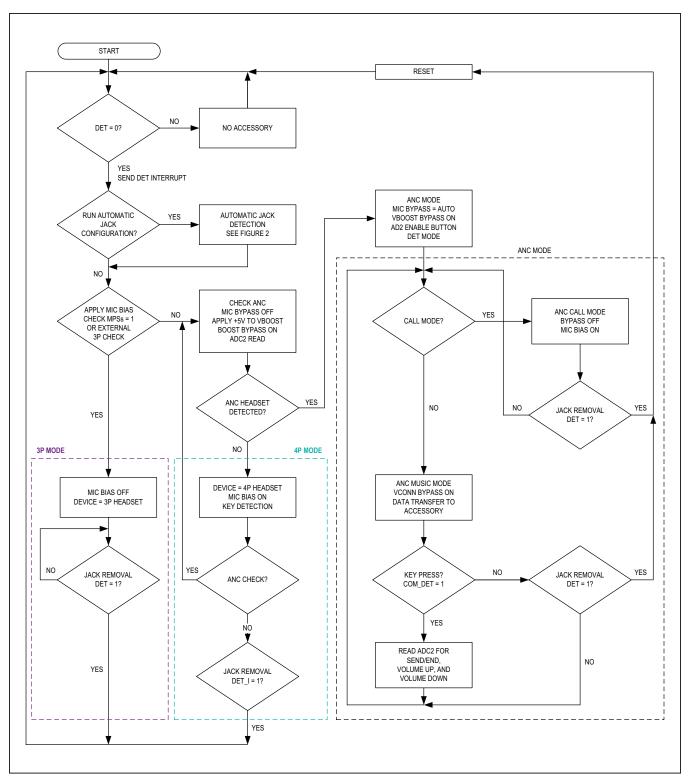


Figure 1. Full operation of the MAX20317

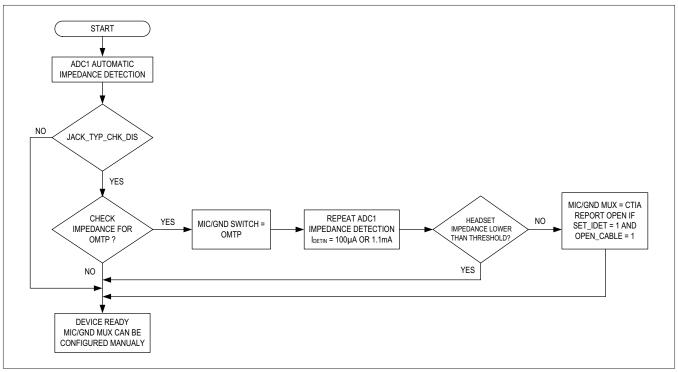


Figure 2. Automatic Jack Detection

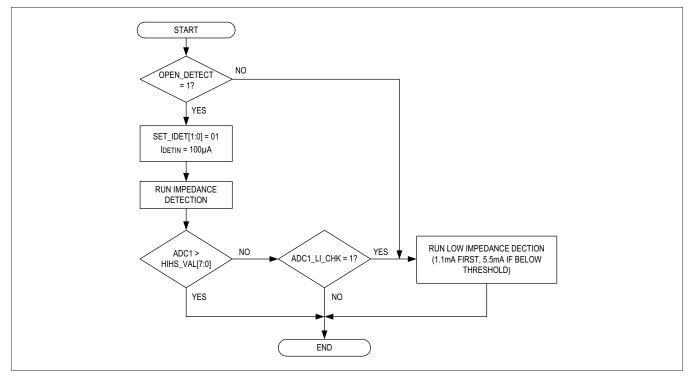


Figure 3. ADC1 Automatic Impedance Detection

CTIA/OMTP Detection

The impedance measurement process is also used to identify a jack as CTIA or OMTP. When JACK_ TYP CHK DIS = 0 (0x0A[6]), CTIA/OMTP detection begins after an automatic impedance measurement. This second measurement keeps the last value of IDETIN. either 100µA or 1.1mA, and measures the L-channel impedance with the MIC and GND MUX switches closed in OMTP mode. If the voltage measured by ADC1 is less than the threshold defined in OMTP VAL (register 0x0F) when testing a low-impedance headset, or HIHS VAL for high-impedance headsets, the MIC and GND MUX switches remain configured for OMTP. Otherwise, the switches connect in the CTIA configuration. Automatic jack detection is disabled when ADC1 is controlled manually or when JACK TYP CHK DIS = 1 and the MIC and GND switches must be set by FORCE MG SW[1:0] (0x09[1:0]) and MANUAL MG SW (0x09[5]).

Open Cable Check

If OPEN_DETECT = 1 (0x09[4], the MAX20317 performs an open cable check after determining the jack type. If a high-impedance measurement exceeds the HIHS_VAL threshold, the cable is considered open and the OPEN_CABLE flag (0x03[4]) is set. This feature helps ensure that a there is a clean connection to a real headset when DET goes LOW after the DETIN debounce period.

ANC Headset Detection

The MAX20317 identifies ANC headsets by measuring the current drawn through an external resistor connected to RSEN. If there is +5V present on V_{BOOST} , an automatic measurement launches when the bypass switch closes. An internal, high-gain differential amplifier measures the current through the sense resistor and is read by ADC2. If the current is higher than HSDET_VAL (register 0x10), the headset is considered to be ANC and the ANC_HS bit (0x05[7]) is set. ANC headset detection is only compatible with CTIA headsets.

ANC Current Sense

The MAX20317 automatically detects ANC button presses while in BYPASS mode through the current sense resistor. When a button is pressed, the microphone voltage drops, triggering a COM_DET interrupt. This also triggers an automatic ADC2 conversion. The ADC2 conversion continues as long as the microphone voltage is below the COM_DET threshold set by COM_THRS[1:0] (0x08[1:0]).

Pop-Up Noise Suppression

In order to prevent any pop-up noise, SLEEVE and RING2 are discharged immediately after a headset is unplugged.

Microphone Short Protection

Overcurrent protection on RSEN protects the MAX20317 from drawing too much current through the sense resistor. When the voltage drop across the sense resistor exceeds V_{SH} for longer than the time set in tSHO_DEB[1:0] (0x0D[1:0]), the MPSs bit (0x04[4]) is set and triggers an interrupt. The MAX20317 exits bypass mode and resets BYPASS to "0." The device also exits bypass mode if an overvoltage condition occurs on V_{BOOST} .

Power Line Communication

A one-wire accessory Power-Line-Communication Protocol (PLC) enables communication between a master device and a single accessory device over the microphone power line. The protocol allows the master to configure, control, and read the status of the attached accessory. When the accessory is powered, power line communication takes place over the microphone using biphase mark code (BMC).

The PLC can be implemented on any single power line between two devices. Error checking, including parity and checksum, is included in the protocol to validate all data transferred between devices. The protocol is defined by a physical layer, which describes the physical communication protocol, and the logical layer that includes high-level commands and handshakes. Figure 4 and Figure 5 show the process of sending and receiving PLC data, respectively. The MAX20317 supports physical data transfer between the master device and slave accessory. The meaning of the data contained in each individual accessory must be defined by the manufacturer of the master device.

SLEEVE and RING2 Ground Sense

Because audio systems require high levels of isolation between audio channels, the MAX20317 incorporates separate ground sense connections for SLEEVE and RING2. These ground sense contacts provide channel isolation with a Kelvin contact, especially when an EMC filter is included between the 3.5mm jack and the MAX20317. Individual left- and right-channel ground sense outputs provide separate return paths for SLEEVE and RING2.

I²C Interface

The MAX20317 uses the two-wire I^2C interface to communicate with a host application processor. The configuration settings and status information provided through this interface are detailed in the register descriptions (<u>Tables 2</u> – <u>31</u>). MAX20317 uses the seven-bit slave address 0b0010101 (0x2A for writes, 0x2B for reads).

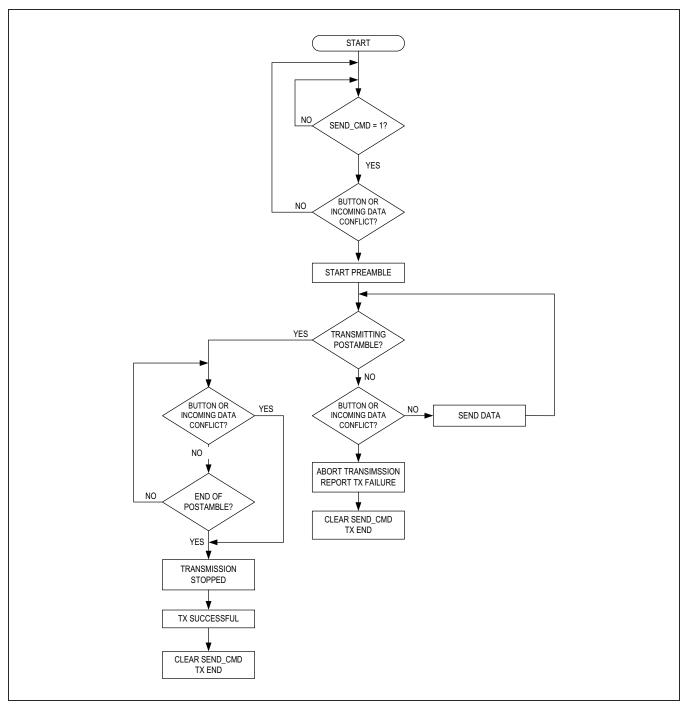


Figure 4. PLC TX Process

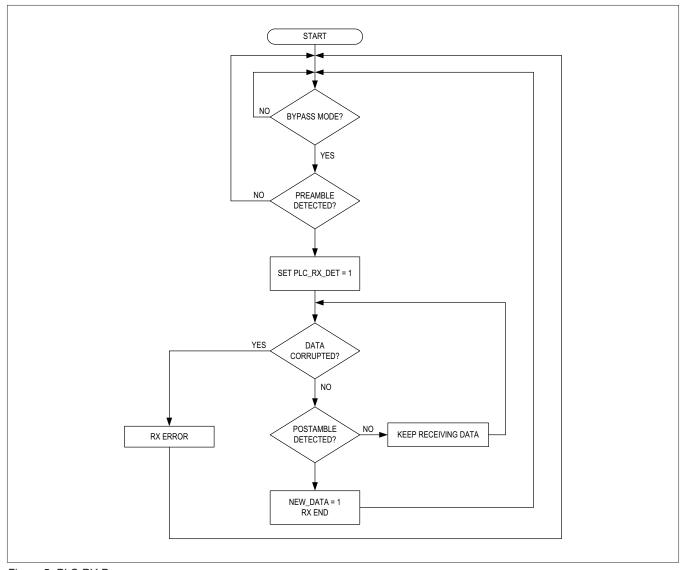


Figure 5. PLC RX Process

Applications Information

I²C Serial Interface

The I 2 C serial interface is used to configure the device. Figure 6 shows the I 2 C timing diagram.

Serial Addressing

When in I²C mode, the device operates as a slave device that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX20317 and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open drain output. A pullup resistor is required on

SDA. The SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open drain SCL output. Each transmission consists of a START condition sent by a master, followed by the MAX20317 7-bit slave address plus R/W bit, a register address byte, one or more data bytes, and finally a STOP condition.

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (Figure 7). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

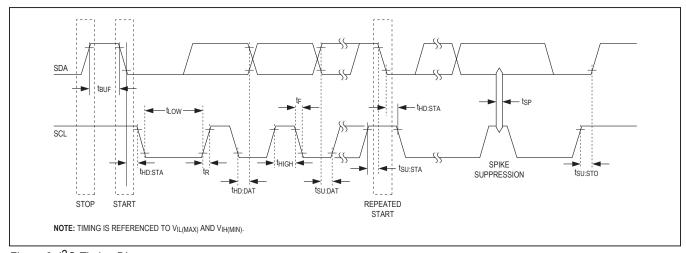


Figure 6. I²C Timing Diagram

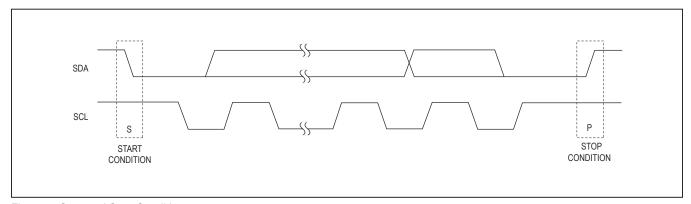


Figure 7. Start and Stop Conditions

Bit Transfer

One data bit is transferred during each clock pulse (<u>Figure 8</u>). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 9), which the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX20317, it generates the acknowledge bit because the device is the recipient. When the device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. If the device does not pull SDA low, a not acknowledge is indicated.

Slave Address

The device has a 7-bit slave address. The bit following a 7-bit slave address is the R/\overline{W} bit, which is low for a write command and high for a read command. The slave address for the device is 0b00101011 for read commands and 0b00101010 for write commands. This is summarized in Table 1.

Table 1. I²C Slave Addresses

ADDRESS FORMAT	VAI	_UE
ADDRESS FORMAT	HEX	BINARY
7-BIT SLAVE ADDRESS	0x15	001 0101
WRITE ADDRESS	0x2A	0010 1010
READ ADDRESS	0x2B	0010 1011

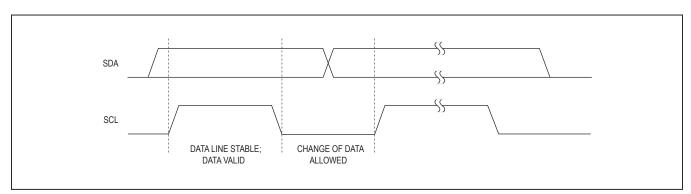


Figure 8. Bit Transfer

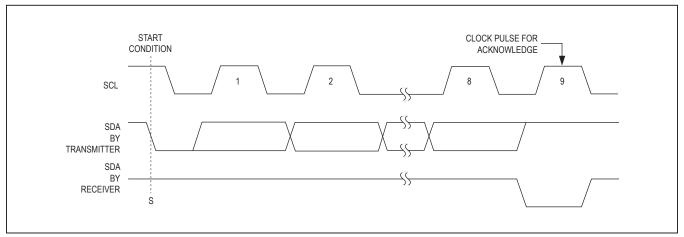


Figure 9. Acknowledge

Bus Reset

The MAX20317 resets the bus with the I 2 C start condition for reads. When the R/ \overline{W} bit is set to 1, the MAX20317 transmits data to the master, thus the master is reading from the device.

Format for Writing

A write to the MAX20317 comprises the transmission of the slave address with the R/\overline{W} bit set to zero, followed by at least 1 byte of information. The first byte of information is the register address or command byte. The register address determines which register of the device is to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, then the device takes no further action beyond storing the register address. Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address and subsequent

data bytes go into subsequent registers (<u>Figure 10</u>). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses auto-increments (Figure 11).

Format for Reading

The MAX20317 is read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer auto-increments after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 12). The master can now read consecutive bytes from the device, with the first data byte being read from the register addressed pointed by the previously written register address (Figure 13). Once the master sends a NACK, the MAX20317 stop sending valid data.

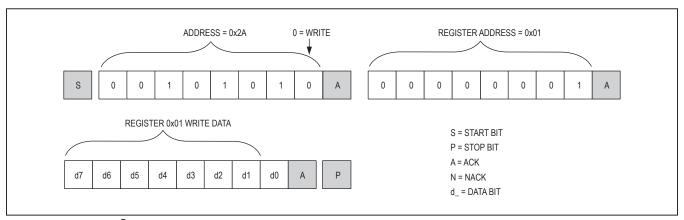


Figure 10. Format for I²C Write

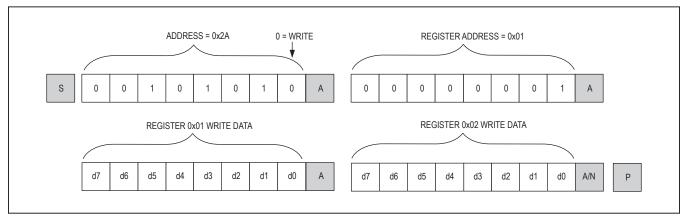


Figure 11. Format for Writing to Multiple Registers

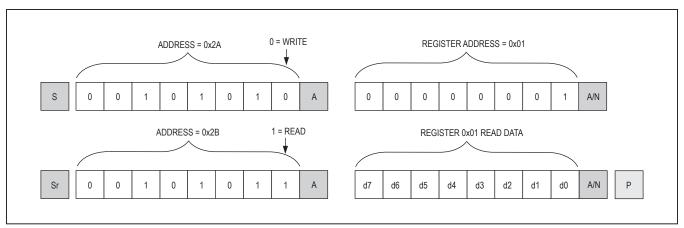


Figure 12. Format for Reads (Repeated Start)

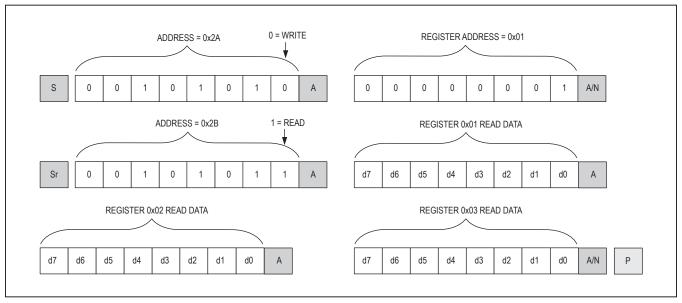


Figure 13. Format for Reading Multiple Registers

Power Line Communication

Physical Structure

In biphase mark code, high and low bits are defined by state transitions. In the MAX20317, the PLC code comprises a time unit and the low and high states of the MIC line. The time unit, t_{UNIT} defines the interval of time in which a bit is determined to be either 0 or 1. By default, $t_{UNIT} = 24\mu s$, but setting the FREQ bit (0x18[4]) HIGH increases t_{UNIT} to 30 μs . A bit is considered 0 if no MIC state transition occurs during t_{UNIT} . If there is a state change, either high to low or low to high, the bit is 1.

When the MIC line is above the V_{COM_DET} threshold, a low state is recorded. Conversely, a high state is recorded when the MIC line is below the V_{COM_DET} threshold. For example, MIC line transitions and their corresponding logic values and BMC bits are shown in Figure 14.

Transmission Format

A valid PLC packet comprises a preamble, two data bytes, checksum, and postamble. The preamble is eight consecutive 1 bits. After a successful preamble, data transfer takes place until an error condition occurs or the end of transmission is reached.

Each byte of data begins with a 0 bit to indicate the start condition followed by one byte of data. A parity and stop bit are transmitted at the end of each byte. The stop bit is always 1. If parity is disabled, a parity bit of 1 will be sent, but ignored by the device.

Following the data bytes, a checksum is transmitted. The checksum is generated as NOT(DATA1 + DATA2). Transmission will end with the checksum unless the postamble is enabled. The postamble transmits 0 for a duration of 50ms. A typical data packet is shown in Figure 15.

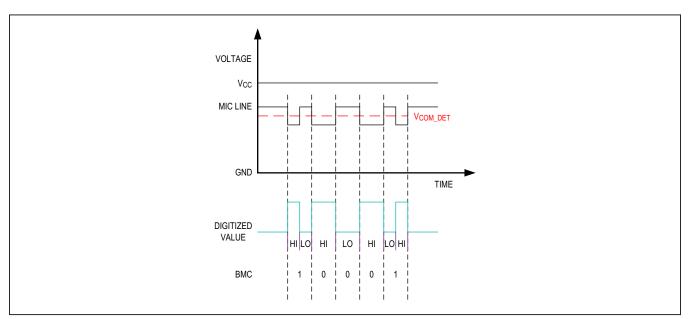


Figure 14. Determination of PLC Data Bit

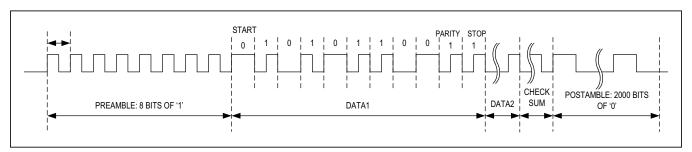


Figure 15. Sample PLC Data Packet

12C Register Map

4			i	Ğ		à	6	Ğ	2	Ġ
ADDRESS	NAME	¥/	ρ/	g	Bo	D 4	20	B 2	2	PO
00X0	DEVICE_ID	~		CHIP_ID[3:0]	[D:E]QI			CHIP_F	CHIP_REV[3:0]	
0x01	ADC1_VAL	R				ADC1_	ADC1_VAL[7:0]			
0x02	ADC2_VAL	æ				ADC2_	ADC2_VAL[7:0]			
0x03	STATUS1	œ	IDET_L	IDET_LVL[1:0]	COM_DET	OPEN_ CABLE	JACK_ TYPE	DEVICE_ RDY	E0C1	EOC2
0x04	STATUS2	œ	VOL_UP	VOL_ DOWN	VBOOST_ OV	MPSs	MIC_IN	SWD	DET	DETIN
0×05	STATUS3	Я	ANC_HS	THT_CMP	SAR_CMP	V94_CMP	I	I	I	VOL_RFU
90x0	IRQ	R/C	SWDi	EOCi	COM_DETi	MPS/ VBOOST_ OVi	MIC_INi	DEVICE_ RDYi	DETI	DETINi
0x0	MASK	R/W	SWDm	EOCm	COM_ DETm	MPS/ VBOOST_ OVm	MIC_INm	DEVICE_ RDYm	DETm	DETINm
0×08	CONTROL1	R/W	I	DEBOUNCE	DETIN_ OVERRIDE	MIC_OUT_ DELAY	I	BYPASS	COM_TI	COM_THRS[1:0]
60×0	CONTROL2	R/W	MANUAL_ G_SNS	MANUAL_ MIC_SW	MANUAL_ MG_SW	OPEN_ DETECT	FORCE_ G_SNS	FORCE_ MIC_SW	FORCE_M	FORCE_MG_SW[1:0]
0x0A	ADC_ CONTROL1	R/W	IDET_FLAT	JACK_TYP_ CHK_DIS	I	ADC1_ L1_CHK	ADC1_(ADC1_CTL[1:0]	ADC2_(ADC2_CTL[1:0]
0x0B	ADC_ CONTROL2	R/W	I	I	SET_ID	SET_IDET[1:0]	I	ADC2_HL	FORCE_ ADC1_ START	FORCE_ ADC2_ START
0×0C	TIMING	R/W	ADC1_A	ADC1_AVG#[1:0]	ADC2_AVG#[1:0]	VG#[1:0]	tANCDET	tANCDET_DEB[1:0]	tANCBPD	tANCBPD_DEB[1:0]

I2C Register Map (continued)

ı										
ADDRESS	NAME	R/W	B7	B6	B5	B4	B3	B2	B1	B0
0x0D	SHORT CURRENT CONTROL	R/W			FU	FU[5:0]			_O_CHS	tSHO_DEB[1:0]
0x0E	HIHS_VAL	R/W				HIHS	HIHS_VAL[7:0]			
0x0F	OMTP_VAL	R/W				OMTP	OMTP_VAL[7:0]			
0x10	HSDET_VAL	R/W				HSDET	HSDET_VAL[7:0]			
0x11	VOL0_TH	R/W				IOA	VOL0[7:0]			
0x12	VOL1_TH	R/W				IOA	VOL1[7:0]			
0x13	VOL2_TH	R/W				10/	VOL2[7:0]			
0x14	VOL3_TH	R/W				IOA	VOL3[7:0]			
0x15	PLC_STAT	ď	I	I	PLC_ TX_ERR	PLC_ TX_OK	PLC_TXP	PLC_ RX_ERR	NEW_DATA	PLC_ RX_DET
0x16	PLC_IRQ	R/C	I	I	PLC_ TX_ERRi	PLC_ TX_OKi	PLC_TXPi	PLC_ RX_ERRi	NEW_DATAi	PLC_ RX_DETI
0x17	PLC_MASK	R/W	I	I	PLC_ TX_ERRm	PLC_ TX_OKm	PLC_TXPm	PLC_ RX_ERRm	NEW_ DATAm	PLC_ RX_DETm
0x18	PLC_CON1	R/W	I	PLC_SINK	POS_ AM_DIS	FREQ	PARIT	PARITY[1:0]	I	SEND_ CMD
0x19	ACC_ID	œ		ACC_ID[3:0]	D[3:0]			ACC_C	ACC_CAT[3:0]	
0x1A	ACC_DB1	œ				ACC	ACC_DB1[7:0]			
0x1B	ACC_DB2	Я				ACC_	ACC_DB2[7:0]			
0x1C	ACC_ADD	R/W				ACC_,	ACC_ADD[7:0]			
0x1D	ACC_DATA	R/W				ACC_	ACC_DAT[7:0]			

Table 2. DEVICE_ID Register (0x00)

ADDRESS	0x00							
MODE	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME		CHIP	_ID[3:0]			CHIP_F	REV[3:0]	
RESET	0	0	0	1	0	0	0	0
CHIP_ID [3:0]	Chip ID Shows info	rmation about th	ne version of M	AX20317				
CHIP_REV [3:0]	Chip Revisi Shows info	on rmation about th	ne revision of M	1AX20317				

Table 3. ADC1_VAL Register (0x01)

ADDRESS	0x01	0x01									
MODE	Read Only	Read Only									
BIT	7	6	5	4	3	2	1	0			
NAME		ADC1_VAL[7:0]									
RESET	0	0	0	0	0	0	0	0			
ADC1_VAL [7:0]	ADC1 Value Read only r	ADC1 Value Read only register for the latest ADC1 conversion (8-bit resolution)									

Table 4. ADC2_VAL Register (0x02)

ADDRESS	0x02	0x02									
MODE	Read Only	Read Only									
BIT	7	6	5	4	3	2	1	0			
NAME		ADC2_VAL[7:0]									
RESET	0	0	0	0	0	0	0	0			
ADC2_VAL [7:0]	ADC2 Value Read only r	ADC2 Value Read only register for the latest ADC2 conversion (8-bit resolution)									

Table 5. STATUS1 Register (0x03)

ADDRESS	0x03									
MODE	Read Only									
BIT	7	6	5	4	3	2	1	0		
NAME	IDET_	_LVL[1:0]	COM_DET	OPEN_ CABLE	JACK_ TYPE	DEVICE_ RDY	EOC1	EOC2		
RESET	0	0	0	0	0	0	0	0		
IDET_LVL [1:0]	Shows the	0 = 1.1mA								
COM_DET	Indicates a 0 = No com	communication Request Status indicates a valid button press when MIC_IN drops below the threshold set by COM_THRS[1:0] = No communication is requested. = MIC voltage is below threshold after the debounce time.								
OPEN_ CABLE	Indicates if 0 = Cable i	Open Cable Detected Indicates if a cable is an open connection 0 = Cable is not open 1 = High impedance is detected for both CTIA and OMTP, and SET_IDET[1:0] = 01.								
JACK_ TYPE		e is disabled if 、 ₋ -R-G-M)	fied by automat JACK_TYP_CH							
DEVICE_ RDY	Indicates the detection if 0 = MIC/GN	Device Ready Indicates the device is ready for manual control after jack detection is complete. This bit is set after impedance detection if JACK_TYP_CHK_DIS = 1. 0 = MIC/GND switch position has NOT been finalized. 1 = MIC/GND SW position is set. Device is ready.								
EOC1	0 = ADC1 d	End of ADC1 conversion 0 = ADC1 conversion is not started or is in progress. 1 = ADC1 conversion is complete and the result is available in ADC1_VAL (register 0x01).								
EOC2	0 = ADC2 d	1 = ADC1 conversion is complete and the result is available in ADC1_VAL (register 0x01). End of ADC2 conversion 0 = ADC2 conversion is not started or is in progress. 1 = ADC2 conversion is complete and the result is available in ADC2_VAL (register 0x02).								

Table 6. STATUS2 Register (0x04)

ADDRESS	0x04									
MODE	Read Only									
BIT	7	6	5	4	3	2	1	0		
NAME	VOL_UP	VOL_DWN	VBOOST_ OV	MPSs	MIC_IN	SWD	DET	DETIN		
RESET	0	0	0	0	0	0	0	0		
VOL_UP	Indicates a Cleared if b Updated in 0 = No volu	bolume Up Status dicates a volume up press was detected in BYPASS mode. ADC2 leared if bypass switch is open or VMIC > COM_THRS[1:0]. pdated in bypass mode with low gain. = No volume up press detected. NOT (VOL1_TH < ADC2 < VOL2_TH) = Volume up press detected VOL1_TH < ADC2 < VOL2_TH								
VOL_ DWN	Cleared if b Updated in Updated in 0 = No Volu	dicates a volume down press was detected in BYPASS mode. VOL2_TH < ADC2 < VOL3_TH leared if bypass switch is open or VMIC > COM_THRS[1:0]. pdated in bypass mode with low gain. pdated in bypass mode with low gain. = No Volume down pressed. NOT (VOL2_TH < ADC2 < VOL3_TH) = Volume down pressed. VOL2_TH < ADC2 < VOL3_TH								
VBOOST_ OV	0 = V _{BOOS}	rpass Mode Over T operating north	mally							
MPSs	0 = Current	rcurrent Status Protection is N Protection is T								
MIC_IN	_	itch Status switch is open switch is close	d							
SWD	Indicates a Cleared if b 0 = No SEN	SEND/END Status Indicates a SEND/END press was detected in BYPASS mode. VOL0_TH< ADC2 <vol1_th bypass="" cleared="" if="" is="" open="" or="" switch="" vmic=""> COM_THRS[1:0]. Updated in bypass mode with low gain. I = SEND/END press detected. NOT(VOL0_TH< ADC2 <vol1_th) <vol1_th<="" adc2="" detected.="" i="SEND/END" press="" td="" vol0_th<=""></vol1_th)></vol1_th>								
DET	0 = Jack wa	Jack Insertion Debounce 0 = Jack was detected after debounce 1 = No jack detected								
DETIN	0 = DETIN	DETIN Detection 0 = DETIN is detected 1 = DETIN is not detected								

Table 7. STATUS3 Register (0x05)

ADDRESS	0x05										
MODE	Read Only										
BIT	7	6	5	4	3	2	1	0			
NAME	ANC_HS	THT_CMP	SAR_CMP	V94_CMP		RFU[2:0]		VOL_RFU			
RESET	0	0 0 0 0 0 0 0									
ANC_HS	0 = No ANC	ANC Headset Detection 0 = No ANC headset detected. VRSEN < HSDET_VAL[7:0] 1 = ANC headset detected. VRSEN > HSDET_VAL[7:0]									
THT_CMP		Thermal Comparator Status Output of the analog thermal comparator									
SAR_CMP		arator Status ne analog SAR	comparator								
V94_CMP		arator Status ne COM_THRS	comparator.								
RFU[2:0]	Reserved for	or future use									
VOL_RFU	Cleared if b ADC2 value 0 = No RFL	Button Press Reserved for Future Use Only. Cleared if bypass is open or VMIC > COM_THRS[1:0]. Updated in BYPASS mode, ADC2 value (VRSEN) with low gain. 0 = No RFU Button pressed. NOT (VOL3_TH < ADC2) 1 = RFU Button pressed. VOL3_TH < ADC2									

Table 8. IRQ Register (0x06)

ADDRESS	0x06								
MODE	Clear On R	ead							
BIT	7	6	5	4	3	2	1	0	
NAME	SWDi	EOCi	COM_DETi	MPS/ VBOOST_ OVi	MIC_INi	DEVICE_ RDYi	DETi	DETINi	
RESET	0	0	0	0	0	0	0	0	
SWDi	0 = Interrup	Button Press I ot not occurred ot occurred (bot		•					
EOCi	0 = Interrup	End of ADC1/2 Conversion Interrupt 0 = Interrupt not occurred 1 = Interrupt occurred (only the rising edge of either EOC1 or EOC2)							
COM_DETi	0 = Interrup	Communication Request Interrupt (Button Press) in Bypass Mode 0 = Interrupt not occurred 1 = Interrupt occurred (both edges of COM_DET, that is button pressed or released)							
MPS/ VBOOST_ OVi	0 = Interrup	e line short or V ot not occurred ot occurred (only			VBOOST_OV)				
MIC_INi	0 = Interrup	ritch Open or Cl ot not occurred ot occurred (bot	•	_IN)					
DEVICE_ RDYi	0 = Interrup	DY MIC/GND Soft not occurred only	•		•				
DETi	0 = Interrup	Jack Insertion and Removal Detection Interrupt 0 = Interrupt not occurred 1 = Interrupt occurred (both edges of debounced DETIN)							
DETINI	0 = Interrup	DETIN Detection Interrupt 0 = Interrupt not occurred 1 = Interrupt occurred							

Table 9. MASK Register (0x07)

ADDRESS	0x07							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	SWDm	EOCm	COM_ DETm	MPS/ VBOOST_ OVm	MIC_INm	DEVICE_ RDYm	DETm	DETINm
RESET	0	0	0	0	0	0	0	0
SWDm	SEND/END 0 = Masked 1 = Not ma		Detection Interr	upt Mask				
EOCm	0 = Masked	End of ADC Conversion Interrupt Mask 0 = Masked 1 = Not masked						
COM_ DETm	0 = Masked	Communication Request Interrupt Mask 0 = Masked 1 = Not masked						
MPS/ VBOOST_ OVm	Microphone 0 = Masked 1 = Not ma		OOST_OV Inte	errupt Mask				
MICINm	MIC_IN Sw 0 = Masked 1 = Not ma		ask					
DEVICE_ RDYm	0 = Masked	Device Ready Interrupt Mask 0 = Masked 1 = Not masked						
DETm	0 = Masked	Jack Insertion Detection Interrupt Mask 0 = Masked 1 = Not masked						
DETINm	DETIN Detection Interrupt Mask 0 = Masked 1 = Not masked							

Table 10. CONTROL1 Register (0x08)

ADDRESS	0x08	0x08									
MODE	Read/Write	1									
BIT	7	6	5	4	3	2	1	0			
NAME	RFU DET_ DETIN_ MIC_OUT DEBOUNCE OVERRIDE DELAY RFU BYPASS COM_THRS[HRS[1:0]				
RESET	0	0**	0**	1**	0	0	0**	1**			
RFU	Reserved F	Reserved For Future Use									
DET_ DEBOUNCE	DET Debou 0 = 115ms, 1 = 300ms										
DETIN_ OVERRIDE	0 = No effe	DETIN Override 0 = No effect 1 = Simulates a jack insertion.									
MIC_OUT_ DELAY	0 = MIC SV	Output Delay C V close output f V close delayed	ollows after DE		er DET becom	es low					
RFU	Reserved F	For Future Use									
BYPASS	BYPASS M 0 = BYPAS 1 = BYPAS										
COM_ THRS[1:0]	COM (Butto 00 = 88% 01 = 90% 10 = 92% 11 = 94%	01 = 90% 10 = 92%									

Table 11. CONTROL2 Register (0x09)

ADDRESS	0x09										
MODE	Read/Write										
BIT	7	6	5	4	3	2	1	0			
NAME	MANUAL_ G_SNS	MANUAL_ MIC_SW	MANUAL_ MG_SW	OPEN_ DETECT	FORCE_ G_SNS	FORCE_ MIC_SW	FORCE_M	G_SW [1:0]			
RESET	0	0 0 1 0 0 0									
MANUAL_ G_SNS	0 = G_SNS	Manual G_SNS Switch Setting 0 = G_SNS operates normally in synch Mic/Ground switch 1 = G_SNS follows FORCE_G_SNS bit									
MANUAL_ MIC_SW	0 = MIC_S\	Manual MIC_IN Switch Setting 0 = MIC_SW operates normally 1 = MIC_SW follows FORCE_MIC_SW bit									
MANUAL_ MG_SW	0 = MG_SV	Manual MG Switch Setting 0 = MG_SW operates normally 1 = MG_SW follows FORCE_MG_SW bit									
OPEN_ DETECT	When high,	enables the first	st automatic im	pedance detect	ion at 100uA.						
FORCE_ G_SNS	0 = Close	_SNS Switch Co Ring2 to G_SN Sleeve to G_SN	S pin `	only when "MA	ANUAL_G_SNS	S = 1")					
FORCE_ MIC_SW	0 = MIC_S\	Force MIC_IN Switch Control (effective only when "MANUAL_MIC_SW = 1") 0 = MIC_SW closed 1 = MIC_SW open									
FORCE_ MG_ SW [1:0]	Force MIC/GND Switch Control (effective only when "MANUAL_MG_SW = 1") 00 = Switches closed in CTIA position 01 = Both MIC-side switches OPEN, ground connection in CTIA position 10 = Switches closed in OMTP position 11 = Both MIC-side switches OPEN, ground connection in OMTP position										

Table 12. ADC CONTROL1 Register (0x0A)

ADDRESS	0x0A										
MODE	Read/Write										
BIT	7	6	5	4	3	2	1	0			
NAME	IDET_ FLAT	JACK_TYP _CHK_DIS	RFU	ADC1_LI _CHK	ADC1_0	CTL [1:0]	ADC2_	CTL [1:0]			
RESET	0**	0** 0** 0 1 1 1 1 1									
IDET_FLAT	0 = 10msec	Flat top period of the IDET for ADC conversion (OTP programmable) 0 = 10msec 1 = 100msec									
JACK_ TYP_CHK_ DIS	0 = Automa	TIA/OMTP Jack Type Detection Disable (OTP programmable) = Automatic Jack Type Detection = Disabled.									
RFU	Reserved F	Reserved For Future Use									
ADC1_ LI_CHK	0 = Disable	ADC1 Low Impedance Check 0 = Disable the 1.1mA/5.5mA impedance detection if ADC1 < HIHS_VAL 1 = Enable the 1.1mA/5.5mA impedance detection if ADC1 < HIHS_VAL									
ADC1_CTL [1:0]	00 = imped 01 = imped 10 = imped	ance detection	is manual and i		when forced.	rsions and avera	aged.				
ADC2_CTL [1:0]	00 = imped 01 = imped 10 = imped 11 = ADC2 If COM_DE	ADC2 Conversion Control 00 = impedance detection and A-D conversion are always off. 01 = impedance detection is manual and one conversion when forced. 10 = impedance detection is manual and multiple (ADC2_AVG#) conversions and averaged. 11 = ADC2 follows FSM. If COM_DET = 0, set ADC2_HL_SET = 1, ADC2 one averaged conversion after tANC_DET from Bypass on =1. ADC2_HL_SET = 0, While COM_DET = 1, ADC2 conversion continuous.									

Table 13. ADC2 CONTROL Register (0x0B)

ADDRESS	0x0B								
MODE	Read/Write								
BIT	7	6	5	4	3	2	1	0	
NAME	F	RFU	SET_ID	DET[1:0]	RFU	ADC2_HL	FORCE_ ADC1_ START	FORCE_ ADC2_ START	
RESET	0	0 0 0 0 0 0 0							
RFU	Reserved F	Reserved For Future Use							
SET_IDET [1:0]	00 = Do no 01 = 100μΑ 10 = 1.1mΑ	Set I _{DETIN} Set the I _{DETIN} current level in manual ADC1 mode. This should be used with Force_ADC1_START 00 = Do not use 01 = 100µA 10 = 1.1mA 11 = 5.5mA							
RFU	Reserved F	or Future Use							
ADC2_HL	0 = ANC Co	Headset Detection Headset Detection Headset Detection Headset Detection Heads	Gain; used for	ANC Button det					
FORCE_ ADC1_ START	Execute a r 0 = ADC1 c	Force ADC1 Start Execute a manual ADC1 measurement when ADC1_CTL[1:0] = 01 or 10 0 = ADC1 operates normally 1 = ADC1 start (only one conversion). End of conversion set the EOC status set.							
FORCE_ ADC2_ START	0 = ADC2 c	2 Start manual ADC2 m operates normal start (only one c	ly	_					

Table 14. Register (0x0C)

ADDRESS	0x0C									
MODE	Read/Write	!								
BIT	7	6	5	4	3	2	1	0		
NAME		1_AVG# 1:0]		_AVG# :0]		ET_DEB :0]		PD_DEB :0]		
RESET	0**	0**	0**	0**	0**	0**	0**	0**		
ADC1_AVG #[1:0]		01 = 4 10 = 8								
ADC2_AVG #[1:0]		01 = 4 10 = 8								
tANCDET_ DEB [1:0]	00 = 20ms 01 = 30ms 10 = 50ms	01 = 30ms								
tANCBPD_ DEB [1:0]	ANC Button Press Detection Debounce Time 00 = 20ms 01 = 30ms 10 = 50ms 11 = 100ms									

Table 15. Short Current Control Register (0x0D)

ADDRESS	0x0D							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	FU[5:0]						tSHO_DEB[1:0]	
RESET		0**	0**	0**	0**	0**	0**	0**
FU [5:0]	Factory Use Only. Do not overwrite							
tSHO_DEB [1:0]	Short Circuit Debounce Sets the debounce time for short-circuit current protection $00 = 360 \mu s$ $01 = 600 \mu s$ $10 = 1080 \mu s$ $11 = 1920 \mu s$							

Table 16. HIHS_VAL Register (0x0E)

ADDRESS	0x0E	0x0E									
MODE	Read/Write	Read/Write									
BIT	7	6	5	4	3	2	1	0			
NAME		HIHS_VAL[7:0]									
RESET	0	0	0	0	0	0	0	0			
HIHS_VAL [7:0]	High imped	High impedance threshold for ADC1 conversions.									

Table 17. OMTP_VAL Register (0x0F)

ADDRESS	0x0F	0x0F									
MODE	Read/Write	Read/Write									
BIT	7	6	5	4	3	2	1	0			
NAME		OMTP_VAL[7:0]									
RESET	0	0	0	0	0	0	0	0			
OMTP_VAL [7:0]	OMTP Head	DMTP Headset Detection Threshold for ADC1 conversion.									

Table 18. HSDET_VAL Register (0x10)

ADDRESS	0x10	0x10									
MODE	Read/Write	Read/Write									
BIT	7	6	5	4	3	2	1	0			
NAME		HSDET_VAL[7:0]									
RESET	0	0	0	0	0	0	0	0			
HSDET_ VAL[7:0]		ANC Headset Detection Threshold for ADC2 conversion when ADC_HL_SET = 1. If ADC2>HSDET_VAL, hen set ANC_HS (0x05h bit7) = 1.									

Table 19. VOL0_TH Register (0x11)

ADDRESS	0x11	0x11									
MODE	Read/Write	Read/Write									
BIT	7	6	5	4	3	2	1	0			
NAME		VOL0_TH[7:0]									
RESET	0	0	0	0	0	0	0	0			
VOL0_TH [7:0]		Headset Button Detection Threshold in BYPASS mode for ADC2 conversion. Higher than or equal to this value and lower than VOL1_TH[7:0] means the SEND/END button is pressed.									

Table 20. VOL1_TH Register (0x12)

ADDRESS	0x12	0x12									
MODE	Read/Write	Read/Write									
BIT	7	6	5	4	3	2	1	0			
NAME		VOL1_TH[7:0]									
RESET	0	0	0	0	0	0	0	0			
VOL1_TH [7:0]		Headset Button Detection Threshold in BYPASS mode for ADC2 conversion. Higher than or equal to this value and lower than VOL2_TH means the Volume up button is pressed.									

Table 21. VOL2_TH Register (0x13)

ADDRESS	0x13										
MODE	Read/Write	Read/Write									
BIT	7	6	5	4	3	2	1	0			
NAME		VOL2_TH[7:0]									
RESET	0	0	0	0	0	0	0	0			
VOL2_TH [7:0]		Headset Button Detection Threshold in BYPASS mode for ADC2 conversion. Higher than or equal to this value and lower than VOL3_TH means the Volume down button is pressed.									

Table 22. VOL3_TH Register (0x14)

ADDRESS	0x14	0x14									
MODE	Read/Write	Read/Write									
BIT	7	6	5	4	3	2	1	0			
NAME		VOL3_TH[7:0]									
RESET	0	0	0	0	0	0	0	0			
VOL3_TH [7:0]		Headset Button Detection Threshold in BYPASS mode for ADC2 conversion. Higher than or equal to this value means the reserved button is pressed.									

Table 23. PLC_STAT: POWER LINE COMMUNICATION STATUS Register (0x15)

ADDRESS	0x15									
MODE	Read Only									
BIT	7	6	5	4	3	2	1	0		
NAME	RFL	J[1:0]	PLC_TX_ ERR	PLC_TX_ OK	PLC_TX_P	PLC_RX_ ERR	NEW_ DATA	PLC_RX_ DET		
RESET	0	0 0 0 0 0 0 0								
RFU[1:0]	Reserved fo	r Future Use								
PLC_TX_ ERR	Cleared whe	Power Line Communication TX Error Cleared when a new SEND_CMD is issued. 0 = No TX Error 1 = TX Error								
PLC_TX_ OK	Cleared whe	Power Line Communication TX Successful Cleared when the new SEND_CMD issued. 0 = Communication not successful 1 = Communication successful								
PLC_TX_P	0 = Not Tran		TX in Progress	3						
PLC_RX_ ERR	0 = No error		RX Error necksum or stal	led line).						
NEW_ DATA	New Data Available Indicates that new data is available. Once ACC_ID/ACC_DB1/ACC_DB2 are read, it is cleared. 0 = No New Data Set 1 = New Data Set Arrived									
PLC_RX_ DET	Power Line Communication Receiving Detection (only during preamble and data excluding post-amble) 0 = No PLC (within 4-bit length of no or invalid signal) 1 = PLC is ongoing (within 4-bit of preamble signal)									

Table 24. PLC_IRQ: POWER LINE COMMUNICATION INTERRUPT Register (0x16)

ADDRESS	0x16								
MODE	Read Only								
BIT	7	6	5	4	3	2	1	0	
NAME	RFL	RFU[1:0] PLC_TX_ PLC_TX_ PLC_TX_PI PLC_RX_ NEW_ PLC_RX_DATAI DETI							
RESET	0	0	0	0	0	0	0	0	
RFU[1:0]	Reserved Fo	or Future Use							
PLC_TX_ ERRi	0 = Interrupt	Power Line Communication TX Error Interrupt 0 = Interrupt Not occurred 1 = Interrupt occurred (rising edge of PLC_TX_ERR)							
PLC_TX_ OKi	0 = Interrupt	Power Line Communication TX OK Interrupt 0 = Interrupt Not occurred 1 = Interrupt occurred (rising edge of PLC_TX_OK)							
PLC_TX_ Pi	0 = Interrupt	Communication Not occurred occurred (both	_	·					
PLC_RX_ ERRi	0 = Interrupt	Communication not occurred occurred (rising		'					
NEW_ DATAi	New Data RX Interrupt. 0 = Interrupt Not occurred 1 = Interrupt occurred (rising edge of NEW_DATA)								
PLC_RX_ DETi	Power Line Communication RX Detection Interrupt 0 = Interrupt Not occurred 1 = Interrupt occurred (both edges of PLC_RX_DET)								

Table 25. PLC_MASK: POWER LINE COMMUNICATION MASK Register (0x17)

ADDRESS	0x17									
MODE	Read/Write									
BIT	7	6	5	4	3	2	1	0		
NAME	RFL	RFU[1:0] PLC_TX_ PLC_TX_ PLC_TX_ PLC_RX_ NEW_ PLC_RX_ DATAM DETM								
RESET	0	0 0 0 0 0 0 0								
RFU[1:0]	Reserved Fo	or Future Use								
PLC_TX_ ERRM	0 = Masked	PLC TX Error Interrupt Mask. 0 = Masked 1 = Not masked								
PLC_TX_ OKm	PLC TX Successful Interrupt Mask. 0 = Masked 1 = Not masked									
PLC_TX_ Pm	PLC TX in P 0 = Masked 1 = Not mask	rogress Interru ked	pt Mask.							
PLC_RX_ ERRm	PLC_RX_EF 0 = Masked 1 = Not mask									
NEW_ DATAm	New Data Interrupt Mask. 0 = Masked 1 = Not masked									
PLC_RX_ DETm	Power Line Communication Receiving Detection Interrupt Mask. 0 = Masked 1 = Not masked									

Table 26. PLC_CON1: POWER LINE COMMUNICATION CONTROL Register (0x18)

ADDDECC	040									
ADDRESS	0x18									
MODE	Read/Write									
BIT	7	6	5	4	3	2	1	0		
NAME	RFU	RFU PLC_SINK POST_ AM_DIS FREQ PARITY[1:0] RFU SEND_ CMD								
RESET	0	0 0 0 0 1 0 0								
RFU	Reserved for	r Future Use								
PLC_SINK	PLC Current 0 = 100mA 1 = 80mA									
POST_ AM_DIS	0 = Post-am proper post-	Transmit Post-Amble Disable 0 = Post-amble enabled. The transmitter sends 2000 low bits. The receiver expects at least 16 low bits as a proper post-amble. 1 = Post-amble disabled								
FREQ	Communicat 0 = 24µsec 1 = 30µsec	tion Time Unit								
PARITY [1:0]	Parity Bit 00/11 = No F 01 = Odd 10 = Even	Parity. A high pa	rity bit is transr	nitted, but is igr	nored by the red	ceiver.				
RFU	Reserved for	r Future Use								
SEND_ CMD	Send Command Send the address (ACC_ADD) and data (ACC_DATA) bytes to the slave. Clears on completion of data transmission. 0 = No action 1 = Transfer the data									

Table 27. ACCESSORY ID Register (0x19)

ADDRESS	0x19	0x19								
MODE	Read Only	Read Only								
BIT	7	7 6 5 4 3 2 1 0								
NAME		ACC_ID[3:0] ACC_CAT[3:0]								
RESET	0	0 0 0 0 0 0 0								
ACC_ID [3:0]	,	Accessory ID Upper four bits of the first valid transmission. Four bit ID of the connected accessory.								
ACC_CAT [3:0]	,	Accessory Category Lower four bits of the first valid transmission. Accessory category or revision information.								

Table 28. ACC_DATA1 Receive Register (0x1A)

ADDRESS	0x1A							
MODE	Read Only							
BIT	7	7 6 5 4 3 2 1 0						
NAME	ACC_DATA1[7:0]							
RESET	0	0	0	0	0	0	0	0
ACC_ DATA1[7:0]	Accessory Data 1 First byte of raw data read from accessory							

Table 29. ACC_DATA2 Receive Register (0x1B)

ADDRESS	0x1B							
MODE	Read Only							
BIT	7	7 6 5 4 3 2 1 0						
NAME	ACC_DATA2[7:0]							
RESET	0	0	0	0	0	0	0	0
ACC_ DATA2[7:0]	Accessory Data 2 Second byte of raw data read from accessory							

Table 30. ACC_ADD Transmit Register (0x1C)

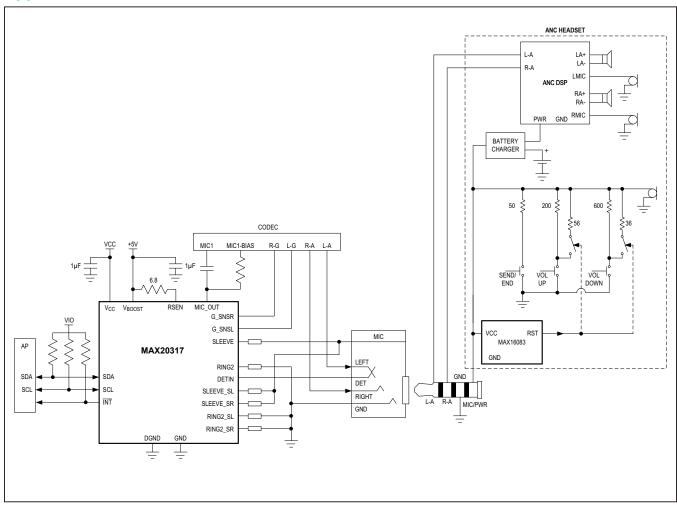
ADDRESS	0x1C							
MODE	Read/Write							
BIT	7	7 6 5 4 3 2 1 0						
NAME	ACC_ADD[7:0]							
RESET	0	0	0	0	0	0	0	0
ACC_ ADD[7:0]	Accessory Target Address							

Table 31. ACC_DATA Transmit Register (0x1D)

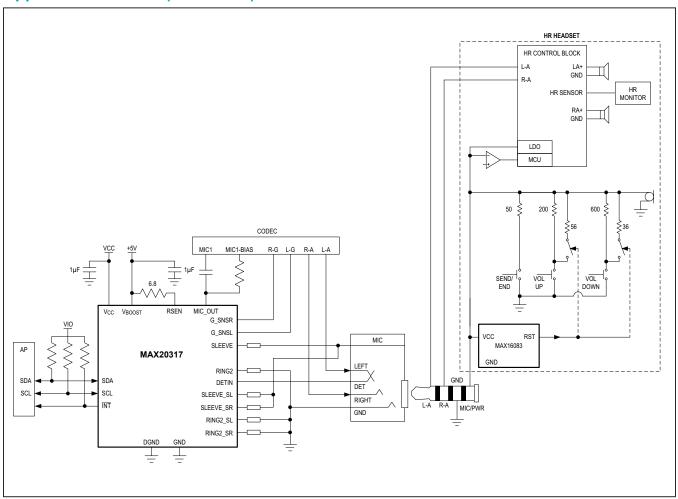
ADDRESS	0x1D							
MODE	Read/Write							
BIT	7	7 6 5 4 3 2 1 0						
NAME	ACC_DATA[7:0]							
RESET	0	0	0	0	0	0	0	0
ACC_ DATA[7:0]	Accessory Target Data							

^{**}Denotes a factory programmable value

Application Circuits



Application Circuits (continued)



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20317EWP+	-40°C to +85°C	20 WLP
MAX20317EWP+T	-40°C to +85°C	20 WLP

⁺Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BICMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE	PACKAGE	OUTLINE	LAND
TYPE	CODE	NO.	PATTERN NO.
20 WLP	W201H2+1	21-100120	Refer to Application Note 1891

T Denotes tape-and-reel

MAX20317

Universal 3.5mmØ Accessory Management IC

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/17	Initial release	_

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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