

# 4-Mbit (512K words × 8 bit) Static RAM with Error-Correcting Code (ECC)

## Features

- High speed: 45 ns/55 ns
- Ultra-low standby power
  - Typical standby current: 3.5 μA
  - Maximum standby current: 8.7 μA
- Embedded ECC for single-bit error correction<sup>[1]</sup>
- Wide voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Pb-free 32-pin SOIC and 32-pin TSOP II packages

## Functional Description

CY62148G is a high-performance CMOS low-power (MoBL) SRAM device with embedded ECC<sup>[1]</sup>. This device is offered multiple pin configurations.

Device is accessed by asserting the chip enable ( $\overline{CE}$ ) input LOW. Data writes are performed by asserting the Write Enable ( $\overline{WE}$ ) input LOW, while providing the data on I/O<sub>0</sub> through I/O<sub>7</sub> and address on A<sub>0</sub> through A<sub>18</sub> pins.

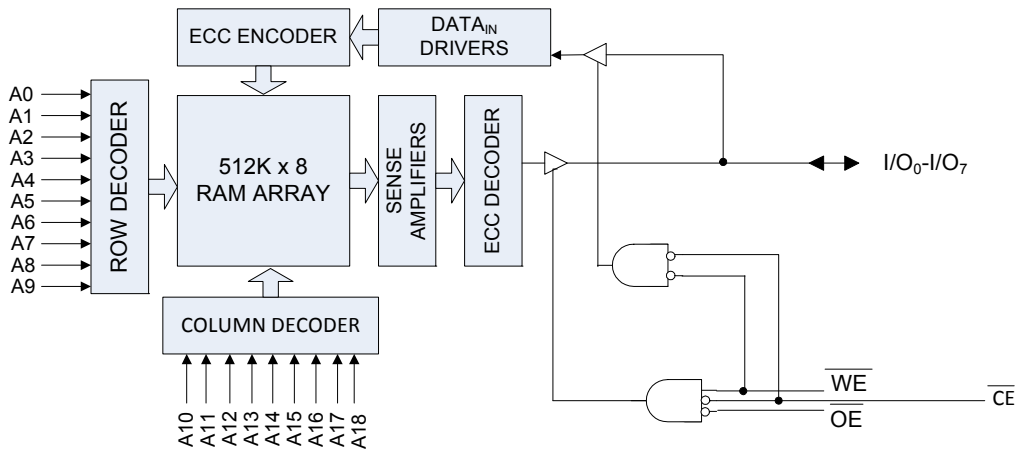
Data reads are performed by asserting the Output Enable ( $\overline{OE}$ ) input and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O<sub>0</sub> through I/O<sub>7</sub>).

All I/Os (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a HI-Z state when the device is deselected ( $\overline{CE}$  HIGH or control signal  $\overline{OE}$  is de-asserted).

See the [Truth Table – CY62148G on page 12](#) for a complete description of read and write modes.

The logic block diagrams are on page 2.

## Logic Block Diagram – CY62148G



### Note

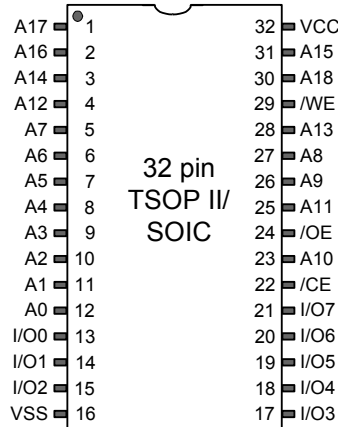
1. This device does not support automatic write-back on error detection.

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## Pin Configurations

Figure 1. 32-pin SOIC/TSOP II pinout



## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)	Speed (ns)	Power Dissipation			
				Operating I <sub>CC</sub> , (mA)		Standby, I <sub>SB2</sub> (μA)	
				f = f <sub>max</sub>		Typ <sup>[2]</sup>	Max
				Typ <sup>[2]</sup>	Max		
CY62148G18	Industrial	1.65 V–2.2 V	55	–	20	–	10
CY62148G30		2.2 V–3.6 V	45	–	20	3.5	8.7
CY62148G		4.5 V–5.5 V					

**Note**

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 1.8 V (for a V<sub>CC</sub> range of 1.65 V–2.2 V), V<sub>CC</sub> = 3 V (for V<sub>CC</sub> range of 2.2 V–3.6 V), and V<sub>CC</sub> = 5 V (for V<sub>CC</sub> range of 4.5 V–5.5 V), T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .....	-65 °C to + 150 °C
Ambient temperature with power applied .....	-55 °C to + 125 °C
Supply voltage to ground potential <sup>[3]</sup> .....	-0.5 V to V <sub>CC</sub> + 0.5 V
DC voltage applied to outputs in HI-Z state <sup>[3]</sup> .....	-0.5 V to V <sub>CC</sub> + 0.5 V

DC input voltage <sup>[3]</sup> .....	-0.5 V to V <sub>CC</sub> + 0.5 V
Output current into outputs (in low state) .....	20 mA
Static discharge voltage (MIL-STD-883, Method 3015) .....	>2001 V
Latch-up current .....	>140 mA

## Operating Range

Grade	Ambient Temperature	V <sub>CC</sub> <sup>[4]</sup>
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

## DC Electrical Characteristics

Over the operating range of -40 °C to 85 °C

Parameter	Description	Test Conditions	45 ns / 55 ns			Unit	
			Min	Typ	Max		
V <sub>OH</sub>	Output HIGH voltage	1.65 V to 2.2 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	1.4	-	-	V
		2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	2	-	-	
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0 mA	2.2	-	-	
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0 mA	2.4	-	-	
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> - 0.5 <sup>[5]</sup>	-	-	
V <sub>OL</sub>	Output LOW voltage	1.65 V to 2.2 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA	-	-	0.2	V
		2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA	-	-	0.4	
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 2.1 mA	-	-	0.4	
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 2.1 mA	-	-	0.4	
V <sub>IH</sub>	Input HIGH voltage	1.65 V to 2.2 V	-	1.4	-	V <sub>CC</sub> + 0.2 <sup>[3]</sup>	V
		2.2 V to 2.7 V	-	1.8	-	V <sub>CC</sub> + 0.3 <sup>[3]</sup>	
		2.7 V to 3.6 V	-	2	-	V <sub>CC</sub> + 0.3 <sup>[3]</sup>	
		4.5 V to 5.5 V	-	2.2	-	V <sub>CC</sub> + 0.5 <sup>[3]</sup>	
V <sub>IL</sub>	Input LOW voltage	1.65 V to 2.2 V	-	-0.2 <sup>[3]</sup>	-	0.4	V
		2.2 V to 2.7 V	-	-0.3 <sup>[3]</sup>	-	0.6	
		2.7 V to 3.6 V	-	-0.3 <sup>[3]</sup>	-	0.8	
		4.5 V to 5.5 V	-	-0.5 <sup>[3]</sup>	-	0.8	
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	-	+1	μA	
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output disabled	-1	-	+1	μA	
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	Max V <sub>CC</sub> , I <sub>OUT</sub> = 0 mA, CMOS levels	f = 22.22 MHz (45 ns)	-	-	20	mA
			f = 18.18 MHz (55 ns)	-	-	20	mA
			f = 1 MHz	-	-	6	mA

### Notes

- V<sub>IL(min)</sub> = -2.0 V and V<sub>IH(max)</sub> = V<sub>CC</sub> + 2 V for pulse durations of less than 20 ns.
- Full Device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.
- This parameter is guaranteed by design and not tested.

**DC Electrical Characteristics** (continued)

Over the operating range of –40 °C to 85 °C

Parameter	Description	Test Conditions	45 ns / 55 ns			Unit	
			Min	Typ	Max		
$I_{SB1}^{[6]}$	Automatic power down current – CMOS inputs; $V_{CC} = 2.2\text{ V to }3.6\text{ V and }4.5\text{ V to }5.5\text{ V}$	$\overline{CE}_1 \geq V_{CC} - 0.2\text{ V or }CE_2 \leq 0.2\text{ V,}$ $V_{IN} \geq V_{CC} - 0.2\text{ V or }V_{IN} \leq 0.2\text{ V,}$	–	–	8.7	$\mu\text{A}$	
	Automatic power down current – CMOS inputs $V_{CC} = 1.65\text{ V to }2.2\text{ V}$	$f = f_{\text{max}}$ (address and data only), $f = 0$ ( $\overline{OE}$ , and $\overline{WE}$ ), Max $V_{CC}$	–	–	10		
$I_{SB2}^{[6]}$	Automatic power down current – CMOS inputs $V_{CC} = 2.2\text{ V to }3.6\text{ V and }4.5\text{ V to }5.5\text{ V}$	$\overline{CE}_1 \geq V_{CC} - 0.2\text{ V or }CE_2 \leq 0.2\text{ V,}$ $V_{IN} \geq V_{CC} - 0.2\text{ V or }V_{IN} \leq 0.2\text{ V,}$ $f = 0, \text{ Max } V_{CC}$	25 °C <sup>[7]</sup>	–	3.5	3.7	$\mu\text{A}$
			40 °C <sup>[7]</sup>	–	–	4.8	
			70 °C <sup>[7]</sup>	–	–	7	
			85 °C	–	–	8.7	
	Automatic power down current – CMOS inputs $V_{CC} = 1.65\text{ V to }2.2\text{ V}$	$\overline{CE}_1 \geq V_{CC} - 0.2\text{ V or }CE_2 \leq 0.2\text{ V,}$ $V_{IN} \geq V_{CC} - 0.2\text{ V or }V_{IN} \leq 0.2\text{ V,}$ $f = 0, \text{ Max } V_{CC}$	25 °C <sup>[7]</sup>	–	3.5	4.3	
			40 °C <sup>[7]</sup>	–	–	5	
			70 °C <sup>[7]</sup>	–	–	7.5	
			85 °C	–	–	10	

**Notes**

6. Chip enables  $\overline{CE}$  must be tied to CMOS levels to meet the  $I_{SB1} / I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.  
 7. The  $I_{SB2}$  limits at 25 °C, 40 °C, 70 °C, and typical limit at 85 °C are guaranteed by design and not 100% tested.

## Capacitance

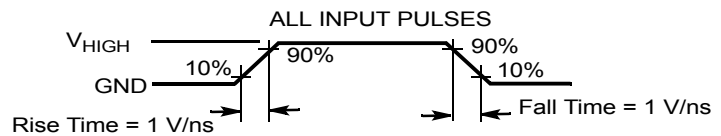
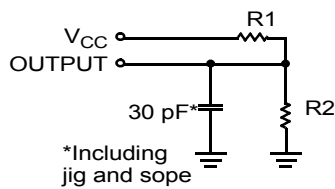
Parameter <sup>[8]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

## Thermal Resistance

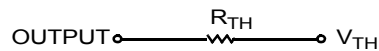
Parameter <sup>[8]</sup>	Description	Test Conditions	32-pin SOIC	32-pin TSOP II	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	51.79	79.03	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		25.12	17.44	°C/W

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms<sup>[9]</sup>



Equivalent to: THÉVENIN EQUIVALENT



Parameters	1.8 V	2.5 V	3.0 V	5.0 V	Unit
R <sub>1</sub>	13500	16667	1103	1800	Ω
R <sub>2</sub>	10800	15385	1554	990	Ω
R <sub>TH</sub>	6000	8000	645	639	Ω
V <sub>TH</sub>	0.80	1.20	1.75	1.77	V

### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Full-device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs.

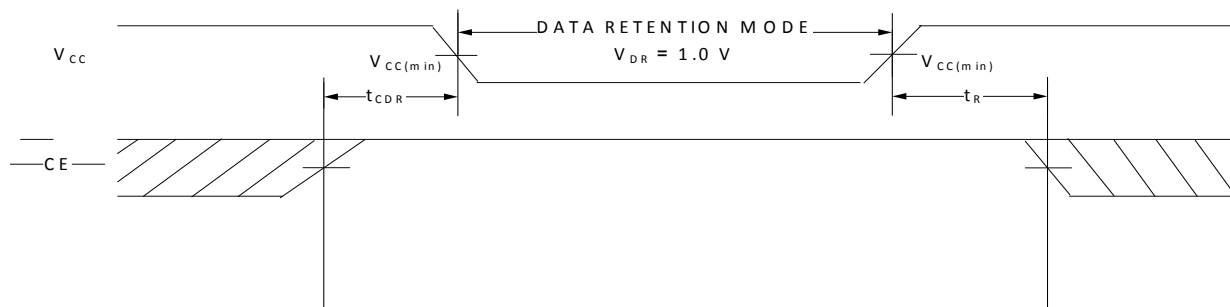
## Data Retention Characteristics

Over the Operating range

Parameter	Description	Conditions	Min	Typ <sup>[10]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1	–	–	V
$I_{CCDR}$ <sup>[11, 12]</sup>	Data retention current	$V_{CC} = 1.2\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	13	$\mu\text{A}$
$t_{CDR}$ <sup>[13, 14]</sup>	Chip deselect to data retention time		0	–	–	ns
$t_R$ <sup>[14]</sup>	Operation recovery time		45/55	–	–	ns

## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

- Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8\text{ V}$  (for  $V_{CC}$  range of 1.65 V–2.2 V),  $V_{CC} = 3\text{ V}$  (for  $V_{CC}$  range of 2.2 V–3.6 V), and  $V_{CC} = 5\text{ V}$  (for  $V_{CC}$  range of 4.5 V–5.5 V),  $T_A = 25\text{ }^\circ\text{C}$ .
- Chip enables  $\overline{CE}$  must be tied to CMOS levels to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.
- $I_{CCDR}$  is guaranteed only after device is first powered up to  $V_{CC(min)}$  and then brought down to  $V_{DR}$ .
- These parameters are guaranteed by design.
- Full-device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .

## AC Switching Characteristics

Parameter <sup>[15, 16]</sup>	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{RC}$	Read cycle time	45	–	55	–	ns
$t_{AA}$	Address to data valid	–	45	–	55	ns
$t_{OHA}$	Data hold from address change	10	–	10	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	45	–	55	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low impedance <sup>[17]</sup>	5	–	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to HI-Z <sup>[17, 18]</sup>	–	18	–	18	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low impedance <sup>[17]</sup>	10	–	10	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to HI-Z <sup>[17, 18]</sup>	–	18	–	18	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up	0	–	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-down	–	45	–	55	ns
<b>Write Cycle</b> <sup>[19, 20]</sup>						
$t_{WC}$	Write cycle time	45	–	55	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	35	–	45	–	ns
$t_{AW}$	Address setup to write end	35	–	45	–	ns
$t_{HA}$	Address hold from write end	0	–	0	–	ns
$t_{SA}$	Address setup to write start	0	–	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	35	–	40	–	ns
$t_{SD}$	Data setup to write end	25	–	25	–	ns
$t_{HD}$	Data hold from write end	0	–	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to HI-Z <sup>[17, 18]</sup>	–	18	–	20	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low impedance <sup>[17]</sup>	10	–	10	–	ns

### Notes

15. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \geq 3$  V) and  $V_{CC}/2$  (for  $V_{CC} < 3$  V), and input pulse levels of 0 to 3 V (for  $V_{CC} \geq 3$  V) and 0 to  $V_{CC}$  (for  $V_{CC} < 3$  V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
16. These parameters are guaranteed by design.
17. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
18.  $t_{HZOE}$ ,  $t_{HZCE}$  and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
19. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
20. The minimum pulse width in Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to sum of  $t_{SD}$  and  $t_{HZWE}$ .



## Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [21, 22]

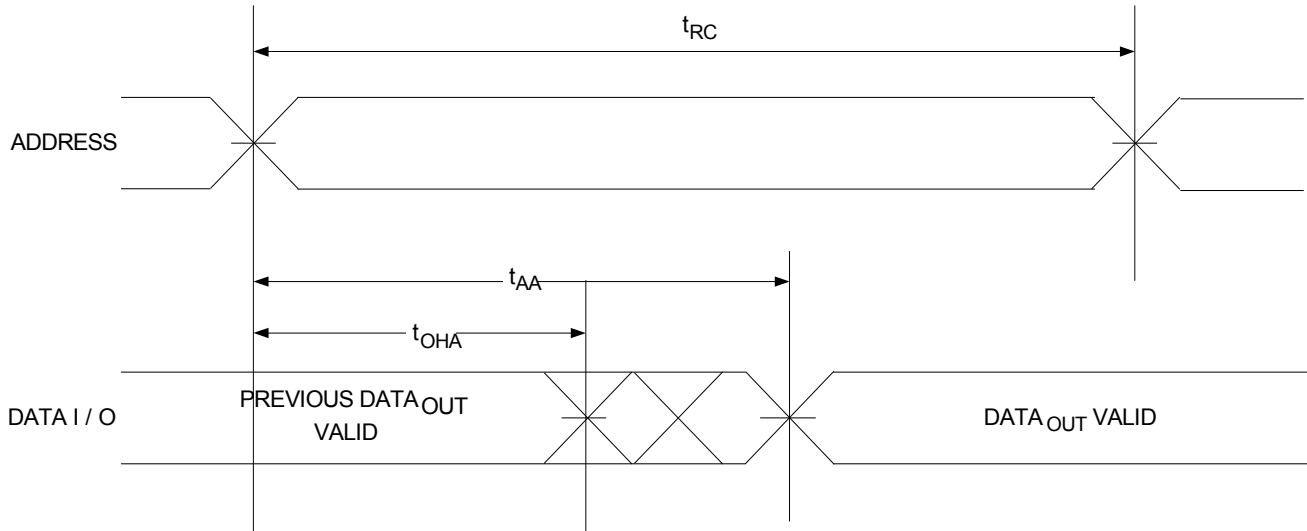
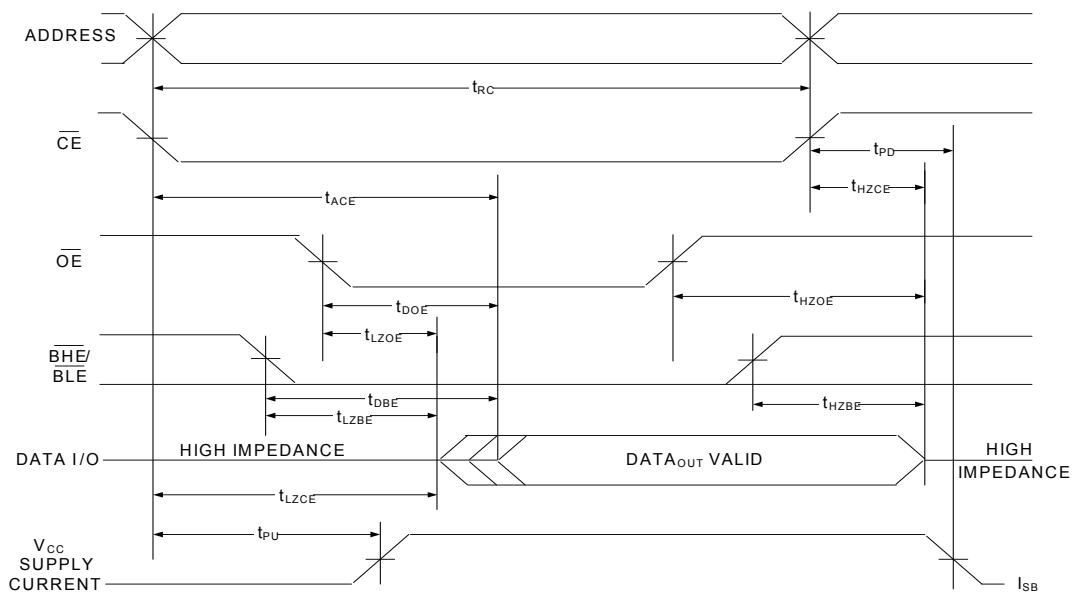


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [22, 23]



### Notes

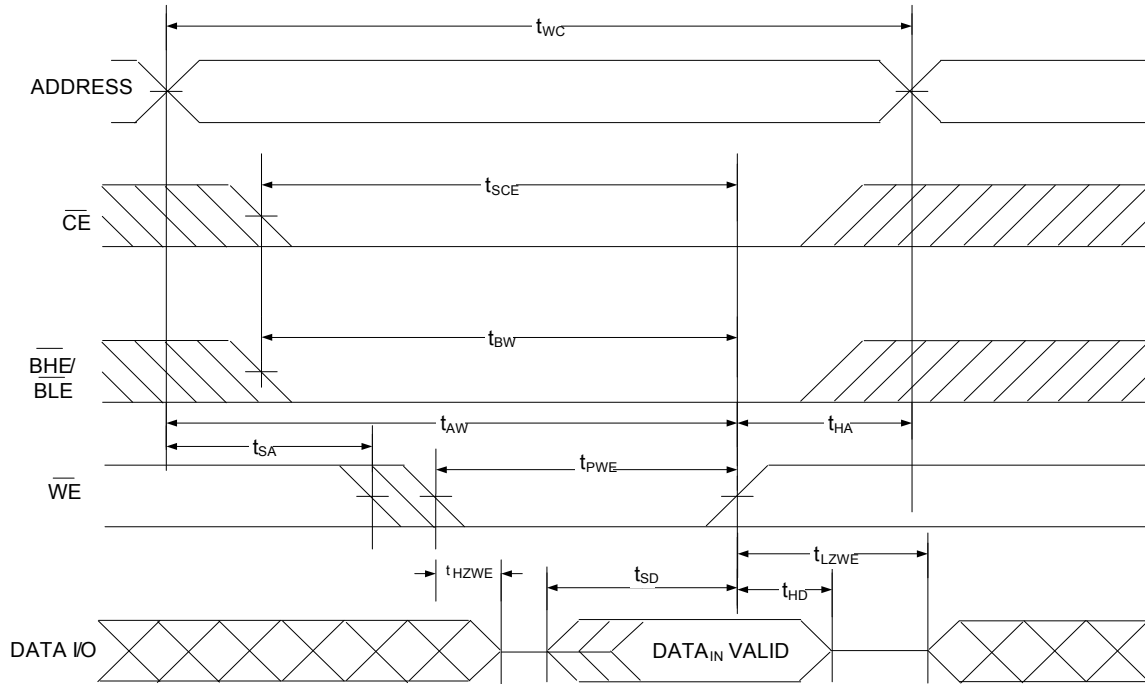
21. The device is continuously selected.  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ .

22.  $\overline{WE}$  is HIGH for Read cycle.

23. Address valid prior to or coincident with  $\overline{CE}$  LOW transition.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled) [24, 25, 26]



Notes

24.  $\overline{\text{WE}}$  is HIGH for Read cycle.

25. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

26. Data I/O is in a HI-Z state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$ .

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled) [27, 28]

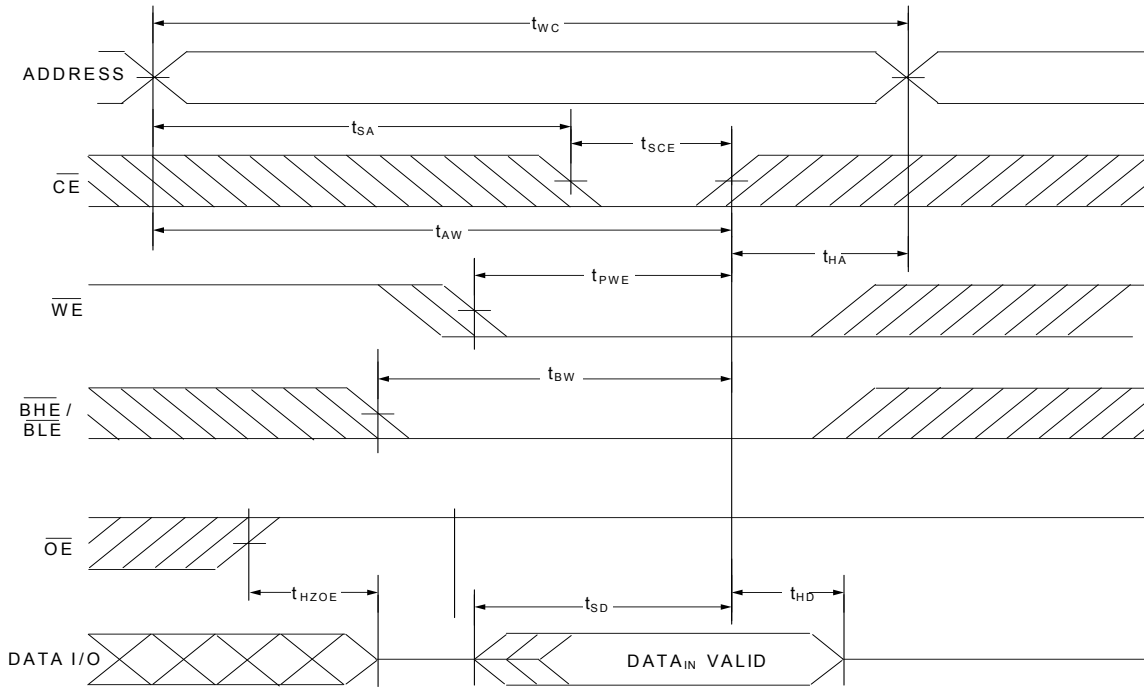
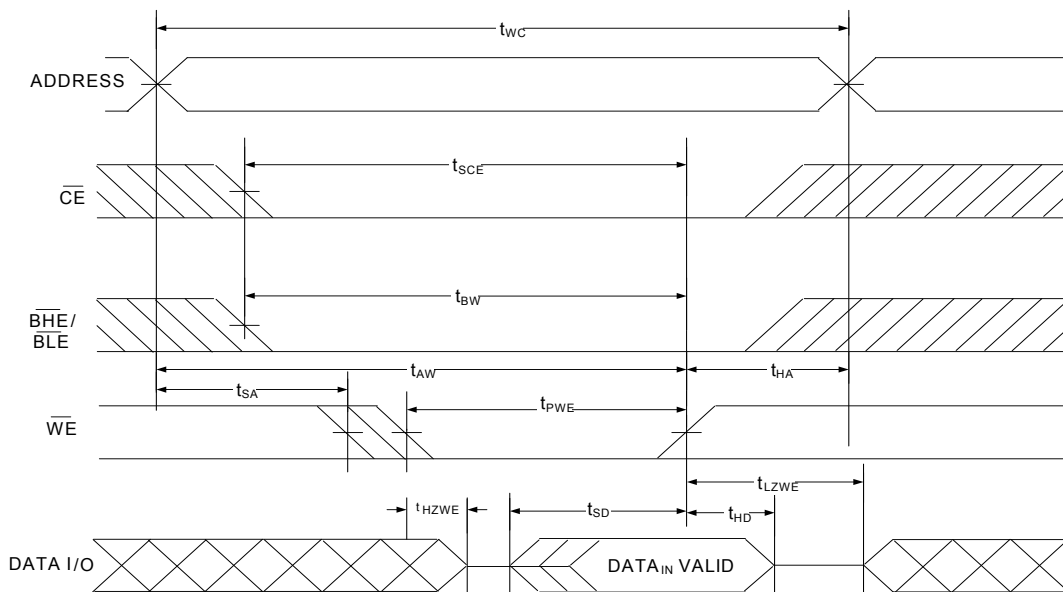


Figure 8. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [27, 28, 29]



Notes

27. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{IL}$ ,  $\overline{\text{CE}} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

28. Data I/O is in HI-Z state if  $\overline{\text{CE}} = V_{IH}$  or  $\overline{\text{OE}} = V_{IH}$

29. The minimum write pulse width for Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) should be sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Truth Table – CY62148G**

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs	Mode	Power	Configuration
H	X <sup>[30]</sup>	X <sup>[30]</sup>	HI-Z	Deselect/Power-down	Standby ( $I_{\text{SB}}$ )	512 K × 8
L	H	L	Data Out (I/O <sub>0</sub> –I/O <sub>7</sub> )	Read	Active ( $I_{\text{CC}}$ )	512 K × 8
L	H	H	HI-Z	Output disabled	Active ( $I_{\text{CC}}$ )	512 K × 8
L	L	X <sup>[30]</sup>	Data In (I/O <sub>0</sub> –I/O <sub>7</sub> )	Write	Active ( $I_{\text{CC}}$ )	512 K × 8

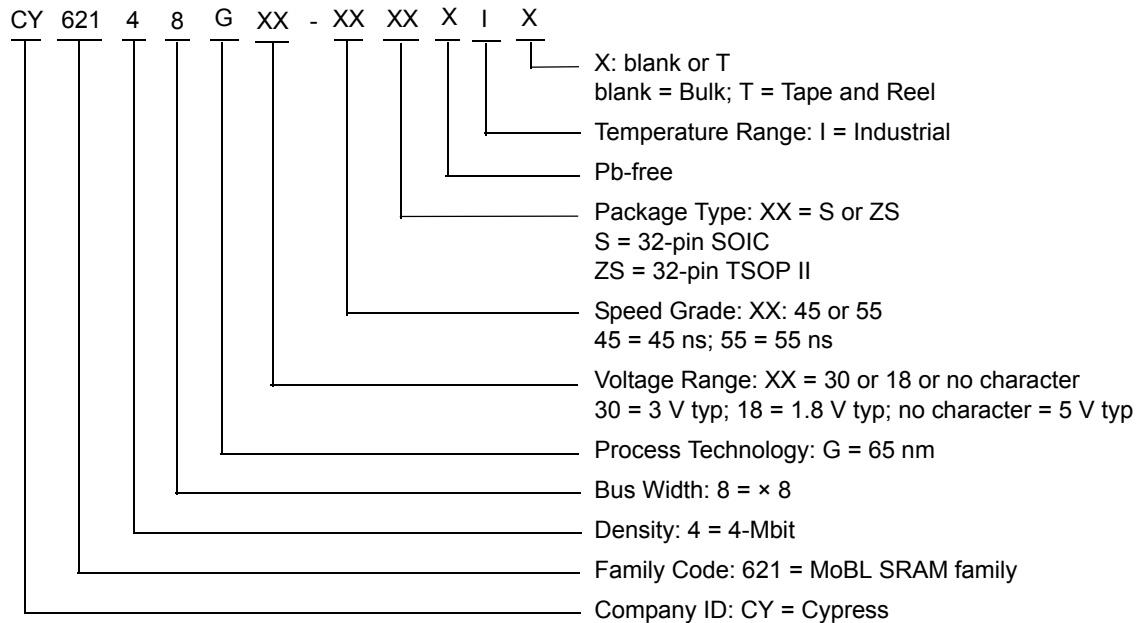
**Note**

30. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

### Ordering Information

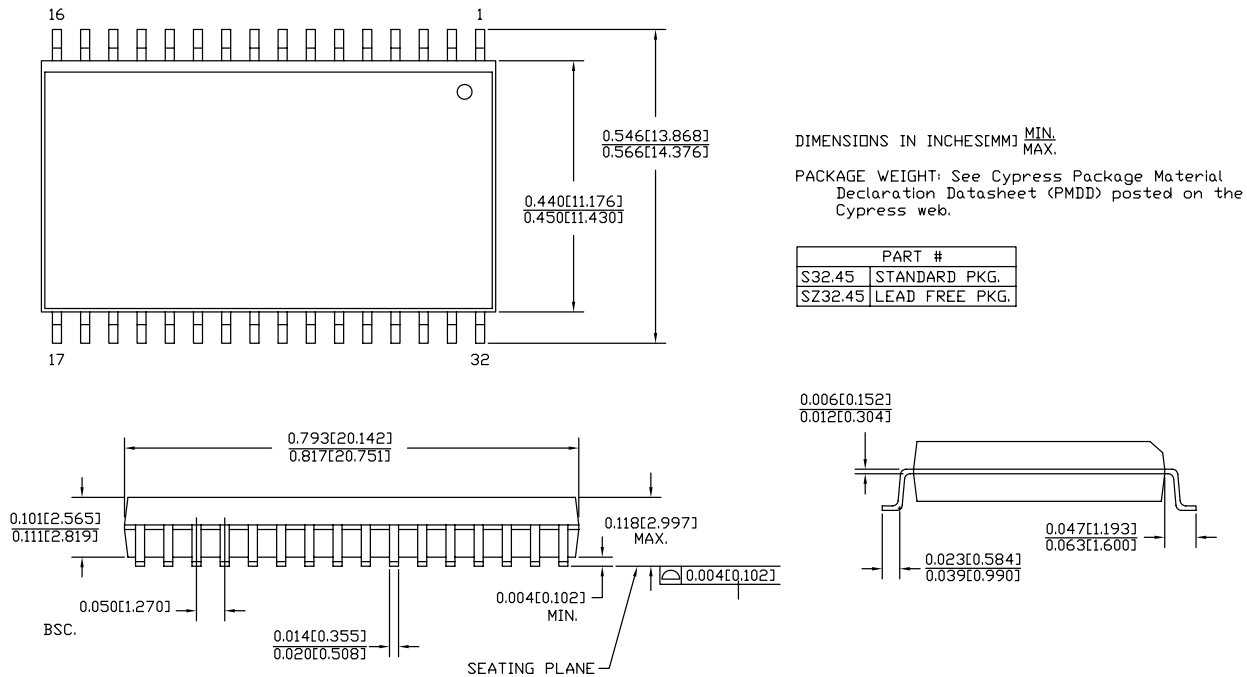
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type	Operating Range
45	2.2 V–3.6 V	CY62148G30-45SXI	51-85081	32-pin SOIC (450 Mils)	Industrial
		CY62148G30-45SXIT	51-85081	32-pin SOIC (450 Mils), Tape and Reel	
		CY62148G30-45ZSXI	51-85095	32-pin TSOP II	
		CY62148G30-45ZSXIT	51-85095	32-pin TSOP II, Tape and Reel	
	4.5 V–5.5 V	CY62148G-45SXI	51-85081	32-pin SOIC (450 Mils)	
		CY62148G-45SXIT	51-85081	32-pin SOIC (450 Mils), Tape and Reel	
		CY62148G-45ZSXI	51-85095	32-pin TSOP II	
		CY62148G-45ZSXIT	51-85095	32-pin TSOP II, Tape and Reel	
55	1.65 V–2.2 V	CY62148G18-55ZSXI	51-85095	32-pin TSOP II	
		CY62148G18-55ZSXIT	51-85095	32-pin TSOP II, Tape and Reel	

### Ordering Code Definitions



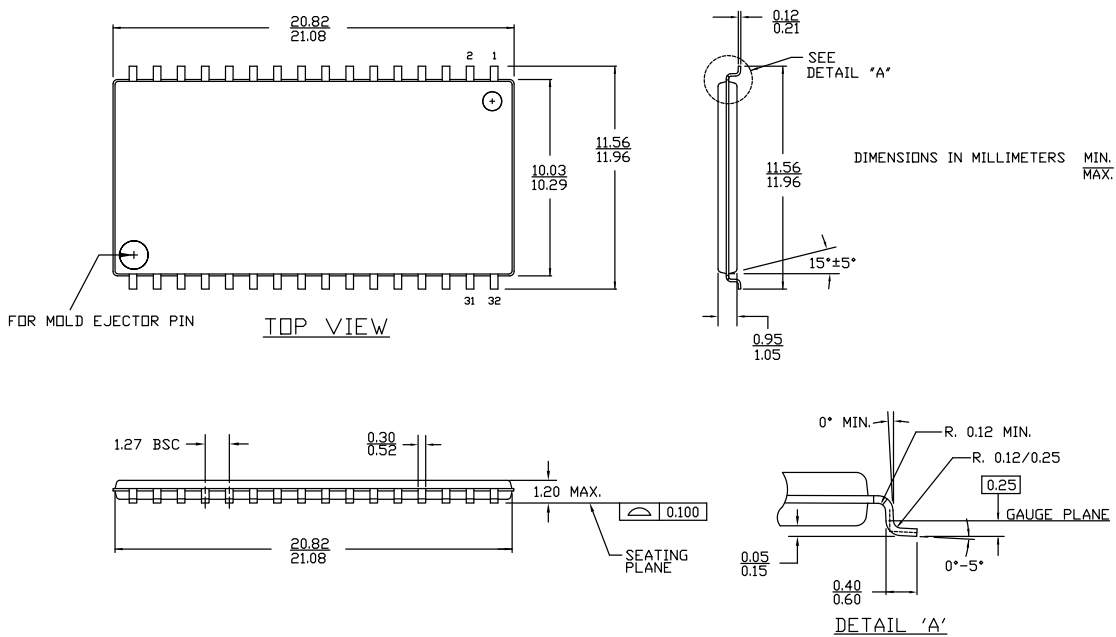
Package Diagrams

Figure 9. 32-pin SOIC (450 Mils) S32.45/SZ32.45 Package Outline, 51-85081



51-85081 \*E

Figure 10. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32 Package Outline, 51-85095



51-85095 \*D

## Acronyms

Acronym	Description
$\overline{\text{CE}}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{\text{OE}}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
VFBGA	very fine-pitch ball grid array
$\overline{\text{WE}}$	write enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microamperes
μs	microseconds
mA	milliamperes
mm	millimeters
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

## Document History Page

Document Title: CY62148G MoBL <sup>®</sup> , 4-Mbit (512K words × 8 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-95415				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*B	5054381	NILE	12/17/2015	Changed status from Preliminary to Final.
*C	5082528	NILE	01/12/2016	Updated <a href="#">Ordering Information</a> : Updated part numbers. Completing Sunset Review.
*D	5432526	NILE	09/10/2016	Updated <a href="#">Maximum Ratings</a> : Updated Note 3 (Replaced "2 ns" with "20 ns"). Updated <a href="#">DC Electrical Characteristics</a> : Changed minimum value of $V_{IH}$ parameter from 2.0 V to 1.8 V corresponding to Operating Range "2.2 V to 2.7 V". Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated to new template.
*E	5979578	AESATMP8	12/01/2017	Updated logo and Copyright.



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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: [ocean@oceanchips.ru](mailto:ocean@oceanchips.ru)

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Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А