# 4-Mbit (512K words × 8 bit) Static RAM with Error-Correcting Code (ECC)

## Features

- High speed: 45 ns/55 ns
- Ultra-low standby power
  - Typical standby current: 3.5 µA
  - Maximum standby current: 8.7 µA
- Embedded ECC for single-bit error correction[1]
- Wide voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Pb-free 32-pin SOIC and 32-pin TSOP II packages

## Functional Description

CY62148G is a high-performance CMOS low-power (MoBL) SRAM device with embedded ECC[1]. This device is offered multiple pin configurations.

Device is accessed by asserting the chip enable ($\overline{CE}$) input LOW. Data writes are performed by asserting the Write Enable ($\overline{WE}$) input LOW, while providing the data on I/$O_0$ through I/$O_7$ and address on $A_0$ through $A_{18}$ pins.

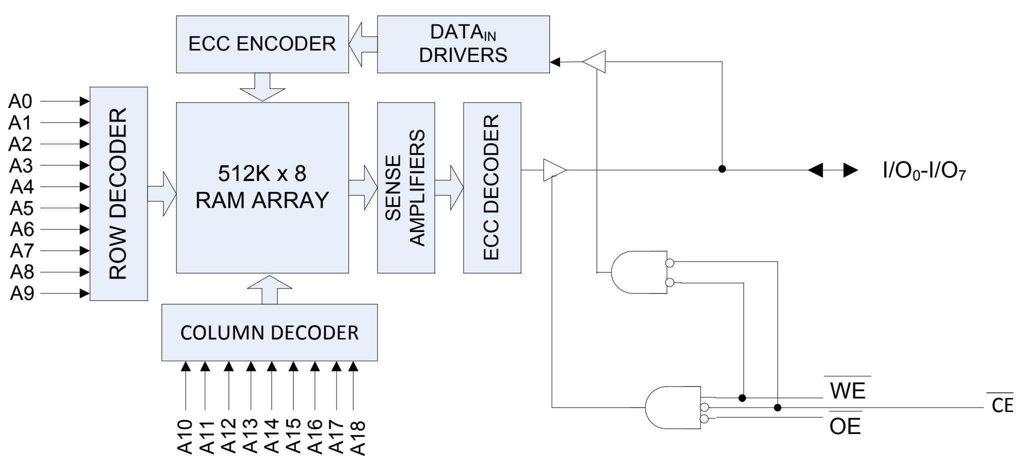
Data reads are performed by asserting the Output Enable ($\overline{OE}$) input and providing the required address on the address lines. Read data is accessible on the I/O lines (I/$O_0$ through I/$O_7$).

All I/Os (I/$O_0$ through I/$O_7$) are placed in a HI-Z state when the device is deselected ($\overline{CE}$ HIGH or control signal $\overline{OE}$ is de-asserted).

See the Truth Table – CY62148G on page 12 for a complete description of read and write modes.

The logic block diagrams are on page 2.

## Logic Block Diagram – CY62148G

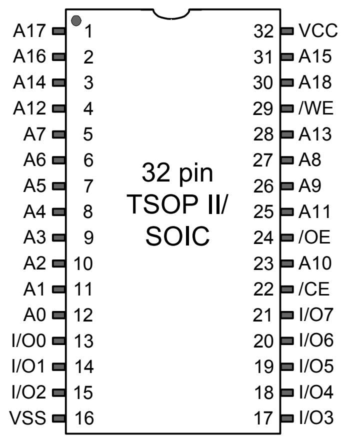



**Note**
1. This device does not support automatic write-back on error detection.

## Contents

## Pin Configurations

**Figure 1. 32-pin SOIC/TSOP II pinout**




## Product Portfolio

| Product | Range | $V_{CC}$ Range (V) | Speed (ns) | Power Dissipation | | | |
|---|---|---|---|---|---|---|---|
| | | | | Operating $I_{CC}$, (mA) f = $f_{max}$ | | Standby, $I_{SB2}$ (µA) | |
| | | | | Typ[2] | Max | Typ[2] | Max |
| CY62148G18 | Industrial | 1.65 V–2.2 V | 55 | – | 20 | – | 10 |
| CY62148G30 | | 2.2 V–3.6 V | 45 | – | 20 | 3.5 | 8.7 |
| CY62148G | | 4.5 V–5.5 V | | | | | |

**Note**
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = 1.8 V (for a $V_{CC}$ range of 1.65 V–2.2 V), $V_{CC}$ = 3 V (for $V_{CC}$ range of 2.2 V–3.6 V), and $V_{CC}$ = 5 V (for $V_{CC}$ range of 4.5 V–5.5 V), $T_A$ = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ............................... –65 °C to + 150 °C

Ambient temperature
with power applied ................................. –55 °C to + 125 °C

Supply voltage
to ground potential[3] ...........................–0.5 V to Vcc + 0.5 V

DC voltage applied to outputs
in HI-Z state[3]..................................... –0.5 V to $V_{CC}$ + 0.5 V

DC input voltage[3] .............................. –0.5 V to $V_{CC}$ + 0.5 V

Output current into outputs (in low state) ................... 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) ................................ >2001 V

Latch-up current .................................................... >140 mA

## Operating Range

| Grade | Ambient Temperature | $V_{CC}$[4] |
|---|---|---|
| Industrial | –40 °C to +85 °C | 1.65 V to 2.2 V,<br>2.2 V to 3.6 V,<br>4.5 V to 5.5 V |

## DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

| Parameter | Description | | Test Conditions | | 45 ns / 55 ns Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH voltage | 1.65 V to 2.2 V | $V_{CC}$ = Min, $I_{OH}$ = –0.1 mA | | 1.4 | – | – | V |
| | | 2.2 V to 2.7 V | $V_{CC}$ = Min, $I_{OH}$ = –0.1 mA | | 2 | – | – | |
| | | 2.7 V to 3.6 V | $V_{CC}$ = Min, $I_{OH}$ = –1.0 mA | | 2.2 | – | – | |
| | | 4.5 V to 5.5 V | $V_{CC}$ = Min, $I_{OH}$ = –1.0 mA | | 2.4 | – | – | |
| | | 4.5 V to 5.5 V | $V_{CC}$ = Min, $I_{OH}$ = –0.1 mA | | $V_{CC}$ – 0.5[5] | – | – | |
| $V_{OL}$ | Output LOW voltage | 1.65 V to 2.2 V | $V_{CC}$ = Min, $I_{OL}$ = 0.1 mA | | – | – | 0.2 | V |
| | | 2.2 V to 2.7 V | $V_{CC}$ = Min, $I_{OL}$ = 0.1 mA | | – | – | 0.4 | |
| | | 2.7 V to 3.6 V | $V_{CC}$ = Min, $I_{OL}$ = 2.1 mA | | – | – | 0.4 | |
| | | 4.5 V to 5.5 V | $V_{CC}$ = Min, $I_{OL}$ = 2.1 mA | | – | – | 0.4 | |
| $V_{IH}$ | Input HIGH voltage | 1.65 V to 2.2 V | – | | 1.4 | – | $V_{CC}$ + 0.2[3] | V |
| | | 2.2 V to 2.7 V | – | | 1.8 | – | $V_{CC}$ + 0.3[3] | |
| | | 2.7 V to 3.6 V | – | | 2 | – | $V_{CC}$ + 0.3[3] | |
| | | 4.5 V to 5.5 V | – | | 2.2 | – | $V_{CC}$ + 0.5[3] | |
| $V_{IL}$ | Input LOW voltage | 1.65 V to 2.2 V | – | | –0.2[3] | – | 0.4 | V |
| | | 2.2 V to 2.7 V | – | | –0.3[3] | – | 0.6 | |
| | | 2.7 V to 3.6 V | – | | –0.3[3] | – | 0.8 | |
| | | 4.5 V to 5.5 V | – | | –0.5[3] | – | 0.8 | |
| $I_{IX}$ | Input leakage current | | GND ≤ $V_{IN}$ ≤ $V_{CC}$ | | –1 | – | +1 | µA |
| $I_{OZ}$ | Output leakage current | | GND ≤ $V_{OUT}$ ≤ $V_{CC}$, Output disabled | | –1 | – | +1 | µA |
| $I_{CC}$ | $V_{CC}$ operating supply current | | Max $V_{CC}$, $I_{OUT}$ = 0 mA, CMOS levels | f = 22.22 MHz (45 ns) | – | – | 20 | mA |
| | | | | f = 18.18 MHz (55 ns) | – | – | 20 | mA |
| | | | | f = 1 MHz | – | – | 6 | mA |

**Notes**
3. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = $V_{CC}$ + 2 V for pulse durations of less than 20 ns.
4. Full Device AC operation assumes a 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after Vcc stabilization.
5. This parameter is guaranteed by design and not tested.

## DC Electrical Characteristics (continued)

Over the operating range of –40 °C to 85 °C

| Parameter | Description | Test Conditions | | 45 ns / 55 ns | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $I_{SB1}$[6] | Automatic power down current – CMOS inputs; $V_{CC}$ = 2.2 V to 3.6 V and 4.5 V to 5.5 V | $\overline{CE}_1 \geq V_{CC}$ – 0.2 V or $CE_2 \leq$ 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = $f_{max}$ (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), Max $V_{CC}$ | | – | – | 8.7 | µA |
| | Automatic power down current – CMOS inputs $V_{CC}$ = 1.65 V to 2.2 V | | | – | – | 10 | |
| $I_{SB2}$[6] | Automatic power down current – CMOS inputs $V_{CC}$ = 2.2 V to 3.6 V and 4.5 V to 5.5 V | $\overline{CE}_1 \geq V_{CC}$ – 0.2 V or $CE_2 \leq$ 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, Max $V_{CC}$ | 25 °C [7] | – | 3.5 | 3.7 | µA |
| | | | 40 °C [7] | – | – | 4.8 | |
| | | | 70 °C [7] | – | – | 7 | |
| | | | 85 °C | – | – | 8.7 | |
| | Automatic power down current – CMOS inputs $V_{CC}$ = 1.65 V to 2.2 V | $\overline{CE}_1 \geq V_{CC}$ – 0.2 V or $CE_2 \leq$ 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, Max $V_{CC}$ | 25 °C [7] | – | 3.5 | 4.3 | |
| | | | 40 °C [7] | – | – | 5 | |
| | | | 70 °C [7] | – | – | 7.5 | |
| | | | 85 °C | – | – | 10 | |

**Notes**

6. Chip enables ($\overline{CE}$ must be tied to CMOS levels to meet the $I_{SB1}$ / $I_{SB2}$ / $I_{CCDR}$ spec. Other inputs can be left floating.
7. The $I_{SB2}$ limits at 25 °C, 40 °C, 70 °C, and typical limit at 85 °C are guaranteed by design and not 100% tested.

## Capacitance

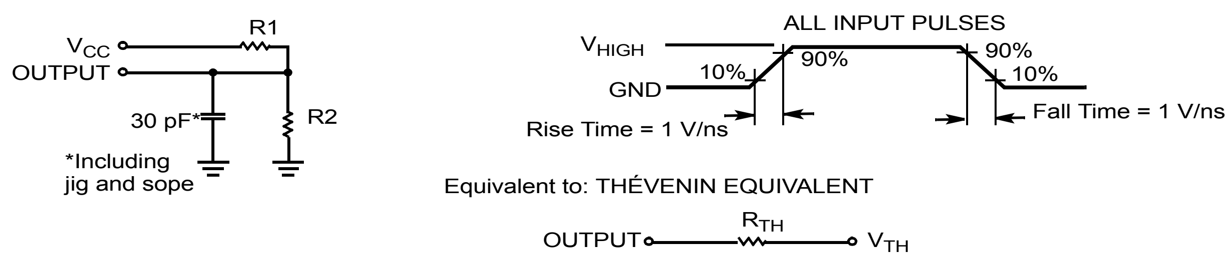
| Parameter [8] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | Output capacitance | | 10 | pF |

## Thermal Resistance

| Parameter [8] | Description | Test Conditions | 32-pin SOIC | 32-pin TSOP II | Unit |
|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 51.79 | 79.03 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 25.12 | 17.44 | °C/W |

## AC Test Loads and Waveforms

**Figure 2. AC Test Loads and Waveforms [9]**




| Parameters | 1.8 V | 2.5 V | 3.0 V | 5.0 V | Unit |
|---|---|---|---|---|---|
| R1 | 13500 | 16667 | 1103 | 1800 | Ω |
| R2 | 10800 | 15385 | 1554 | 990 | Ω |
| $R_{TH}$ | 6000 | 8000 | 645 | 639 | Ω |
| $V_{TH}$ | 0.80 | 1.20 | 1.75 | 1.77 | V |

**Notes**
8. Tested initially and after any design or process changes that may affect these parameters.
9. Full-device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min)} \geq 100\ \mu s$ or stable at $V_{CC(min)} \geq 100\ \mu s$.

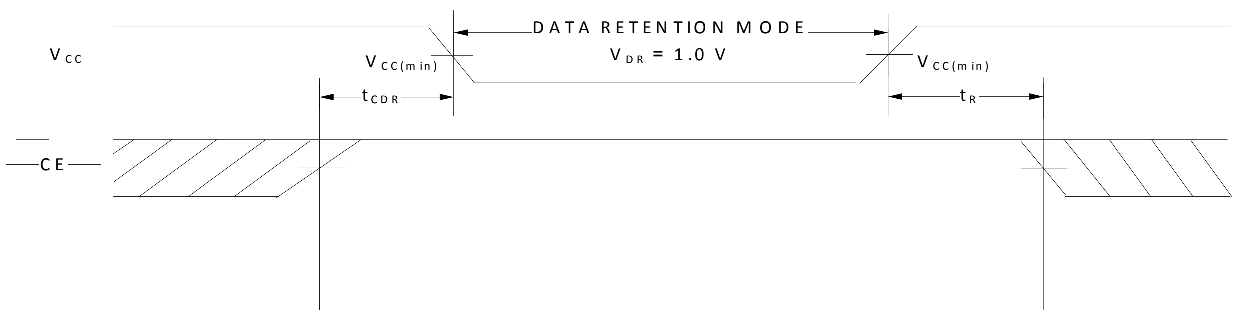
## Data Retention Characteristics

Over the Operating range

| Parameter | Description | Conditions | Min | Typ [10] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for data retention | | 1 | – | – | V |
| $I_{CCDR}$[11, 12] | Data retention current | $V_{CC}$ = 1.2 V,<br>$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V,<br>$V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V | – | – | 13 | µA |
| $t_{CDR}$[13, 14] | Chip deselect to data retention time | | 0 | – | – | ns |
| $t_R$[14] | Operation recovery time | | 45/55 | – | – | ns |

## Data Retention Waveform

**Figure 3. Data Retention Waveform**




**Notes**

10. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = 1.8 V (for $V_{CC}$ range of 1.65 V–2.2 V), $V_{CC}$ = 3 V (for $V_{CC}$ range of 2.2 V–3.6 V), and $V_{CC}$ = 5 V (for $V_{CC}$ range of 4.5 V–5.5 V), $T_A$ = 25 °C.
11. Chip enables $\overline{CE}$ must be tied to CMOS levels to meet the $I_{SB1}$ / $I_{SB2}$ / $I_{CCDR}$ spec. Other inputs can be left floating.
12. $I_{CCDR}$ is guaranteed only after device is first powered up to $V_{CC(min)}$ and then brought down to $V_{DR}$.
13. These parameters are guaranteed by design.
14. Full-device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

## AC Switching Characteristics

| Parameter [15, 16] | Description | 45 ns | | 55 ns | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| **Read Cycle** | | | | | | |
| $t_{RC}$ | Read cycle time | 45 | – | 55 | – | ns |
| $t_{AA}$ | Address to data valid | – | 45 | – | 55 | ns |
| $t_{OHA}$ | Data hold from address change | 10 | – | 10 | – | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to data valid | – | 45 | – | 55 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to data valid | – | 22 | – | 25 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low impedance[17] | 5 | – | 5 | – | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to HI-Z[17, 18] | – | 18 | – | 18 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to Low impedance[17] | 10 | – | 10 | – | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to HI-Z[17, 18] | – | 18 | – | 18 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to power-up | 0 | – | 0 | – | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to power-down | – | 45 | – | 55 | ns |
| **Write Cycle** [19, 20] | | | | | | |
| $t_{WC}$ | Write cycle time | 45 | – | 55 | – | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to write end | 35 | – | 45 | – | ns |
| $t_{AW}$ | Address setup to write end | 35 | – | 45 | – | ns |
| $t_{HA}$ | Address hold from write end | 0 | – | 0 | – | ns |
| $t_{SA}$ | Address setup to write start | 0 | – | 0 | – | ns |
| $t_{PWE}$ | $\overline{WE}$ pulse width | 35 | – | 40 | – | ns |
| $t_{SD}$ | Data setup to write end | 25 | – | 25 | – | ns |
| $t_{HD}$ | Data hold from write end | 0 | – | 0 | – | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to HI-Z[17, 18] | – | 18 | – | 20 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low impedance[17] | 10 | – | 10 | – | ns |

**Notes**

15. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to $V_{CC}$ (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
16. These parameters are guaranteed by design.
17. At any temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any device.
18. $t_{HZOE}$, $t_{HZCE}$ and $t_{HZWE}$ transitions are measured when the outputs enter a high-impedance state.
19. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$.All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
20. The minimum pulse width in Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of $t_{SD}$ and $t_{HZWE}$.

## Switching Waveforms

**Figure 4. Read Cycle No. 1 (Address Transition Controlled)** [21, 22]

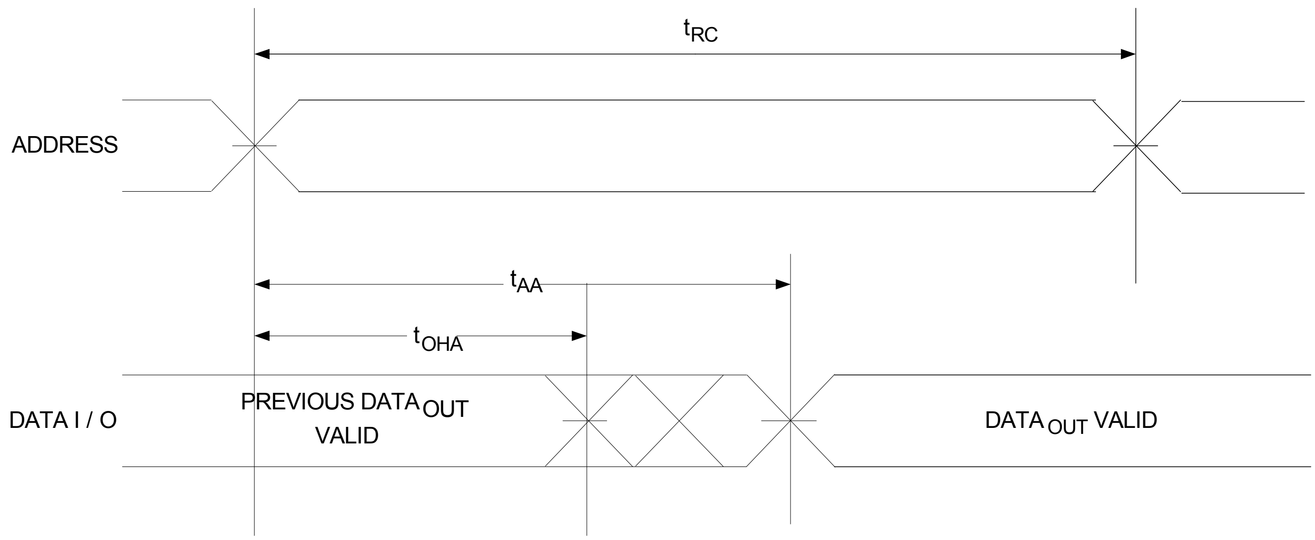
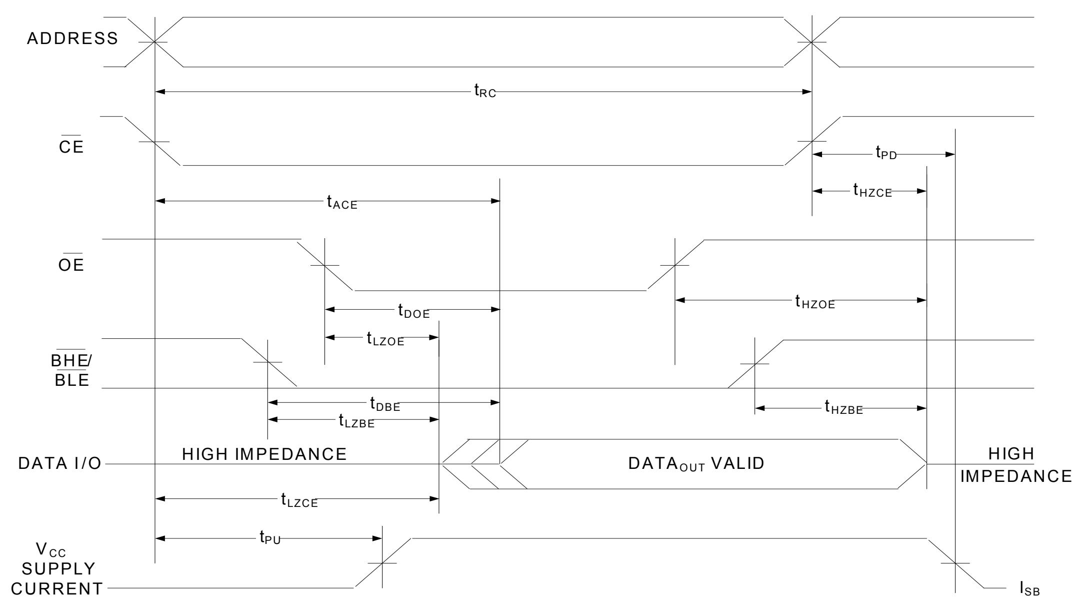



**Figure 5. Read Cycle No. 2 (OE Controlled)** [22, 23]

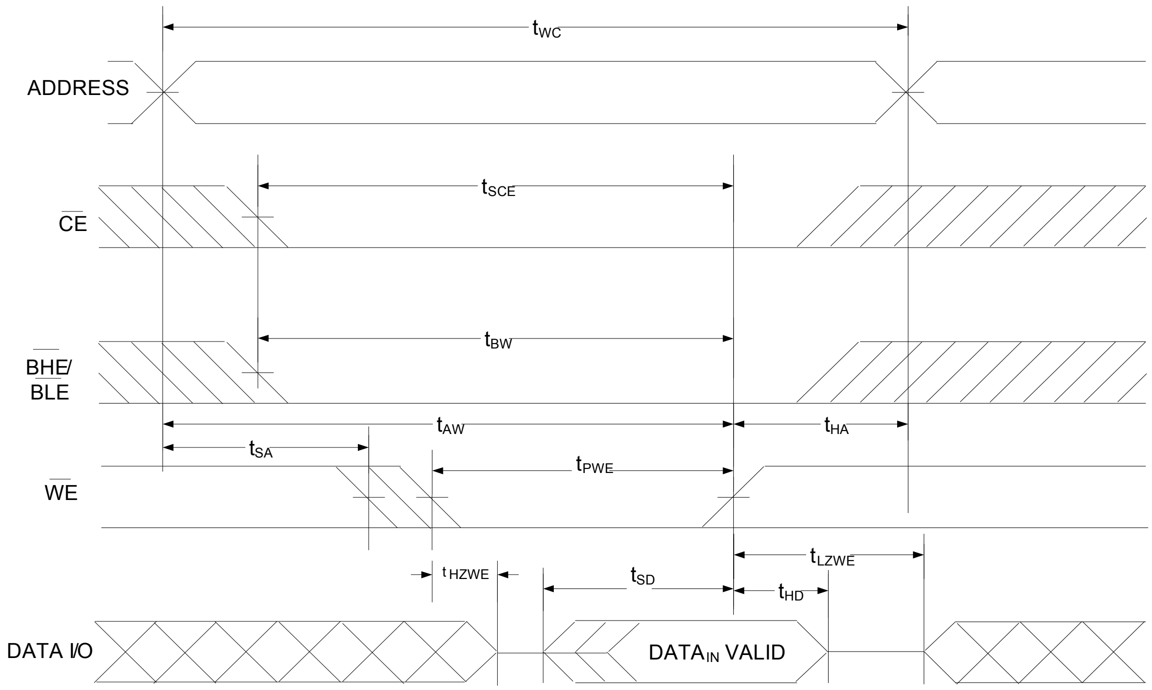



**Notes**

21. The device is continuously selected. $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$.
22. $\overline{WE}$ is HIGH for Read cycle.
23. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

## Switching Waveforms (continued)

**Figure 6. Write Cycle No. 1 (WE Controlled)** [24, 25, 26]




**Notes**

24. WE is HIGH for Read cycle.
25. The internal write time of the memory is defined by the overlap of WE = $V_{IL}$, CE = $V_{IL}$, All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
26. Data I/O is in a HI-Z state if CE = $V_{IH}$, or OE = $V_{IH}$.

## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 2 ($\overline{CE}$ Controlled) [27, 28]**

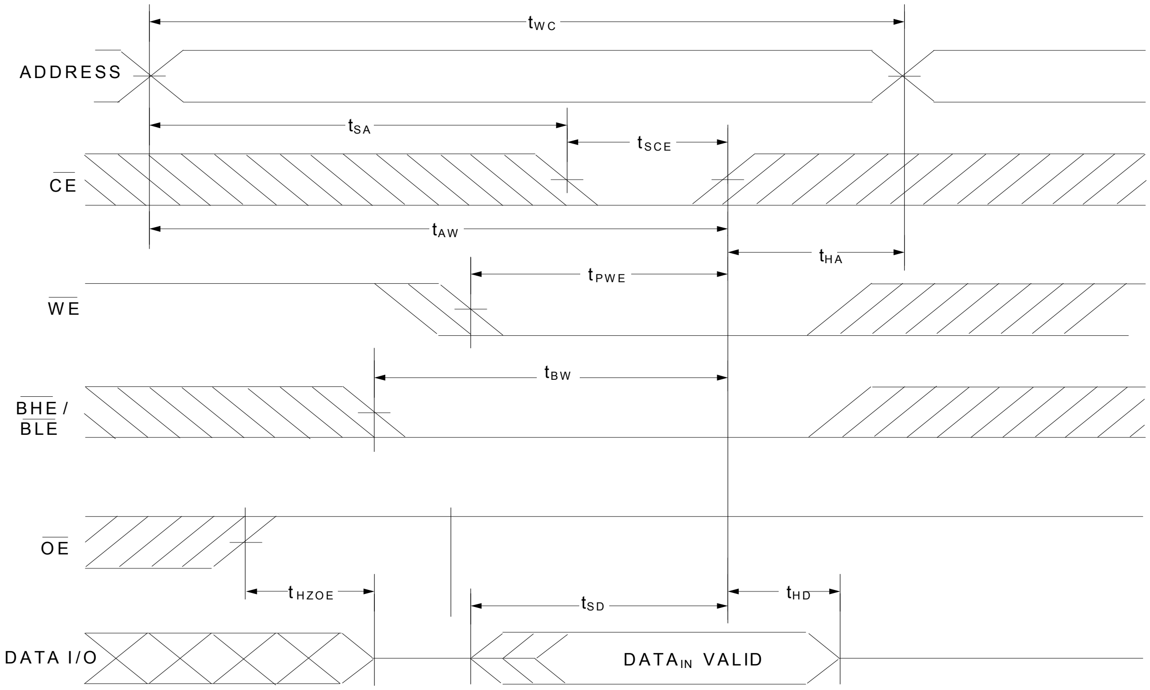
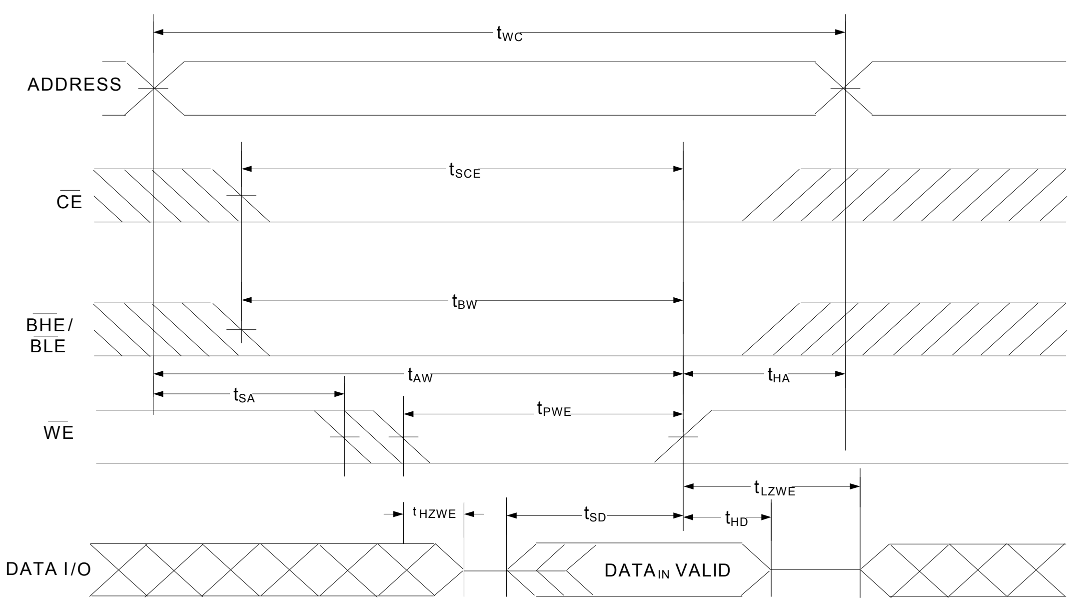



**Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [27, 28, 29]**




**Notes**

27. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = $V_{IL}$, $\overline{CE}$ = $V_{IL}$, All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
28. Data I/O is in HI-Z state if $\overline{CE}$ = $V_{IH}$, or $\overline{OE}$ = $V_{IH}$
29. The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of $t_{HZWE}$ and $t_{SD}$.

## Truth Table – CY62148G

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | Inputs/Outputs | Mode | Power | Configuration |
|---|---|---|---|---|---|---|
| H | X[30] | X[30] | HI-Z | Deselect/Power-down | Standby ($I_{SB}$) | 512 K × 8 |
| L | H | L | Data Out ($I/O_0$–$I/O_7$) | Read | Active ($I_{CC}$) | 512 K × 8 |
| L | H | H | HI-Z | Output disabled | Active ($I_{CC}$) | 512 K × 8 |
| L | L | X[30] | Data In ($I/O_0$–$I/O_7$) | Write | Active ($I_{CC}$) | 512 K × 8 |

**Note**

30. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

| Speed (ns) | Voltage Range | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|---|
| 45 | 2.2 V–3.6 V | CY62148G30-45SXI | 51-85081 | 32-pin SOIC (450 Mils) | Industrial |
| | | CY62148G30-45SXIT | 51-85081 | 32-pin SOIC (450 Mils), Tape and Reel | |
| | | CY62148G30-45ZSXI | 51-85095 | 32-pin TSOP II | |
| | | CY62148G30-45ZSXIT | 51-85095 | 32-pin TSOP II, Tape and Reel | |
| | 4.5 V–5.5 V | CY62148G-45SXI | 51-85081 | 32-pin SOIC (450 Mils) | |
| | | CY62148G-45SXIT | 51-85081 | 32-pin SOIC (450 Mils), Tape and Reel | |
| | | CY62148G-45ZSXI | 51-85095 | 32-pin TSOP II | |
| | | CY62148G-45ZSXIT | 51-85095 | 32-pin TSOP II, Tape and Reel | |
| 55 | 1.65 V–2.2 V | CY62148G18-55ZSXI | 51-85095 | 32-pin TSOP II | |
| | | CY62148G18-55ZSXIT | 51-85095 | 32-pin TSOP II, Tape and Reel | |

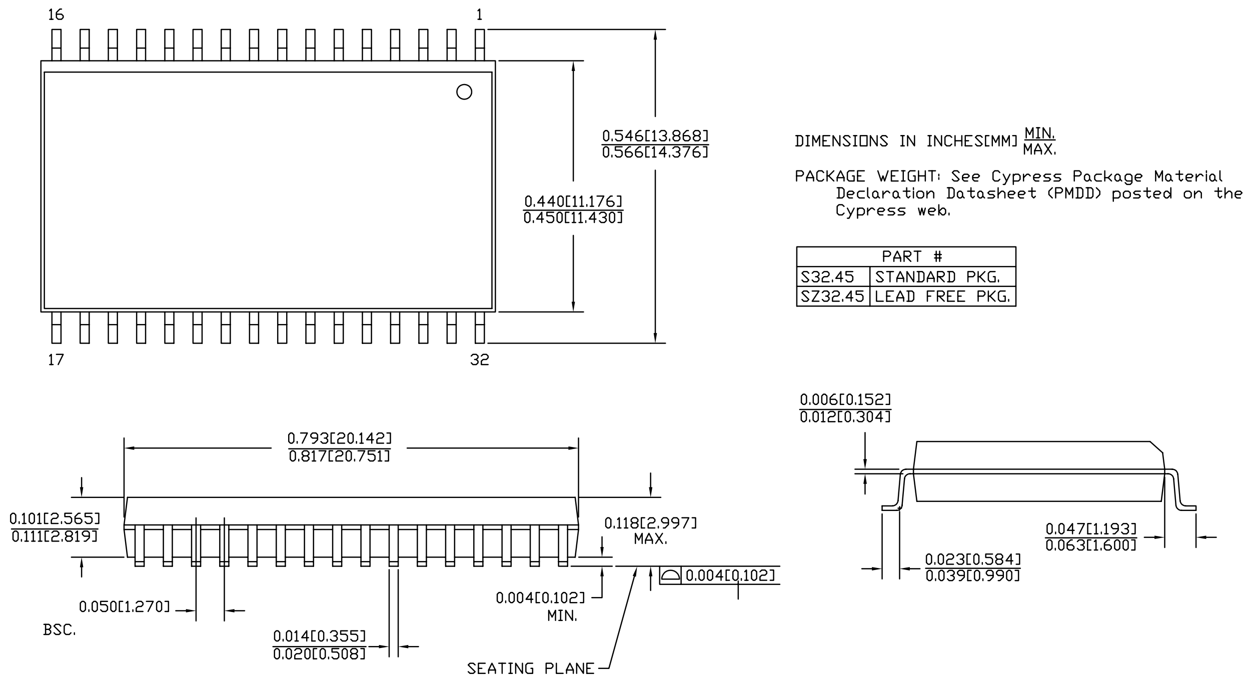
### Ordering Code Definitions

CY 621 4 8 G XX - XX XX X I X

- X: blank or T
  blank = Bulk; T = Tape and Reel
- Temperature Range: I = Industrial
- Pb-free
- Package Type: XX = S or ZS
  S = 32-pin SOIC
  ZS = 32-pin TSOP II
- Speed Grade: XX: 45 or 55
  45 = 45 ns; 55 = 55 ns
- Voltage Range: XX = 30 or 18 or no character
  30 = 3 V typ; 18 = 1.8 V typ; no character = 5 V typ
- Process Technology: G = 65 nm
- Bus Width: 8 = × 8
- Density: 4 = 4-Mbit
- Family Code: 621 = MoBL SRAM family
- Company ID: CY = Cypress

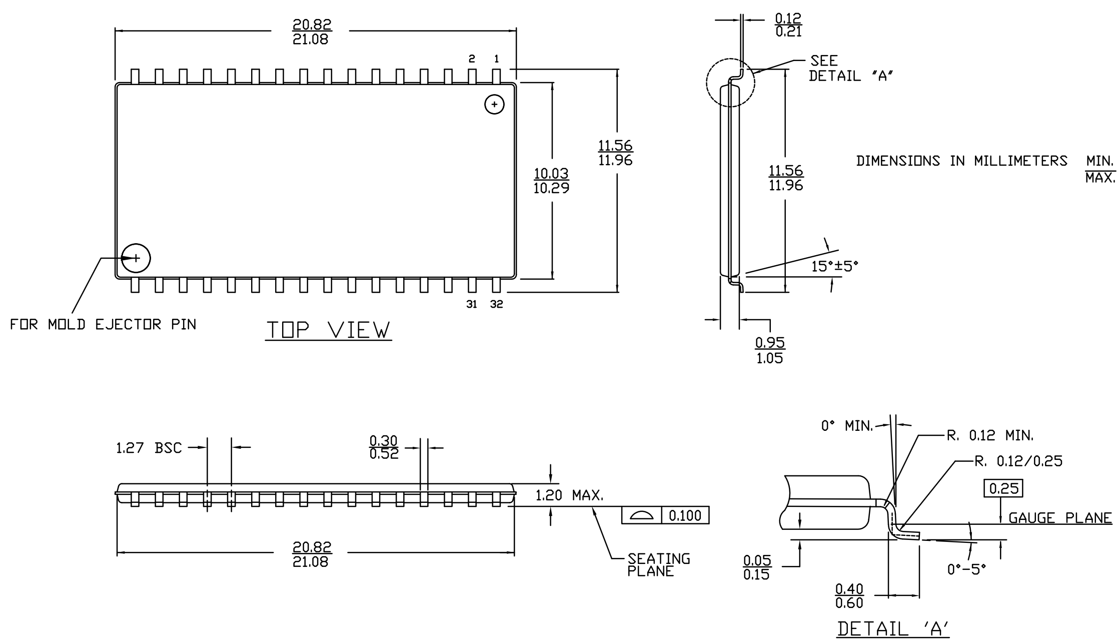
## Package Diagrams

**Figure 9. 32-pin SOIC (450 Mils) S32.45/SZ32.45 Package Outline, 51-85081**




51-85081 *E

**Figure 10. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32 Package Outline, 51-85095**




51-85095 *D

## Acronyms

| Acronym | Description |
|---|---|
| $\overline{CE}$ | chip enable |
| CMOS | complementary metal oxide semiconductor |
| I/O | input/output |
| $\overline{OE}$ | output enable |
| SRAM | static random access memory |
| TSOP | thin small outline package |
| VFBGA | very fine-pitch ball grid array |
| $\overline{WE}$ | write enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microamperes |
| µs | microseconds |
| mA | milliamperes |
| mm | millimeters |
| ns | nanoseconds |
| Ω | ohms |
| % | percent |
| pF | picofarads |
| V | volts |
| W | watts |

## Document History Page

| Document Title: CY62148G MoBL®, 4-Mbit (512K words × 8 bit) Static RAM with Error-Correcting Code (ECC)<br>Document Number: 001-95415 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *B | 5054381 | NILE | 12/17/2015 | Changed status from Preliminary to Final. |
| *C | 5082528 | NILE | 01/12/2016 | Updated Ordering Information:<br>Updated part numbers.<br>Completing Sunset Review. |
| *D | 5432526 | NILE | 09/10/2016 | Updated Maximum Ratings:<br>Updated Note 3 (Replaced “2 ns” with “20 ns”).<br>Updated DC Electrical Characteristics:<br>Changed minimum value of $V_{IH}$ parameter from 2.0 V to 1.8 V corresponding to Operating Range “2.2 V to 2.7 V”.<br>Updated Ordering Information:<br>Updated part numbers.<br>Updated to new template. |
| *E | 5979578 | AESATMP8 | 12/01/2017 | Updated logo and Copyright. |

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Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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