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January 2016

# Single-Channel: 6N135M, 6N136M, HCPL4503M Dual-Channel: HCPL2530M, HCPL2531M 8-Pin DIP High Speed Transistor Optocouplers

## Features

- High Speed – 1 MBit/s
- Dual-Channel: HCPL2530M, HCPL2531M
- CTR Guaranteed 0°C to 70°C
- No Base Connection for Improved Noise Immunity (HCPL4503M)
- Superior CMR of 15,000 V/μs Minimum (HCPL4503M)
- Safety and Regulatory Approvals
  - UL1577, 5,000 VAC<sub>RMS</sub> for 1 Minute
  - DIN EN/IEC60747-5-5

## Applications

- Line Receivers
- Pulse Transformer Replacement
- Output Interface to CMOS-LSTTL-TTL
- Wide-Bandwidth Analog Coupling

## Description

The 6N135M, 6N136M, HCPL4503M, HCPL2530M, and HCPL2531M optocouplers consist of an AlGaAs LED optically coupled to a high speed photodetector transistor for each channel.

A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base-collector capacitance of the input transistor.

The HCPL4503M has no internal connection to the phototransistor base for improved noise immunity. An internal noise shield provides superior common mode rejection of up to 50,000 V/μs.

## Related Resources

- [www.fairchildsemi.com/products/optoelectronics/](http://www.fairchildsemi.com/products/optoelectronics/)
- [www.fairchildsemi.com/pf/HC/HCPL0500.html](http://www.fairchildsemi.com/pf/HC/HCPL0500.html)
- [www.fairchildsemi.com/pf/FO/FODM452.html](http://www.fairchildsemi.com/pf/FO/FODM452.html)
- [www.fairchildsemi.com/pf/FO/FOD050L.html](http://www.fairchildsemi.com/pf/FO/FOD050L.html)

## Schematics



Pin 7 is not connected in the HCPL4503M

Figure 1. Schematics

## Package Outlines

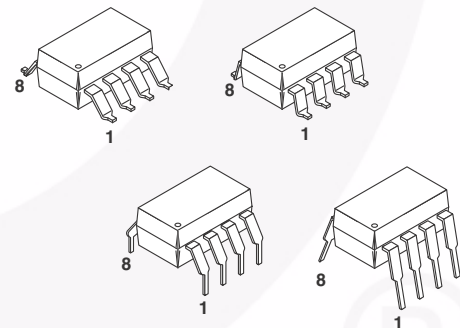


Figure 2. Package Outlines

Single-Channel: 6N135M, 6N136M, HCPL4503M  
Dual-Channel: HCPL2530M, HCPL2531M — 8-Pin DIP High Speed Transistor Optocouplers

## Safety and Insulation Ratings

As per DIN EN/IEC 60747-5-5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Parameter	Characteristics	
Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	< 150 V <sub>RMS</sub>	I-IV
	< 300 V <sub>RMS</sub>	I-IV
	< 450 V <sub>RMS</sub>	I-III
	< 600 V <sub>RMS</sub>	I-III
Climatic Classification	40/100/21	
Pollution Degree (DIN VDE 0110/1.89)	2	
Comparative Tracking Index	175	

Symbol	Parameter	Value	Unit
V <sub>PR</sub>	Input-to-Output Test Voltage, Method A, V <sub>IORM</sub> × 1.6 = V <sub>PR</sub> , Type and Sample Test with t <sub>m</sub> = 10 s, Partial Discharge < 5 pC	1,335	V <sub>peak</sub>
	Input-to-Output Test Voltage, Method B, V <sub>IORM</sub> × 1.875 = V <sub>PR</sub> , 100% Production Test with t <sub>m</sub> = 1 s, Partial Discharge < 5 pC	1,669	V <sub>peak</sub>
V <sub>IORM</sub>	Maximum Working Insulation Voltage	890	V <sub>peak</sub>
V <sub>IOTM</sub>	Highest Allowable Over-Voltage	6,000	V <sub>peak</sub>
	External Creepage	≥ 8.0	mm
	External Clearance	≥ 7.4	mm
	External Clearance (for Option TV, 0.4" Lead Spacing)	≥ 10.16	mm
DTI	Distance Through Insulation (Insulation Thickness)	≥ 0.5	mm
T <sub>S</sub>	Case Temperature <sup>(1)</sup>	150	°C
I <sub>S,INPUT</sub>	Input Current <sup>(1)</sup>	200	mA
P <sub>S,OUTPUT</sub>	Output Power (Duty Factor ≤ 2.7%) <sup>(1)</sup>	300	mW
R <sub>IO</sub>	Insulation Resistance at T <sub>S</sub> , V <sub>IO</sub> = 500 V <sup>(1)</sup>	> 10 <sup>9</sup>	Ω

**Note:**

1. Safety limit value - maximum values allowed in the event of a failure.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Test Conditions	Value	Unit
$T_{\text{STG}}$	Storage Temperature		-40 to +125	$^\circ\text{C}$
$T_{\text{OPR}}$	Operating Temperature		-40 to +100	$^\circ\text{C}$
$T_J$	Junction Temperature		-40 to +125	$^\circ\text{C}$
$T_{\text{SOL}}$	Lead Solder Temperature		260 for 10 sec	$^\circ\text{C}$
<b>EMITTER</b>				
$I_F$ (avg)	DC/Average Forward Input Current Each Channel <sup>(2)</sup>		25	mA
$I_F$ (pk)	Peak Forward Input Current Each Channel <sup>(3)</sup>	50% Duty Cycle, 1 ms P.W.	50	mA
$I_F$ (trans)	Peak Transient Input Current Each Channel	$\leq 1 \mu\text{s}$ P.W., 300 pps	1.0	A
$V_R$	Reverse Input Voltage Each Channel		5	V
$P_D$	Input Power Dissipation Each Channel <sup>(4)</sup>		45	mW
<b>DETECTOR</b>				
$I_O$ (avg)	Average Output Current Each Channel		8	mA
$I_O$ (pk)	Peak Output Current Each Channel		16	mA
$V_{\text{EBR}}$	Emitter-Base Reverse Voltage	6N135M and 6N136M	5	V
$V_{\text{CC}}$	Supply Voltage		-0.5 to 30	V
$V_O$	Output Voltage		-0.5 to 20	V
$I_B$	Base Current	6N135M and 6N136M	5	mA
$P_D$	Output Power Dissipation Each Channel <sup>(5)</sup>		100	mW

### Notes:

- Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $0.8 \text{ mA}/^\circ\text{C}$ .
- Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $1.6 \text{ mA}/^\circ\text{C}$ .
- Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $0.9 \text{ mW}/^\circ\text{C}$ .
- Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $2.0 \text{ mW}/^\circ\text{C}$ .

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_{\text{CC}}$	Supply Voltage	4.5	20.0	V
$T_A$	Ambient Operating Temperature	0	70	$^\circ\text{C}$
$I_{\text{FL}}$	Input Current, Low Level	0	250	$\mu\text{A}$
$I_{\text{FH}}$	Input Current, High Level <sup>(6)</sup>	6.3	20.0	mA

### Note:

- 6.3 mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0 mA or less.

## Electrical Characteristics

$V_{CC} = 5.0\text{ V}$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  unless otherwise specified.

### Individual Component Characteristics

Symbol	Parameter	Device	Test Conditions	Min.	Typ.	Max.	Unit
<b>EMITTER</b>							
$V_F$	Input Forward Voltage	All	$I_F = 16\text{ mA}$ , $T_A = 25^\circ\text{C}$		1.45	1.70	V
		All	$I_F = 16\text{ mA}$			1.80	
$B_{VR}$	Input Reverse Breakdown Voltage	All	$I_R = 10\ \mu\text{A}$	5	21		V
$\Delta V_F/\Delta T_A$	Temperature Coefficient of Forward Voltage	All	$I_F = 16\text{ mA}$		-1.7		mV/ $^\circ\text{C}$
<b>DETECTOR</b>							
$I_{OH}$	Logic High Output Current	All	$I_F = 0\text{ mA}$ , $V_O = V_{CC} = 5.5\text{ V}$ , $T_A = 25^\circ\text{C}$		0.0007	0.5	$\mu\text{A}$
		6N135M, 6N136M, HCPL4503M	$I_F = 0\text{ mA}$ , $V_O = V_{CC} = 15\text{ V}$ , $T_A = 25^\circ\text{C}$		0.0019	1	
		All	$I_F = 0\text{ mA}$ , $V_O = V_{CC} = 15\text{ V}$			50	
$I_{CCL}$	Logic Low Supply Current	6N135M, 6N136M, HCPL4503M	$I_F = 16\text{ mA}$ , $V_O = \text{Open}$ , $V_{CC} = 15\text{ V}$		163	200	$\mu\text{A}$
		HCPL2530M, HCPL2531M	$I_{F1} = I_{F2} = 16\text{ mA}$ , $V_O = \text{Open}$ , $V_{CC} = 15\text{ V}$			400	
$I_{CCH}$	Logic High Supply Current	6N135M, 6N136M, HCPL4503M	$I_F = 0\text{ mA}$ , $V_O = \text{Open}$ , $V_{CC} = 15\text{ V}$		0.0004	2	$\mu\text{A}$
		HCPL2530M, HCPL2531M	$I_F = 0\text{ mA}$ , $V_O = \text{Open}$ , $V_{CC} = 15\text{ V}$			4	

## Electrical Characteristics (continued)

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  unless otherwise specified.

### Transfer Characteristics

Symbol	Parameter	Device	Test Conditions	Min.	Typ.	Max.	Unit	
<b>COUPLED</b>								
CTR	Current Transfer Ratio <sup>(7)</sup>	6N135M, HCPL2530M	$I_F = 16\text{ mA}, V_O = 0.4\text{ V},$ $V_{CC} = 4.5\text{ V}, T_A = 25^\circ\text{C}$	7	38	50	%	
		6N136M, HCPL4503M, HCPL2531M		19	38	50	%	
		6N135M	$I_F = 16\text{ mA},$ $V_{CC} = 4.5\text{ V}$	$V_{OL} = 0.4\text{ V}$	5			%
		HCPL2530M		$V_{OL} = 0.5\text{ V}$				
		6N136M, HCPL4503M		$V_{OL} = 0.4\text{ V}$	15			%
		HCPL2531M		$V_{OL} = 0.5\text{ V}$				
$V_{OL}$	Logic LOW Output Voltage	6N135M	$I_F = 16\text{ mA}, I_O = 1.1\text{ mA},$ $V_{CC} = 4.5\text{ V}, T_A = 25^\circ\text{C}$		0.12	0.4	V	
		HCPL2530M				0.5		
		6N136M, HCPL4503M	$I_F = 16\text{ mA}, I_O = 3\text{ mA},$ $V_{CC} = 4.5\text{ V}, T_A = 25^\circ\text{C}$		0.20	0.4		
		HCPL2531M				0.5		
		6N135M, HCPL2530M	$I_F = 16\text{ mA}, I_O = 0.8\text{ mA},$ $V_{CC} = 4.5\text{ V}$		0.11	0.5		
		HCPL4503M, HCPL2531M	$I_F = 16\text{ mA}, I_O = 2.4\text{ mA},$ $V_{CC} = 4.5\text{ V}$		0.18	0.5		

**Note:**

7. Current Transfer Ratio is defined as a ratio of output collector current,  $I_O$ , to the forward LED input current,  $I_F$ , times 100%.

## Electrical Characteristics (continued)

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  unless otherwise specified.

### Switching Characteristics

Symbol	Parameter	Device	Test Conditions	Min.	Typ.	Max.	Unit	
$t_{PHL}$	Propagation Delay Time to Logic LOW	6N135M	$T_A = 25^\circ\text{C}$ , $R_L = 4.1\text{ k}\Omega$ , $I_F = 16\text{ mA}^{(8)}$ (Figure 15)		0.23	1.5	$\mu\text{s}$	
		HCPL2530M			0.25			
		6N136M, HCPL4503M	$T_A = 25^\circ\text{C}$ , $R_L = 1.9\text{ k}\Omega$ , $I_F = 16\text{ mA}^{(9)}$ (Figure 15)		0.25	0.8	$\mu\text{s}$	
		HCPL2531M			0.28			
		6N135M, HCPL2530M	$R_L = 4.1\text{ k}\Omega$ , $I_F = 16\text{ mA}^{(8)}$ (Figure 15)				2.0	$\mu\text{s}$
		6N136M, HCPL4503M, HCPL2531M	$R_L = 1.9\text{ k}\Omega$ , $I_F = 16\text{ mA}^{(9)}$ (Figure 15)				1.0	$\mu\text{s}$
$t_{PLH}$	Propagation Delay Time to Logic HIGH	6N135M	$T_A = 25^\circ\text{C}$ , $R_L = 4.1\text{ k}\Omega$ , $I_F = 16\text{ mA}^{(8)}$ (Figure 15)		0.45	1.5	$\mu\text{s}$	
		HCPL2530M			0.29			
		6N136M, HCPL4503M	$T_A = 25^\circ\text{C}$ , $R_L = 1.9\text{ k}\Omega$ , $I_F = 16\text{ mA}^{(9)}$ (Figure 15)		0.26	0.8	$\mu\text{s}$	
		HCPL2531M			0.18			
		6N135M, HCPL2530M	$R_L = 4.1\text{ k}\Omega$ , $I_F = 16\text{ mA}^{(8)}$ (Figure 15)				2.0	$\mu\text{s}$
		6N136M, HCPL4503M, HCPL2531M	$R_L = 1.9\text{ k}\Omega$ , $I_F = 16\text{ mA}^{(9)}$ (Figure 15)				1.0	$\mu\text{s}$
$ CM_H $	Common Mode Transient Immunity at Logic High	6N135M, HCPL2530M	$I_F = 0\text{ mA}$ , $V_{CM} = 10\text{ V}_{P-P}$ , $R_L = 4.1\text{ k}\Omega$ , $T_A = 25^\circ\text{C}^{(10)}$ (Figure 16)		10,000		$\text{V}/\mu\text{s}$	
		6N136M, HCPL2531M	$I_F = 0\text{ mA}$ , $V_{CM} = 10\text{ V}_{P-P}$ , $R_L = 1.9\text{ k}\Omega$ , $T_A = 25^\circ\text{C}^{(10)}$ (Figure 16)		10,000			
		HCPL4503M	$I_F = 0\text{ mA}$ , $V_{CM} = 1,500\text{ V}_{P-P}$ , $R_L = 4.1\text{ k}\Omega$ , $T_A = 25^\circ\text{C}^{(10)}$ (Figure 16)	15,000	50,000			
$ CM_L $	Common Mode Transient Immunity at Logic Low	6N135M, HCPL2530M	$I_F = 16\text{ mA}$ , $V_{CM} = 10\text{ V}_{P-P}$ , $R_L = 4.1\text{ k}\Omega$ , $T_A = 25^\circ\text{C}^{(10)}$ (Figure 16)		10,000		$\text{V}/\mu\text{s}$	
		6N136M, HCPL2531M	$I_F = 16\text{ mA}$ , $V_{CM} = 10\text{ V}_{P-P}$ , $R_L = 1.9\text{ k}\Omega^{(10)}$ (Figure 16)		10,000			
		HCPL4503M	$I_F = 0\text{ mA}$ , $V_{CM} = 1,500\text{ V}_{P-P}$ , $R_L = 4.1\text{ k}\Omega$ , $T_A = 25^\circ\text{C}^{(10)}$ (Figure 16)	15,000	50,000			

#### Notes:

8. The 4.1 k $\Omega$  load represents 1 LSTTL unit load of 0.36 mA and 6.1 k $\Omega$  pull-up resistor.
9. The 1.9 k $\Omega$  load represents 1 TTL unit load of 1.6 mA and 5.6 k $\Omega$  pull-up resistor.
10. Common mode transient immunity in logic high level is the maximum tolerable (positive)  $dV_{CM}/dt$  on the leading edge of the common mode pulse signal,  $V_{CM}$ , to assure that the output will remain in a logic high state (i.e.,  $V_O > 2.0\text{ V}$ ). Common mode transient immunity in logic low level is the maximum tolerable (negative)  $dV_{CM}/dt$  on the trailing edge of the common mode pulse signal,  $V_{CM}$ , to assure that the output will remain in a logic low state (i.e.,  $V_O < 0.8\text{ V}$ ).

**Isolation Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise specified.)

Symbol	Parameter	Device	Test Conditions	Min.	Typ.	Max.	Unit
$V_{ISO}$	Withstand Isolation Test Voltage	All	$RH \leq 50\%$ , $I_{I-O} \leq 10 \mu\text{A}$ $t = 1 \text{ minute}$ , $f = 50 \text{ Hz}^{(11)(13)}$	5,000			$\text{VAC}_{RMS}$
$R_{I-O}$	Resistance (Input to Output)	All	$V_{I-O} = 500 \text{ V}_{DC}^{(11)}$		$10^{11}$		$\Omega$
$C_{I-O}$	Capacitance (Input to Output)	All	$f = 1 \text{ MHz}$ , $V_{I-O} = 0 \text{ V}_{DC}^{(11)}$		1		pF
$I_{I-I}$	Input-Input Insulation Leakage Current	HCPL2530M, HCPL2531M	$RH \leq 45\%$ , $V_{I-I} = 500 \text{ V}_{DC}$ , $t = 5 \text{ s}^{(12)}$		< 1		nA
$R_{I-I}$	Input-Input Resistance	HCPL2530M, HCPL2531M	$V_{I-I} = 500 \text{ V}_{DC}^{(12)}$		$10^{12}$		$\Omega$
$C_{I-I}$	Input-Input Capacitance	HCPL2530M, HCPL2531M	$f = 1 \text{ MHz}^{(12)}$		0.2		pF

**Notes:**

11. Device is considered a two terminal device: pins 1, 2, 3 and 4 are shorted together and pins 5, 6, 7 and 8 are shorted together.
12. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
13. 5000  $V_{RMS}$  for 1 minute duration is equivalent to 6000  $V_{RMS}$  for 1 second duration.



## Typical Performance Curves

For single-channel devices; 6N135M, 6N136M, and HCPL4503M.

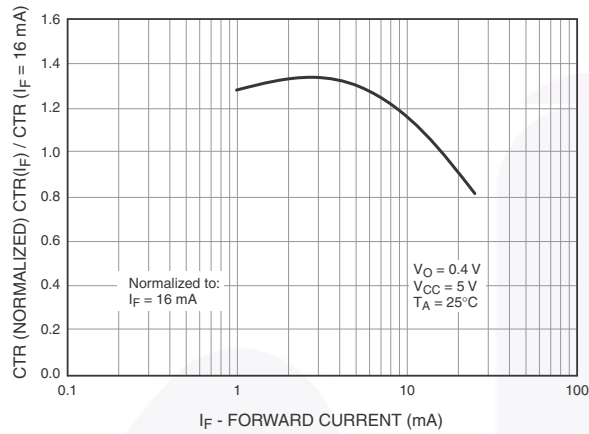


Figure 3. Normalized CTR vs. Forward Current

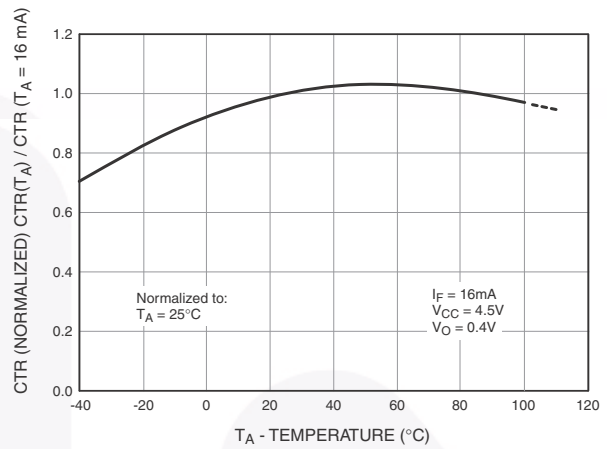


Figure 4. Normalized CTR vs. Temperature



Figure 5. Output Current vs. Output Voltage



Figure 6. Logic High Output Current vs. Temperature



Figure 7. Propagation Delay vs. Temperature



Figure 8. Propagation Delay vs. Load Resistance

## Typical Performance Curves (Continued)

For dual-channel devices; HCPL2530M and HCPL2531M.



Figure 9. Normalized CTR vs. Forward Current



Figure 10. Normalized CTR vs. Temperature

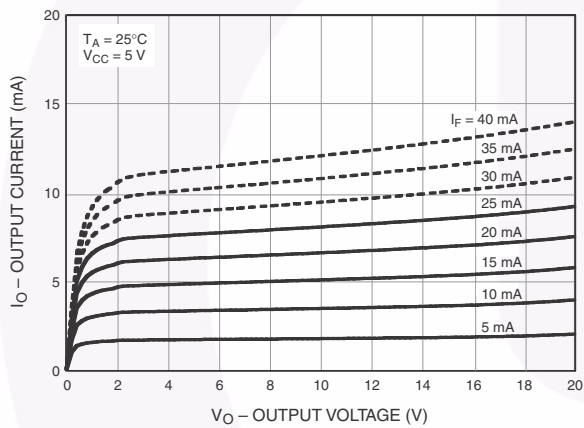


Figure 11. Output Current vs. Output Voltage



Figure 12. Logic High Output Current vs. Temperature

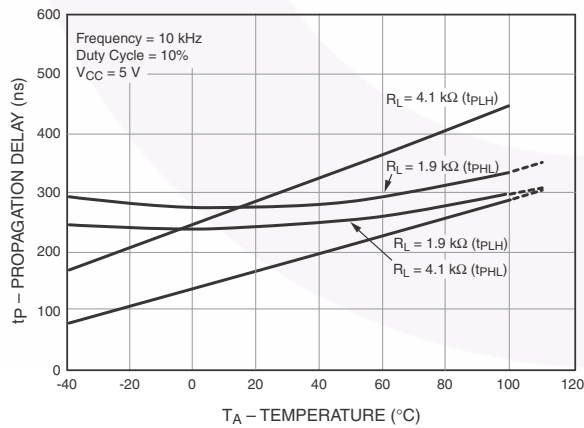


Figure 13. Propagation Delay vs. Temperature

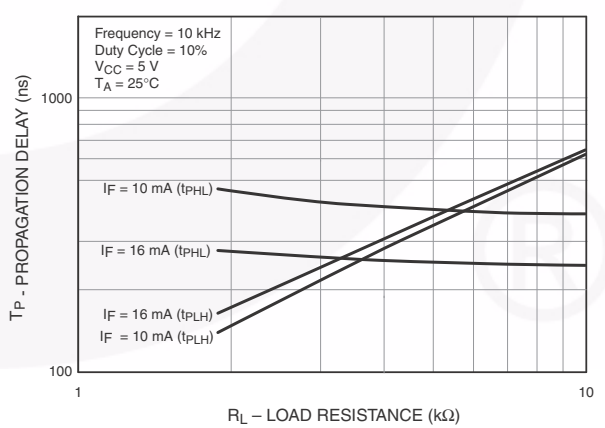
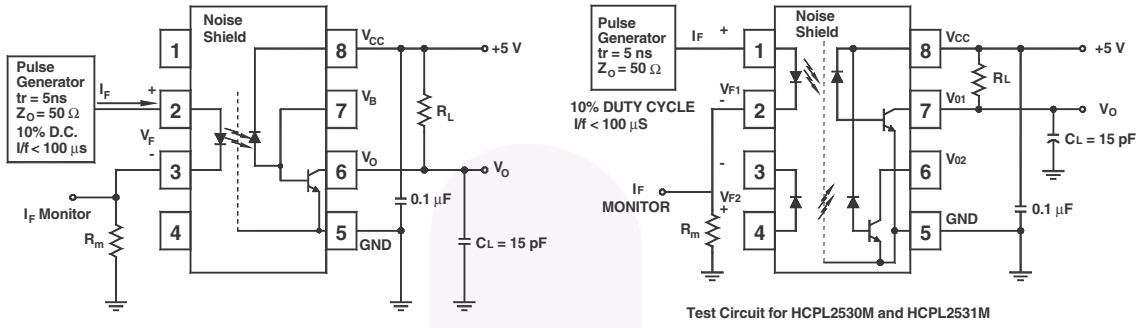


Figure 14. Propagation Delay vs. Load Resistance

### Test Circuits



Test Circuit for 6N135M, 6N136M, and HCPL4503M

Test Circuit for HCPL2530M and HCPL2531M

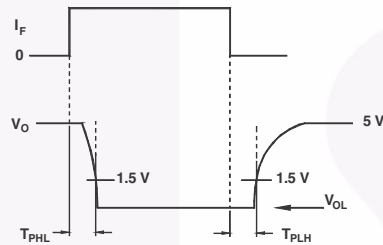


Figure 15. Switching Time Test Circuit



Test Circuit for 6N135M, 6N136M, and HCPL4503M

Test Circuit for HCPL2530M and HCPL2531M



Figure 16. Common Mode Immunity Test Circuit

## Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (T <sub>smín</sub> )	150°C
Temperature Max. (T <sub>smáx</sub> )	200°C
Time (t <sub>s</sub> ) from (T <sub>smín</sub> to T <sub>smáx</sub> )	60 to 120 s
Ramp-up Rate (t <sub>L</sub> to t <sub>p</sub> )	3°C/second maximum
Liquidous Temperature (T <sub>L</sub> )	217°C
Time (t <sub>L</sub> ) Maintained Above (T <sub>L</sub> )	60 to 150 s
Peak Body Package Temperature	260°C +0°C / -5°C
Time (t <sub>p</sub> ) within 5°C of 260°C	30 s
Ramp-down Rate (T <sub>p</sub> to T <sub>L</sub> )	6°C/s maximum
Time 25°C to Peak Temperature	8 minutes maximum

Figure 17. Reflow Profile

## Ordering Information

Part Number	Package	Packing Method
6N135M	DIP 8-Pin	Tube (50 units per tube)
6N135SM	SMT 8-Pin (Lead Bend)	Tube (50 units per tube)
6N135SDM	SMT 8-Pin (Lead Bend)	Tape and Reel (1,000 units per reel)
6N135VM	DIP 8-Pin, DIN EN/IEC 60747-5-5 Option	Tube (50 units per tube)
6N135SVM	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 Option	Tube (50 units per tube)
6N135SDVM	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 Option	Tape and Reel (1,000 units per reel)
6N135TVM	DIP 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-5 Option	Tube (50 units per tube)
6N135TSVM	SMT 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-5 Option	Tube (50 units per tube)
6N135TSR2VM	SMT 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-5 Option	Tape and Reel (1,000 units per reel)

### Note:

The product orderable part number system listed in this table also applies to the 6N136M, HCPL4503M, HCPL2530M, and HCPL2531M product families.

## Marking Information

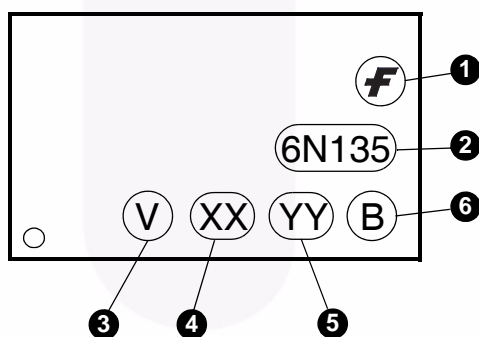
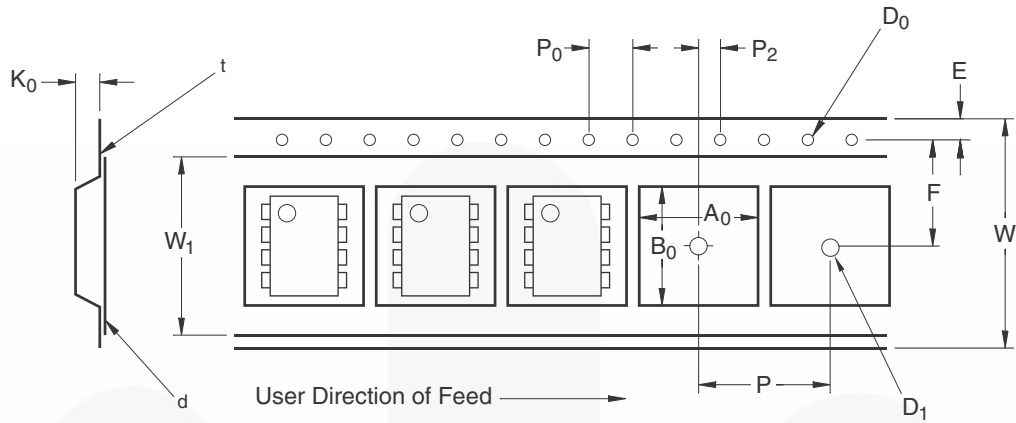


Figure 14. Top Mark

Definitions	
1	Fairchild Logo
2	Device Number
3	DIN EN/IEC60747-5-5 Option (only appears on component ordered with this option)
4	Two Digit Year Code, e.g., '15'
5	Two Digit Work Week Ranging from '01' to '53'
6	Assembly Package Code

## Carrier Tape Specifications (Option SD)

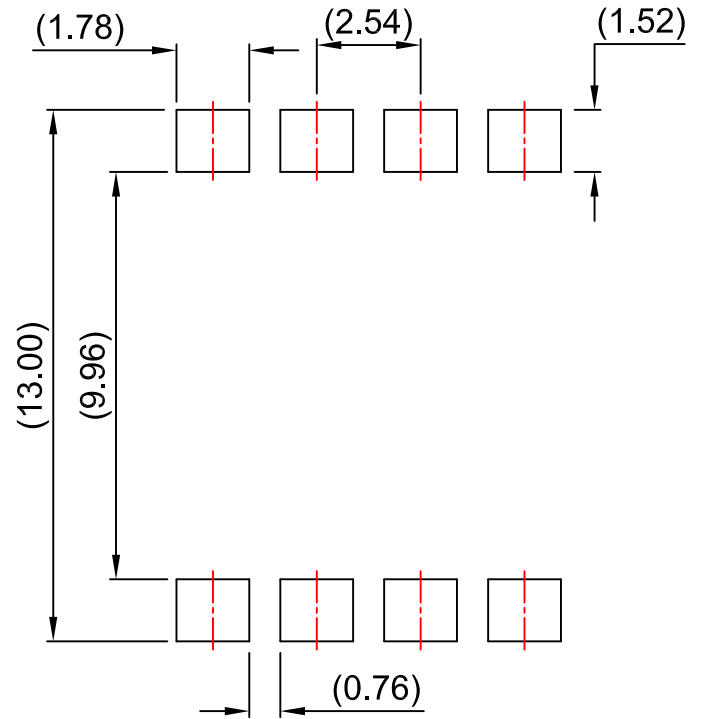


Symbol	Description	Dimension in mm
W	Tape Width	$16.0 \pm 0.3$
t	Tape Thickness	$0.30 \pm 0.05$
$P_0$	Sprocket Hole Pitch	$4.0 \pm 0.1$
$D_0$	Sprocket Hole Diameter	$1.55 \pm 0.05$
E	Sprocket Hole Location	$1.75 \pm 0.10$
F	Pocket Location	$7.5 \pm 0.1$
$P_2$		$2.0 \pm 0.1$
P	Pocket Pitch	$12.0 \pm 0.1$
$A_0$	Pocket Dimensions	$10.30 \pm 0.20$
$B_0$		$10.30 \pm 0.20$
$K_0$		$4.90 \pm 0.20$
$W_1$	Cover Tape Width	$13.2 \pm 0.2$
d	Cover Tape Thickness	0.1 Maximum
	Maximum Component Rotation or Tilt	$10^\circ$
R	Minimum Bending Radius	30

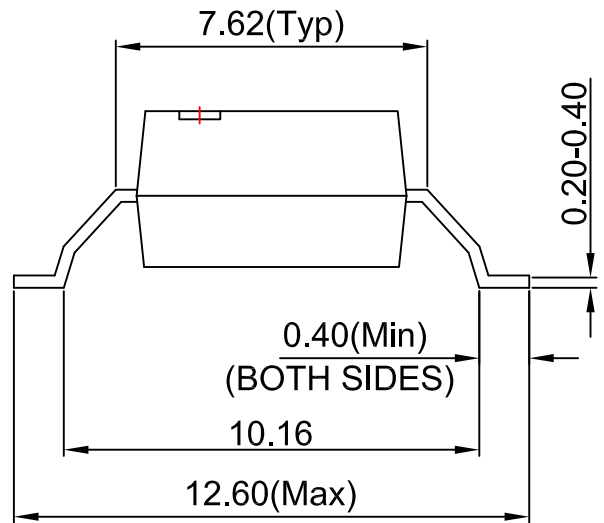
### Carrier Tape Specifications (Option TSR2)



Symbol	Description	Dimension in mm
W	Tape Width	24.0 ± 0.3
t	Tape Thickness	0.40 ± 0.1
P <sub>0</sub>	Sprocket Hole Pitch	4.0 ± 0.1
D <sub>0</sub>	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	11.5 ± 0.1
P <sub>2</sub>		2.0 ± 0.1
P	Pocket Pitch	16.0 ± 0.1
A <sub>0</sub>	Pocket Dimensions	12.80 ± 0.1
B <sub>0</sub>		10.35 ± 0.1
K <sub>0</sub>		5.7 ± 0.1
W <sub>1</sub>	Cover Tape Width	21.0 ± 0.1
d	Cover Tape Thickness	0.1 Maximum
	Maximum Component Rotation or Tilt	10°
R	Minimum Bending Radius	30



LAND PATTERN RECOMMENDATION

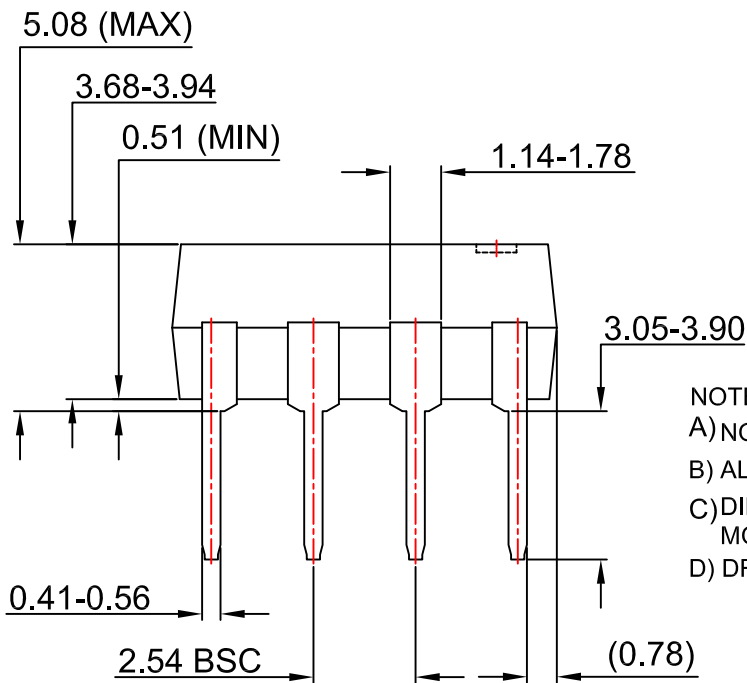


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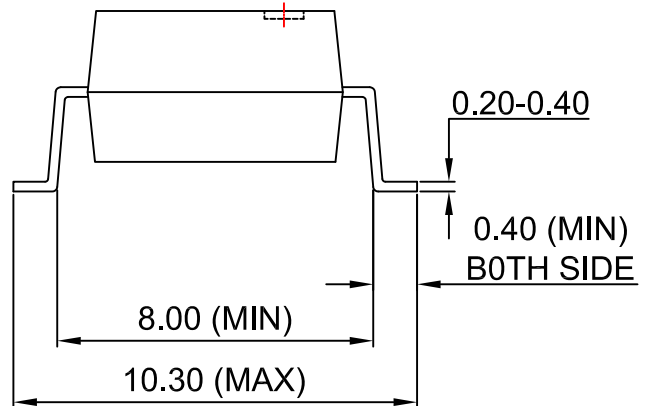


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LAND PATTERN RECOMMENDATION



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PIN 1

15.0° (MAX)

10.16 (TYP)

0.20-0.40



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