

PI6CFGL601B

6-Output Low Power PCIe Gen 1-2-3 Clock Generator

Features

- 25MHz crystal or reference clock input
- 100MHz low power HCSL or LVDS compatible outputs
- PCIe 3.0, 2.0 and 1.0 compliant
- Selectable spread spectrum of -0.5% and no spread
- Programmable output amplitude
- Cycle-to-cycle jitter (typ.) ~ 30ps
- Supply voltage of 3.3V+/-10%
- Output supply voltage of 1.8V
- Industrial ambient operating temperature
- Available in lead-free package: 32-TQFN

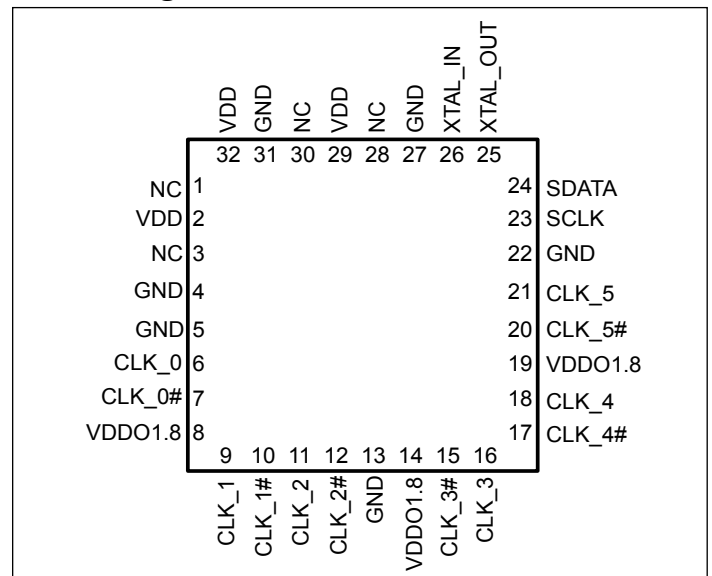
Application

- PCIe 3.0/2.0/1.0 clock generation

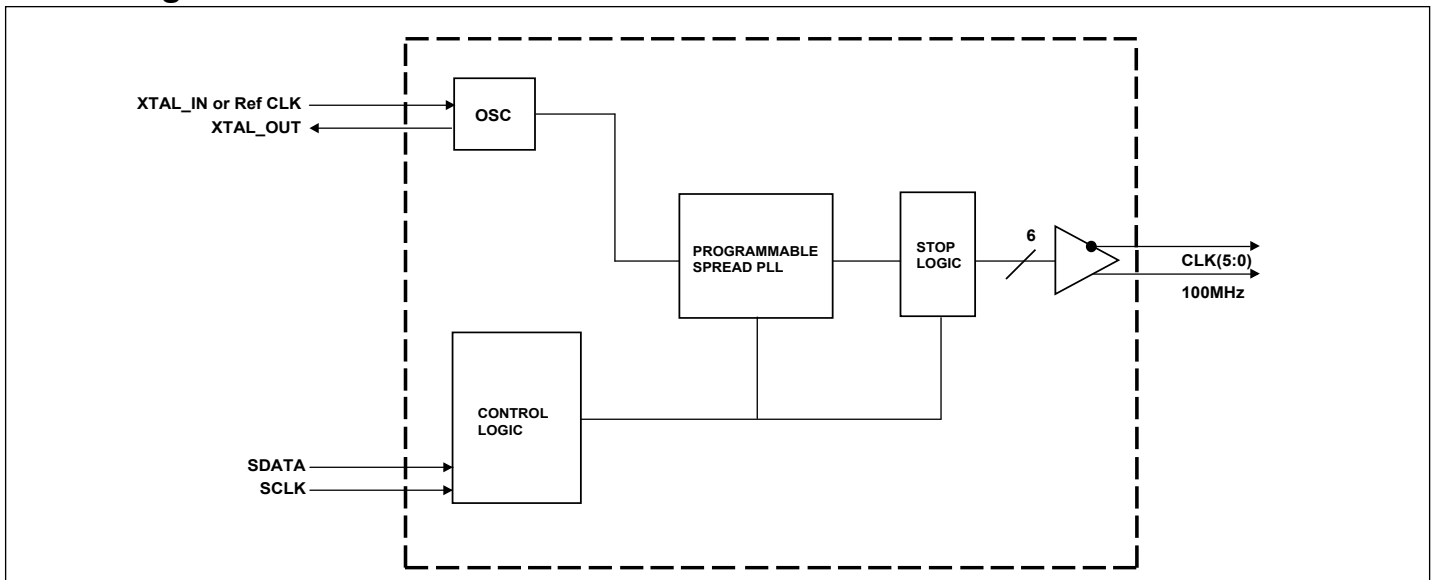
Description

The PI6CFGL601B is a 6-output low-power 100MHz clock synthesizer for PCIe Gen 1-2-3. It runs from a 25MHz XTAL, provides spread spectrum capability, and has an SMBus for software control of the device.

Pin Configuration



Block Diagram



Pin Description

Pin #	Pin Name	Type	Description
1	NC	N/A	No Connection.
2	VDD	Power	Power supply, nominal 3.3V
3	NC	N/A	No Connection.
4	GND	Power	Ground pin.
5	GND	Power	Ground pin.
6	CLK_0	Output	0.7V differential true clock output, LOW when output is disabled.
7	CLK_0#	Output	0.7V differential Complementary clock output, LOW when output is disabled.
8	VDDO1.8	Power	Power supply for outputs, nominally 1.8V, range 1.05 to 3.3V
9	CLK_1	Output	0.7V differential true clock output, LOW when output is disabled.
10	CLK_1#	Output	0.7V differential Complementary clock output, LOW when output is disabled.
11	CLK_2	Output	0.7V differential true clock output, LOW when output is disabled.
12	CLK_2#	Output	0.7V differential Complementary clock output, LOW when output is disabled.
13	GND	Power	Ground pin.
14	VDDO1.8	Power	Power supply for outputs, nominally 1.8V, range 1.05 to 3.3V
15	CLK_3#	Output	0.7V differential Complementary clock output, LOW when output is disabled.
16	CLK_3	Output	0.7V differential true clock output, LOW when output is disabled.
17	CLK_4#	Output	0.7V differential Complementary clock output, LOW when output is disabled.
18	CLK_4	Output	0.7V differential true clock output, LOW when output is disabled.
19	VDDO1.8	Power	Power supply for outputs, nominally 1.8V, range 1.05 to 3.3V
20	CLK_5#	Output	0.7V differential Complementary clock output, LOW when output is disabled.
21	CLK_5	Output	0.7V differential true clock output, LOW when output is disabled.
22	GND	Power	Ground pin.
23	SCLK	Input	Clock pin of SMBUS circuitry, 5V tolerant
24	SDATA	Input/output	Data pin of SMBUS circuitry, 5V tolerant
25	XTAL_OUT	Output	Crystal output, Nominally 25.00MHz.
26	XTAL_IN	Input	Crystal input or reference input clock, Nominally 25.00MHz.
27	GND	Power	Ground pin.
28	NC	N/A	No Connection.
29	VDD	Power	Power supply, nominal 3.3V
30	NC	N/A	No Connection.
31	GND	Power	Ground pin.
32	VDD	Power	Power supply, nominal 3.3V

Serial Data Interface (SMBus)

This part is a slave only device that supports blocks read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer by issuing STOP.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	0	0	1	0/1

Data Protocol

(Write)

1 bit	8 bits	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	Slave Addr: D2	Ack	Register offset	Ack	Byte Count=N	Ack	Data Byte 0	Ack	...	Data Byte N-1	Ack	Stop bit

(Read)

1 bit	8 bits	1	8 bits	1	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	Slave Addr: D2	Ack	Register offset	Ack	Repeat start	Slave Addr: D3	Ack	Byte Count=N	Ack	Data Byte 0	Ack	...	Data Byte N-1	NOT Ack	Stop bit

Note:

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

SMBus Table: Device Control Register, READ/WRITE ADDRESS (D2/D3)

BYTE 0							
Bit	Pin#	Name	Control Function	Type	0	1	Default
7		Reserved					0
6		Reserved					0
5		Spread Enable		R/W	Off	-0.50%	1
4		Reserved					0
3		Reserved					0
2		Reserved					0
1		Reserved					0
0		Reserved					0

SMBus Table: Output Enable Register

BYTE 1							
Bit	Pin#	Name	Control Function	Type	0	1	Default
7		Reserved					0
6		CLK_0 OE	Output Enable	R/W	Disable	Enable	1
5		Reserved					0
4		Reserved					0
3		CLK_1 OE	Output Enable	R/W	Disable	Enable	1
2		Reserved					0
1		Reserved					0
0		Reserved					0

SMBus Table: Reserved Register

BYTE 2							
Bit	Pin#	Name	Control Function	Type	0	1	Default
7		Reserved					0
6		Reserved					0
5		Reserved					0
4		Reserved					0
3		Reserved					0
2		Reserved					0
1		Reserved					0
0		Reserved					0

SMBus Table: Output Enable Register

BYTE 3							
Bit	Pin#	Name	Control Function	Type	0	1	Default
7		CLK_5 OE	Output Enable	R/W	Disable	Enable	1
6		CLK_4 OE	Output Enable	R/W	Disable	Enable	1
5		Reserved					0
4		Reserved					0
3		Reserved					0
2		Reserved					0
1		Reserved					0
0		Reserved					0

SMBus Table: Reserved Register

BYTE 4							
Bit	Pin#	Name	Control Function	Type	0	1	Default
7		Reserved					0
6		Reserved					0
5		Reserved					0
4		Reserved					0
3		Reserved					0
2		Reserved					0
1		Reserved					0
0		Reserved					0

SMBus Table: Output amplitude adjustment

BYTE 5							
Bit	Pin#	Name	Control Function	Type	0	1	Default
7		Reserved					0
6		Reserved					0
5		Reserved					0
4		Reserved					0
3		Reserved					0
2		Reserved					0
1		CLK_0/1/2/3/4/5 AMP	Amplitude adjustment	R/W	00=700mV 01=800mV		0
0	R/W			10=900mV 11=1000mV		1	

SMBus Table: Reserved Register

BYTE 6							
Bit	Pin#	Name	Control Function	Type	0	1	Default
7		Reserved					0
6		Reserved					0
5		Reserved					0
4		Reserved					0
3		Reserved					0
2		Reserved					0
1		Reserved					0
0		Reserved					0

SMBus Table: Vendor & Revision ID Register

BYTE 7							
Bit	Pin#	Name	Control Function	Type	0	1	Default
7		RID3	REVISION ID	R			0
6		RID2		R			0
5		RID1		R			0
4		RID0		R			0
3		VID3	VENDOR ID	R			0
2		VID2		R			0
1		VID1		R			0
0		VID0		R			0

SMBus Table: Reserved Register

BYTE 8							
Bit	Pin#	Name	Control Function	Type	0	1	Default
7		Reserved					0
6		Reserved					0
5		Reserved					0
4		Reserved					0
3		Reserved					1
2		Reserved					1
1		Reserved					1
0		Reserved					1

SMBus Table: Output Enable Register

BYTE 9							
Bit	Pin#	Name	Control Function	Type	0	1	Default
7		Reserved					0
6		CLK_3 OE	Output Enable	R/W	Disable	Enable	1
5		CLK_2 OE	Output Enable	R/W	Disable	Enable	1
4		Reserved					0
3		Reserved					0
2		Reserved					0
1		Reserved					0
0		Reserved					0

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential.....	4.6V
All Inputs and Output.....	-0.5V to V _{DD} +0.5V
Ambient Operating Temperature.....	-40°C to +85°C
Storage Temperature.....	-65°C to +150°C
Junction Temperature	125°C
Soldering Temperature.....	260°C
ESD Protection (Input)	2000V (HBM)

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics—Current Consumption

T_A = -40~85°C; Supply Voltage VDD = 3.3 V +/-10%; VDDO = 1.8V +/-10%, See Test Loads for loading conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
I _{DD3,3}	Operating Supply Current ¹	VDD, All outputs active @100MHz		50	65	mA

Notes:

1. Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics—Input/Supply/Common Output Parameters

T_A = -40~85°C; Supply Voltage VDD = 3.3 V +/-10%; VDDO = 1.8V +/-10%

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V _{DD}	Supply Voltage ¹	Supply voltage for core, analog	3.0	3.3	3.6	V
V _{DDO}	Supply Voltage ¹	Supply voltage outputs	1.65	1.8	2.0	V
V _{IH}	Input High Voltage ¹	Single-ended inputs, except SMBus	0.65 V _{DD}		V _{DD} +0.3	V
V _{IL}	Input Low Voltage ¹	Single-ended inputs, except SMBus	-0.3		0.35 V _{DD}	V
V _{OH}	Output High Voltage ¹	Single-ended outputs, except SMBus. I _{OH} = -2mA	V _{DD} -0.45			V
V _{OL}	Output Low Voltage ¹	Single-ended outputs, except SMBus. I _{OL} = -2mA			0.45	V
I _{IN}	Input Current ¹	Single-ended inputs, V _{IN} = GND, V _{IN} = VDD (exclude XTAL_IN pin)	-5		5	uA
I _{INP}		Single-ended inputs V _{IN} = 0 V; Inputs with internal pull-up resistors V _{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA
T _{ind}	Ambient Operating Temperature ¹	Industrial range	-40		85	°C
F _{in}	Input Frequency ¹	XTAL_IN		25.000		MHz
L _{pin}	Pin Inductance ¹				7	nH

Electrical Characteristics–Input/Supply/Common Output Parameters Cont.

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
C_{IN}	Capacitance ¹	Logic Inputs	1.5		5	pF
C_{INXTAL}		Crystal inputs			6	pF
C_{OUT}		Output pin capacitance			6	pF
T_{STAB}	Clk Stabilization ^{1,2}	From V_{DD} Power-Up and after input clock stabilization to 1st clock			1.8	ms
f_{MODIN}	SS Modulation Frequency ¹	Allowable Frequency (Triangular Modulation)	30	31.500	33	kHz
t_F	Tfall ^{1,2}	Fall time of control inputs			5	ns
t_R	Trise ^{1,2}	Rise time of control inputs			5	ns
V_{ILSMB}	SMBus Input Low Voltage ¹				0.8	V
V_{IHSMB}	SMBus Input High Voltage ¹		2.1		V_{DDSMB}	V
V_{OLSMB}	SMBus Output Low Voltage ¹	@ I_{PULLUP}			0.4	V
I_{PULLUP}	SMBus Sink Current ¹	@ V_{OL}	4			mA
V_{DDSMB}	Nominal Bus Voltage ¹	3V to 5V +/- 10%	2.7		5.5	V
t_{RSMB}	SCLK/SDATA Rise Time ¹	(Max $V_{IL} - 0.15$) to (Min $V_{IH} + 0.15$)			1000	ns
t_{FSMB}	SCLK/SDATA Fall Time ¹	(Min $V_{IH} + 0.15$) to (Max $V_{IL} - 0.15$)			300	ns
f_{MAXSMB}	SMBus Operating Frequency ¹	Delay from assertion of first output enable register to first clock Maximum SMBus operating frequency			100	kHz

Notes:

1. Guaranteed by design and characterization, not 100% tested in production.
2. Control input must be monotonic from 20% to 80% of input swing.

Electrical Characteristics–CLK 0.7V Low Power Differential Outputs

 $T_A = -40 \sim 85^\circ\text{C}$; Supply Voltage VDD = 3.3 V +/-10%; VDDO = 1.8V +/-10%, See Test Loads for loading conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
Trf	Slew rate ^{1,2,3}	Scope averaging on	1		4	V/ns
ΔTrf	Slew rate matching ^{1,2,4}	Slew rate matching, Scope averaging on			20	%
VHigh	Voltage High ¹	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660		850	mV
VLow	Voltage Low ¹		-150		150	
Vmax	Max Voltage ¹	Measurement on single ended signal using absolute value. (Scope averaging off)			1150	mV
Vmin	Min Voltage ¹		-300			
Vswing	Vswing ^{1,2}	Scope averaging off	300			mV
Vcross_abs	Crossing Voltage (abs) ^{1,5}	Scope averaging off	300		550	mV
$\Delta\text{-Vcross}$	Crossing Voltage (var) ^{1,6}	Scope averaging off			140	mV
t_{DC}	Duty Cycle ¹	Measured differentially, PLL Mode	45		55	%
tskew	Skew, Output to Output ¹	VT = 50%			50	ps
$t_{\text{JCYC-CYC}}$	Jitter, Cycle to cycle ^{1,2}	PLL mode			50	ps

- Notes:**
1. Guaranteed by design and characterization, not 100% tested in production. CL = 2pF with RS = 33Ω for Zo = 50Ω (100Ω differential trace impedance).
 2. Measured from differential waveform.
 3. Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.
 4. Matching applies to rising edge rate of Clock / falling edge rate of Clock#. It is measured in a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations.
 5. Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).
 6. The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than V_cross_abs.

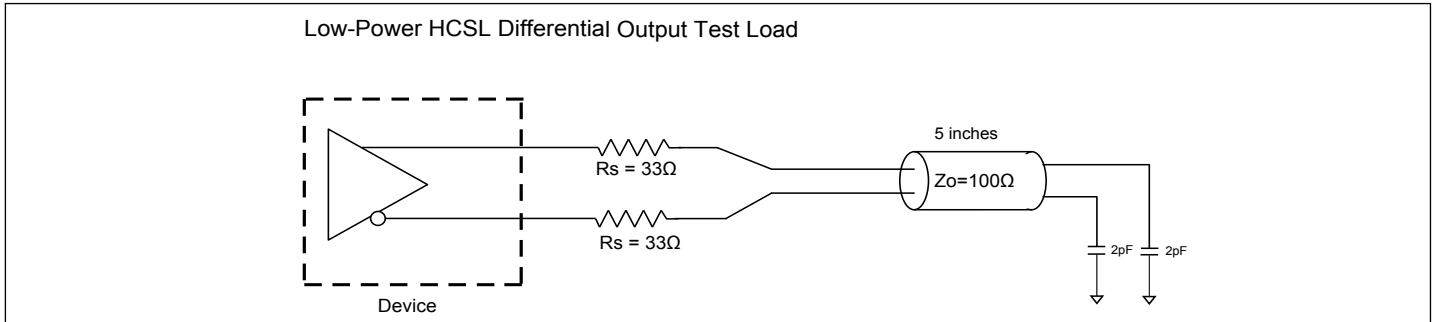
Electrical Characteristics–Phase Jitter Parameters

 $T_A = -40 \sim 85^\circ\text{C}$; Supply Voltage VDD = 3.3 V +/-10%; VDDO = 1.8V +/-10%, See Test Loads for Loading Conditions

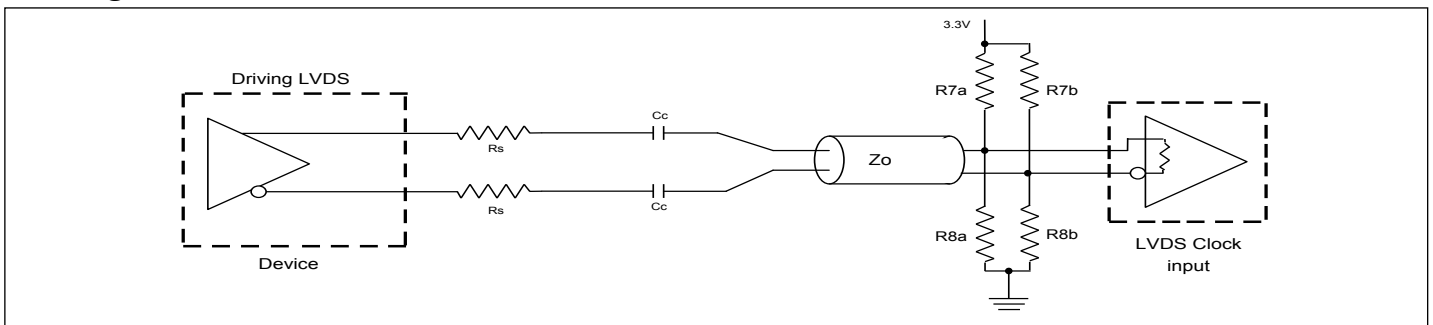
Symbol	Parameters	Condition	Min.	Typ.	INDUSTRY LIMIT	Units
$t_{\text{jphPCIeG1}}$	Phase Jitter, PCI Express ^{1,2,3,5}	PCIe Gen 1		27	86	ps (p-p)
$t_{\text{jphPCIeG2}}$	Phase Jitter, PCI Express ^{1,2,5}	PCIe Gen 2 Low Band 10kHz < f < 1.5MHz		0.5	3	ps (rms)
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		2.1	3.1	ps (rms)
$t_{\text{jphPCIeG3}}$	Phase Jitter, PCI Express ^{1,2,4,5}	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.5	1	ps (rms)

- Notes:**
1. Guaranteed by design and characterization, not 100% tested in production.
 2. See <http://www.pcisig.com> for complete specs.
 3. Sample size of at least 100k cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.
 4. Calculated from Intel-supplied Clock Jitter Tool.
 5. Applies to all different outputs.

Test Loads



Driving LVDS



Driving LVDS inputs with the PI6CFGL601B

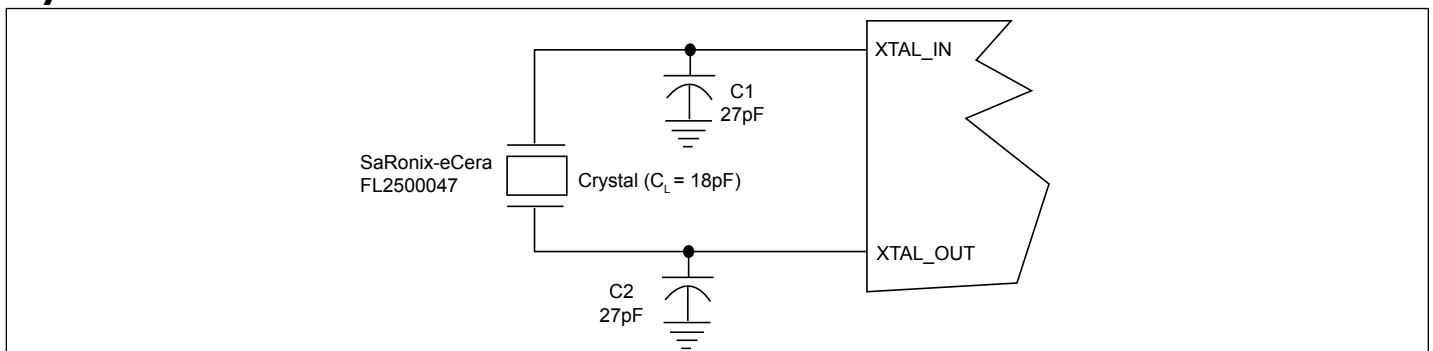
Component	Value	
	Receiver has termination	Receiver does not have termination
R7a, R7b	10K Ω	140 Ω
R8a, R8b	5.6K Ω	75 Ω
C_c	0.1 uF	0.1 uF
V_{cm}	1.2 V	1.2 V

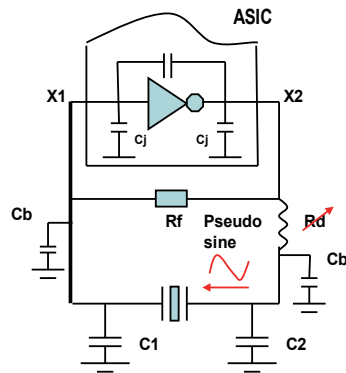
Application Notes

Crystal circuit connection

The following diagram shows crystal circuit connection with a parallel crystal. For the $C_L = 18\text{pF}$ crystal, it is suggested to use $C_1 = 27\text{pF}$, $C_2 = 27\text{pF}$. C_1 and C_2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

Crystal Oscillator Circuit





CL = crystal spec. loading cap.
 Cj = chip in/output cap. (3-5pF)
 Cb = PCB trace/via cap. (2-4pF)
 C1,2 = load cap. components
 Rd = drive level res. (100Ω)

Final choose/trim $C1=C2=2 * CL - (Cb + Cj)$ for the target +/--ppm
 Example: $C1=C2=2*(18pF) - (4pF+5pF)=27pF$

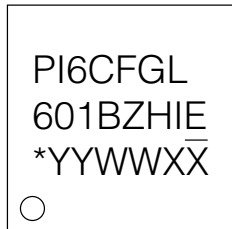
Recommended Crystal Specification

Pericom recommends:

- a) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm, <http://www.pericom.com/pdf/datasheets/se/FL.pdf>
- b) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

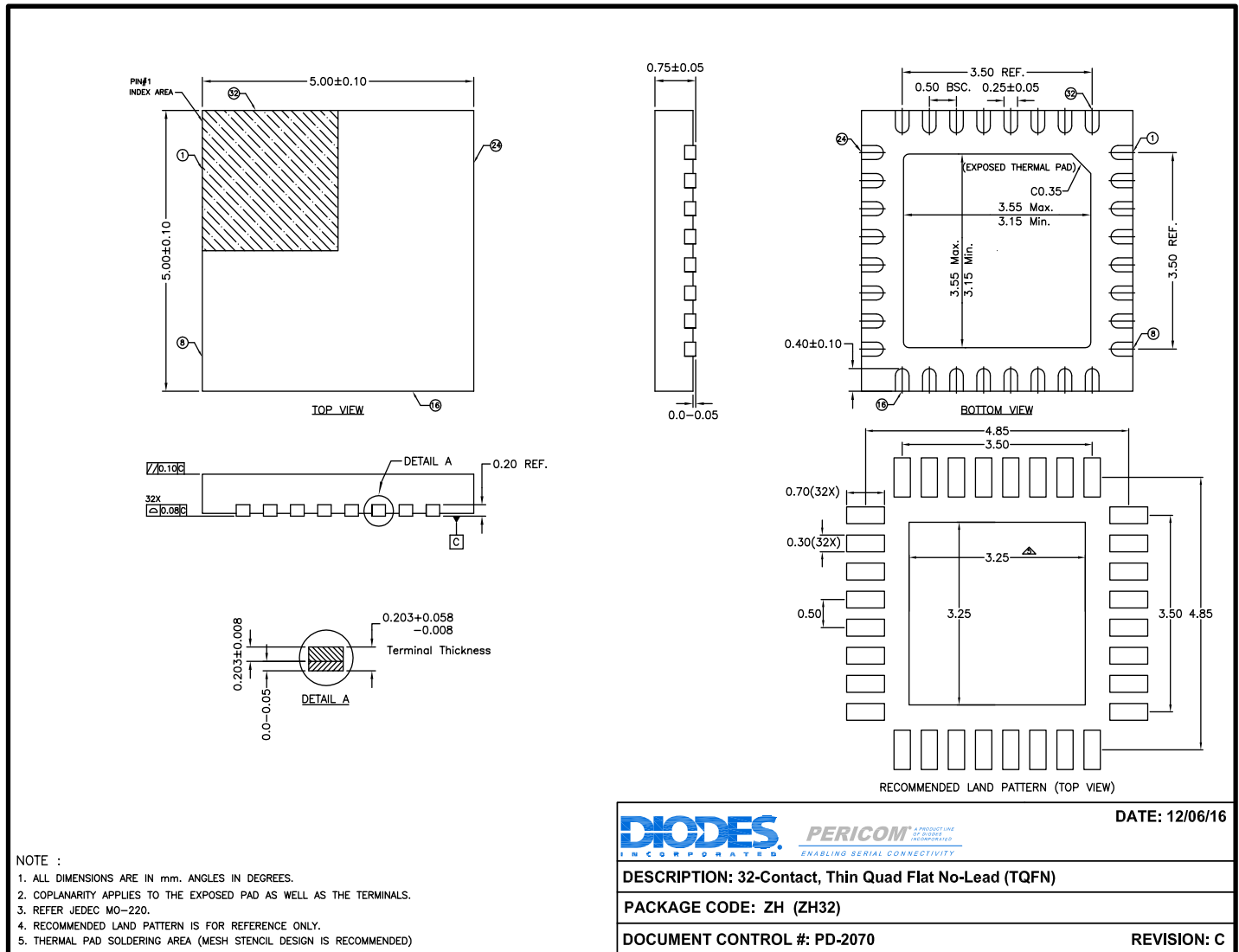
Part Marking

ZH package



*: Die Rev
 YY: Year
 WW: Workweek
 1st X: Assembly Code
 2nd X: Fab Code

Packaging Mechanical: 32-TQFN (ZH)



17-0570

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

Ordering Code	Package Code	Package Description
PI6CFGL601BZHIEX	ZH	32-contact, Thin Quad Flat No-Lead (TQFN)

Notes:

1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See <http://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
3. E = Pb-free and Green
4. X suffix = Tape/Reel

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- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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