

# 74HC112; 74HCT112

Dual JK flip-flop with set and reset; negative-edge trigger

Rev. 3 — 9 August 2016

Product data sheet

## 1. General description

The 74HC112; 74HCT112 is a dual negative-edge triggered JK flip-flop. It features individual J and K inputs, clock ( $\overline{nCP}$ ) set ( $\overline{nSD}$ ) and reset ( $\overline{nRD}$ ) inputs. It also has complementary  $\overline{nQ}$  and  $\overline{n\overline{Q}}$  outputs. The set and reset are asynchronous active LOW inputs and operate independently of the clock input. The J and K inputs control the state changes of the flip-flops as described in the mode select function table. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

## 2. Features and benefits

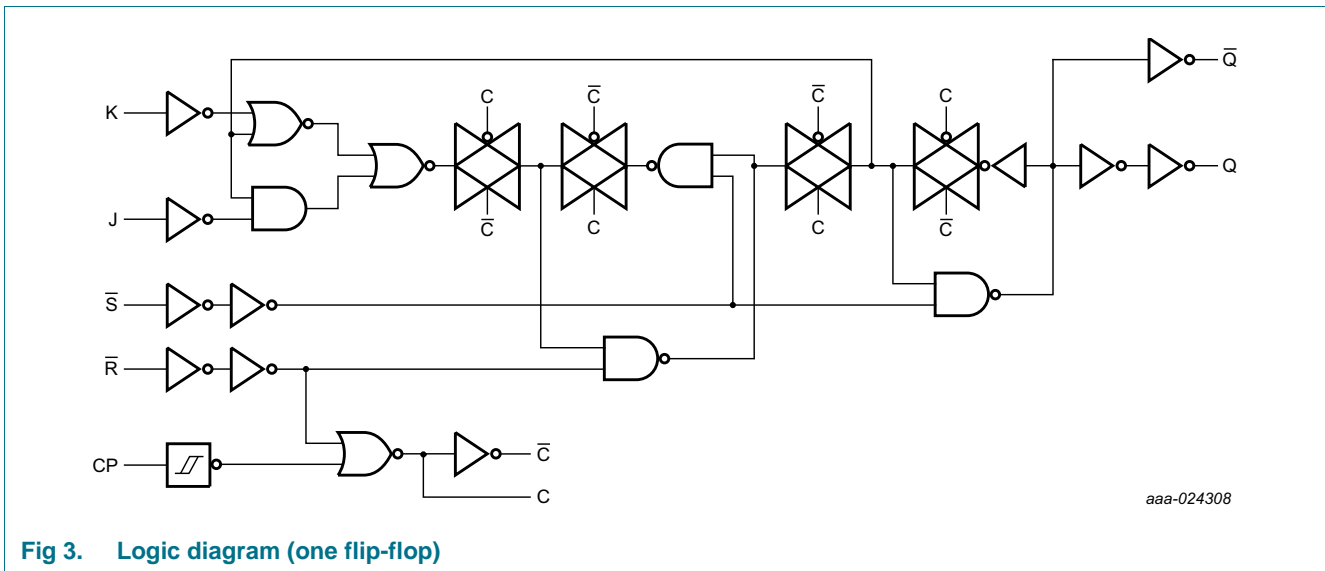
- Input levels:
  - ◆ For 74HC112: CMOS level
  - ◆ For 74HCT112: TTL level
- Asynchronous set and reset
- Specified in compliance with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

## 3. Ordering information

Table 1. Ordering information

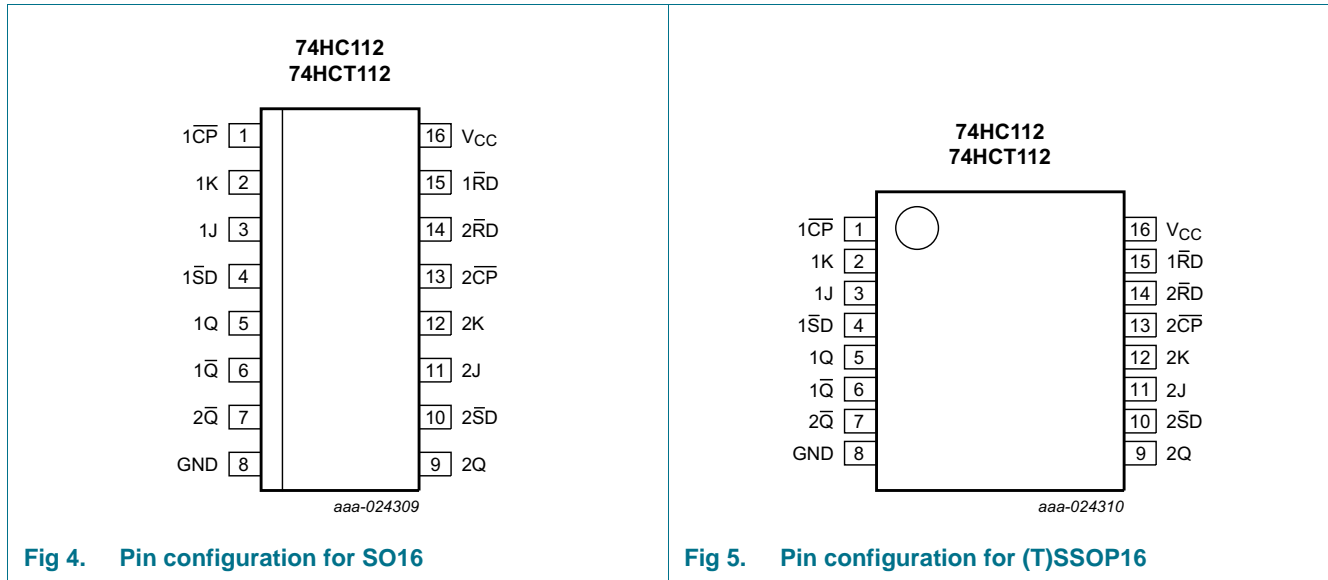
Type number	Package			
	Temperature range	Name	Description	Version
74HC112D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT112D				
74HC112DB	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT112DB				
74HC112PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT112PW				

## 4. Functional diagram



## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1CP, 2CP	1, 13	clock input (HIGH-to-LOW; edge-triggered)
1K, 2K	2, 12	data input
1J, 2J	3, 11	data input
1SD, 2SD	4, 10	set input (active LOW)
1Q, 2Q	5, 9	true flip-flop output
1Q̄, 2Q̄	6, 7	complement flip-flop output
GND	8	ground (0 V)
1RD, 2RD	15, 14	reset input (active LOW)
V <sub>CC</sub>	16	supply voltage

## 6. Functional description

Table 3. Function selection<sup>[1]</sup>

Operating modes	Input					Output	
	nSD	nRD	nCP	nJ	nK	nQ	nQ
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	L
Toggle	H	H	↓	h	h	$\bar{q}$	q
Load 0 (reset)	H	H	↓	l	h	L	H
Load 1 (set)	H	H	↓	h	l	H	L
Hold no change	H	H	↓	l	l	q	$\bar{q}$

[1] If nSD and nRD simultaneously go from LOW-to-HIGH, the output states are unpredictable.

H = HIGH voltage level

h = HIGH voltage level one set-up time before the HIGH-to-LOW clock transition

L = LOW voltage level

l = LOW voltage level one set-up time before the HIGH-to-LOW clock transition

q = lowercase letters indicate the state of the referenced output one set-up time before the HIGH-to-LOW clock transition

X = don't care

↓ = HIGH-to-LOW clock transition

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	-	±20	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	-	±20	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	+50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	SO16 and (T)SSOP16 packages <sup>[1]</sup>	-	500	mW

[1] For SO16 packages: above 70 °C, the value of P<sub>tot</sub> derates linearly with 8 mW/K.

For (T)SSOP16 packages: above 60 °C, the value of P<sub>tot</sub> derates linearly with 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC112			74HCT112			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC112</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V		
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	4.0	-	40	-	80	μA

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF
<b>74HCT112</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = −20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = −4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 5.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1	-	±1	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	4.0	-	40	-	80	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> − 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V								
		nSD inputs	-	50	180	-	225	-	245	μA
		nK inputs	-	60	216	-	270	-	294	μA
		nRD inputs	-	65	236	-	293	-	319	μA
		nJ, and nCP inputs	-	100	360	-	450	-	490	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
<b>74HC112</b>										
$t_{pd}$	propagation delay	$\overline{nCP}$ to $nQ$ ; see <a href="#">Figure 6</a> <sup>[2]</sup>								
		$V_{CC} = 2.0$ V	-	55	175	-	220	-	265	ns
		$V_{CC} = 4.5$ V	-	20	35	-	44	-	53	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	16	30	-	37	-	45	ns
		$\overline{nCP}$ to $\overline{nQ}$ ; see <a href="#">Figure 6</a>								
		$V_{CC} = 2.0$ V	-	55	175	-	220	-	265	ns
		$V_{CC} = 4.5$ V	-	20	35	-	44	-	53	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	16	30	-	37	-	45	ns
		$\overline{nRD}$ to $nQ$ , $\overline{nQ}$ ; see <a href="#">Figure 7</a>								
		$V_{CC} = 2.0$ V	-	58	180	-	225	-	270	ns
		$V_{CC} = 4.5$ V	-	21	36	-	45	-	54	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	18	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	17	31	-	38	-	46	ns
		$\overline{nSD}$ to $nQ$ , $\overline{nQ}$ ; see <a href="#">Figure 7</a>								
$V_{CC} = 2.0$ V	-	50	155	-	295	-	235	ns		
$V_{CC} = 4.5$ V	-	18	31	-	39	-	47	ns		
$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns		
$V_{CC} = 6.0$ V	-	14	26	-	33	-	40	ns		
$t_t$	transition time	$nQ$ , $\overline{nQ}$ ; see <a href="#">Figure 6</a> <sup>[3]</sup>								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns
$t_w$	pulse width	$\overline{nCP}$ HIGH or LOW; see <a href="#">Figure 6</a>								
		$V_{CC} = 2.0$ V	80	22	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	8	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	6	-	17	-	20	-	ns
		$\overline{nSD}$ , $\overline{nRD}$ LOW; see <a href="#">Figure 7</a>								
		$V_{CC} = 2.0$ V	80	22	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	8	-	20	-	24	-	ns
$V_{CC} = 6.0$ V	14	6	-	17	-	20	-	ns		

**Table 7. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
$t_{rec}$	recovery time	$\overline{nRD}$ to $\overline{nCP}$ ; see <a href="#">Figure 7</a>								
		$V_{CC} = 2.0$ V	80	22	-	125	-	150	-	ns
		$V_{CC} = 4.5$ V	16	8	-	25	-	30	-	ns
		$V_{CC} = 6.0$ V	14	6	-	21	-	26	-	ns
		$\overline{nSD}$ to $\overline{nCP}$ ; see <a href="#">Figure 7</a>								
		$V_{CC} = 2.0$ V	80	−19	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	−7	-	20	-	24	-	ns
$V_{CC} = 6.0$ V	14	−6	-	17	-	20	-	ns		
$t_{su}$	set-up time	$nJ$ and $nK$ to $\overline{nCP}$ ; see <a href="#">Figure 6</a>								
		$V_{CC} = 2.0$ V	80	19	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	7	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	6	-	17	-	20	-	ns
$t_h$	hold time	$nJ$ and $nK$ to $\overline{nCP}$ ; see <a href="#">Figure 6</a>								
		$V_{CC} = 2.0$ V	0	−11	-	0	-	0	-	ns
		$V_{CC} = 4.5$ V	0	−4	-	0	-	0	-	ns
		$V_{CC} = 6.0$ V	0	−3	-	0	-	0	-	ns
$f_{max}$	maximum frequency	$\overline{nCP}$ ; see <a href="#">Figure 6</a>								
		$V_{CC} = 2.0$ V	6	20	-	4.8	-	4.0	-	MHz
		$V_{CC} = 4.5$ V	30	60	-	24	-	20	-	MHz
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	66	-	-	-	-	-	MHz
		$V_{CC} = 6.0$ V	35	71	-	28	-	24	-	MHz
$C_{PD}$	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = \text{GND to } V_{CC}$ <sup>[4]</sup>	-	27	-			-	-	pF



**Table 7. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
<b>74HCT112</b>										
$t_{pd}$	propagation delay	$\overline{nCP}$ to nQ; see <a href="#">Figure 6</a> <sup>[2]</sup>								
		$V_{CC} = 4.5$ V	-	21	35	-	44	-	53	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	19	-	-	-	-	-	ns
		$\overline{nCP}$ to $\overline{nQ}$ ; see <a href="#">Figure 6</a> <sup>[2]</sup>								
		$V_{CC} = 4.5$ V	-	23	40	-	50	-	60	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	19	-	-	-	-	-	ns
		$\overline{nRD}$ to nQ, $\overline{nQ}$ ; see <a href="#">Figure 7</a>								
		$V_{CC} = 4.5$ V	-	22	37	-	46	-	56	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	19	-	-	-	-	-	ns
		$\overline{nSD}$ to nQ, $\overline{nQ}$ ; see <a href="#">Figure 7</a>								
$V_{CC} = 4.5$ V	-	18	32	-	40	-	48	ns		
$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns		
$t_t$	transition time	nQ, $\overline{nQ}$ ; see <a href="#">Figure 6</a> <sup>[3]</sup>								
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
$t_w$	pulse width	$\overline{nCP}$ HIGH or LOW; see <a href="#">Figure 6</a>								
		$V_{CC} = 4.5$ V	16	8	-	20	-	24	-	ns
		$\overline{nSD}$ , $\overline{nRD}$ LOW; see <a href="#">Figure 7</a>								
$V_{CC} = 4.5$ V	18	10	-	23	-	27	-	ns		
$t_{rec}$	recovery time	$\overline{nRD}$ to $\overline{nCP}$ ; see <a href="#">Figure 7</a>								
		$V_{CC} = 4.5$ V	20	11	-	25	-	30	-	ns
		$\overline{nSD}$ to $\overline{nCP}$ ; see <a href="#">Figure 7</a>								
$V_{CC} = 4.5$ V	20	-8	-	25	-	30	-	ns		
$t_{su}$	set-up time	nJ and nK to $\overline{nCP}$ ; see <a href="#">Figure 6</a>								
		$V_{CC} = 4.5$ V	16	7	-	20	-	24	-	ns
$t_h$	hold time	nJ and nK to $\overline{nCP}$ ; see <a href="#">Figure 6</a>								
		$V_{CC} = 4.5$ V	0	-7	-	0	-	0	-	ns
$f_{max}$	maximum frequency	$\overline{nCP}$ ; see <a href="#">Figure 6</a>								
		$V_{CC} = 4.5$ V	30	64	-	24	-	20	-	MHz
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	70	-	-	-	-	-	MHz

**Table 7. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
$C_{PD}$	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; <a href="#">[4]</a> $V_I = \text{GND to } V_{CC}$	-	30	-	-	-	-	-	pF

[1] All typical values are measured at  $T_{amb} = 25$  °C.

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

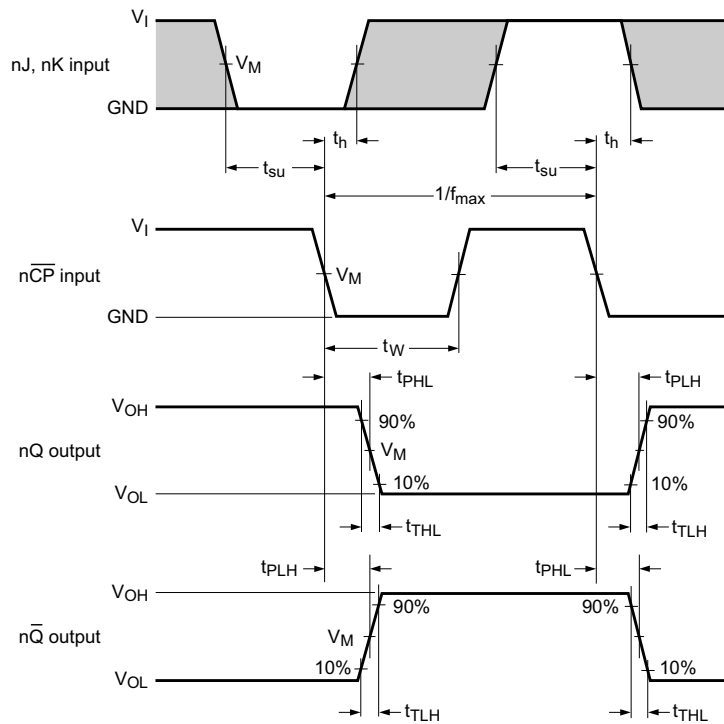
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## 11. Waveforms

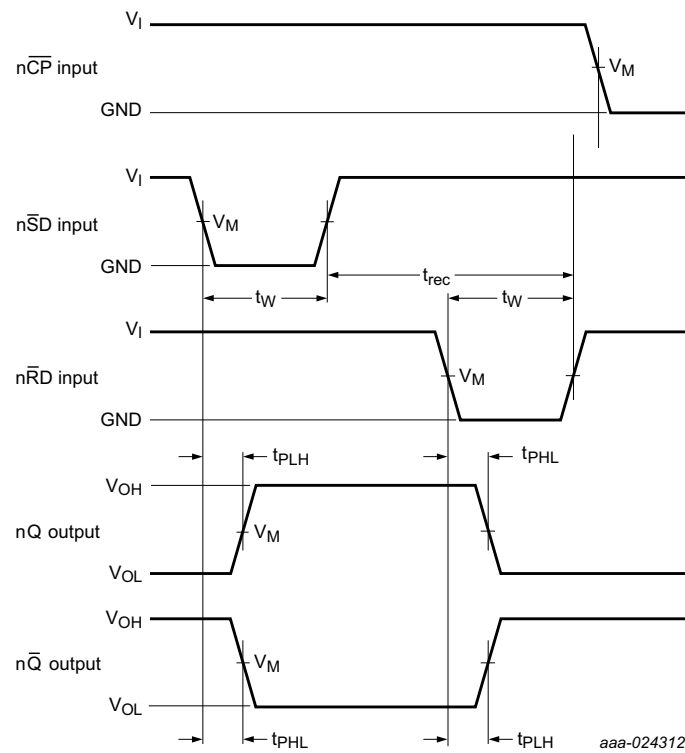


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Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 6. Clock propagation delays, output transition time, pulse width, set-up, hold times, and maximum frequency**



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. Set and reset propagation delays, pulse widths and recovery time**

**Table 8. Measurement points**

Type	Input	Output
	$V_M$	$V_M$
74HC112	$0.5V_{CC}$	$0.5V_{CC}$
74HCT112	1.3 V	1.3 V



001aah768

Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

**Fig 8. Test circuit for measuring switching times**

**Table 9. Test data**

Type	Input		Load	Test
	$V_I$	$t_r, t_f$	$C_L$	
74HC112	$V_{CC}$	6 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$
74HCT112	3 V	6 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

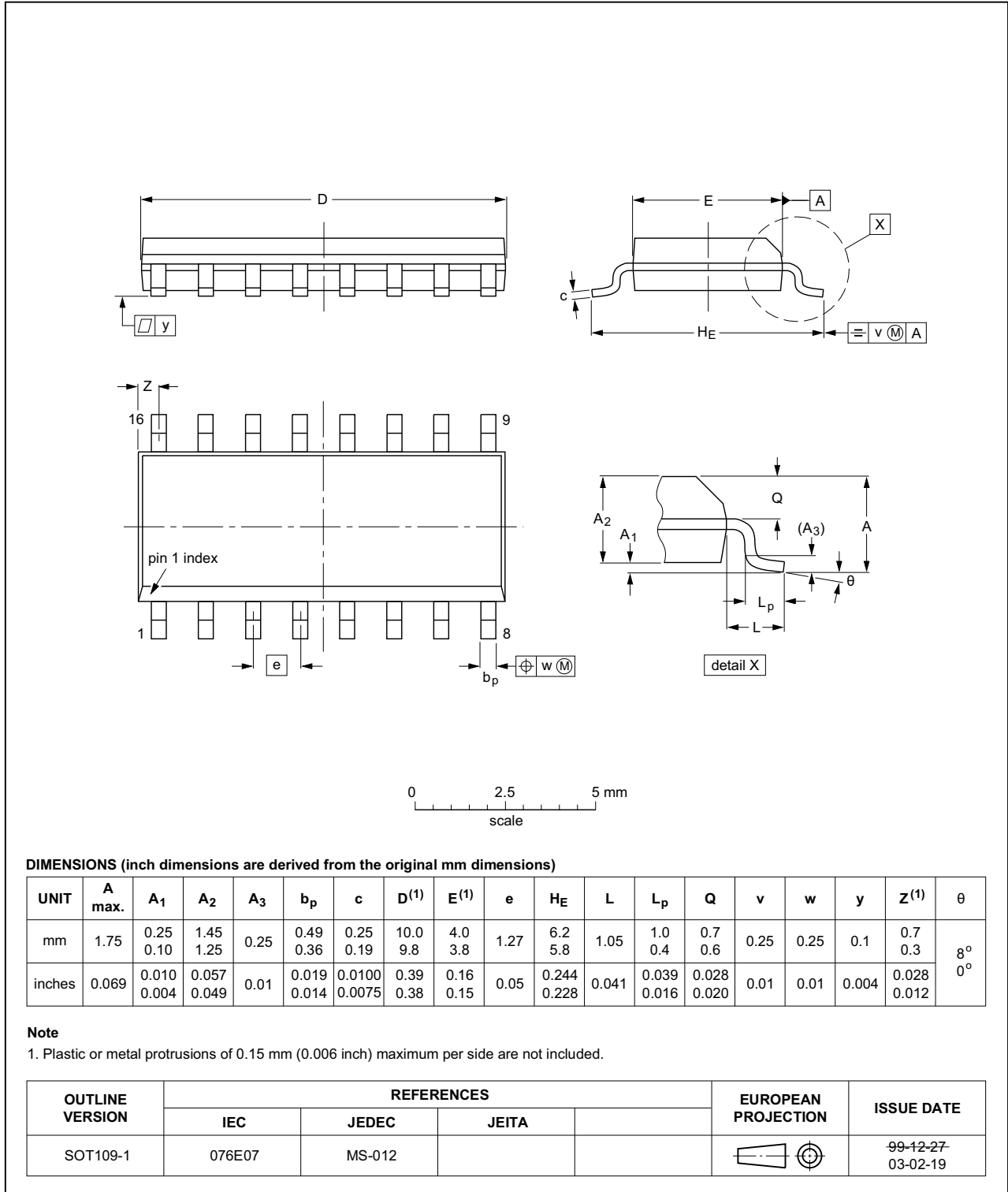


Fig 9. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

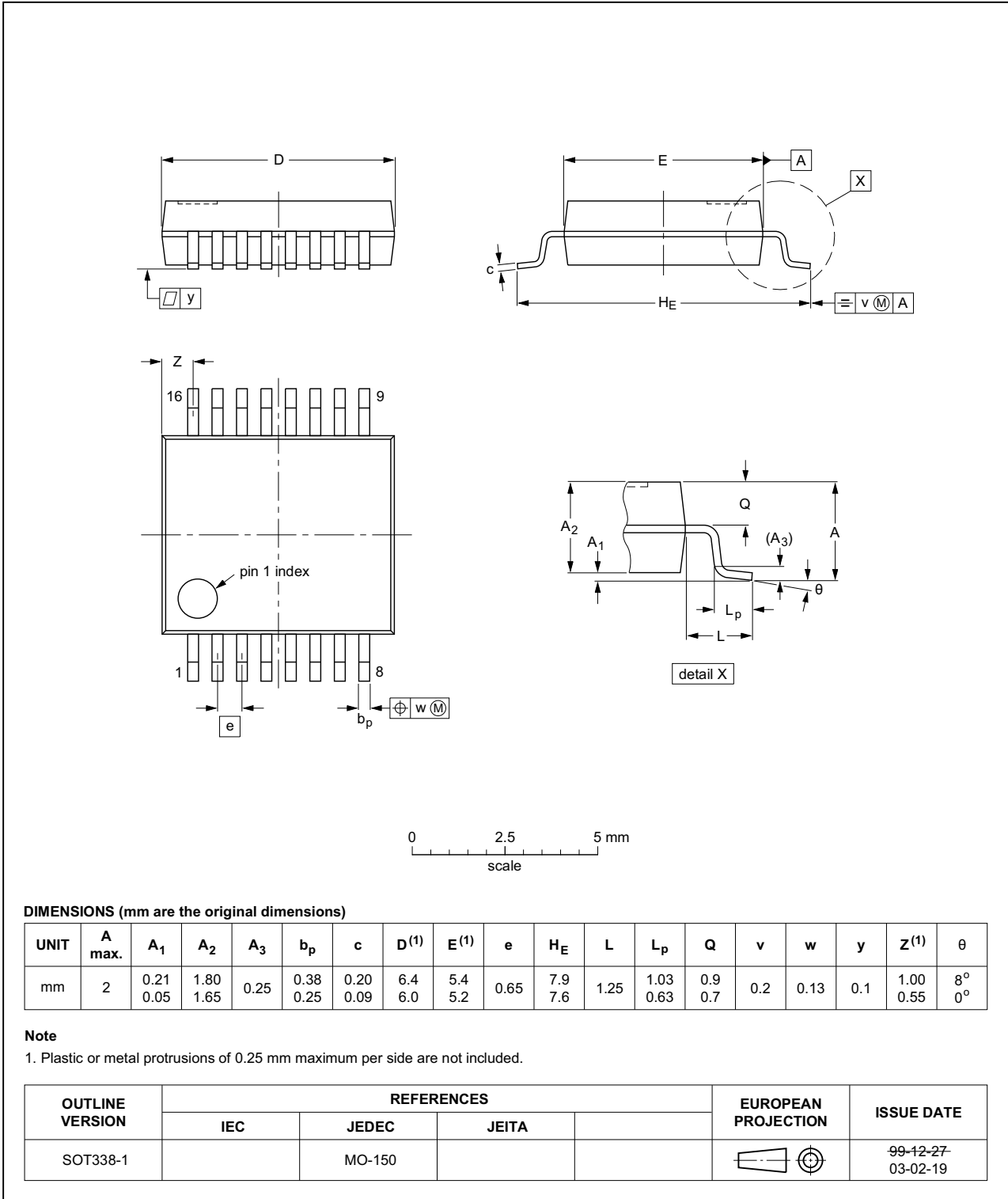


Fig 10. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

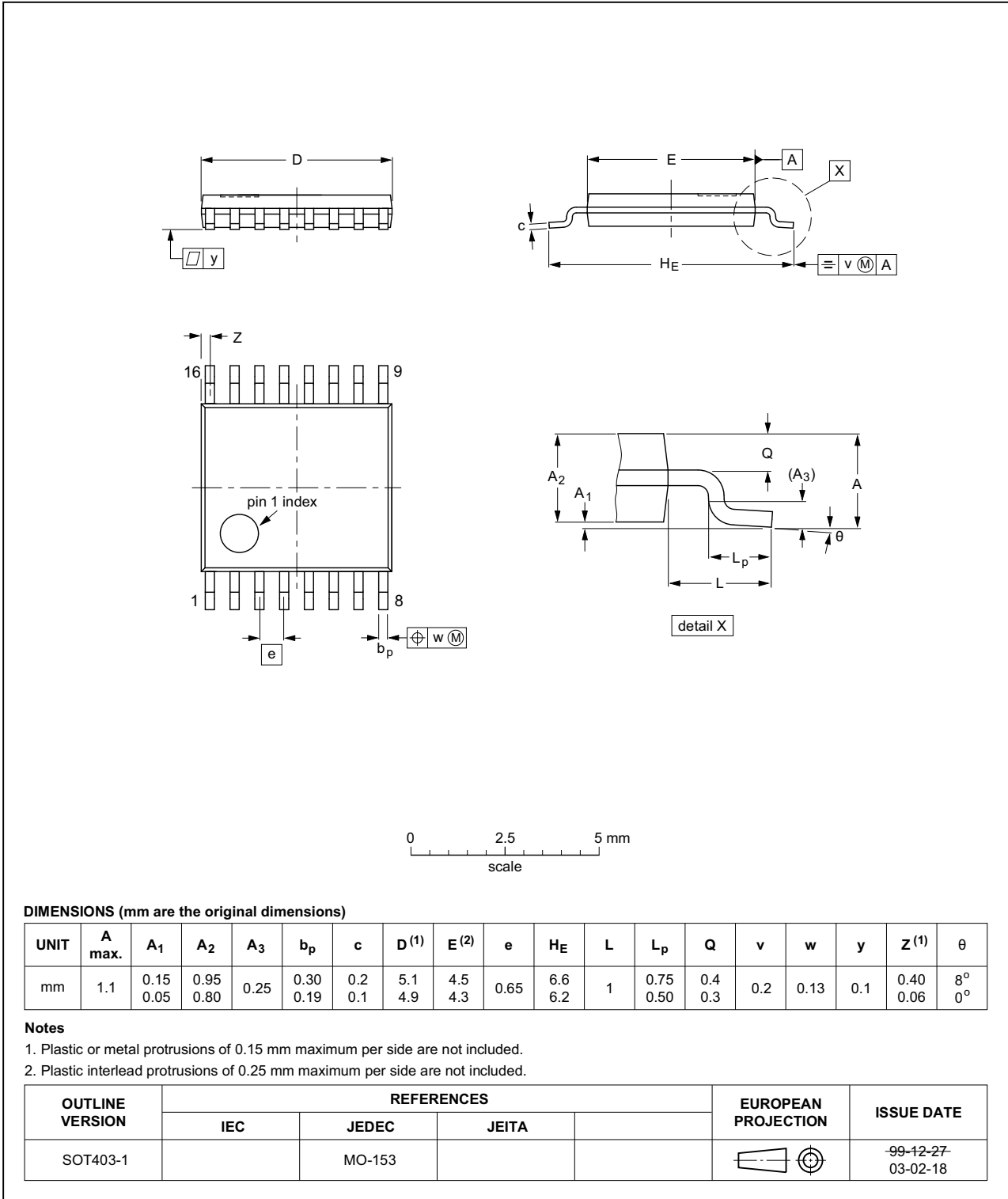


Fig 11. Package outline SOT403-1 (TSSOP16)



## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT112 v.3	20160809	Product data sheet	-	74HC_HCT112_CNV v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74HC112N and 74HCT112N removed.</li> </ul>			
74HC_HCT112_CNV v.2	19980610	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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