19-5732; Rev 2; 8/11

IEEE 802.3af/at-Compliant, Powered Device Interface Controllers with Integrated Power MOSFET

General Description

The MAX5981 provides a complete interface for a powered device (PD) to comply with the IEEE® 802.3af/at standard in a power-over-ethernet (PoE) system. The MAX5981 provides the PD with a detection signature, classification signature, and an integrated isolation power switch with inrush current control. During the inrush period, the MAX5981 limits the current to less than 180mA before switching to the higher current limit (720mA to 880mA) when the isolation power MOSFET is fully enhanced. The device features an input UVLO with wide hysteresis and long deglitch time to compensate for twisted-pair cable resistive drop and to assure glitch-free transition during power-on/-off conditions. The MAX5981 can withstand up to 100V at the input.

The MAX5981 supports a 2-Event classification method as specified in the IEEE 802.3at standard and provides a signal to indicate when probed by a Type 2 power sourcing equipment (PSE). The device detects the presence of a wall adapter power source connection and allows a smooth switch over from the PoE power source to the wall power adapter.

The MAX5981 also provides a power-good (PG) signal, two-step current limit and foldback, overtemperature protection, and di/dt limit. A sleep mode feature in the MAX5981 provides low power consumption while supporting Maintain Power Signature (MPS). An ultra-low-power sleep mode feature in the MAX5981 further reduces power consumption while still supporting MPS. The MAX5981 also features an LED driver that is automatically activated during sleep mode. During sleep mode, the LED driver sources a periodic current (I_{LED}) at 250Hz (MAX5981A) or 15.625kHz (MAX5981B).

The MAX5981 is available in a 16-pin, 5mm x 5mm TQFN power package. The device is rated over the -40°C to +85°C extended temperature range.

Features

- **Sleep Mode and Ultra-Low Power**
- **IEEE 802.3af/at Compliant**
- **2-Event Classification or an External Wall Adapter Indicator Output**
- **Simplified Wall Adapter Interface**
- **PoE Classification 0–5**
- **100V Input Absolute Maximum Rating**
- **Inrush Current Limit of 180mA Maximum**
- **Current Limit During Normal Operation Between 720mA and 880mA**
- **Current Limit and Foldback**
- **Legacy UVLO at 36V**
- **LED Driver with Programmable LED Current**
- **Overtemperature Protection**
- **Thermally Enhanced, 5mm x 5mm, 16-Pin TQFN**

Applications

IEEE 802.3af/at Powered Devices

IP Phones, Wireless Access Nodes, IP Security Cameras

WiMAX™ Base Stations

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	SLEEP MODE
MAX5981AETE+	-40°C to +85°C	16 TQFN-EP*	Yes
MAX5981BETE+	-40°C to +85°C	16 TQFN-EP*	Yes

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

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ABSOLUTE MAXIMUM RATINGS

V_{DD} to V_{SS} .....-0.3V to +100V
DET, RTN, WAD, PG, $\overline{2EC}$ to V_{SS} .....-0.3V to +100V
CLS, $\overline{SL}$, $\overline{WK}$, $\overline{ULP}$, LED to V_{SS}.....-0.3V to +6V
Maximum Current on CLS (100ms maximum).....100mA
Continuous Power Dissipation (T_A = +70°C) (Note 1)
TQFN (derate 28.6mW/°C above +70°C)
Multilayer Board 2285.7mW

Package Thermal Resistance (Note 2)
θ_{JA}.....35°C/W
θ_{JC} .....2.7°C/W
Operating Temperature Range ..... -40°C to +85°C
Maximum Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature ..... +260°C

Note 1: Maximum power dissipation is obtained using JEDEC JESD51-5 and JESD51-7 specifications.
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{DET} = 24.9kΩ, R_{CLS} = 615Ω, and $R_{\overline{SL}}$ = 60.4kΩ. RTN, WAD, PG, $\overline{2EC}$, $\overline{WK}$, and $\overline{ULP}$ unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DETECTION MODE							
Input Offset Current	I_{OFFSET}	V_{IN} = 1.4V to 10.1V (Note 4)				10	µA
Effective Differential Input Resistance	dR	V_{IN} = 1.4V up to 10.1V with 1V step, V_{DD} = RTN = WAD = PG = $\overline{2EC}$ (Note 5)		23.95	25.00	25.50	kΩ
CLASSIFICATION MODE							
Classification Disable Threshold	$V_{TH,CLS}$	V_{IN} rising (Note 6)		22.0	22.8	23.6	V
Classification Stability Time					0.2		ms
Classification Current	I_{CLASS}	V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG = $\overline{2EC}$	Class 0, R_{CLS} = 619Ω	0		3.96	mA
			Class 1, R_{CLS} = 117Ω	9.12		11.88	
			Class 2, R_{CLS} = 66.5Ω	17.2		19.8	
			Class 3, R_{CLS} = 43.7Ω	26.3		29.7	
			Class 4, R_{CLS} = 30.9Ω	36.4		43.6	
			Class 5, R_{CLS} = 21.3Ω	52.7		63.3	
TYPE 2 (802.3at) CLASSIFICATION MODE							
Mark Event Threshold	V_{THM}	V_{IN} falling		10.1	10.7	11.6	V
Hysteresis on Mark Event Threshold					0.84		V
Mark Event Current	I_{MARK}	V_{IN} falling to enter mark event, 5.2V ≤ V_{IN} ≤ 10.1V		0.25		0.85	mA
Reset Event Threshold	V_{THR}	V_{IN} falling		2.8	4	5.2	V
POWER MODE							
V_{IN} Supply Voltage Range						60	V
V_{IN} Supply Current	I_Q				0.27	0.55	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{DET} = 24.9kΩ, R_{CLS} = 615Ω, and $R_{\overline{SL}}$ = 60.4kΩ. RTN, WAD, PG, $\overline{2EC}$, $\overline{WK}$, and $\overline{ULP}$ unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Turn-On Voltage	V_{ON}	V_{IN} rising		34.3	35.4	36.6	V
V_{IN} Turn-Off Voltage	V_{OFF}	V_{IN} falling		30			V
V_{IN} Turn-On/-Off Hysteresis	V_{HYST_UVLO}	(Note 7)		4.2			V
V_{IN} Deglitch Time	t_{OFF_DLY}	V_{IN} falling from 40V to 20V (Note 8)		30	120		µs
Inrush to Operating Mode Delay	t_{DELAY}	t_{DELAY} = minimum PG current pulse width after entering into power mode		87	96	105	ms
Isolation Power MOSFET On-Resistance	R_{ON_ISO}	I_{RTN} = 600mA	T_J = +25°C		0.5	0.7	Ω
			T_J = +85°C		0.65	1	
			T_J = +125°C		0.8		
RTN Leakage Current	I_{RTN_LKG}	V_{RTN} = 12.5V to 30V				10	µA
CURRENT LIMIT							
Inrush Current Limit	I_{INRUSH}	During initial turn-on period, V_{RTN} = 1.5V		90	135	180	mA
Current Limit During Normal Operation	I_{LIM}	After inrush completed, V_{RTN} = 1V		720	800	880	mA
Foldback Threshold		V_{RTN} (Note 9)		13		16.5	V
LOGIC							
WAD Detection Threshold	$V_{WAD-REF}$	V_{WAD} rising, V_{IN} = 14V to 48V (referenced to RTN)		8	9	10	V
WAD Detection Threshold Hysteresis		V_{WAD} falling, V_{RTN} = 0V, V_{SS} unconnected			0.725		V
WAD Input Current	$I_{WAD-LKG}$	V_{WAD} = 10V (referenced to RTN)				3.5	µA
$\overline{2EC}$ Sink Current		$V_{\overline{2EC}}$ = 3.5V (referenced to RTN), V_{SS} disconnected		1	1.5	2.25	mA
$\overline{2EC}$ Off-Leakage Current		$V_{\overline{2EC}}$ = 48V				1	µA
PG Sink Current		V_{RTN} = 1.5V, V_{PG} = 0.8V, during inrush period		125	230	375	µA
PG Off-Leakage Current		V_{PG} = 60V				1	µA
SLEEP MODE							
$\overline{WK}$ and $\overline{ULP}$ Logic Threshold	V_{TH}	$V_{\overline{WK}}$ falling and $V_{\overline{ULP}}$ rising and falling		1.5		3	V
$\overline{SL}$ Logic Threshold		Falling		0.75	0.8	0.85	V
$\overline{SL}$ Current		$R_{\overline{SL}}$ = 0Ω			140		µA
LED Current Amplitude	I_{LED}	$R_{\overline{SL}}$ = 60.4kΩ, V_{LED} = 3.5V		10	10.5	11.5	mA
		$R_{\overline{SL}}$ = 30.2kΩ, V_{LED} = 3.75V		19.5	20.9	22.5	
		$R_{\overline{SL}}$ = 30.2kΩ, V_{LED} = 4V		19			

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{DET} = 24.9kΩ, R_{CLS} = 615Ω, and $R_{\overline{SL}}$ = 60.4kΩ. RTN, WAD, PG, $\overline{2EC}$, $\overline{WK}$, and $\overline{ULP}$ unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LED Current Programmable Range				10		20	mA
LED Current with Grounded $\overline{SL}$		$V_{\overline{SL}}$ = 0V		20.5	24.5	28.5	mA
LED Current Frequency	f_{ILED}	Normal and ULP sleep mode	MAX5981A		250		Hz
			MAX5981B		15.625		kHz
LED Current Duty Cycle	D_{ILED}	Normal and ULP sleep mode			25		%
V_{DD} Current Amplitude	I_{VDD}	Normal sleep mode, V_{LED} = 3.5V		10	11	12	mA
Internal Current Duty Cycle	D_{IVDD}	Normal and $\overline{ULP}$ sleep modes			75		%
Internal Current Enable Time	t_{MPS}	$\overline{ULP}$ sleep mode		76	84	92	ms
Internal Current Disable Time	t_{MPDO}	$\overline{ULP}$ sleep mode		205	228	250	ms
THERMAL SHUTDOWN							
Thermal-Shutdown Threshold	T_{SD}	T_J rising			+140		°C
Thermal-Shutdown Hysteresis		T_J falling			28		°C

Note 3: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

Note 4: The input offset current is illustrated in Figure 1.

Note 5: Effective differential input resistance is defined as the differential resistance between V_{DD} and V_{SS}. See Figure 1.

Note 6: Classification current is turned off whenever the device is in power mode.

Note 7: UVLO hysteresis is guaranteed by design, not production tested.

Note 8: A 20V glitch on input voltage, which takes V_{DD} below V_{ON} shorter than or equal to t_{OFF_DLY} does not cause the MAX5981A/MAX5981B to exit power-on mode.

Note 9: In power mode, current-limit foldback is used to reduce the power dissipation in the isolation MOSFET during an overload condition across V_{DD} and RTN.

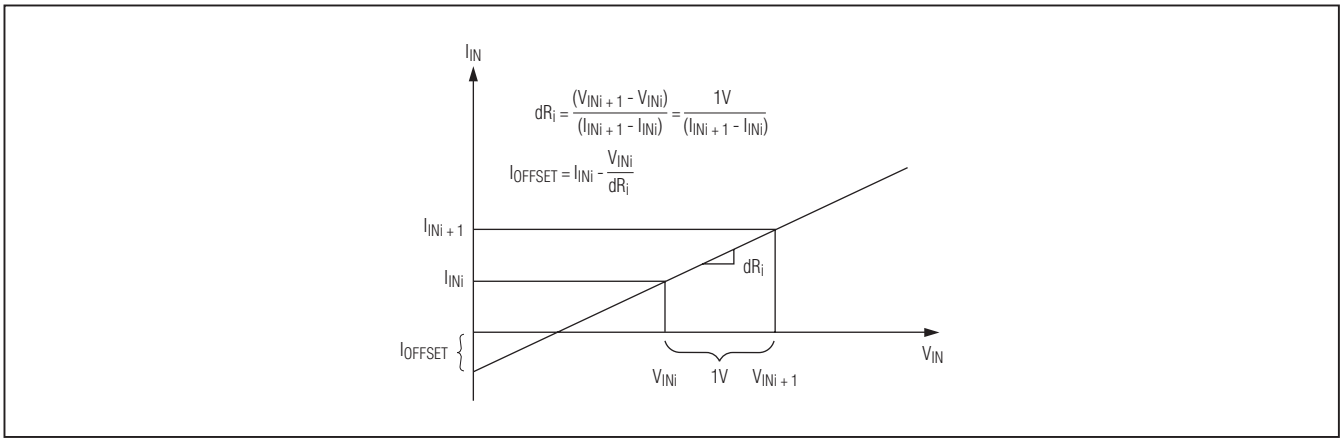

Figure 1. Effective Differential Input Resistance/Offset Current

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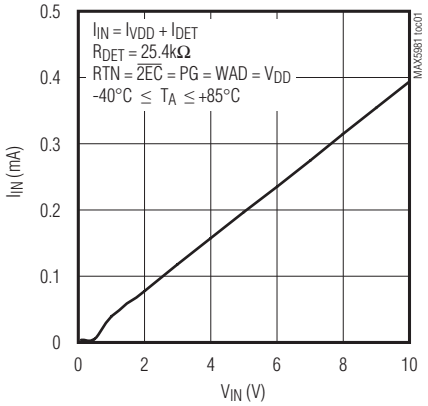
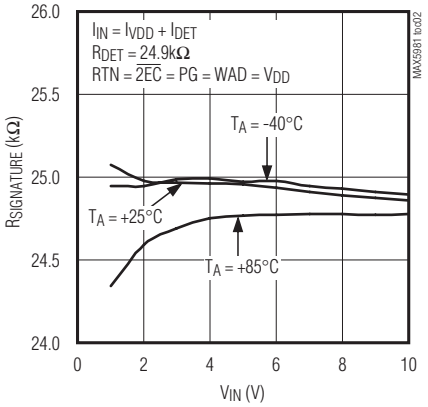
Typical Operating Characteristics

(V_{IN} = (V_{DD} - V_{SS}) = 54V, R_{DET} = 24.9kΩ, R_{CLS} = 615Ω, and $R_{\overline{SL}}$ = 60.4kΩ. RTN, WAD, PG, $\overline{2EC}$, $\overline{WK}$, and $\overline{ULP}$ unconnected; all voltages are referenced to V_{SS}.)

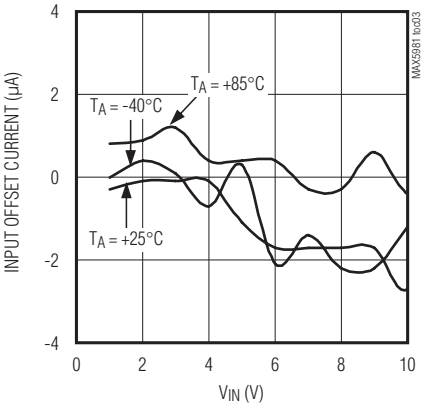
DETECTION CURRENT vs. INPUT VOLTAGE



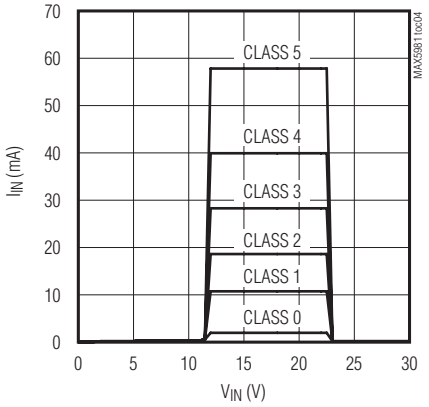
SIGNATURE RESISTANCE vs. INPUT VOLTAGE



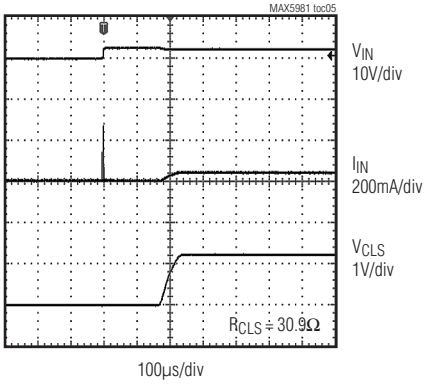
INPUT OFFSET CURRENT vs. INPUT VOLTAGE



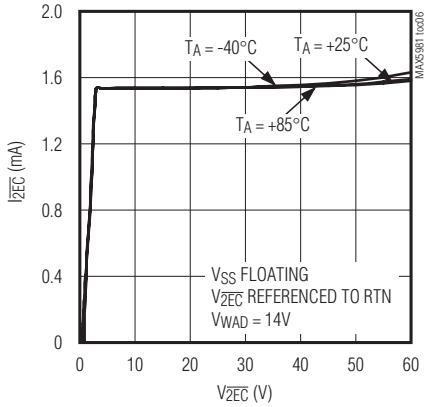
CLASSIFICATION CURRENT vs. INPUT VOLTAGE



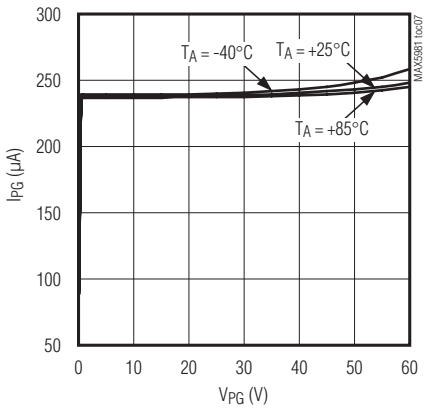
CLASSIFICATION SETTLING TIME



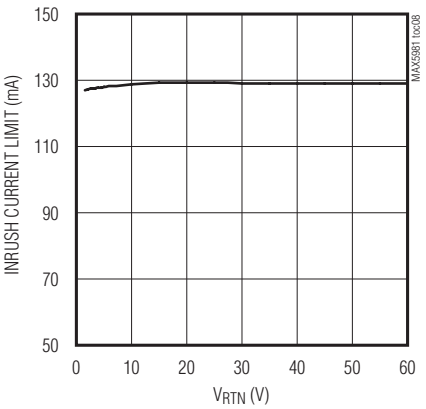
$\overline{2EC}$ SINK CURRENT vs. $\overline{2EC}$ VOLTAGE



PG SINK CURRENT vs. PG VOLTAGE



INRUSH CURRENT LIMIT vs. RTN VOLTAGE



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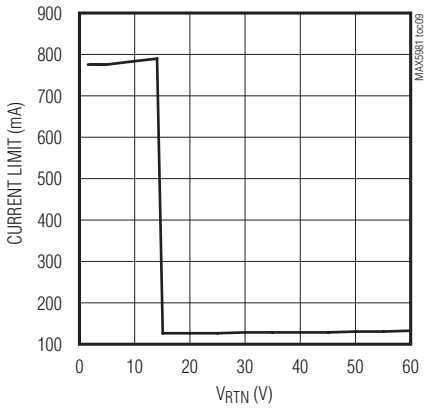
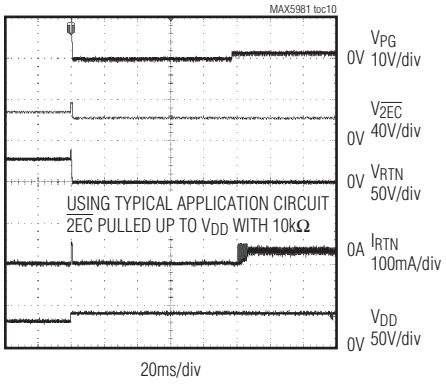
Typical Operating Characteristics (continued)

(V_{IN} = (V_{DD} - V_{SS}) = 54V, R_{DET} = 24.9kΩ, R_{CLS} = 615Ω, and $R_{\overline{SL}}$ = 60.4kΩ. RTN, WAD, PG, $\overline{2EC}$, $\overline{WK}$, and $\overline{ULP}$ unconnected; all voltages are referenced to V_{SS}.)

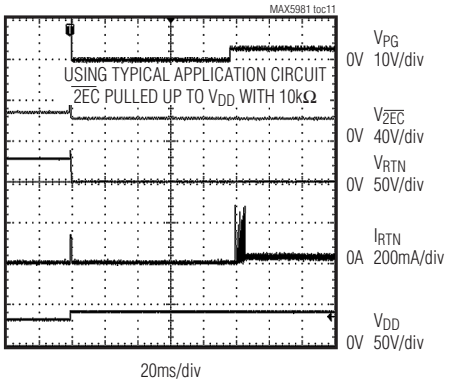
NORMAL OPERATION CURRENT LIMIT vs. RTN VOLTAGE



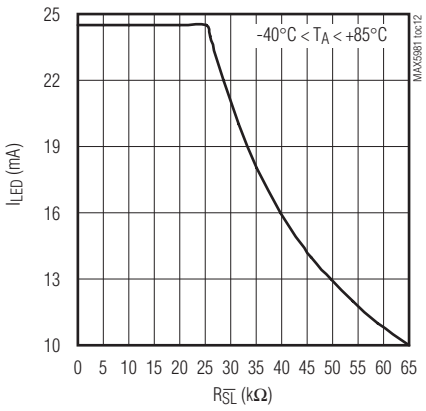
INRUSH CONTROL WAVEFORM WITH TYPE 2 CLASSIFICATION



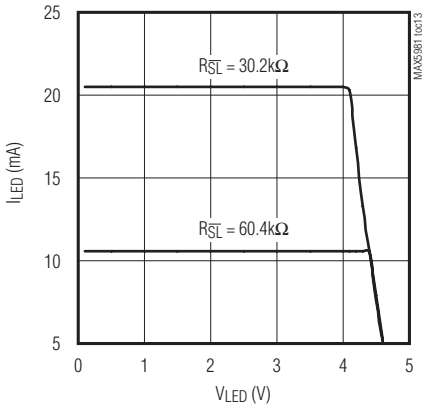
INRUSH CONTROL WAVEFORM WITH TYPE 2 CLASSIFICATION



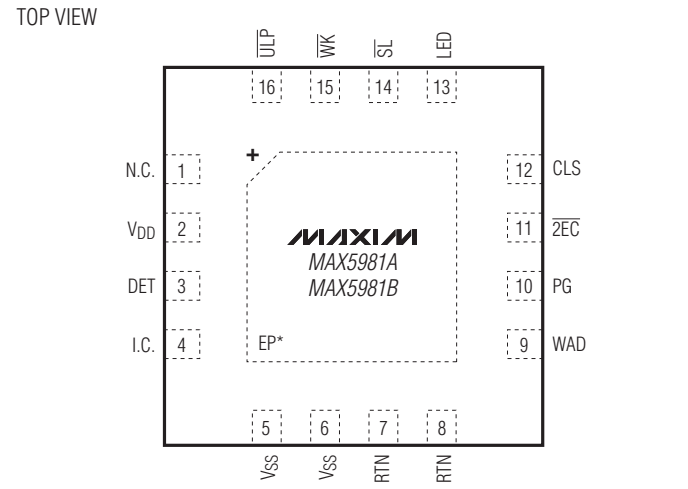
LED CURRENT vs. $R_{\overline{SL}}$



LED CURRENT vs. LED VOLTAGE



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	N.C.	No Connection. Not internally connected.
2	V_{DD}	Positive Supply Input. Connect a 68nF (min) bypass capacitor between V_{DD} and V_{SS}.
3	DET	Detection Resistor Input. Connect a signature resistor (R_{DET} = 24.9kΩ) from DET to V_{DD}.
4	I.C.	Internally Connected. Leave unconnected.
5, 6	V_{SS}	Negative Supply Input. V_{SS} connects to the source of the integrated isolation n-channel power MOSFET.
7, 8	RTN	Drain of Isolation MOSFET. RTN connects to the drain of the integrated isolation n-channel power MOSFET. Connect RTN to the downstream DC-DC converter ground as shown in the *Typical Application Circuit*.
9	WAD	Wall Power Adapter Detector Input. Wall adapter detection is enabled the moment V_{DD} - V_{SS} crosses the mark event threshold. Detection occurs when the voltage from WAD to RTN is greater than 9V. When a wall power adapter is present, the isolation n-channel power MOSFET turns off, $\overline{2EC}$ current sink turns on. Connect WAD directly to RTN when the wall power adapter or other auxiliary power source is not used.
10	PG	Open-Drain Power-Good Indicator Output. PG sinks 230µA to disable the downstream DC-DC converter while turning on the hot-swap MOSFET switch. PG current sink is disabled during detection, classification, and in the steady-state power mode. The PG current sink is turned on to disable the downstream DC-DC converter when the device is in sleep mode.

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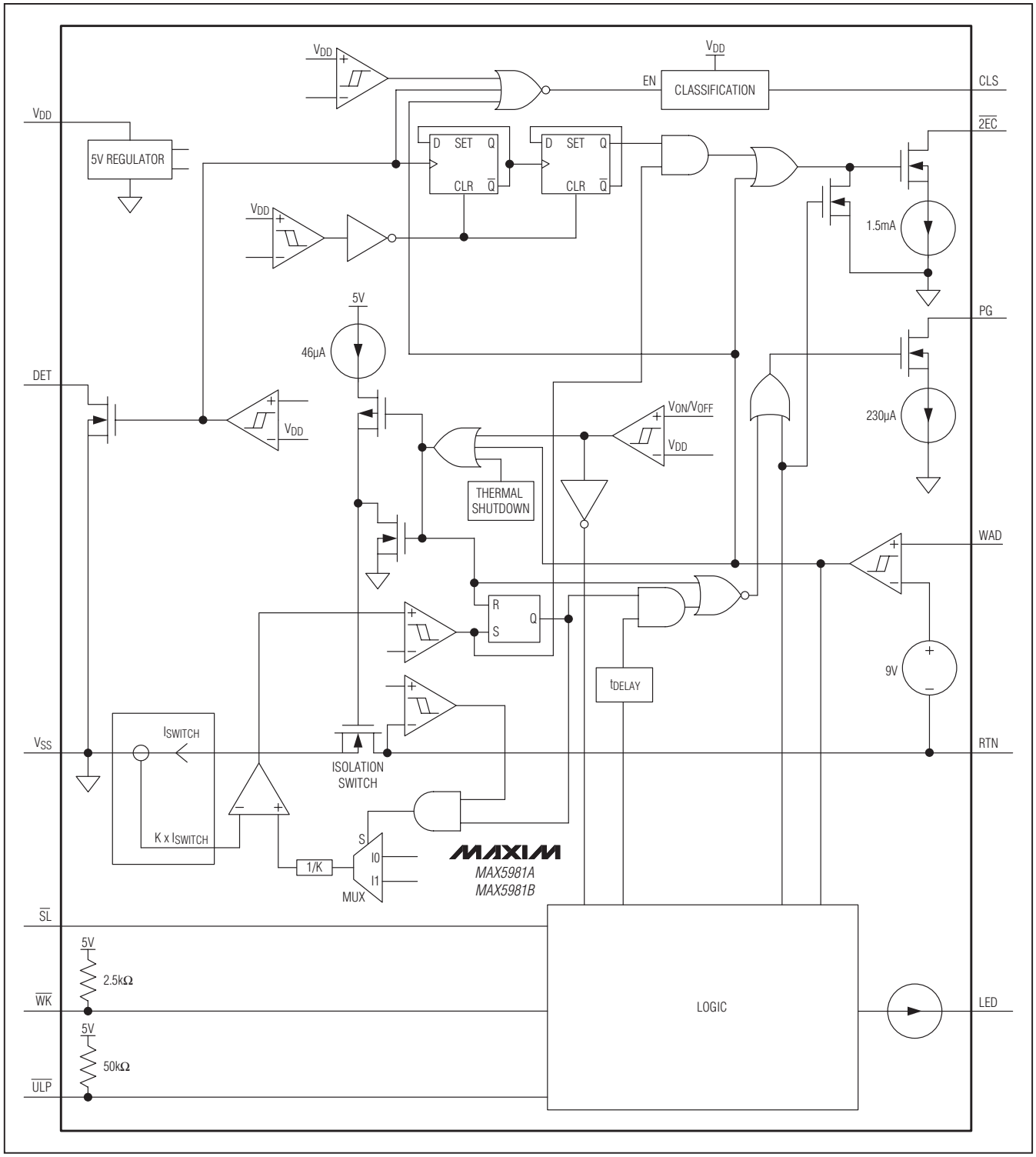
Pin Description (continued)

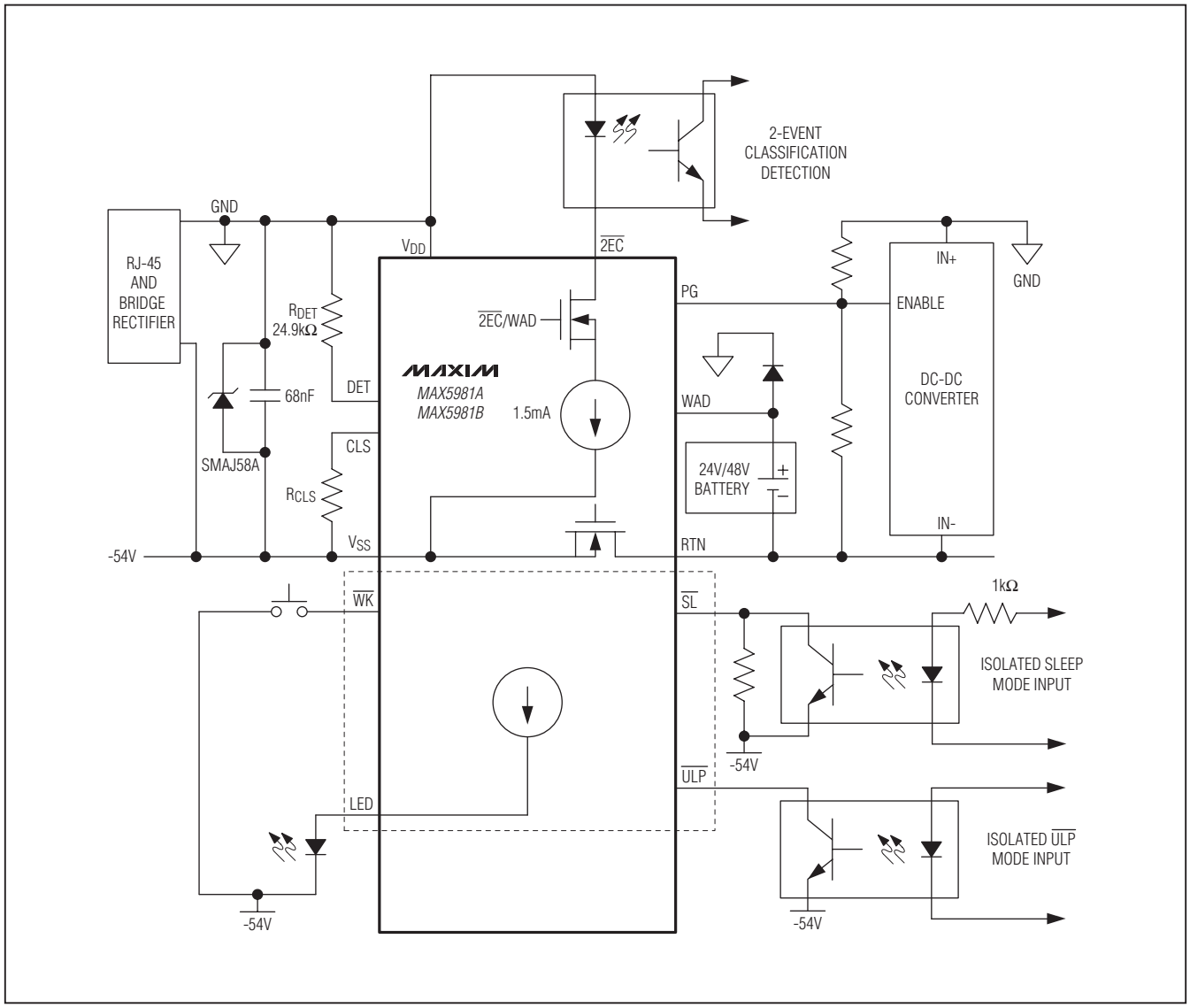
PIN	NAME	FUNCTION
11	$\overline{2EC}$	2-Event Classification Detect or Wall Adapter Detect Output. A 1.5mA current sink is enabled at $\overline{2EC}$ when a Type 2 PSE or a wall adapter is detected. When powered by a Type 2 PSE, the $\overline{2EC}$ current sink is enabled after the isolation MOSFET is fully on until V_{IN} drops below the UVLO threshold. $\overline{2EC}$ is latched when powered by a Type 2 PSE until V_{IN} drops below the reset threshold. $\overline{2EC}$ also asserts when a wall adapter supply, typically greater than 9V, is applied between WAD and RTN. $\overline{2EC}$ is not latched if asserted by WAD. The $\overline{2EC}$ current sink is turned off when the device is in sleep mode.
12	CLS	Classification Resistor Input. Connect a resistor (R_{CLS}) from CLS to V_{SS} to set the desired classification current. See the classification current specifications in the *Electrical Characteristics* table to find the resistor value for a particular PD classification.
13	LED	LED Driver Output. During sleep mode, LED sources a periodic current (I_{LED}). The amplitude of I_{LED} is set by $R_{\overline{SL}}$ according to the formula I_{LED} (in A) = 645.75/($R_{\overline{SL}}$ + 1200).
14	$\overline{SL}$	Sleep Mode Enable Input. A falling edge on $\overline{SL}$ brings the device into sleep mode ($V_{\overline{SL}}$ must drop below 0.75V). An external resistor ($R_{\overline{SL}}$) connected between $\overline{SL}$ and V_{SS} sets the LED current (I_{LED}).
15	$\overline{WK}$	Wake Mode Enable Input. $\overline{WK}$ has an internal 2.5kΩ pullup resistor to the internal 5V bias rail. A falling edge on $\overline{WK}$ brings the device out of sleep mode and into the normal operating mode (wake mode).
16	$\overline{ULP}$	Ultra-Low-Power Enable Input (in Sleep Mode). $\overline{ULP}$ has an internal 50kΩ pullup resistor to the internal 5V bias rail. A falling edge on $\overline{SL}$ while $\overline{ULP}$ is asserted low enables ultra-low-power mode. When ultra-low-power mode is enabled, the power consumption of the device is reduced even lower than normal sleep while still supporting MPS.
—	EP	Exposed Pad. Do not use EP as an electrical connection to V_{SS}. EP is internally connected to V_{SS} through a resistive path and must be connected to V_{SS} externally. To optimize power dissipation, solder the exposed pad to a large copper power plane.

Simplified Block Diagram



IEEE 802.3af/at-Compliant, Powered Device Interface Controllers with Integrated Power MOSFET

Typical Operating Circuit



Detailed Description

Operating Modes

Depending on the input voltage (V_{IN} = V_{DD} - V_{SS}), the MAX5981 operates in four different modes: PD detection, PD classification, mark event, and PD power. The devices enter PD detection mode when the input voltage is between 1.4V and 10.1V. The device enters PD classification mode when the input voltage is between 12.6V and 20V. The device enters PD power mode once the input voltage exceeds V_{ON}.

Detection Mode ($1.4V \le V_{IN} \le 10.1V$)

In detection mode, the power source equipment (PSE) applies two voltages on V_{IN} in the 1.4V to 10.1V range (1V step minimum) and then records the current measurements at the two points. The PSE then computes DV/DI to ensure the presence of the 24.9kΩ signature resistor. Connect the signature resistor (R_{DET}) from V_{DD} to DET for proper signature detection. The MAX5981 pulls DET low in detection mode. DET goes high impedance when the input voltage exceeds 12.5V. In detection mode, most of the MAX5981 internal circuitry is off and the offset current is less than 10µA.

If the voltage applied to the PD is reversed, install protection diodes at the input terminal to prevent internal damage to the MAX5981 (see the *Typical Application Circuit*). Since the PSE uses a slope technique (DV/DI) to calculate the signature resistance, the DC offset due to the protection diodes is subtracted and does not affect the detection process.

Classification Mode ($12.6V \le V_{IN} \le 20V$)

In the classification mode, the PSE classifies the PD based on the power consumption required by the PD. This allows the PSE to efficiently manage power distribution. Class 0–5 is defined as shown in Table 1. (The IEEE 802.3af/at standard defines only Class 0–4 and Class 5 for any special requirement.) An external resistor (R_{CLS}) connected from CLS to V_{SS} sets the classification current.

The PSE determines the class of a PD by applying a voltage at the PD input and measuring the current sourced out of the PSE. When the PSE applies a voltage between 12.6V and 20V, the MAX5981A/MAX5981B exhibit a current characteristic with a value shown in Table 1. The PSE uses the classification current information to classify the power requirement of the PD. The classification current includes the current drawn by R_{CLS} and the supply current of the MAX5981A/MAX5981B so the total current drawn by the PD is within the IEEE 802.3af/at standard figures. The classification current is turned off whenever the device is in power mode.

2-Event Classification and Detection

During 2-Event classification, a Type 2 PSE probes PD for classification twice. In the first classification event, the PSE presents an input voltage between 12.6V and 20.5V and the MAX5981A/MAX5981B present the programmed load I_{CLASS}. The PSE then drops the probing voltage below the mark event threshold of 10.1V and the MAX5981A/MAX5981B present the mark current (I_{MARK}). This sequence is repeated one more time.

When the MAX5981A/MAX5981B are powered by a Type 2 PSE, the 2-Event identification output $\overline{2EC}$ asserts low after the internal isolation n-channel MOSFET is fully turned on. $\overline{2EC}$ current sink is turned off when V_{DD} goes below the UVLO threshold (V_{OFF}) and turns on when V_{DD} goes above the UVLO threshold (V_{ON}), unless V_{DD} goes below VTHR to reset the latched output of the

Table 1. Setting Classification Current

CLASS	MAXIMUM POWER USED BY PD (W)	R_{CLS} (Ω)	V_{IN}* (V)	CLASS CURRENT SEEN AT V_{IN} (mA)		IEEE 802.3at PD CLASSIFICATION CURRENT SPECIFICATION (mA)	
				MIN	MAX	MIN	MAX
0	0.44 to 12.95	615	12.6 to 20	0	4	0	5
1	0.44 to 3.84	117	12.6 to 20	9	12	8	13
2	3.84 to 6.49	66.5	12.6 to 20	17	20	16	21
3	6.49 to 12.95	43.7	12.6 to 20	26	30	25	31
4	12.95 to 25.5	30.9	12.6 to 20	36	44	35	45
5	> 25.5	21.3	12.6 to 20	54	64	51	68

V_{IN} is measured across the MAX5981A/MAX5981B input V_{DD} to V_{SS}.

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Type 2 PSE detection flag. Alternatively, the $\overline{2EC}$ output also serves as a wall adapter detection output when the MAX5981A/MAX5981B are powered by an external wall power adapter. See the *Wall Power Adapter Detection and Operation* section for more information.

Power Mode (Wake Mode)

The MAX5981A/MAX5981B enter power mode when V_{IN} rises above the undervoltage lockout threshold (V_{ON}). When V_{IN} rises above V_{ON}, the MAX5981A/MAX5981B turn on the internal n-channel isolation MOSFET to connect V_{SS} to RTN with inrush current limit internally set to 135mA (typ). The isolation MOSFET is fully turned on when the voltage at RTN is near V_{SS} and the inrush current is reduced below the inrush limit. Once the isolation MOSFET is fully turned on, the MAX5981A/MAX5981B change the current limit to 800mA. The open-drain power-good output (PG) remains low for a minimum of t_{DELAY} until the power MOSFET fully turns on to keep the downstream DC-DC converter disabled during inrush.

Undervoltage Lockout

The MAX5981A/MAX5981B operate up to a 60V supply voltage with a turn-on UVLO threshold (V_{ON}) at 35.4V and a turn-off UVLO threshold (V_{OFF}) at 31V. When the input voltage is above V_{ON}, the MAX5981A/MAX5981B enter power mode and the internal MOSFET is turned on. When the input voltage goes below V_{OFF} for more than t_{OFF_DLY}, the MOSFET turns off.

Sleep and Ultra-Low-Power Sleep Modes

The MAX5981A/MAX5981B feature a sleep mode, which pulls PG low while keeping the internal n-channel isolation MOSFET turned on. The PG output is used to disable downstream DC-DC converters reducing the power consumption of the overall PD system in sleep mode. In sleep mode, the LED driver output (LED) sources periodic current pulses. The LED current I_{LED} is set by an external resistor R_{SL}, see the *Applications Information* section for more information.

An ultra-low-power sleep mode allows the MAX5981A/MAX5981B to further reduce power consumption while maintaining the power signature of the standard. The ultra-low-power enable input $\overline{ULP}$ is internally held high with a 50kΩ pullup resistor to the internal 5V bias of the MAX5981A/MAX5981B. Set $\overline{ULP}$ to logic-low and apply a falling edge to SL to enable ultra-low-power sleep mode. Apply a falling edge on the wake-mode enable input ($\overline{WK}$) to disable sleep or ultra-low-power sleep mode and resume normal operation.

LED Driver

The MAX5981A/MAX5981B drive an LED connected from the output LED to V_{SS}. During sleep mode/ultra-low-power sleep mode, the LED is driven by current pulses with the amplitude set by the resistor connected from $\overline{SL}$ to V_{SS}. The LED driver current amplitude is programmable from 10mA to 20mA using R_{SL} according to the following formula:

$$I_{LED} = \frac{645.75}{R_{\overline{SL}} + 1200} \text{ (in amperes)}$$

Power-Good Output

An open-drain output (PG) is used to allow disabling downstream DC-DC converter until the n-channel isolation MOSFET is fully turned on. PG is pulled low to V_{SS} for a period of t_{DELAY} and until the internal isolation MOSFET is fully turned on. The PG is also pulled low during sleep mode and coming out of thermal shutdown.

Thermal-Shutdown Protection

The MAX5981A/MAX5981B include thermal protection from excessive heating. If the junction temperature exceeds the thermal-shutdown threshold of +140°C, the MAX5981A/MAX5981B turn off the internal power MOSFET, LED driver, and $\overline{2EC}$ current sink. When the junction temperature falls below +112°C, the device enters inrush mode and then return to power mode. Inrush mode ensures the downstream DC-DC converter is turned off as the internal power MOSFET is turned on.

Wall Power Adapter Detection and Operation

For applications where an auxiliary power source such as a wall power adapter is used to power the PD, the MAX5981A/MAX5981B feature wall power adapter detection. The MAX5981A/MAX5981B give highest priority to the WAD and smoothly switch the power supply to WAD when it is detected. Once the input voltage (V_{DD} - V_{SS}) exceeds the mark event threshold, the MAX5981A/MAX5981B enable wall adapter detection. The wall power adapter is connected from WAD to RTN. The MAX5981A/MAX5981B detect the wall power adapter when the voltage from WAD to RTN is greater than 9V. When a wall power adapter is detected, the internal n-channel isolation MOSFET turns off, $\overline{2EC}$ current sink turns on, and classification current is disabled if V_{IN} is in the classification range.

Applications Information

Operation with 12V Adapter

Layout Procedure

Careful PCB layout is critical to achieve high efficiency and low EMI. Follow these layout guidelines for optimum performance:

1) Place the input capacitor, classification resistor, and transient voltage suppressor as close as possible to the MAX5981A/MAX5981B.
2) Use large SMT component pads for power dissipating devices such as the MAX5981A/MAX5981B and the external diodes.
3) Use short and wide traces for high-power paths.
4) Use the MAX5981A/MAX5981B evaluation kit layout as a reference.
5) Place enough vias in the pad for the EP of the MAX5981A/MAX5981B so that heat generated inside can be effectively dissipated by the PCB copper. The recommended spacing for the vias is 1mm to 1.2mm pitch. The thermal vias should be plated (1oz copper) and have a small barrel diameter (0.3mm to 0.33mm).

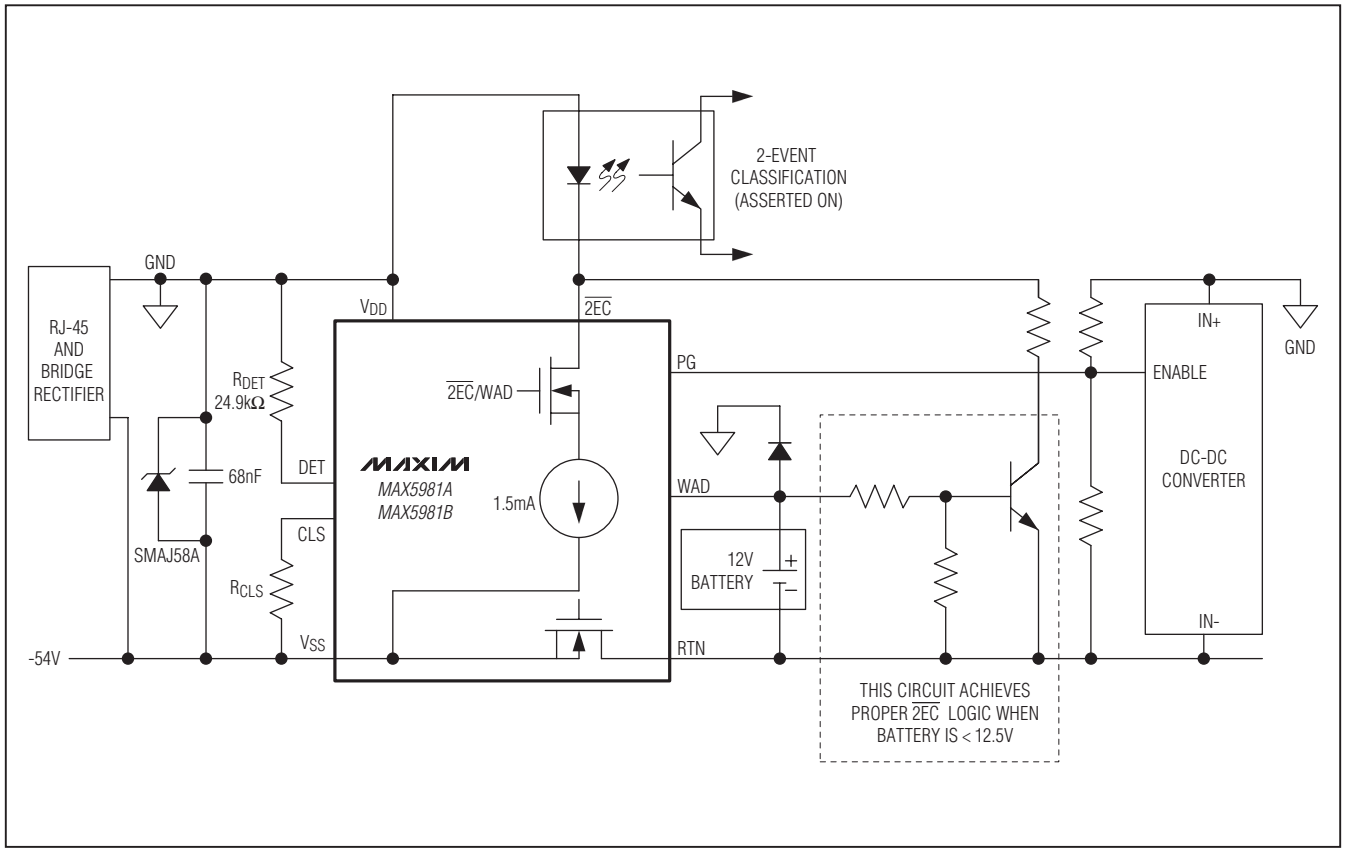

Figure 2. Typical Configuration When Using a 12V Wall Power Adapter

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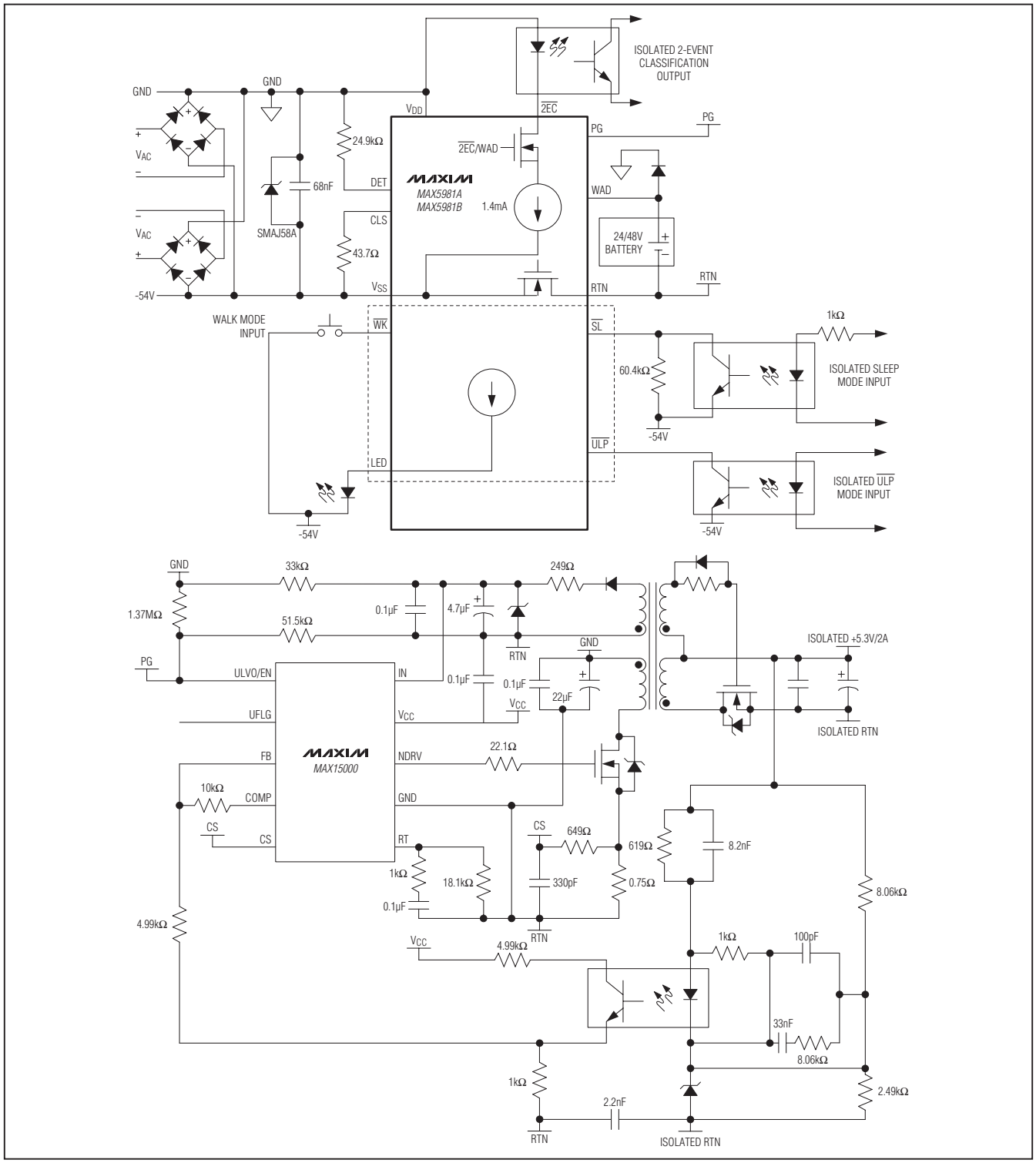
Typical Application Circuit



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, (footprints) go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1655+4	21-0140	90-0121

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/11	Initial release	—
1	8/11	Revised *General Description*, *Absolute Maximum Ratings*, *Electrical Characteristics*, *Pin Description*, *Typical Operating Circuit*, *LED Driver* section, and *Typical Application Circuit.*	1–8, 10, 11, 12, 14
2	8/11	Revised *General Description*, *Electrical Characteristics*, *Typical Operating Characteristics*, and *Pin Description.*	1, 4, 6, 8

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