

1x, 2x, 4x, and 8x Clock Multiplier with Internal LCO

Features

- ◆ Clock Multiplier / Jitter Reduction
 - Generates a Low Jitter 6 - 75 MHz Clock from a Jittery 750 kHz to 30 MHz Clock Source
- ◆ Internal LCO Reference Clock
- ◆ 1 Hz Loop Filter Bandwidth
- ◆ Selectable Multiplication Factors
 - 1x, 2x, 4x, and 8x
- ◆ Output Enable Pin
- ◆ Lock Indicator
- ◆ Minimal Board Space Required
 - No External Analog Loop-filter Components

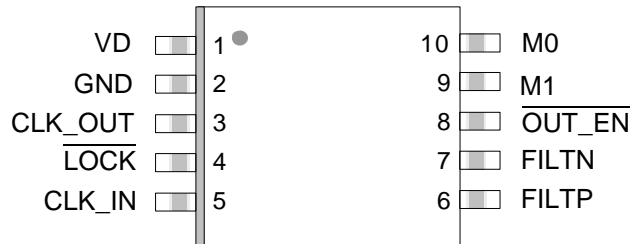
General Description

The CS2300-01 is an extremely versatile system clocking device that utilizes a programmable phase lock loop. The CS2300-01 is based on a hybrid analog-digital PLL architecture comprised of a unique combination of a Delta-Sigma Fractional-N Frequency Synthesizer and a Digital PLL. This architecture allows for generation of a low-jitter clock relative to an external noisy synchronization clock with frequencies as low as 750 kHz. The CS2300-01 is a CS2300-OTP device that has been pre-configured at the factory. There are three hardware configuration pins available for mode and feature selection.

Ordering Information

The CS2300-01 is available in a 10-pin MSOP package in Commercial (-10°C to +70°C) grade. Customer development kits are also available for custom device prototyping and device evaluation. Please see “[Ordering Information](#)” on page 2 for complete details.

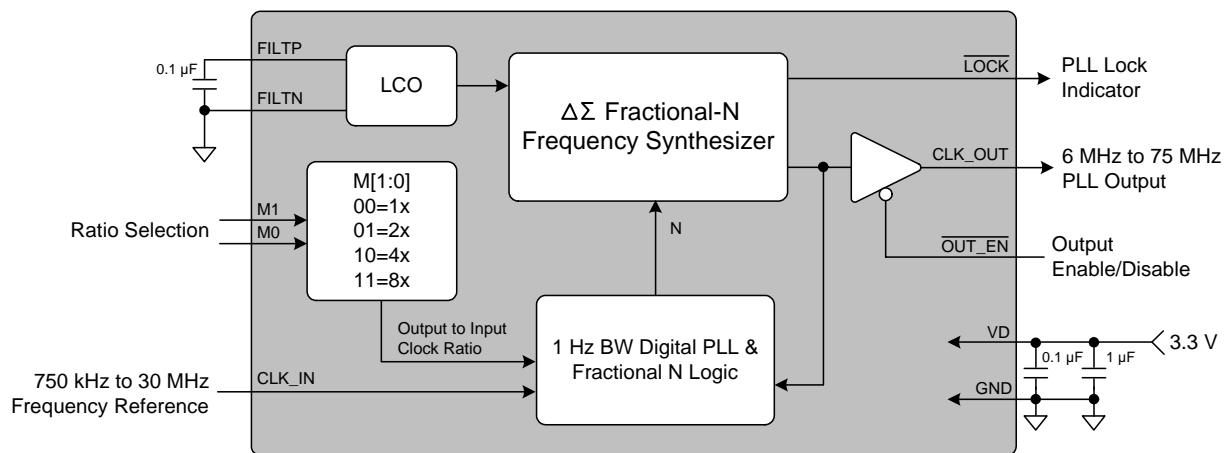
Pin-Out Diagram



Hardware Controls Settings

| M1 | M0 | PLL_OUT |
|----|----|-----------|
| 0 | 0 | 1x CLK_IN |
| 0 | 1 | 2x CLK_IN |
| 1 | 0 | 4x CLK_IN |
| 1 | 1 | 8x CLK_IN |

| OUT_EN | CLK_OUT |
|--------|----------------|
| 0 | Enabled |
| 1 | High Impedance |



1. PIN DESCRIPTIONS

| Pin Name | # | Pin Description |
|----------|----|---------------------------------|
| VD | 1 | Digital Power |
| GND | 2 | Ground |
| CLK_OUT | 3 | PLL Clock Output |
| LOCK | 4 | Active Low PLL Lock Indicator |
| CLK_IN | 5 | Clock Input |
| FILTP | 6 | LCO Filter Connections |
| FILT_N | 7 | |
| OUT_EN | 8 | Active Low CLK_OUT Enable Input |
| M1 | 9 | Mode Selection Inputs |
| M0 | 10 | |

See the CS2300-OTP datasheet for additional pin description information.

2. SPECIFICATIONS

Please see the CS2300-OTP datasheet for package information, device characteristics, and specifications except where noted due to specific programming options.

3. OPERATIONAL INFORMATION

Complete operational information can be found in the CS2300-OTP datasheet. Specific operational details dictated by the programming of the CS2300-01 are included below.

- The PLL clock output is forced to 0 when the PLL is unlocked, both upon loss of the CLK_IN signal or briefly when switching mode pin configurations.
- The minimum loop filter bandwidth once locked is 1 Hz.

4. CONFIGURATION INFORMATION

The CS2300-01 has been factory pre-programmed with a unique configuration. The following table outlines the specific configuration profile which can be compared to the CS2300-OTP datasheet for detailed functional descriptions.

| <i>OTP Modal and Global Configuration Parameters Form</i> | | | | | | |
|---|-------------|-------------|-------------|-------------|--------|--------|
| | Mode 0 | Mode 1 | Mode 2 | Mode 3 | | |
| Ratio 0 (dec) | 1 | 2 | 4 | 8 | | |
| Ratio 0 (hex) | 00:10:00:00 | 00:20:00:00 | 00:40:00:00 | 00:80:00:00 | | |
| RModSel1 | 0 | 0 | 0 | 0 | | |
| RModSel0 | 0 | 0 | 0 | 0 | | |
| AuxOutSrc1 | 1 | 1 | 1 | 1 | | |
| AuxOutSrc0 | 1 | 1 | 1 | 1 | | |
| AutoRMod | 0 | 0 | 0 | 0 | | |
| Global Configuration Set | | | | | | |
| ClkSkipEn | AuxLockCfg | ClkOutUnl | LFRatioCfg | M2Cfg2 | M2Cfg1 | M2Cfg0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| ClkIn_BW2 | ClkIn_BW1 | ClkIn_BW0 | | | | |
| 0 | 0 | 0 | | | | |

5. ORDERING INFORMATION

| Product | Description | Package | Pb-Free | Grade | Temp Range | Container | Order# |
|-----------|---------------------|----------|---------|------------|---------------|---------------|---------------|
| CS2300-01 | Clocking Device | 10L-MSOP | Yes | Commercial | -10° to +70°C | Rail | CS230001-CZZ |
| | | | | | | Tape and Reel | CS230001-CZZR |
| CDK-2000 | Evaluation Platform | - | Yes | - | - | - | CDK-2000-LCO |

6. REVISION HISTORY

| Release | Changes |
|---------|---|
| A1 | Initial Release |
| A2 | Corrected part number |
| A3 | Reduced page count and updated formatting |
| A4 | Updated formatting |

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