## Sound Processors for Home Theater Systems

## 7.1ch Sound Processor for High-Quality Audio with Built-in Micro-step Volume

## BD34704KS2

## General description

The BD34704KS2 is an 8ch independent volume system realized high-quality sound by improved specification of op-amp and optimized layout of the element.The system is designed to allow 7.1 ch surround system application. Micro-step volume can reduce the switching pop noise during volume attenuation, so a high quality audio system could be achieved.
This IC is available 12ch single-end input selectors to maximum 3 zones. And also available 2 system multi input selector.

## Features

- 12ch input selectors
(It is extendable to up to 18 in case of no use other functions such as Multi input, REC output and SUB output)
■ Micro-step volume can reduce the switching pop noise during volume attenuation
- Zone 3 is supported
- 2ch sub-volume for zone output that is available for independent control with a micro step function
- 2-wire serial bus control, corresponding to $3.3 / 5 \mathrm{~V}$


## Key Specifications

- Total harmonic distortion:
0.0004\%(Typ)
- Maximum output voltage:
4.2Vrms(Typ)

■ Output noise voltage:

- Residual output noise voltage:
$1.2 \mu \mathrm{Vrms}(\mathrm{Typ})$
$1.0 \mu \mathrm{Vrms}(\mathrm{Typ})$
-105dB(Typ)
-105dB(Typ)
Package
$W($ Typ $) \times D($ Typ $) \times H($ Max $)$
SQFP-T80C
$16.00 \mathrm{~mm} \times 16.00 \mathrm{~mm} \times 1.60 \mathrm{~mm}$


SQFP-T80C

## Applications

■ Suitable for the AV receivers, home theater systems, etc

## Typical Application Circuit



Figure 1. Application Circuit

## Pin Configuration



Figure 2. Pin Configuration

## Description of terminal

| Terminal Number | Symbol | Function | Terminal Number | Symbol | Function |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | DA | Data and latch input terminal | 41 | INR9(SBRIN2) | Rch input terminal 9 |
| 2 | CL | Clock input terminal | 42 | INL9(SBLIN2) | Lch input terminal 9 |
| 3 | VCC | Positive power supply terminal | 43 | INR8 | Rch input terminal 8 |
| 4 | DGND | Digital ground terminal | 44 | INL8 | Lch input terminal 8 |
| 5 | VEE1 | Negative power supply terminal 1 | 45 | INR7 | Rch input terminal 7 |
| 6 | N.C. | No connect | 46 | INL7 | Lch input terminal 7 |
| 7 | VEE2 | Negative power supply terminal 2 | 47 | INR6 | Rch input terminal 6 |
| 8 | OUTFL | FLch Output terminal | 48 | INL6 | Lch input terminal 6 |
| 9 | N.C. | No connect | 49 | INR5 | Rch input terminal 5 |
| 10 | OUTFR | FRch Output terminal | 50 | INL5 | Lch input terminal 5 |
| 11 | N.C. | No connect | 51 | INR4 | Rch input terminal 4 |
| 12 | OUTSW | SWch Output terminal | 52 | INL4 | Lch input terminal 4 |
| 13 | N.C. | No connect | 53 | INR3 | Rch input terminal 3 |
| 14 | OUTC | Cch Output terminal | 54 | INL3 | Lch input terminal 3 |
| 15 | OUTSL | SLch Output terminal | 55 | INR2 | Rch input terminal 2 |
| 16 | OUTSR | SRch Output terminal | 56 | INL2 | Lch input terminal 2 |
| 17 | OUTSBL | SBLch Output terminal | 57 | INR1 | Rch input terminal 1 |
| 18 | OUTSBR | SBRch Output terminal | 58 | INL1 | Lch input terminal 1 |
| 19 | OUTPL | Lch PRE Output terminal | 59 | GND | Analog ground terminal |
| 20 | OUTPR | Rch PRE Output terminal | 60 | SBRIN | SBRch DSP input terminal |
| 21 | GND | Analog ground terminal | 61 | SBLIN | SBLch DSP input terminal |
| 22 | GND | Analog ground terminal | 62 | SRIN | SRch DSP input terminal |
| 23 | GND | Analog ground terminal | 63 | SLIN | SLch DSP input terminal |
| 24 | GND | Analog ground terminal | 64 | CIN | Cch DSP input terminal |
| 25 | GND | Analog ground terminal | 65 | SWIN | SWch DSP input terminal |
| 26 | GND | Analog ground terminal | 66 | FRIN | FRch DSP input terminal |
| 27 | GND | Analog ground terminal | 67 | FLIN | FLch DSP input terminal |
| 28 | SUBR | Rch SUB Output terminal | 68 | FRIN3 | FRch DSP input terminal 3 |
| 29 | SUBL | Lch SUB Output terminal | 69 | FLIN3 | FLch DSP input terminal 3 |
| 30 | RECR | Rch REC Output terminal | 70 | GND | Analog ground terminal |
| 31 | RECL | Lch REC Output terminal | 71 | ADCR | Rch ADC Output terminal |
| 32 | GND | Analog ground terminal | 72 | ADCL | Lch ADC Output terminal |
| 33 | INR12(FRIN2) | Rch input terminal 12 | 73 | GND | Analog ground terminal |
| 34 | INL12(FLIN2) | Lch input terminal 12 | 74 | GND | Analog ground terminal |
| 35 | INR11(CIN2) | Rch input terminal 11 | 75 | GND | Analog ground terminal |
| 36 | INL11(SWIN2) | Lch input terminal 11 | 76 | GND | Analog ground terminal |
| 37 | INR10(SRIN) | Rch input terminal 10 | 77 | GND | Analog ground terminal |
| 38 | INL10(SLIN2) | Lch input terminal 10 | 78 | GND | Analog ground terminal |
| 39 | GND | Analog ground terminal | 79 | GND | Analog ground terminal |
| 40 | N.C. | No connect | 80 | CHIP | Chip select terminal |

## Block Diagram



Figure 3. Block Diagram

## Absolute Maximum Ratings

| Item | Symbol | Rating | Unit |
| :---: | :---: | :---: | :---: |
| Positive power supply | VCC | +7.75 (Note1) | V |
| Negative power supply | VEE | -7.75 (Note1) | V |
| Power dissipation | Pd | 1.75 (Note2) | W |
| Input voltage | Vin | VEE-0.2 ~ VCC+0.2 | V |
| Operating temperature | Topr | -40~+85 (Note3) | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature | Tastg | $-55 \sim+150$ | ${ }^{\circ} \mathrm{C}$ |

(Note1) The maximum voltage that can be applied based on GND.
(Note2) Derating at $14.0 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ for operating above $\mathrm{Ta} \geq 25^{\circ} \mathrm{C}$ (mounted on $70 \times 70 \times 1.6 \mathrm{~mm}$ ROHM standard board)
(Note3) If it is within the operating voltage range, circuit functions and operation are guaranteed within this operating temperature.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

## Operating Condition

| Item | Symbol | Rating | Unit |
| :--- | :---: | :---: | :---: |
| Positive power supply | VCC | $+6.5 \sim+7 . \mathbf{7}^{\text {(Note4,5) }}$ | V |
| Negative power supply | VEE | $-6.5 \sim-7$. (Note4,5) $^{\text {V }}$ |  |

(Note4) Applying voltage based on GND.
(Note5) Within the operating temperature range, basic circuit function and operation are guaranteed within this operation voltage range. But please confirm the setting of the constants, temperature, etc. Please take note that electrical characteristics other than defined values cannot be guaranteed, however original function will retain.

## Electrical characteristic

Unless otherwise specified, $\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{VCC}=7 \mathrm{~V}$, VEE $=-7 \mathrm{~V}, \mathrm{f}=1 \mathrm{kHz}$, Vin=1Vrms, RL=10k $\Omega$,
Stereo input selector(MAIN, SUB1, SUB2)=IN1, Mode selector(FL, FRch)=MAIN,
Mode selector(SW, C, SL, SRch)=MULTI, Mode selector(SBL, SBRch)=MULTI, SB OUTSEL=SB, Input $\mathrm{Att}=0 \mathrm{~dB}$, Input gain=0dB, Volume $=0 \mathrm{~dB}$.

|  | Item | Symbol | Limit |  |  | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| TOTAL | Positive circuit current | Iqp | - | 32 | 45 | mA | No signal |
|  | Negative circuit current | Iqn | -45 | -32 | - | mA | No signal |
|  | Output voltage gain | Gv | -1.5 | 0 | 1.5 | dB | 8, 10, 12, 14~18 pin output |
|  | Channel balance | CB | -0.5 | 0 | 0.5 | dB | C Channel reference, 8, 10, 12, 14~18 pin output |
|  | Total harmonic distortion <br> + Noise | THD | - | 0.0004 | 0.02 | \% | BW $=400 \sim 30 \mathrm{kHz}$ <br> 8, 10, 12, 14~18 pin output |
|  | Maximum output voltage | Vom | 3.8 | 4.2 | - | Vrms | $\begin{aligned} & \text { THD }=1 \%, \\ & \text { VOLUME }=+10 \mathrm{~dB} \\ & 8,10,12,14 \sim 18 \text { pin } \\ & \text { output } \\ & \hline \end{aligned}$ |
|  | Output noise voltage * | Vno | - | 1.2 | 10 | $\mu \mathrm{V}$ rms | $\mathrm{Rg}=0 \Omega$, $\mathrm{BW}=\mathrm{IHF}-\mathrm{A}$ 8, 10, 12, 14~18 pin output |
|  | Residual output noise voltage * | Vnor | - | 1 | 8 | $\mu \mathrm{Vrms}$ | ```Volume=Mute, Rg=0\Omega, BW=IHF-A 8, 10, 12, 14~18 pin output``` |
|  | Cross-talk between channels * | CT | - | -105 | -80 | dB | $\mathrm{Rg}=0 \Omega$, $\mathrm{BW}=\mathrm{IHF}-\mathrm{A}$ <br> 8, 10 pin output |
|  | Cross-talk between selectors * | CS | - | -105 | -80 | dB | $\mathrm{Rg}=0 \Omega$, $\mathrm{BW}=\mathrm{IHF}-\mathrm{A}$ 8, 10, 12, 14~18 pin output |
|  | Input impedance | Rin | 70 | 100 | 130 | k $\Omega$ | $\begin{aligned} & 28 \sim 31,33 \sim 38,41 \sim 58 \\ & 60 \sim 69 \text { pin input } \\ & \hline \end{aligned}$ |
| VOLUME | Maximum attenuation * | ATTmax | - | -115 | -100 | dB | Volume=Mute, BW=IHF-A |
| REC OUT | Total harmonic distortion | THDR | - | 0.0005 | 0.02 | \% | $\begin{aligned} & \mathrm{BW}=400 \sim 30 \mathrm{kHz}, \\ & \mathrm{RL}=6.8 \mathrm{k} \Omega \\ & 28 \sim 31 \text { pin output } \end{aligned}$ |
| PRE OUT | Output impedance | Ron | 520 | 800 | 1080 | $\Omega$ | 19, 20 pin output |

※VP-9690(Average value detection, effective value display) filter by Panasonic is used for * measurement.

## Typical Performance Curve(s)



Figure 4. Circuit Currents vs. Circuit Voltage


Figure 6. Volume Gain vs. Input Frequency (0dB to -32 dB setting)


Figure 5. Volume Gain vs. Input Frequency (32dB to 0 dB setting)


Figure 7. Volume Gain vs. Input Frequency (-32dB to -64 dB setting)


Figure 8. Volume Gain vs. Input Frequency (-64dB to -95 dB setting)


Figure 9. THD + N vs. Input Voltage
(Note) The measurement results of Figure 4 to Figure 8 used by 80 kHz LPF.

## Specifications for Control Signal

(4) Timing of control signal

Data is read at the rising edge of clock.
Latch is read at the falling edge of clock. Data on the latest 16bit is taken inside the IC.
Ensure to set DA and CL to LOW after Latch.
1 byte $=16$ bit


Figure 10. The timing definition of the control signal

| Item | Symbol | Limit |  |  | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Clock width | twc | 1.0 | - | - | $\mu \mathrm{sec}$ |
| Data width | twd | 1.0 | - | - | $\mu \mathrm{sec}$ |
| Latch width | twl | 1.0 | - | - | $\mu \mathrm{sec}$ |
| Low hold width | twh | 1.0 | - | - | $\mu \mathrm{sec}$ |
| Data setup time (DATA $\rightarrow$ CLK) | tsd | 0.5 | - | - | $\mu \mathrm{sec}$ |
| Data hold time (CLK $\rightarrow$ DATA) | thd | 0.5 | - | - | $\mu \mathrm{sec}$ |
| Latch setup time (CLK $\rightarrow$ LATCH) | tsl | 0.5 | - | - | $\mu \mathrm{sec}$ |
| Latch hold time (DATA $\rightarrow$ LATCH) | thl | 0.5 | - | - | $\mu \mathrm{sec}$ |
| Latch Low setup time | ts | 0.5 | - | - | $\mu \mathrm{sec}$ |
| Latch Low hold time | th | 0.5 | - | - | $\mu \mathrm{sec}$ |

(2) Voltage of control signal (CL, DA, CHIP)

| Item | Conditions | Limit |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | $\begin{gathered} \operatorname{Max} \\ (<\mathrm{VCC}) \end{gathered}$ |  |
| High input voltage | $\begin{aligned} & \text { VCC }=+6.5 \text { to }+7.5 \mathrm{~V} \\ & \text { VEE }=-6.5 \text { to }-7.5 \mathrm{~V} \end{aligned}$ | 2.3 | - | 5.5 | V |
| Low input voltage |  | 0 | - | 1.0 | V |

(3) Basic Structure of Control Data
$\leftarrow$ Input Direction

|  | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Data ${ }^{\text {a }}$ Select Addre |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

(4) Table of Control Data

| Select Address No. | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | Input Selector (MAIN) |  |  |  |  |  | $\begin{gathered} \text { REC } \\ \text { ON/OFF } \end{gathered}$ | 0 | 0 | $\begin{aligned} & \text { SUB } \\ & \text { ON/OFF } \end{aligned}$ | 1 | 0 | 0 | Chip <br> Select | 0 | 0 |
| 1 | Input Selector (SUB1) |  |  |  |  |  | 0 | Input Selector (SUB2) |  |  |  |  | 0 |  | 0 | 1 |
| 2 | Mode Select FL, FRch |  | Mode Select C, SWch |  | Mode Select SL, SRch |  | Mode Select SBL, SBRch |  | 0 | ADC ATT |  |  | 0 |  | 1 | 0 |
| 3 | Volume channel Select |  |  | Volume + *Sub Volume |  |  |  |  |  |  |  |  | 0 |  | 1 | 1 |
| 4 | PREOU | T SEL | MSEL FRONT | $\begin{aligned} & \text { MSEL } \\ & \text { C,SWW } \end{aligned}$ | MSEL SUR | MSEL SURB | $\begin{gathered} \text { SB } \\ \text { OUTSEL } \end{gathered}$ | $\begin{aligned} & \text { SUB } \\ & \text { MUTE } \end{aligned}$ | 0 | 0 | 0 | Volume Select2 | 1 |  | 0 | 0 |
| 6 | Mode $R E$ | Select | $\begin{array}{r} \text { Mode } \\ \text { SU } \end{array}$ | Select <br> B | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  | 1 | 0 |
| 7 |  | $A \rightarrow B$ <br> itch-ti |  |  | $\underset{\text { vitch-tir }}{\mathrm{B} \rightarrow \mathrm{~A}}$ |  | $\begin{aligned} & \text { Base } \\ & \text { Clock } \end{aligned}$ | 0 | 0 | System | 0 | 0 | 1 |  | 1 | 1 |
| BD3843FS (6ch Selector IC) |  |  |  |  |  |  |  |  |  |  |  |  | * | 1 | 0 | 0 |
| BD3841FS (9ch Selector IC) |  |  |  |  |  |  |  |  |  |  |  |  | * | 1 | 0 | 1 |
| BD3812F (2ch volume IC) |  |  |  |  |  |  |  |  |  |  |  |  | * | 1 | 1 | * |

- Serial control lines can be shared with BD3471KS2, BD3473KS2 and BD3474KS2.
(In case using the serial bus commonly, please set chip select in "1")
- Serial control lines can be shared with BD3843FS(6ch selector IC), BD3841FS(9ch selector IC) and BD3812F(2chvolume IC).
- Initialize all data at every turning on the power supply.
※The Sub Volume is available by L/Rch independence and 0.5 dB step.
The Sub volume attenuation is set by address No.3. (A combination of "Volume select2" and "Volume channel select" , please determine the volume setting channel)
(例)

- At the second time after turning on the power supply, eight any data to be changed.
(5) Chip Select Setting Table

| CHIP terminal condition | D2 |
| :---: | :---: |
| 0 (LOW) | 0 |
| 1 (HIGH) | 1 |

BD34704KS2 can be operated in combination with another by setting the CHP terminal.

Select Address No. 0 Setting Table

| Fun | ion \& Setting | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MUTE | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |
|  | IN1 |  | 0 | 0 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |
|  | IN2 |  | 0 | 0 | 0 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |
|  | IN3 |  | 0 | 0 | 0 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |
|  | IN4 |  | 0 | 0 | 1 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |
|  | IN5 |  | 0 | 0 | 1 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |
|  | IN6 |  | 0 | 0 | 1 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |
|  | IN7 |  | 0 | 0 | 1 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |
|  | IN8 |  | 0 | 1 | 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |
|  | IN9 |  | 0 | 1 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |
|  | IN10 |  | 0 | 1 | 0 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |
|  | IN11 |  | 0 | 1 | 0 | 1 | 1 | $\underset{\text { Rec }}{\text { Reff }}$ |  |  |  |  |  |  |  |  |  |
|  | IN12 |  | 0 | 1 | 1 | 0 | 0 |  |  |  | Sub |  |  |  |  |  |  |
|  | IN13 |  | 0 | 1 | 1 | 0 | 1 |  |  |  | on/off |  |  |  |  |  |  |
|  | IN14 |  | 0 | 1 | 1 | 1 | 0 |  | 0 | 0 |  | 1 | 0 | 0 | $\begin{gathered} \text { Chip } \\ \text { Select } \end{gathered}$ | 0 | 0 |
|  | IN15 |  | 0 | 1 | 1 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |
|  | IN16 |  | 1 | 0 | 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |
|  | IN17(REC) |  | 1 | 0 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |
|  | IN18(SUB) |  | 1 | 0 | 0 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |
|  |  |  | 1 | 0 | 0 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |
|  | Prohibition |  | : | : | : | : | ! |  |  |  |  |  |  |  |  |  |  |
|  |  |  | 1 | 1 | 1 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |
| ○ 殅 | OFF |  | Input Selector (MAIN) |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |
| ${ }^{\Upsilon}$ | ON |  |  |  |  |  |  | 1 |  |  |  |  |  |  |  |  |  |
|  | OFF |  |  |  |  |  |  | Rec on/off |  |  | 0 |  |  |  |  |  |  |
|  | ON |  |  |  |  |  |  |  |  | 1 |  |  |  |  |  |  |

Select Address No. 1 Setting Table


Select Address No. 2 Setting Table ※Select Address No. 4 MSEL="0"(Front,C,SW,SR,SRB)

| Function \& Setting |  | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MUTE | 0 | 0 | Mode Selector C, SWch |  | Mode Selector SL, SRch |  | Mode Selector SBL, SBRch |  | 0 | ADC ATT |  |  | 0 | Chip Select | 1 | 0 |
|  | MAIN | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MULTI1 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SUB1 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MUTE | Mode Selector FL, FRch |  | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MAIN |  |  | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MULTI1 |  |  | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SUB1 |  |  | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MUTE |  |  | Mode Selector C, SWch |  | 0 | 0 |  |  |  |  |  |  |  |  |  |  |
| $\bigcirc$ | MAIN |  |  | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MULTI1 |  |  | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SUB1 |  |  | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MUTE |  |  | Mode Selector SL, SRch |  | 0 | 0 |  |  |  |  |  |  |  |  |  |  |
|  | MULTI1 |  |  | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SUB1 |  |  | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MAIN |  |  | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |

$\square$ : Initial condition
Select Address No. 2 Setting Table ※Select Address No. 4 MSEL="1"(Front,C,SW,SR,SRB)

| Function \& Setting |  | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MUTE | 0 | 0 | Mode Selector C, SWch |  | Mode Selector SL, SRch |  | Mode Selector SBL, SBRch |  | 0 | ADC ATT |  |  | 0 | Chip Select | 1 | 0 |
|  | SUB2 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MULTI2 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MULTI3 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MUTE | Mode Selector FL, FRch |  | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SUB2 |  |  | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MULTI2 |  |  | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | Prohibition |  |  | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MUTE |  |  | Mode Selector C, SWch |  | 0 | 0 |  |  |  |  |  |  |  |  |  |  |
| \% 능응 | SUB2 |  |  | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |
| $\stackrel{\text { ¢ }}{\text { ¢ }}$ | MULTI2 |  |  | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | Prohibition |  |  | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MUTE |  |  | Mode Selector SL, SRch |  | 0 | 0 |  |  |  |  |  |  |  |  |  |  |
|  | SUB2 |  |  | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MULTI2 |  |  | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | Prohibition |  |  | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |

Select Address No. 2 Setting Table

| Function \& Setting |  | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $$ | MUTE | Mode Selector FL, FRch |  | Mode Selector C, SWch |  | Mode Selector SL, SRch |  | Mode Selector SBL, SBRch |  | 0 | 0 | 0 | 0 | 0 | Chip Select | 1 | 0 |
|  | OdB |  |  | 0 | 0 |  |  | 1 |  |  |  |  |  |
|  | -6dB |  |  | 0 | 1 |  |  | 0 |  |  |  |  |  |
|  | -6.5dB |  |  | 0 | 1 |  |  | 1 |  |  |  |  |  |
|  | -7.5dB |  |  | 1 | 0 |  |  | 0 |  |  |  |  |  |
|  | -9dB |  |  | 1 | 0 |  |  | 1 |  |  |  |  |  |
|  | -12dB |  |  | 1 | 1 |  |  | 0 |  |  |  |  |  |
|  | Prohibition |  |  | 1 | 1 |  |  | 1 |  |  |  |  |  |

Select Address No. 3 Setting Table

| Function \& Setting |  | Volume Select2 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | FR | 0 | 0 | 0 | 0 | Volume |  |  |  |  |  |  |  |  | 0 | Chip Select | 1 | 1 |
|  | FL | 0 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SW | 0 | 0 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | C | 0 | 0 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SR | 0 | 1 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SL | 0 | 1 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SBR | 0 | 1 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SBL | 0 | 1 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SUBR | 1 | 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SUBL | 1 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | 1 | 0 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | 1 | 0 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | Prohibition | 1 | 1 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | Prohibition | 1 | 1 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | 1 | 1 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | 1 | 1 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |

※Volume Select2 is available setting by Select Address No. 4

## (Note) Considerations in the volume data transmission

※Setting range of $F R, F L, S W, C E N, S R, S L, S B R$ and $S B L$ is $+32 d B$ to $-95 d B$.
※Setting range of SUBR and SUBL is +7.5 dB to -91.5 dB .
※The data transmission to NOT assigned place in data format is prohibition.
Setting table of dynamic range of 7.1ch and Sub Volume

|  | FR | FL | SW | C | SR | SL | SBR | SBL | SUBR | SUBL |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MAX | +32 | +32 | +32 | +32 | +32 | +32 | +32 | +32 | MUTE | MUTE |
| MAXS | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | +7.5 | +7.5 |
|  | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ |
| MINS | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | $:$ | -91.5 | -91.5 |
| MIN | -95 | -95 | -95 | -95 | -95 | -95 | -95 | -95 | MUTE | MUTE |

MAX : maximum value of 7.1 ch Volume MAXS : maximum value of Sub Volume MIN : minimum value of 7.1 ch Volume MINS : minimum value of Sub Volume

Select Address No. 3 Setting Table

| Function \& Setting |  | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MUTE | Volume Channel Select |  |  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | Chip Select | 1 | 1 |
| $\begin{aligned} & \text { © } \\ & \frac{1}{\bar{O}} \\ & \hline \end{aligned}$ |  |  |  |  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | Prohibition |  |  |  | . | : | : | : |  |  |  | : |  |  |  |  |
|  |  |  |  |  | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | +32.0dB |  |  |  | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | +31.5dB |  |  |  | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  |  |  |  |
|  | +31.0dB |  |  |  | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | +30.5dB |  |  |  | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |  |  |  |  |
|  | +30.0dB |  |  |  | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |  |  |  |  |
|  | +29.5dB |  |  |  | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |  |  |  |  |
|  | +29.0dB |  |  |  | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |  |  |  |  |
|  | +28.5dB |  |  |  | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |  |  |  |  |
|  | +28.0dB |  |  |  | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |  |  |  |  |
|  | +27.5dB |  |  |  | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |  |  |  |  |
|  | +27.0dB |  |  |  | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |  |  |  |  |
|  | +26.5dB |  |  |  | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |  |  |  |  |
|  | +26.0dB |  |  |  | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |  |  |  |  |
|  | +25.5dB |  |  |  | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |  |  |  |  |
|  | +25.0dB |  |  |  | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |  |  |  |  |
|  | +24.5dB |  |  |  | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | +24.0dB |  |  |  | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | +23.5dB |  |  |  | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |  |  |  |  |
|  | +23.0dB |  |  |  | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | +22.5dB |  |  |  | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |  |  |  |  |
|  | +22.0dB |  |  |  | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |  |  |  |  |

Select Address No. 3 Setting Table

| Fun | \& Setting | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \otimes \\ & \stackrel{0}{5} \\ & \stackrel{亏}{0} \end{aligned}$ | +21.5dB | Volume Channel Select |  |  | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | Chip Select | 1 |  |
|  | +21.0dB |  |  |  | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |  |  |  |  |
|  | +20.5dB |  |  |  | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |  |  |  |  |
|  | +20.0dB |  |  |  | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |  |  |  |  |
|  | +19.5dB |  |  |  | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |  |  |  |  |
|  | +19.0dB |  |  |  | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |  |  |  |  |
|  | +18.5dB |  |  |  | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |  |  |  |  |
|  | +18.0dB |  |  |  | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |  |  |  |  |
|  | +17.5dB |  |  |  | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |  |  |  |  |
|  | +17.0dB |  |  |  | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |  |  |  |  |
|  | +16.5dB |  |  |  | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | +16.0dB |  |  |  | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | +15.5dB |  |  |  | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |  |  |  |  |
|  | +15.0dB |  |  |  | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | +14.5dB |  |  |  | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |  |  |  |  |
|  | +14.0dB |  |  |  | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |  |  |  |  |
|  | +13.5dB |  |  |  | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |  |  |  |  |
|  | +13.0dB |  |  |  | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |  |  |  |  |
|  | +12.5dB |  |  |  | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |  |  |  |  |
|  | +12.0dB |  |  |  | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |  |  |  |  |
|  | +11.5dB |  |  |  | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |  |  |  |  |
|  | +11.0dB |  |  |  | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |  |  |  |  |
|  | +10.5dB |  |  |  | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |  |  |  |  |
|  | +10.0dB |  |  |  | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |  |  |  |
|  | +9.5dB |  |  |  | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |  |  |  |  |
|  | +9.0dB |  |  |  | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |  |  |  |  |
|  | $+8.5 \mathrm{~dB}$ |  |  |  | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | +8.0dB |  |  |  | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | +7.5dB |  |  |  | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |  |  |  |  |
|  | +7.0dB |  |  |  | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | $+6.5 \mathrm{~dB}$ |  |  |  | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |  |  |  |  |
|  | +6.0dB |  |  |  | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |  |  |  |  |
|  | $+5.5 \mathrm{~dB}$ |  |  |  | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |  |  |  |  |
|  | $+5.0 \mathrm{~dB}$ |  |  |  | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |  |  |  |  |
|  | $+4.5 \mathrm{~dB}$ |  |  |  | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |  |  |  |  |
|  | +4.0dB |  |  |  | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |  |  |  |  |
|  | $+3.5 \mathrm{~dB}$ |  |  |  | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |  |  |  |  |
|  | +3.0dB |  |  |  | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |  |  |  |  |
|  | $+2.5 \mathrm{~dB}$ |  |  |  | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |  |  |  |  |
|  | +2.0dB |  |  |  | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |  |  |  |  |
|  | +1.5dB |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |  |  |  |  |
|  | +1.0dB |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |  |  |  |  |
|  | $+0.5 \mathrm{~dB}$ |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | Prohibition |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | -0dB |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | -0.5dB |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | -1.0dB |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |  |  |  |  |
|  | -1.5dB |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |  |  |  |  |

Select Address No. 3 Setting Table

| Fun | \& Setting | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \mathbb{\otimes} \\ & \frac{1}{\bar{O}} \\ & \hline \end{aligned}$ | -2.0dB | Volume Channel Select |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Chip Select | 1 | (100 |
|  | -2.5dB |  |  |  | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |  |  |  |  |
|  | -3.0dB |  |  |  | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |  |  |  |  |
|  | -3.5dB |  |  |  | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |  |  |  |  |
|  | -4.0dB |  |  |  | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |  |  |  |  |
|  | -4.5dB |  |  |  | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |  |  |  |  |
|  | -5.0dB |  |  |  | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |  |  |  |  |
|  | -5.5dB |  |  |  | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |  |  |  |  |
|  | -6.0dB |  |  |  | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |  |  |  |  |
|  | -6.5dB |  |  |  | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |  |  |  |  |
|  | -7.0dB |  |  |  | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | -7.5dB |  |  |  | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |  |  |  |  |
|  | -8.0dB |  |  |  | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | -8.5dB |  |  |  | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | -9.0dB |  |  |  | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |  |  |  |  |
|  | -9.5dB |  |  |  | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |  |  |  |  |
|  | -10.0dB |  |  |  | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |  |  |  |  |
|  | -10.5dB |  |  |  | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |  |  |  |  |
|  | -11.0dB |  |  |  | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |  |  |  |  |
|  | -11.5dB |  |  |  | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |  |  |  |  |
|  | -12.0dB |  |  |  | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |  |  |  |  |
|  | -12.5dB |  |  |  | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |  |  |  |  |
|  | -13.0dB |  |  |  | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |  |  |  |  |
|  | -13.5dB |  |  |  | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |  |  |  |  |
|  | -14.0dB |  |  |  | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |  |  |  |  |
|  | -14.5dB |  |  |  | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |  |  |  |  |
|  | -15.0dB |  |  |  | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | -15.5dB |  |  |  | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |  |  |  |  |
|  | -16.0dB |  |  |  | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | -16.5dB |  |  |  | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | -17.0dB |  |  |  | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |  |  |  |  |
|  | -17.5dB |  |  |  | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |  |  |  |  |
|  | -18.0dB |  |  |  | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |  |  |  |  |
|  | -18.5dB |  |  |  | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |  |  |  |  |
|  | -19.0dB |  |  |  | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |  |  |  |  |
|  | -19.5dB |  |  |  | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |  |  |  |  |
|  | -20.0dB |  |  |  | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |  |  |  |  |
|  | -20.5dB |  |  |  | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |  |  |  |  |
|  | -21.0dB |  |  |  | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |  |  |  |  |
|  | -21.5dB |  |  |  | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |  |  |  |  |
|  | -22.0dB |  |  |  | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |  |  |  |  |
|  | -22.5dB |  |  |  | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |  |  |  |  |
|  | -23.0dB |  |  |  | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | -23.5dB |  |  |  | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |  |  |  |  |
|  | -24.0dB |  |  |  | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | -24.5dB |  |  |  | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | -25.0dB |  |  |  | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |  |  |  |  |
|  | -25.5dB |  |  |  | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |  |  |  |  |

Select Address No. 3 Setting Table

| Fun | \& Setting | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & 0 \\ & \stackrel{0}{5} \\ & \stackrel{\rightharpoonup}{0} \end{aligned}$ | -26.0dB | Volume Channel Select |  |  | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | Chip Select | 1 | 1 |
|  | -26.5dB |  |  |  | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |  |  |  |  |
|  | -27.0dB |  |  |  | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |  |  |  |  |
|  | -27.5dB |  |  |  | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |  |  |  |  |
|  | -28.0dB |  |  |  | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |  |  |  |  |
|  | -28.5dB |  |  |  | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |  |  |  |  |
|  | -29.0dB |  |  |  | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |  |  |  |  |
|  | -29.5dB |  |  |  | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |  |  |  |  |
|  | -30.0dB |  |  |  | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |  |  |  |  |
|  | -30.5dB |  |  |  | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |  |  |  |  |
|  | -31.0dB |  |  |  | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | -31.5dB |  |  |  | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  |  |  |  |
|  | -32.0dB |  |  |  | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | -32.5dB |  |  |  | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | -33.0dB |  |  |  | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |  |  |  |  |
|  | -33.5dB |  |  |  | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |  |  |  |  |
|  | -34.0dB |  |  |  | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |  |  |  |  |
|  | -34.5dB |  |  |  | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |  |  |  |  |
|  | -35.0dB |  |  |  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |  |  |  |  |
|  | -35.5dB |  |  |  | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |  |  |  |  |
|  | -36.0dB |  |  |  | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |  |  |  |  |
|  | -36.5dB |  |  |  | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |  |  |  |  |
|  | -37.0dB |  |  |  | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |  |  |  |  |
|  | -37.5dB |  |  |  | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |  |  |  |  |
|  | -38.0dB |  |  |  | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |  |  |  |  |
|  | -38.5dB |  |  |  | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |  |  |  |  |
|  | -39.0dB |  |  |  | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | -39.5dB |  |  |  | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |  |  |  |  |
|  | -40.0dB |  |  |  | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | -40.5dB |  |  |  | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | -41.0dB |  |  |  | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |  |  |  |  |
|  | -41.5dB |  |  |  | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |  |  |  |  |
|  | -42.0dB |  |  |  | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |  |  |  |  |
|  | -42.5dB |  |  |  | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |  |  |  |  |
|  | -43.0dB |  |  |  | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |  |  |  |  |
|  | -43.5dB |  |  |  | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |  |  |  |  |
|  | -44.0dB |  |  |  | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |  |  |  |  |
|  | -44.5dB |  |  |  | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |  |  |  |  |
|  | -45.0dB |  |  |  | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |  |  |  |  |
|  | -45.5dB |  |  |  | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |  |  |  |  |
|  | -46.0dB |  |  |  | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |  |  |  |  |
|  | -46.5dB |  |  |  | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |  |  |  |  |
|  | -47.0dB |  |  |  | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | -47.5dB |  |  |  | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |  |  |  |  |
|  | -48.0dB |  |  |  | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | -48.5dB |  |  |  | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | -49.0dB |  |  |  | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |  |  |  |  |
|  | -49.5dB |  |  |  | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |  |  |  |  |

Select Address No. 3 Setting Table

| Function \& Setting |  | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & 0 \\ & \stackrel{0}{5} \\ & \stackrel{\rightharpoonup}{0} \end{aligned}$ | -50.0dB | Volume Channel Select |  |  | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | Chip Select | 1 | 1 |
|  | -50.5dB |  |  |  | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |  |  |  |  |
|  | -51.0dB |  |  |  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |  |  |  |  |
|  | -51.5dB |  |  |  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |  |  |  |  |
|  | -52.0dB |  |  |  | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |  |  |  |  |
|  | -52.5dB |  |  |  | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |  |  |  |  |
|  | -53.0dB |  |  |  | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |  |  |  |  |
|  | -53.5dB |  |  |  | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |  |  |  |  |
|  | -54.0dB |  |  |  | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |  |  |  |  |
|  | -54.5dB |  |  |  | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |  |  |  |  |
|  | -55.0dB |  |  |  | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | -55.5dB |  |  |  | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |  |  |  |  |
|  | -56.0dB |  |  |  | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | -56.5dB |  |  |  | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | -57.0dB |  |  |  | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |  |  |  |  |
|  | -57.5dB |  |  |  | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |  |  |  |  |
|  | -58.0dB |  |  |  | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |  |  |  |  |
|  | -58.5dB |  |  |  | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |  |  |  |  |
|  | -59.0dB |  |  |  | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |  |  |  |  |
|  | -59.5dB |  |  |  | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |  |  |  |  |
|  | -60.0dB |  |  |  | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |  |  |  |  |
|  | -60.5dB |  |  |  | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |  |  |  |  |
|  | -61.0dB |  |  |  | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |  |  |  |  |
|  | -61.5dB |  |  |  | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |  |  |  |  |
|  | -62.0dB |  |  |  | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |  |  |  |  |
|  | -62.5dB |  |  |  | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |  |  |  |  |
|  | -63.0dB |  |  |  | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | -63.5dB |  |  |  | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |  |  |  |
|  | -64.0dB |  |  |  | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | -64.5dB |  |  |  | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | -65.0dB |  |  |  | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |  |  |  |  |
|  | -65.5dB |  |  |  | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |  |  |  |  |
|  | -66.0dB |  |  |  | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |  |  |  |  |
|  | -66.5dB |  |  |  | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |  |  |  |  |
|  | -67.0dB |  |  |  | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |  |  |  |  |
|  | -67.5dB |  |  |  | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |  |  |  |  |
|  | -68.0dB |  |  |  | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |  |  |  |  |
|  | -68.5dB |  |  |  | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |  |  |  |  |
|  | -69.0dB |  |  |  | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |  |  |  |  |
|  | -69.5dB |  |  |  | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |  |  |  |  |
|  | -70.0dB |  |  |  | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |  |  |  |  |
|  | -70.5dB |  |  |  | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |  |  |  |  |
|  | -71.0dB |  |  |  | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | -71.5dB |  |  |  | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |  |  |  |  |
|  | -72.0dB |  |  |  | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | -72.5dB |  |  |  | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | -73.0dB |  |  |  | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |  |  |  |  |
|  | -73.5dB |  |  |  | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |  |  |  |  |

Select Address No. 3 Setting Table

| Fun | n \& Setting | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & 0 \\ & \frac{1}{\bar{O}} \\ & \hline \end{aligned}$ | -74.0dB | Volume Channel Select |  |  | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | Chip Select | 1 | 1 |
|  | -74.5dB |  |  |  | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |  |  |  |  |
|  | -75.0dB |  |  |  | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |  |  |  |  |
|  | -75.5dB |  |  |  | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |  |  |  |  |
|  | -76.0dB |  |  |  | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |  |  |  |  |
|  | -76.5dB |  |  |  | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |  |  |  |  |
|  | -77.0dB |  |  |  | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |  |  |  |  |
|  | -77.5dB |  |  |  | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |  |  |  |  |
|  | -78.0dB |  |  |  | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |  |  |  |  |
|  | -78.5dB |  |  |  | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |  |  |  |  |
|  | -79.0dB |  |  |  | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | -79.5dB |  |  |  | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |  |  |  |  |
|  | -80.0dB |  |  |  | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | -80.5dB |  |  |  | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | -81.0dB |  |  |  | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |  |  |  |  |
|  | -81.5dB |  |  |  | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |  |  |  |  |
|  | -82.0dB |  |  |  | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |  |  |  |  |
|  | -82.5dB |  |  |  | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |  |  |  |  |
|  | -83.0dB |  |  |  | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |  |  |  |  |
|  | -83.5dB |  |  |  | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |  |  |  |  |
|  | -84.0dB |  |  |  | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |  |  |  |  |
|  | -84.5dB |  |  |  | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |  |  |  |  |
|  | -85.0dB |  |  |  | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |  |  |  |  |
|  | -85.5dB |  |  |  | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |  |  |  |  |
|  | -86.0dB |  |  |  | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |  |  |  |  |
|  | -86.5dB |  |  |  | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |  |  |  |  |
|  | -87.0dB |  |  |  | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | -87.5dB |  |  |  | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |  |  |  |  |
|  | -88.0dB |  |  |  | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |  |  |  |  |
|  | -88.5dB |  |  |  | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |  |  |  |  |
|  | -89.0dB |  |  |  | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |  |  |  |  |
|  | -89.5dB |  |  |  | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |  |  |  |  |
|  | -90.0dB |  |  |  | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |  |  |  |  |
|  | -90.5dB |  |  |  | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |  |  |  |  |
|  | -91.0dB |  |  |  | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |  |  |  |  |
|  | -91.5dB |  |  |  | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |  |  |  |  |
|  | -92.0dB |  |  |  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |  |  |  |  |
|  | -92.5dB |  |  |  | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |  |  |  |  |
|  | -93.0dB |  |  |  | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |  |  |  |  |
|  | -93.5dB |  |  |  | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |  |  |  |  |
|  | -94.0dB |  |  |  | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |  |  |  |  |
|  | -94.5dB |  |  |  | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |  |  |  |  |
|  | -95.0dB |  |  |  | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |  |  |  |  |
|  | Prohibition |  |  |  | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |  |  |  |  |
|  |  |  |  |  | : | $\vdots$ | : | : | : | : | : | : |  |  |  |  |
|  |  |  |  |  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |  |  |  |

Select Address No． 4 Setting Table ※ON／OFF of each MSEL is reflected by a mode selector of Address No． 2

| Function \＆Setting |  | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MUTE | 0 | 0 | MSELFRONT | MSEL <br> C．，SW | MSEL | MSELSURB | $\begin{gathered} \text { SB } \\ \text { Select } \end{gathered}$ | $\begin{gathered} \text { SUB } \\ \text { MUTE } \end{gathered}$ | 0 | 0 | 0 | Volume Select2 | 1 | $\begin{aligned} & \text { Chip } \\ & \text { Select } \end{aligned}$ | 0 |  |
|  | FRONT | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SURB | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | OPEN | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 爫 | OFF | $\underset{\text { SEL }}{\substack{\text { PREOUT }}}$ |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $\sum$ | ON |  |  | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 山 3 | OFF |  |  | MSEL FRONT | 0 |  |  |  |  |  |  |  |  |  |  |  |  |
| $\sum_{\sum 0}^{\infty}$ | ON |  |  | 1 |  |  |  |  |  |  |  |  |  |  |  |  |
| 岗 | OFF |  |  | MSEL c，sw | 0 | 0 |  |  |  |  |  |  |  |  |  |  |
| ミ ¢ | ON |  |  | 1 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | OFF |  |  | $\begin{aligned} & \text { MSEL } \\ & \text { SUR } \end{aligned}$ | 0 |  |  |  |  |  |  |  |  |  |  |  |
| ミ ら | ON |  |  | 1 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SURB |  |  | $\begin{aligned} & \text { MSEL } \\ & \text { SURB } \end{aligned}$ | 0 |  |  |  |  |  |  |  |  |  |  |  |
| の | FRONT |  |  | 1 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MUTE OFF |  |  | $\begin{gathered} \text { SB } \\ \text { Select } \end{gathered}$ | 0 |  |  |  |  |  |  |  |  |  |  |  |
| のさ | MUTE ON |  |  | 1 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | OFF |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |
|  | ON |  |  | mUTE | 1 |  |  |  |  |  |  |  |  |  |  |  |

Select Address No． 6 Setting Table

| Function \＆Setting |  | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MAIN | 0 | 0 | Mode Selector SUB |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Chip Select | 1 | 0 |
|  | SUB1 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SUB2 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MULTI | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MAIN | Mode Selector REC |  | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SUB1 |  |  | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | SUB2 |  |  | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | MULTI |  |  | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |

Select Address No. 7 setting table

| Function \& Setting |  | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 11.2 msec | 0 | 0 | 0 | $\mathrm{B} \rightarrow \mathrm{~A}$ <br> switching-time |  |  | Base Clock | 0 | 0 | System Reset | 0 | 0 | 1 | Chip Select | 1 | 1 |
|  | 4.7 msec | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 7.2 msec | 0 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 14.4 msec | 0 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 3.2 msec | 1 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 2.3 msec | 1 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | Prohibition | 1 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | 1 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 11.2 msec | $A \rightarrow B$ <br> switching-time |  |  | 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |
|  | 4.7 msec |  |  |  | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |
|  | 7.2 msec |  |  |  | 0 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |
|  | 14.4 msec |  |  |  | 0 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |
|  | 3.2 msec |  |  |  | 1 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |
|  | 2.3 msec |  |  |  | 1 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |
|  | Prohibition |  |  |  | 1 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |
|  | Prohibition |  |  |  | 1 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |
|  | x1 |  |  |  | $\mathrm{B} \rightarrow \mathrm{~A}$ <br> switching-time |  |  | 0 |  |  |  |  |  |  |  |  |  |
| 0 | $\times 1 / 2$ |  |  |  | 1 |  |  |  |  |  |  |  |  |  |  |
|  | Normal |  |  |  | Base Clock | 0 |  |  |  |  |  |  |  |  |  |  |
|  | Reset |  |  |  | 1 |  |  |  |  |  |  |  |  |  |  |

Select Address No.7, Data = D15-D13 : Below A $\rightarrow \mathrm{B}$ switching time is adjustable.
Select Address No.7, Data = D12-D10 : Below $B \rightarrow A$ switching time is adjustable.
※Switching time over 11.2 msec is recommended for both $A \rightarrow B$ and $B \rightarrow A$.
※Set to same switching time for both $A \rightarrow B, B \rightarrow A$ is recommended if the switching times need to be changed.


Figure 11. Micro step volume switching time

If the base clock is set to $x 1 / 2$, the switching time will be doubled.

## Micro step volume circuit

1. Micro step volume technology.

1-1. Micro step volume effects.
Micro step volume is Rohm original switching pop noise prevention technology. The audible signal is discontinuous during the gain switching instantly which cause the noise to occur. This micro step volume will prevent this discontinuous signal by completing the signal waveform and will significantly reduce the noise.

Control signal


Figure 12. Micro step volume waveform
This micro step volume will start the switching when received the signal sent from the micon.
At any constant time, the switching waveform is shown as above figure. This IC will optimally operates by internally processes the data sent from the micon to prevent the switching shock.

However, sometimes the switching waveform is not like the intended form depends on the transmission timing. Therefore, below is the example of the relationship between the transmission timing and actual switching time. Please consider this relationship for the setting.

1-2. Micro step volume application target block

- Micro step volume application target blocks are 7.1ch volume and SUB volume

2. About data transmission of Micro step volume circuit

## 2-1. Switching time of Micro step volume

This switching time includes [Wait time], $[A \rightarrow B$ switching time] and $[B \rightarrow A$ switching time]. Every switching time needs around 25 msec . (Tsoft = Twait +2 * $\mathrm{Tsft}, \quad$ Twait $=2.3 \mathrm{msec}, \mathrm{Tsft=} 11.2 \mathrm{msec}$ )
Please take note that Twait is wait time for starting switching and the setting is 2.3 msec . (Twait considers the internal IC tolerance, therefore this time need to be set within 1.3 msec (Min.) to 4.6 msec (Max.).


Figure 13. $[A \rightarrow B$ switching time $]$ and $[B \rightarrow A$ switching time $]$
In addition, base clock can change the frequency using the internal oscillation device. For example, when base clock $x 1 / 2$ is selected, [Wait time], [ $A \rightarrow B$ switching time] and $[B \rightarrow A$ switching time] are doubled.

2-2. Same block data transmission timing and switching operation.

- Transmission example 1

The time chart from data transmission to switching start time is shown as below.
At first, below figure shows transmitted data with the same block which is separated with enough interval.
This enough interval refers to the tolerance margin time of Tsoft multiplied by 1.4.


Transmission example 2
Next, below figure shows the example of when the transmission interval is not enough (smaller than above interval). When the data transmitted during the first operation of the switching, the second data transmission will continue after complete the first operation. In this case, there is no wait time (Twait) before the second transmission.


- Transmission example 3

Next is the example for switching operation with smaller data transmission interval.


Data (2) is the data during the $\mathrm{A} \rightarrow \mathrm{B}$ operation, so this data is valid, and then during $\mathrm{B} \rightarrow \mathrm{A}$ operation, data (1) promptly switches to data (2).
Data (3) and data (4) are data during $B \rightarrow A$ operation, therefore these data are valid for the next switching, but data (3) got overwritten by data (4) so data (3) will become invalid. Only data (4) is valid.
There is no regulation on the transmission timing.
For data transmission to multi-channels, there is a caution. The combination of Lch and Rch for same block will make the switching is possible to change at same timing. When the setting is data (1) for FL (Lch) and data (2) for FR (Rch), same switching timing is possible if the data transmission is set as below figure.


Figure 14. The operation during multi-channels (Lch, Rch) data transmission (smaller than Twait interval).
Next, when data (2) is not transmitted during the Twait, the switching operation is as following figure.


Figure 15. The operation during multi-channels (Lch, Rch) data transmission (larger than Twait interval).

2-3. Multi-blocks data transmission timing and switching operation.
In case of the data is transmitted to the multi-blocks, the processing is performed to each sequence which is defined by the IC internally.
This sequence determines the Micro step volume starting order operation.
-Transmission example 1
In case of multi-channels operates as transmission order (during 3 channels transmission).

$\qquad$ SW output
$\qquad$


There is no constraint for the data transmission timing, however the timing of switching start becomes to switching after the current timing is ended.
Please take note that, the timing of switching start is not depending on data setting order but only based on the regulated order by Figure16. (Transmission example 2)


Figure 16. Volume switching stage
※ Blocks in the same stage is possible to start the switching at the same timing.
-Transmission example 2
In case of the transmission order is different with actual switching order.
Serial data

During FL switching, in case of FL/SW/SL continuously received, SW and SL switching are the priority.
If you want the switching starts as the data transmission order, please transmit the next data after current switching is ended.

## -Transmission example 3

For same data transmission, the IC will internally judge that there is no difference with the current data setting and therefore gain switching operation will not start.

Continuing the same data transmission and transmit the other block data.


## $2-4$. How to reduce pop noise

Pop noise level is different base on the Micro step internal state $A$ and $B$ output DC offset difference.
To reduce the pop noise level, set for longer switching time might solve this problem.
Change the setting for $[A \rightarrow B$ switching time] and $[B \rightarrow A$ switching time], and confirm pop the noise level.
At this time, if $[A \rightarrow B$ switching time] and $[A \rightarrow B$ switching time] setting is different, the pop noise reduction effect will decrease. Therefore, it is recommended to set these switching with same time.

## Application Circuit Diagram



Figure 17. Application Circuit Diagram

Notes on wiring

1. GND has to be wired from reference point and it should be thick. Setting error occur by common impedance on GND line to be big in case of big attenuation setting
2. Wiring pattern of CL and DA shall be away from the analog unit and cross-talk is not acceptable.
3. If possible, lines of CL and DA are not parallel. If they are adjacent to each other, the lines should be shielded.
4. Please concentrate on wiring pattern of the input terminal for input selector to the crosstalk. It is recommended that it is shielded during wiring period.
5. Please connect the decoupling capacitor of the power supply in the shortest distance as much as possible to VCC and GND, VEE.

## Power Dissipation

Thermal design for the IC
Temperature has great influence to the IC characteristics, and exceeding the absolute maximum ratings may degrade and damage the IC. A proper consideration must be given from two points, immediate damage and long-term reliability of operation


Figure 18. Temperature Derating Curve
(Note) Values mentioned above are based on actual measurement, and not guaranteed.
Power dissipation value varies depending to the board on which the IC is mounted

## I/O equivalence circuit(s)

| Terminal Number | Terminal Name | Terminal Voltage (V) | Equivalent Circuit | Terminal Description |
| :---: | :---: | :---: | :---: | :---: |
| $\begin{gathered} 21 \sim 27 \\ 32 \\ 39 \\ 59 \\ 70 \\ 73 \sim 79 \end{gathered}$ | GND | 0 |  | Analog ground terminals. |
| $\begin{aligned} & 3 \\ & 5 \\ & 7 \end{aligned}$ | VCC <br> VEE1 <br> VEE2 | $\begin{aligned} & +7 \\ & -7 \end{aligned}$ |  | Positive power supply terminal Negative power supply terminal |
| 4 | DGND | 0 |  | Digital ground terminal. |
| $\begin{gathered} 1 \\ 2 \\ 80 \end{gathered}$ | $\begin{aligned} & \text { DA } \\ & \text { CL } \\ & \text { CHIP } \end{aligned}$ | - |  | Input terminals for a clock and data. |
| $\begin{gathered} 8 \\ 10 \\ 12 \\ 14 \\ 15 \\ 16 \\ 17 \\ 18 \\ 71 \\ 72 \end{gathered}$ | OUTFL <br> OUTFR <br> OUTSW OUTC OUTSL OUTSR OUTSBL OUTSBR ADCR ADCL | 0 |  | Output terminal s for analog sound signal. |
| $\begin{aligned} & 28 \\ & 29 \\ & 30 \\ & 31 \end{aligned}$ | SUBR <br> SUBL <br> RECR <br> RECL | 0 |  | Output terminals for analog sound signal. (SUB/REC) |


| Terminal Number | Terminal Name | Terminal Voltage (V) | Equivalent Circuit | Terminal Description |
| :---: | :---: | :---: | :---: | :---: |
| 33 34 35 36 37 38 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 | INR12 <br> INL12 <br> INR11 <br> INL11 <br> INR10 <br> INL10 <br> INR9 <br> INL9 <br> INR8 <br> INL8 <br> INR7 <br> INL7 <br> INR6 <br> INL6 <br> INR5 <br> INL5 <br> INR4 <br> INL4 <br> INR3 <br> INL3 <br> INR2 <br> INL2 <br> INR1 <br> INL1 | 0 |  | Input terminals for stereo sound signal. Input impedance is $100 \mathrm{k} \Omega$ (Typ) |
| $\begin{aligned} & 60 \\ & 61 \\ & 62 \\ & 63 \\ & 64 \\ & 65 \\ & 66 \\ & 67 \\ & 68 \\ & 69 \end{aligned}$ | SBRIN <br> SBLIN <br> SRIN <br> SLIN <br> CIN <br> SWIN <br> FRIN <br> FLIN <br> FRIN3 <br> FLIN3 | 0 |  | Input terminals for an analog multi sound signal. <br> Input impedance is $100 \mathrm{k} \Omega$ (Typ) |
| $\begin{aligned} & 19 \\ & 20 \end{aligned}$ | OUTPL OUTPR | 0 |  | Output terminal for FRONT pre-output. The impedance of output switch is $0.8 \mathrm{k} \Omega$ (Typ) |

## Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.
2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.
3. VEE Voltage

Ensure that no pins are at a voltage below that of the VEE pin at any time, even during transient condition.
4. Ground Wiring Pattern

GND pins which are digital ground(4pin) and analog ground(21-27,32,39,59,70,73-79pin) are not connected inside LSI. These ground pins traces should be routed separately but connected to a single ground at the reference point of the application board. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

## 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a $70 \mathrm{~mm} \times 70 \mathrm{~mm} \times 1.6 \mathrm{~mm}$ glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.
6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.
7. Rush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.
8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to IC pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

## 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

## 11. Unused Input Terminals

Because the input impedance of the terminal becomes $100 \mathrm{k} \Omega$ when the signal input terminal makes a terminal open, the plunge noise from outside sometimes becomes a problem. Please connect the no using input pin to GND. And please open the no using output pin.

## Operational Notes - continued 1

## 12. Regarding the Input Pin of the IC

This monolithic IC contains $\mathrm{P}+$ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When VEE > Pin A and VEE > Pin B, the P-N junction operates as a parasitic diode.
When VEE > Pin B, the P-N junction operates as a parasitic transistor.
Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the VEE voltage to an input pin (and thus to the $P$ substrate) should be avoided.


Figure 19. Example of monolithic IC structure
13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.
14. About power ON/OFF

1. At power ON/OFF, a pop sound will be generated and, therefore, use MUTE on the set.
2. When turning on power supplies, VEE and VCC should be powered on simultaneously or VEE first; then followed by VCC.(tdelay should be VEE=<VCC on power ON, VCC=<VEE on power OFF) If the VCC side is started up first, an excessive current may pass VCC through VEE.
3. This IC include power ON reset circuit. To be effective this function, trise should be more than $20 \mu \mathrm{sec}$.


Figure 20. Timing chart of power ON/OFF
15. About function switching

When switching Input Selector, Mode selector or Input Gain, use MUTE on Volume.
16. Volume gain switching

In case of the boost of the volume when changing to the high gain which exceeds +20 dB especially, the switching pop noise sometimes becomes big. In this case, we recommend changing every 1 dB step without changing a gain at once. Also, the pop noise sometimes can reduce by making micro-step volume switching time long, too.

## Operational Notes - continued 2

17. Output load characteristic

The usages of load for output are below (reference). Please use the load more than $10 \mathrm{k} \Omega$ (TYP)
Output terminal

| Terminal <br> No. | Terminal <br> Name | Terminal <br> No. | Terminal <br> Name | Terminal <br> No. | Terminal <br> Name | Terminal <br> No. | Terminal <br> Name |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 8 | OUTFL | 15 | OUTSL | 29 | SUBL | 71 | ADCR |
| 10 | OUTFR | 16 | OUTSR | 28 | SUBR | 72 | ADCL |
| 12 | OUTSW | 17 | OUTSBL | 31 | RECL | - | - |
| 14 | OUTC | 18 | OUTSBR | 30 | RECR | - | - |



Figure 21. Output load characteristic at VCC=+7V, VEE=-7V(Reference)

## Ordering Information



## Marking Diagram(TOP VIEW)



Physical Dimension, Tape and Reel Information

| Package Name | SQFP-T80C |
| :--- | :--- |



## Revision History

| Date | Revision |  | Changes |
| :---: | :---: | :--- | :--- |
| 7.Nov.2014 | 001 | New Release |  |
| 25.Feb.2015 | 002 | Add Micro-step volume specification |  |

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