Bt8370/8375/8376

Fully Integrated T1/E1 Framer and Line Interface

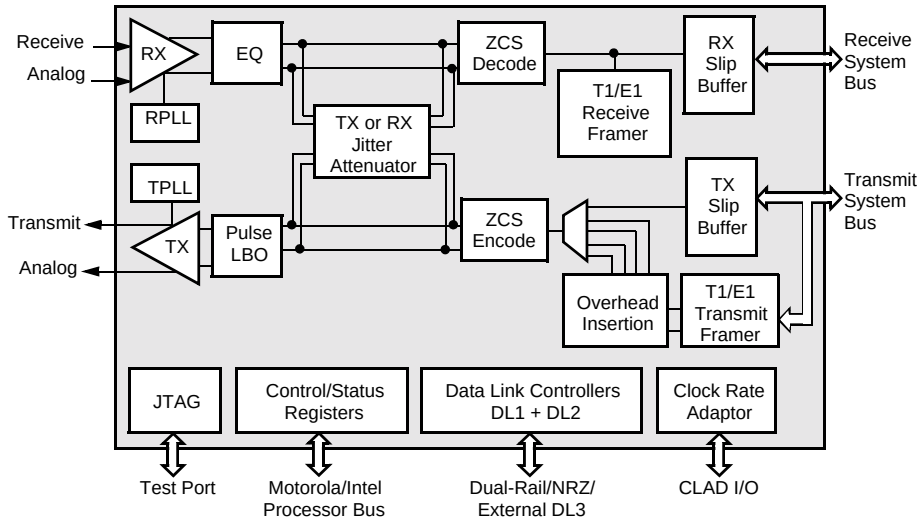
The Bt8370/8375/8376 is a family of single chip transceivers for T1/E1 and Integrated Service Digital Network (ISDN) primary rate interfaces, operating at 1.544 Mbps or 2.048 Mbps. These devices combine a sophisticated framer, transmit and receive slip buffers, and an on-chip physical line interface to provide a complete T1/E1 transceiver.

The fully featured Bt8370 and short-haul Bt8375 and Bt8376 devices provide a programmable clock rate adapter for simplifying system bus interfacing. The adapter synthesizes standard clock signals from the receive or transmit line rate clocks or from an external reference.

Operations are controlled through memory-mapped registers accessible via a parallel microprocessor port. Current ANSI, ETSI, ITU-T, and Bellcore standards are supported for alarm and error monitoring, signaling supervision (e.g., LAPD/SS7), per-channel trunk conditioning, and Facility Data Link (FDL) maintenance. A serial Time Division Multiplexed (TDM) system bus interface allows the backplane Pulse Code Modulation (PCM) data highway to operate at rates from 1.536 to 8.192 Mbps. Extensive test and diagnostic functions include a full set of digital and analog loopbacks, PRBS test pattern generation, BER meter, and forced error insertion.

The physical line interface circuit recovers clock and data from analog signals with +3 to –43 dB cable attenuation, appropriate for both short (–18 dB) and long-haul T1/E1 applications. Receive line equalization (EQ) and transmit Line Build Out (LBO) filters are implemented using Digital Signal Processor (DSP) circuits for reliable performance. Data and/or clock jitter attenuation can be inserted on either the receive or transmit path. The transmit section includes precision pulse shaping and amplitude pre-emphasis for cross connect applications, as well as a set of LBO filters for long-haul Channel Service Unit (CSU) applications. A complementary driver output is provided to couple 75/100/120 Ω lines via an external transformer.

Functional Block Diagram

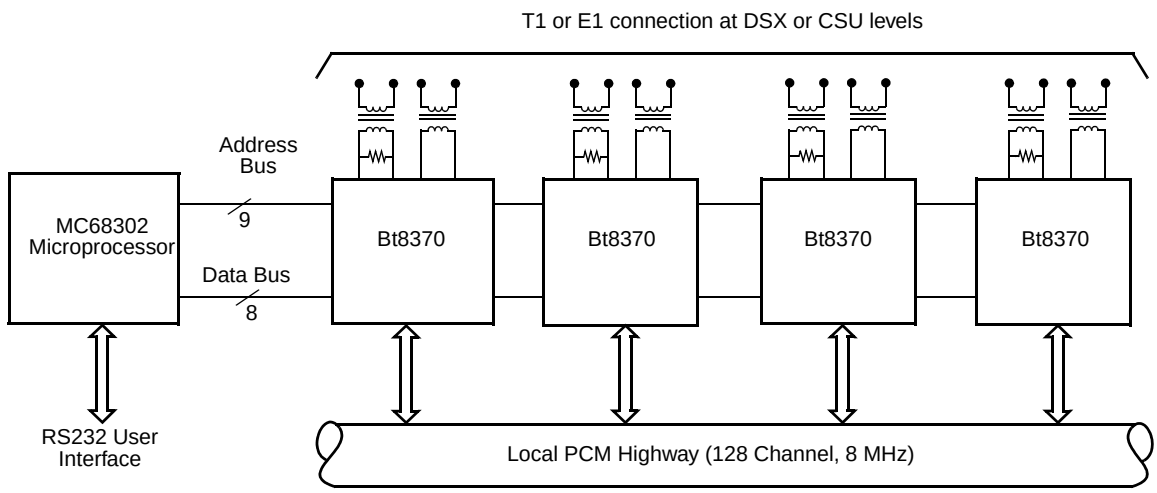


Distinguishing Features

- Single-chip T1/E1 framer with short/long-haul physical line interface
- Frames to popular T1/E1 standards:
  - T1: SF, ESF, SLC® 96, T1DM
  - E1: PCM-30, G.704, G.706, G.732 ISDN primary rate
- On-chip physical line interface compatible with:
  - DSX-1/E1 short-haul signals
  - DS-1 (T1.403) and ETSI long-haul signals
- Two-frame transmit and receive PCM slip buffers
- Clock rate adapter synthesizes jitter attenuated system clocks from an internal or external reference
- Parallel 8-bit microprocessor port supports Intel or Motorola buses
- Automated Facility Data Link (FDL) management
- BERT generation and counting
- Two full-duplex HDLC controllers for data link and LAPD/SS7 signaling
- B8ZS/HDB3/Bit 7 zero suppression
- 80-pin MQFP surface-mount package
- Operates from a single +5 Vdc ±5% power supply
- Low-power CMOS technology

Applications

- T1/E1 Channel Service Unit/Data Service Unit (CSU/DSU)
- Digital Access Cross-Connect Systems (DACS)
- T1/E1 Multiplexer (MUX)
- PBXs and PCM channel bank
- T1/E1 HDSL terminal unit
- ISDN Primary Rate Access (PRA)



An evaluation module is available and provides a convenient platform to test and evaluate Bt8370 performance and features. The Bt8370EVM provides up to four T1/E1 transceivers, all necessary line interface circuitry for T1 and E1 connections, and a simple RS232 serial user interface for setting device parameters and displaying status information on any VT100 compatible terminal. Contact the local sales representative for ordering information and pricing.

Ordering Information

Model Number	Package	Operating Temperature	Reduced Features[(1)]
Bt8370EPF	80-Pin MQFP	–40 to 85 °C	none
Bt8370KPF	80-Pin MQFP	0 to 70 °C	none
Bt8375EPF	80-Pin MQFP	–40 to 85 °C	Short-Haul
Bt8375KPF	80-Pin MQFP	0 to 70 °C	Short-Haul
Bt8376EPF	80-Pin MQFP	–40 to 85 °C	Short-Haul, No CLAD output
Bt8376KPF	80-Pin MQFP	0 to 70 °C	Short-Haul, No CLAD output

NOTE(S):
(1) Cost reduced Bt8375 and Bt8376 are pin and register-compatible versions of Bt8370 with reduced features. Contact the local sales representative for ordering information and pricing.

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1.0 Pin Descriptions

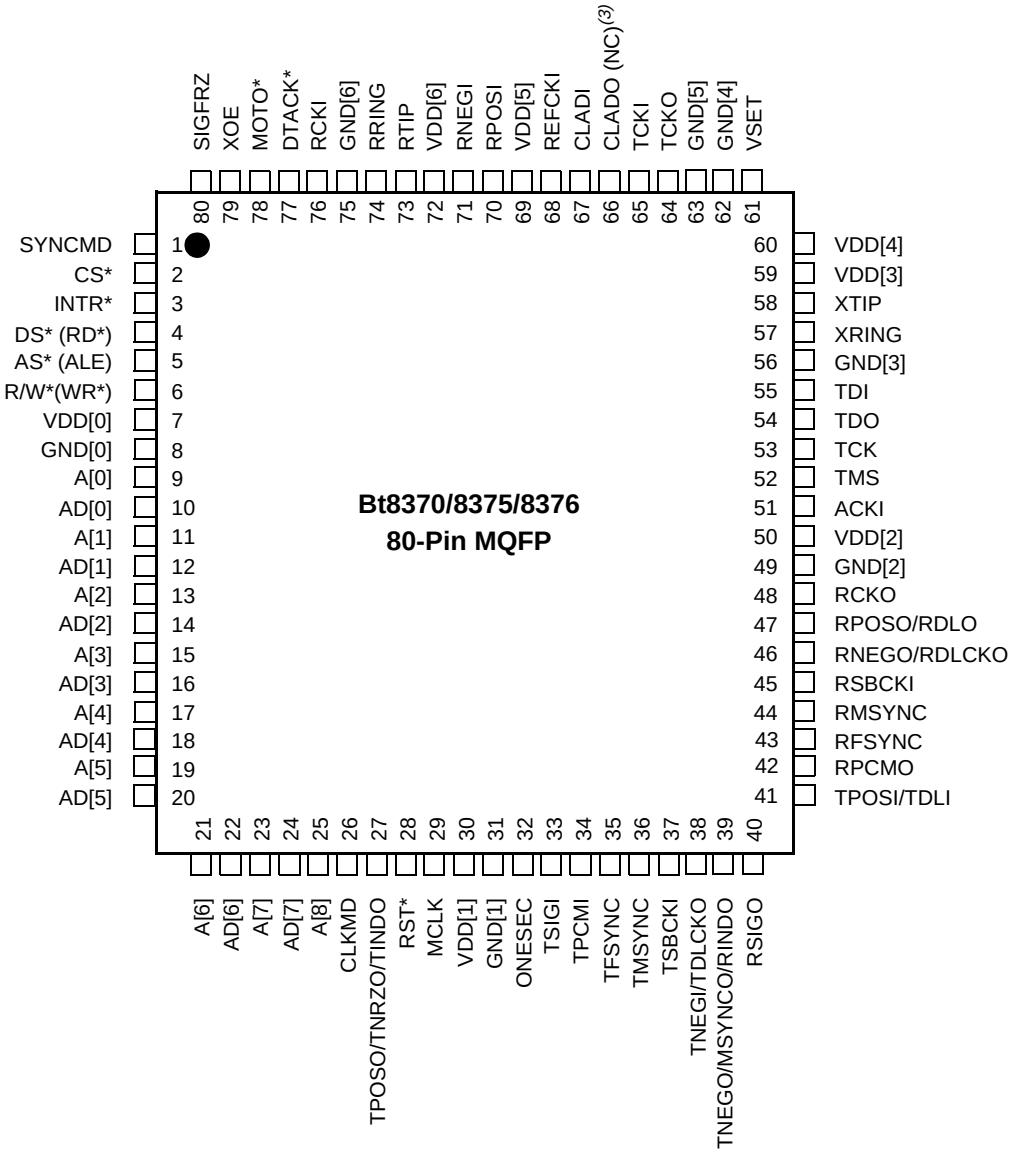
1.1 Pin Assignments

Bt8370/8375/8376 is packaged in an 80-pin Metric Quad Flat Pack (MQFP). A pinout diagram of this device is illustrated in Figure 1-1. Figure 1-2 details a Bt8370/8375/8376 logic diagram. Pin labels, names, I/O functions, and descriptions are provided in Table 1-1.

The input pins listed below contain an internal pullup resistor (>50 kΩ) and can remain unconnected if the active-high input state is desired. All other unused input pins should be either pulled up or grounded.

1	A[7:0]	Address lines unused in INTEL bus mode
2	XOE	Active-high enables analog bipolar output
3	MOTO*	Pullup selects INTEL bus mode if unconnected
4	SYNCMD	Pullup selects synchronous processor interface
5	RCKI	Receive clock unused if analog inputs enabled
6	TDI	Unused if JTAG not connected
7	TMS	Disables JTAG if not connected
8	TCK	Unused if JTAG not connected
9	RST*	Disables hardware reset if not connected
10	TDLI	Unused if no external data link
11	TSIGI	Unused if signaling data not supported by system bus

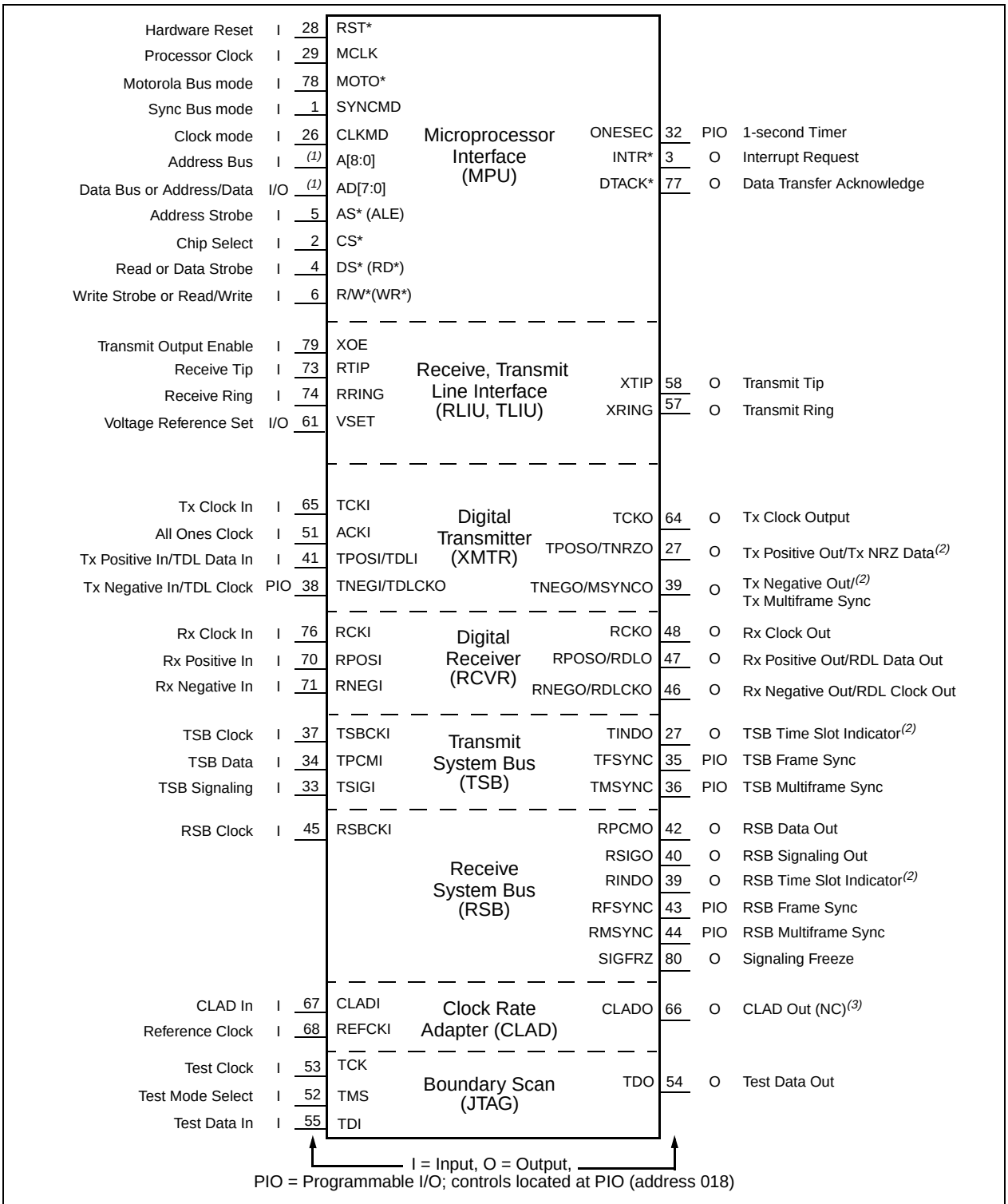
Figure 1-1. Bt8370/8375/8376 Pinout Diagram



NOTE(S):

1. Default pin assignments listed first for pins with multiple modes.
2. Motorola-style processor pin names listed first with Intel pins in parentheses.
3. Pin 66 is not connected for the Bt8376 device.

Figure 1-2. Bt8370/8375/8376 Logic Diagram



NOTE(S):

(1) Refer to Figure 1-1 *Bt8370/8375/8376 Pinout Diagram*.

(2) Pins 27 and 39 shown twice for clarity; pin function controlled by PIO (addr 018).

(3) Pin 66 is not connected for the Bt8376 device.

Table 1-1. Hardware Signal Definitions *(1 of 8)*

Pin Label	Signal Name	I/O	Definition
Microprocessor Interface (MPU)			
RST*	Hardware Reset	I	RST* low-to-high transition forces registers to their default, power-up state and forces all PIO pins to the input state. RST* is not mandatory, because internal power on reset circuit performs an identical function. RST* can be applied asynchronously, but must remain asserted for a minimum of 2 clock cycles (external MCLK or internal 32 MHz) for the low-to-high transition to be sampled and detected (see also [RESET; addr 001]).
MCLK	Processor Clock	I	System applies MCLK in the range of 8–36 MHz for external clock (CLKMD = 1) and synchronous bus modes (SYNCMD = 1). During internal clock modes (CLKMD = 0), the Bt8370/8375/8376 uses an internally generated 32 MHz clock to control processor timing, and MCLK input is ignored.
MOTO*	Motorola Bus mode	I	Selects Intel- or Motorola-style microprocessor interface. DS*, R/W*, A[8:0], and AD[7:0] functions are affected. 0 = Motorola; AD[7:0] is data, A[8:0] is address, DS* is data strobe, and R/W* indicates the read (high) or write (low) data direction. 1 = Intel; AD[7:0] is multiplexed address/data, A[7:0] ignored, A[8] is address line, DS* is read strobe (RD*), and R/W* is write strobe (WR*).
SYNCMD	Sync mode	I	Selects whether read/write cycle timing is synchronous with MCLK. Supports Intel- or Motorola-style buses: 0 = Asynchronous bus; read data enable and write data input latch are asynchronously controlled by CS*, DS*, and R/W* signals. Latched write data is still synchronized internally to 32 MHz clock for transfer to addressed register. 1 = Synchronous bus; applicable only if the external clock is also selected (CLKMD = 1). MCLK rising edge samples CS*, DS*, and R/W* to determine valid read/write cycle timing. Allows 0 wait state processor cycles for MCLK speeds up to 36 MHz, for M68000 type buses.
CLKMD	Clock mode	I	Selects whether MCLK is enabled (high) or ignored (low). When enabled, MCLK frequency determines update rate of internal registers and sampling rate of CS*, DS*, and R/W* signals.
A[8:0]	Address Bus	I	AS* falling edge asynchronously latches A[8:0] (Motorola) or A[8] (Intel) to identify 1 register for subsequent read/write data transfer cycle.
AD[7:0]	Data Bus or Address Data	I/O	Multiplexed address/data (Intel) or only data (Motorola). Refer to MOTO* signal definition.
AS* (ALE)	Address Strobe	I	For all processor bus modes, AS* falling edge asynchronously latches address from A[8:0] (Motorola) or from A[8] and AD[7:0] (Intel). For sync modes (SYNCMD = 1), each read/write data cycle requires both AS* and CS* active-low on MCLK rising edge.
CS*	Chip Select	I	Active-low enables read/write decoder. Active-high ends current read or write cycle and places data bus output in high impedance.
DS*(RD*)	Data Strobe or Read Strobe	I	Active-low read data strobe (RD*) for MOTO* = 1, or read/write data strobe (DS*) for MOTO* = 0.
R/W*(WR*)	Read/Write Direction or Write Strobe	I	Active-low write data strobe (WR*) for MOTO* = 1, or read/write data select (R/W*) for MOTO = 0.

Table 1-1. Hardware Signal Definitions *(2 of 8)*

Pin Label	Signal Name	I/O	Definition
Microprocessor Interface (MPU) (Continued)			
ONESEC	1-second Timer	PIO	Controls or marks 1-second interval used for status reporting. When input, the timer is aligned to ONESEC rising edge. When output, rising edge indicates start of each 1-second interval. Typically, 1 device in a multi-line system is configured to output ONESEC to synchronize other Bt8370/8375/8376 status reports on a common 1-second interval.
INTR*	Interrupt Request	O	Open drain active-low output signifies 1 or more pending interrupt requests. INTR* goes to high-impedance state after processor has serviced all pending interrupt requests.
DTACK*	Data Transfer Acknowledge	O	Open drain active-low output signifies in-progress data transfer cycle. DTACK* remains asserted (low) for as long as AS* and CS* are both active-low. DTACK* is only implemented during synchronous Motorola processor interface modes. Refer to the timing diagrams in Section 5.5, *MPU Interface Timing*.
Line Interface Unit (LIU)			
XOE	Transmit Output Enable	I	Active-high input enables XTIP and XRING output drivers; otherwise, both outputs are placed in high-impedance state. XOE contains internal pullup so systems that do not require three-stated outputs can leave XOE unconnected. XOE needs to be disabled during Power-On Reset (POR) and re-enabled after configuring the part. Refer to Power-On Reset procedure in Section 2.10.4, *Device Reset*.
RTIP, RRING	Receive Tip/Ring	I	Differential AMI data inputs for direct connection to receive transformer.
VSET	Voltage Reference Set	I/O	Constant voltage output. Must be connected to an external 1% resistor equal to 14 kΩ to ground (GND[4] pin 62). The VSET resistor sets the internal precision current reference of 100 µA and also controls the transmit pulse height.
XTIP, XRING	Transmit Tip/Ring	O	Complementary AMI data outputs for direct connection to transmit transformer. Optionally, both outputs are three-stated when XOE is negated.
Digital Transmitter (XMTR)			
TCKI	Tx Clock Input	I	Primary TX line rate clock applied on TCKI, or the system chooses from 1 of four different clocks to act as TX clock source (see [CMUX; addr 01A]). The selected source is used to clock digital transmitter signals TPOSI, TNEGI, TPOSO, TNEGO, TNRZO, MSYNCO, TDLI, and TDLCKO. If TSLIP is bypassed, selected source also clocks TSB signals.
ACKI	All Ones Clock	I	System optionally applies ACKI for AIS transmission, if the selected primary transmit clock source fails. ACKI is either manually or automatically switched to replace TCKI (see [AISCLK; addr 068]). Systems without an AIS clock must tie ACKI to ground.

Table 1-1. Hardware Signal Definitions *(3 of 8)*

Pin Label	Signal Name	I/O	Definition
Digital Transmitter (XMTR) (Continued)			
TPOSI	TX Positive Rail Input	I	Line rate data input on TCKI falling edge. Replaces all data that would otherwise be supplied by ZCS encoder. Bt8370/8375/8376 default power on state selects TPOSI/TNEGI as source for all transmitted XTIP/XRING output pulses, encoded as follows: TPOSI / TNEGI / TX Pulse Polarity 0 / 0 / No pulse 0 / 1 / Negative AMI pulse 1 / 0 / Positive AMI pulse 1 / 1 / Invalid ***NOTE(S):*** Software must set TDL_IO (addr 018) to enable normal data from internal transmitter.
TNEGI	TX Negative Rail Input	I	Line rate data input on TCKI falling edge. Replaces all data that would otherwise be supplied by ZCS encoder. Refer to TPOSI signal definition.
TPOSO	TX Positive Rail Output	O	Line rate data output from ZCS encoder or JAT on rising edge of TCKO. Active-high marks transmission of a positive AMI pulse. Used to monitor transmit data or for systems that employ an external line interface unit.
TNEGO	TX Negative Rail Output	O	Line-rate data output from ZCS encoder or JAT on rising edge of TCKO. Active-high marks transmission of a negative AMI pulse. Used to monitor transmit data or for systems that use an external line interface unit.
TDLI	TX Data Link Input	I	Selected time slot bits are sampled on TDLCKO falling edge for insertion into the transmit output stream during external data link applications.
TDLCKO	TX Data Link Clock	O	Gapped version of TCKI for external data link applications. TDLCKO high clock pulse coincides with low TCKI pulse interval during selected time slot bits (see [DL3_TS; addr 015]).
TCKO	TX Clock Output	O	Line rate clock used to align XTIP/XRING outputs. If transmit jitter attenuator (TJAT) is disabled, TCKO equals selected TCKI or ACKI. If TJAT is enabled, TCKO equals the jitter attenuated clock (JCLK).
TNRZO	TX Non Return to Zero Data	O	Line rate data output from transmitter on rising edge of TCKI. TNRZO does not include ZCS encoded bipolar violations.
MSYNCO	TX Multiframe Sync	O	Active-high for 1 TCKI clock cycle to mark the first bit of TX multiframe coincident with TNRZO. Output on rising edge of TCKI.

Table 1-1. Hardware Signal Definitions *(4 of 8)*

Pin Label	Signal Name	I/O	Definition
Digital Receiver (RCVR)			
RCKI	RX Clock Input	I	Line rate clock samples RPOSI and RNEGI when RLIU configured to accept dual-rail digital data (see [RDIGI; addr 020]); otherwise, RCKI is ignored.
RPOSI	RX Positive Rail Input	I	Line rate data input on falling edge of RCKI. RPOSI and RNEGI levels are interpreted as received AMI pulses, encoded as follows: RPOSI / RNEGI / RX Pulse Polarity 0 / 0 / No pulse 0 / 1 / Negative AMI pulse 1 / 0 / Positive AMI pulse 1 / 1 / Invalid ***NOTE:*** The NRZ data can be input at RPOSI or RNEGI if the other input is connected to ground.
RNEGI	RX Negative Rail Input	I	Line rate data input on falling edge of RCKI. See RPOSI signal definition.
RCKO	RX Clock Output	O	RPLL recovered line rate clock (RXCLK) or jitter attenuated clock (JCLK) output, based on programmed clock selection (see [JAT_CR; addr 002]).
RPOSO	RX Positive Rail Output	O	Line rate data output on rising edge of RCKO. Active-high indicates receipt of a positive AMI pulse on RTIP/RING inputs.
RNEGO	RX Negative Rail Output	O	Line rate data output on rising edge of RCKO. Active-high indicates receipt of a negative AMI pulse on RTIP/RING inputs.
RDLO	RX Data Link Output	O	Line rate NRZ data output from receiver on falling edge of RCKO, all data from RLIU is represented at the RDLO pin. However, selective RDLO bit positions are also marked by RDLCKO for external data link applications.
RDLCKO	RX Data Link Clock Output	O	Gapped version of RCKO for external data link applications. RDLCKO high clock pulse coincides with low RCKO pulse interval during selected time slot bits, else RDLCKO low (see Figure 2-12, *Receive External Data Link Waveforms*, External Data Link).

Table 1-1. Hardware Signal Definitions *(5 of 8)*

Pin Label	Signal Name	I/O	Definition
Transmit System Bus (TSB)			
TSBCKI	TSB Clock Input	I	Bit clock and I/O signal timing for TSB according to system bus mode (see [SBI_CR; addr 0D0]). System chooses from 1 of four different clocks to act as TSB clock source (see [CMUX; addr 01A]). Rising or falling edge clocks are independently configurable for data signals TPCMI, TSIGI, TINDO and sync signals TFSYNC and TMSYNC (see [TPCM_NEG and TSYN_NEG; addr 0D4]). When configured to operate at twice the data rate, TSB clock is internally divided by two before clocking TSB data signals.
TPCMI	TSB Data Input	I	Serial data formatted into TSB frames consisting of DS0 channel time slots and optional F-bits. One group of 24 T1 time slots or 32 E1 time slots is selected from up to four available groups; data from the group is sampled by TSBCKI, then sent towards transmitter output. Time slots are routed through transmit slip buffer (see [TSLIPn; addr 140–17F]) according to TSLIP mode (see [TSBI; addr 0D4]). F-bits are taken from the start of each TSB frame or from within an embedded time slot (see [EMBED; addr 0D0]) and optionally inserted into the transmitter output (see [TFRM; addr 072] register).
TSIGI	TSB Signaling Input	I	Serial data formatted into TSB frames containing ABCD signaling bits for each system bus time slot. Four bits of TSIGI time slot carry signaling state for each accompanying TPCMI time slot. Signaling state of every time slot is sampled during first frame of the TSB multiframe, and then transferred into transmit signaling buffer [TSIGn; addr 120–13F].
TINDO	TSB Time Slot Indicator	O	Active-high output pulse marks selective transmit system bus time slots as programmed by SBCn [addr 0E0–0FF]. TINDO occurs on TSBCKI rising or falling edges as selected by TPCM_NEG (see [TSBI; addr 0D4]).
TFSYNC	TSB Frame Sync	PIO	Input or output TSB frame sync (see [TFSYNC_IO; addr 018]). TFSYNC output is active-high for 1 TSB clock cycle at programmed offset bit location (see [TSYNC_BIT; addr 0D5]), marking offset bit position within each TSB frame and repeating once every 125 µs. When transmit framer is also enabled, TSB timebase and TFSYNC output frame alignment are established by transmit framer's examination of TPCMI serial data input. When TFSYNC is programmed as an input, the low-to-high signal transition is detected and aligns TSB timebase to programmed offset bit value. TSB timebase flywheels at 125 µs frame interval after the last TFSYNC is applied.
TMSYNC	TSB Multiframe Sync	PIO	Input or output TSB multiframe sync (see [TMSYNC_IO; addr 018]). TMSYNC output is active-high for 1 TSB clock cycle at programmed offset bit location (see [TSYNC_BIT; addr 0D5]), marking offset bit position within each TSB multiframe and repeating once every 6 ms coincident with TFSYNC. When transmit framer is also enabled, TSB timebase and TMSYNC output multiframe alignment are established by transmit framer's examination of TPCMI serial data input. When TMSYNC is programmed as an input, the low-to-high signal transition is detected and aligns TSB timebase to the programmed offset bit value and first frame of the multiframe. TSB timebase flywheels at 6 ms multiframe interval after the last TMSYNC is applied. If system bus applies TMSYNC input, TFSYNC input is not needed.

Table 1-1. Hardware Signal Definitions *(6 of 8)*

Pin Label	Signal Name	I/O	Definition
Receive System Bus (RSB)			
RSBCKI	RSB Clock Input	I	Bit clock and I/O signal timing for RSB according to system bus mode (see [SBI_CR; addr 0D0]). System chooses from 1 of four different clocks to act as RSB clock source (see [CMUX; addr 01A]). Rising or falling edge clocks are independently configurable for data signals RPCMO, RSIGO, RINDO and sync signals RFSYNC, RMSYNC (see [RPCM_NEG and RSYN_NEG; addr 0D1]). When configured to operate at twice the data rate, RSB clock is internally divided by 2 before clocking RSB data signals.
RPCMO	RSB Data Output	O	Serial data formatted into RSB frames consisting of DS0 channel time slots, optional F-bits, and optional ABCD signaling. Time slots are routed through receive slip buffer (see [RSLIPn; addr 1C0–1FF]) according to RSLIP mode (see [RSBI; addr 0D1]). Data for each output time slot is assigned sequentially from received time slot data according to system bus channel programming (see [ASSIGN; addr 0E0–0FF]). F-bits are output at the start of each RSB frame or at the embedded time slot location (see [EMBED; addr 0D0]). ABCD signaling is optionally inserted on a per-channel basis (see [INSERT; addr 0E0–0FF]) from the local signaling buffer (see [RLOCAL; addr 180–19F]) or from the receive signaling buffer [RSIGn; addr 1A0–1BF]. When enabled, robbed bit signaling or CAS reinsertion is performed according to T1/E1 mode: the eighth time slot bit of every sixth T1 frame is replaced, or the 4-bit signaling value in the E1 time slot 16 is replaced.
RSIGO	RSB Signaling Output	O	Serial data formatted into RSB frames consisting of ABCD signaling bits for each system bus time slot. Four bits of RSIGO time slot carry signaling state for each accompanying RPCMO time slot. Local or through signaling bits are output in every frame for each time slot and updated once per RSB multiframe, regardless of per-channel RPCMO signaling reinsertion.
RINDO	RSB Time Slot Indicator	O	Active-high output pulse marks selective receive system bus time slots as programmed by SBCn [addr 0E0–0FF]. RINDO occurs on RSBCKI rising or falling edges as selected by RPCM_NEG (see [RSBI; addr 0D1]).
RFSYNC	RSB Frame Sync	PIO	Input or output RSB frame sync (see [RFSYNC_IO; addr 018]). RFSYNC output is active-high for 1 RSB clock cycle at programmed offset bit location (see [RSYNC_BIT; addr 0D2]), marking offset bit within each RSB frame and repeating once every 125 µs. RSB timebase and RFSYNC output frame alignment begins at an arbitrary position and changes alignment according to RSLIP mode (see [RSBI; addr 0D1]). When RFSYNC is programmed as an input, the low-to-high signal transition is detected and aligns RSB timebase to the programmed offset. RSB timebase flywheels at 125 µs frame interval after the last RFSYNC is applied.
RMSYNC	RSB Multiframe Sync	PIO	Input or output RSB multiframe sync (see [RMSYNC_IO; addr 018]). RMSYNC output is active-high for 1 RSB clock cycle at programmed offset bit location (see [RSYNC_BIT; addr 0D2]), marking offset bit within each RSB multiframe and repeating once every 6 ms coinciding with RFSYNC. RSB timebase and RMSYNC output multiframe alignment begins at an arbitrary position and changes alignment according to RSLIP mode (see [RSBI; addr 0D1]). When RMSYNC is programmed as input, the low-to-high signal transition is detected and aligns the RSB timebase to the programmed offset and the first frame of the multiframe. RSB timebase flywheels at 6 ms multiframe interval after the last RMSYNC is applied.

Table 1-1. Hardware Signal Definitions *(7 of 8)*

Pin Label	Signal Name	I/O	Definition
Receive System Bus (RSB) (Continued)			
SIGFRZ	Signaling Freeze	O	Active-high indicates that signaling bit updates are suspended for both receive signaling buffer [RSIGn; addr 1A0–1BF] and stack [STACK; addr 0DA] register. SIGFRZ, clocked by RSB clock, goes high coinciding with receive loss of frame alignment (see RLOF; addr 047) and returns low 6–9 ms after recovery of frame alignment.

NOTE(S):
1. All RSB and TSB outputs can be placed in high-impedance state (see SBI_OE; addr 0D0).
2. Receive System Bus (RSB)

Table 1-1. Hardware Signal Definitions *(8 of 8)*

Pin Label	Signal Name	I/O	Definition
Clock Rate Adapter (CLAD)			
CLADI	CLAD Input	I	Optional CLAD input timing reference used to phase lock CLADO and JCLK outputs to 1 of 44 different input clock frequencies selected in the range of 8 kHz to 16384 kHz (see [CLAD registers; addr 090–092]).
REFCKI	Reference Clock	I	System must apply a 10 MHz ±50 ppm clock signal to act as frequency reference for internal Numerical Controlled Oscillator (NCO). REFCKI determines frequency accuracy and stability of CLADO and jitter attenuator (JCLK) clocks when the NCO operates in free running mode (see [JFREE; addr 002]). REFCKI is the baseband reference for all CLAD/JAT functions and is used internally to generate clocks of various frequencies, locked to a selected receive, transmit, or external clock. Hence, REFCKI is always required.
CLADO	CLAD Output	O	CLADO is configured to operate at 1 of 14 different clock frequencies (see [CSEL; addr 091]) that include T1, E1 or system bus rates. CLADO is typically programmed to supply RSB and TSB clocks that are phase-locked to the selected transmit, receive or CLADI timing reference (see [JEN; addr 002 and CEN; addr 090]). On the Bt8376 device, CLAD0 drives low when enabled.
Test Access			
TDI	JTAG Test Data Input	I	Test data input per *IEEE Std 1149.1-1990*. Used for loading all serial instructions and data into internal test logic. Sampled on the rising edge of TCK. TDI can be left unconnected if it is not being used because it is pulled up internally.
TMS	JTAG Test mode Select	I	Active-low test mode select input per *IEEE Std 1149.1-1990*. Internally pulled-up input signal used to control the test-logic state machine. Sampled on the rising edge of TCK. TMS can be left unconnected if it is not being used because it is pulled up internally.
TDO	JTAG Test Data Output	O	Test data output per *IEEE Std 1149.1-1990*. Three-state output used for reading all serial configuration and test data from internal test logic. Updated on the falling edge of TCK.
TCK	JTAG Test Clock	I	Test clock input per IEEE Std 1149.1-1990. Used for all test interface and internal test-logic operations. If unused, TCK must be pulled low.
Power Supply			
VDD[6:0]	Power	I	+5 VDC ±5%
GND[6:0]	Ground	I	0 VDC

NOTE(S):
1. I = Input, O = Output
2. PIO = Programmable I/O; controls located at address 018.
3. Multiple signal names show mutually exclusive pin functions.
4. All output pins power up in the high-impedance state within 3,000 cycles of the applied REFCKI (see POE; addr 019, SBI_OE; addr 0D0).

2.0 Circuit Description

2.1 Bt8370/8375/8376 Block Diagrams

Detailed block diagrams are illustrated in Figure 2-1 (Bt8370), Figure 2-2 (Bt8375), and Figure 2-3 (Bt8376). To show the details of this circuit, individual block diagrams, along with descriptions, appear throughout this section.

1. Receive Line Interface Unit (RLIU)
2. Jitter Attenuator (JAT)
3. Digital Receiver (RCVR)
4. Receive System Bus (RSB)
5. Clock Rate Adapter (CLAD)
6. Transmit System Bus (TSB)
7. Digital Transmitter (XMTR)
8. Transmit Line Interface Unit (TLIU)
9. Microprocessor Interface (MPU)
10. Joint Test Access Group Port (JTAG)

NOTE: The Bt8375 differs from the Bt8370 only in that the Bt8375 does not have LBO filters in the transmit LIU. The Bt8376 differs from Bt8375 in that Bt8376 has neither a CLADO output, nor a DLINK2.

Figure 2-1. Detailed Bt8370 Block Diagram

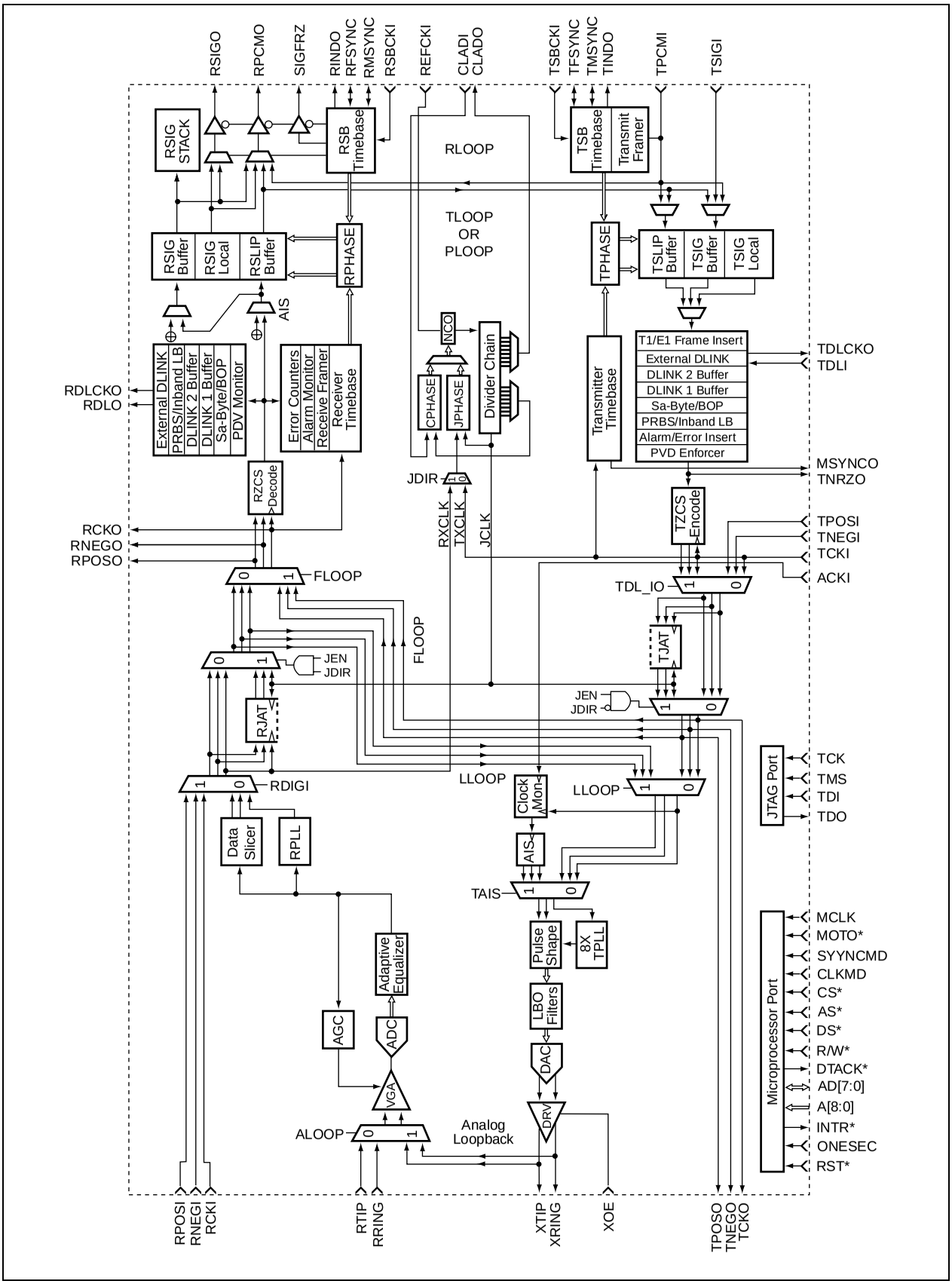


Figure 2-2. Detailed Bt8375 Block Diagram

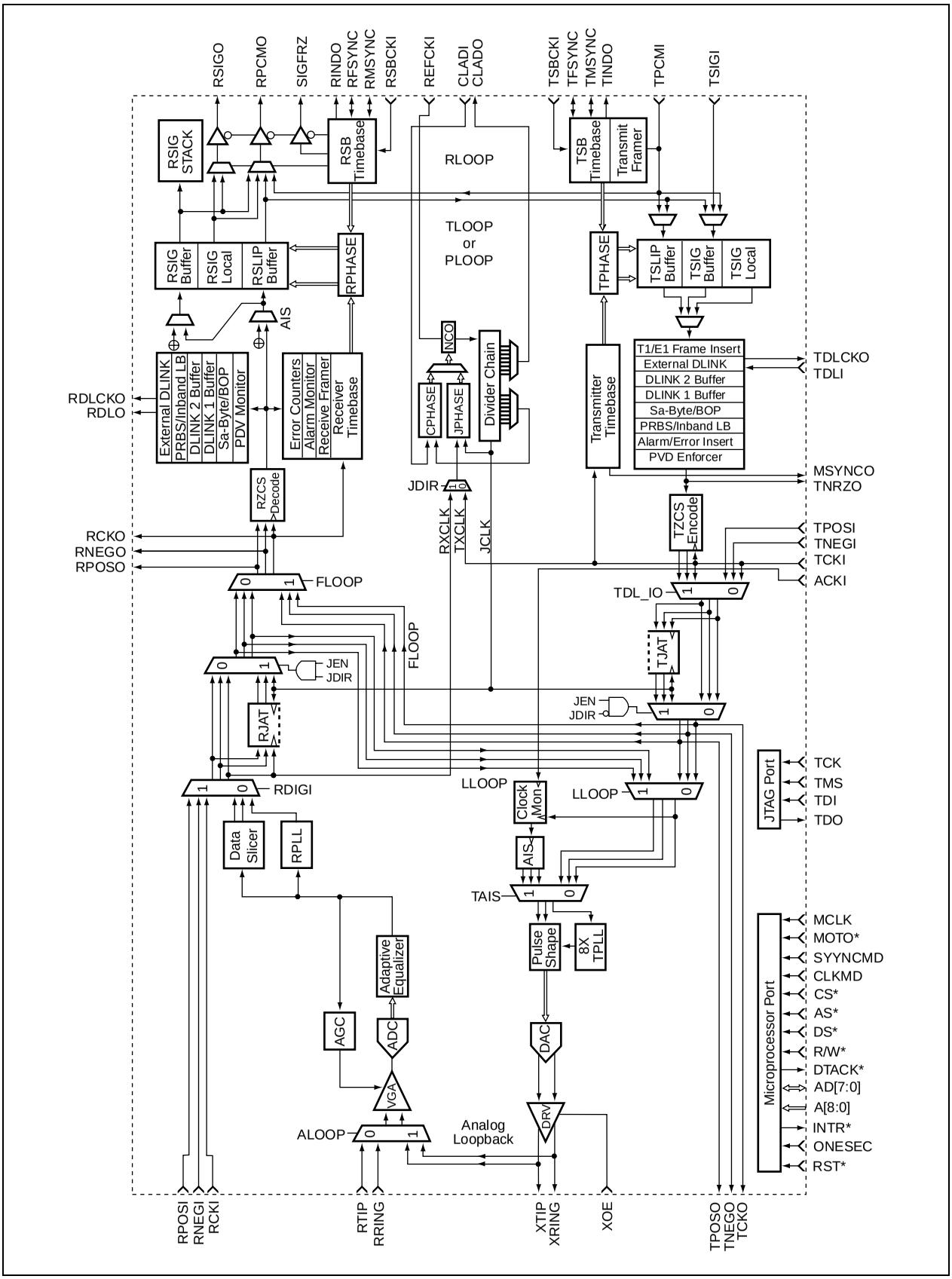
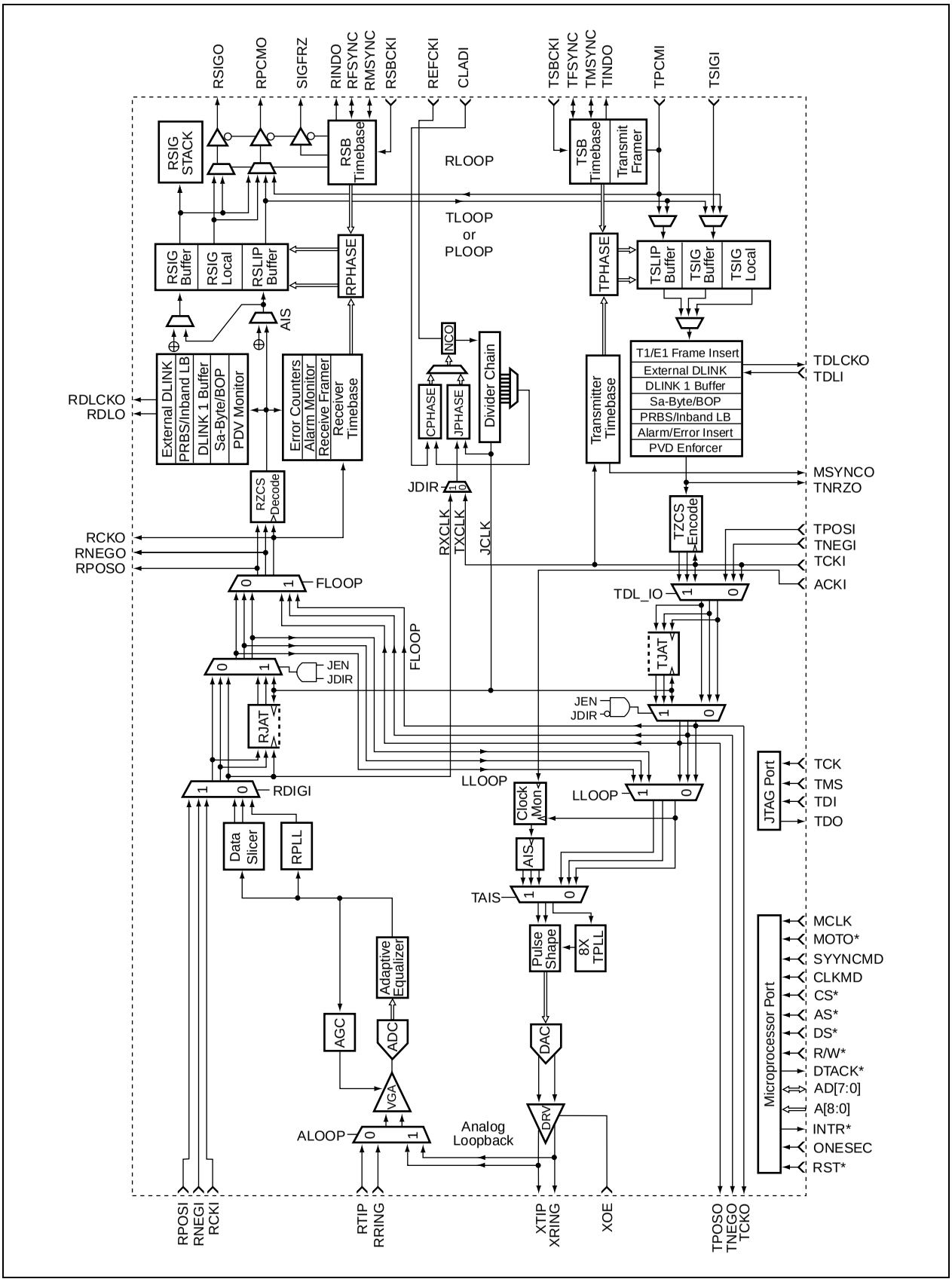


Figure 2-3. Detailed Bt8376 Block Diagram



2.2 Receive Line Interface Unit

The Receive Line Interface Unit (RLIU) recovers clock and data from the bipolar Alternate Mark Inversion (AMI) line signal that has been attenuated and distorted due to the characteristics of the line. In the Bt8370 device, the RLIU is sensitive to signals attenuated in the range of 0 to –48 dB in E1 and T1 modes. In the Bt8375 and Bt8376 devices, RLIU sensitivity is limited for short-haul only applications. In addition, the RLIU interfaces at the DSX-1 Bridge Monitor Level (–20 dB for DS1 and –30 dB for E1/CEPT).

The RLIU converts AMI pulses into P and N rail Non-Return to 0 (NRZ) data. The AMI pulses are input on the receive tip and ring pins: RTIP and RRING (Figure 2-4). The P and N rail NRZ data is then passed to the RCVR. The RCVR dual rail output is available on RPOSO/RNEGO. Figure 2-5 illustrates the relationship between the AMI received signal, the recovered clock, and the RCVR dual rail outputs.

Figure 2-4. RLIU Diagram

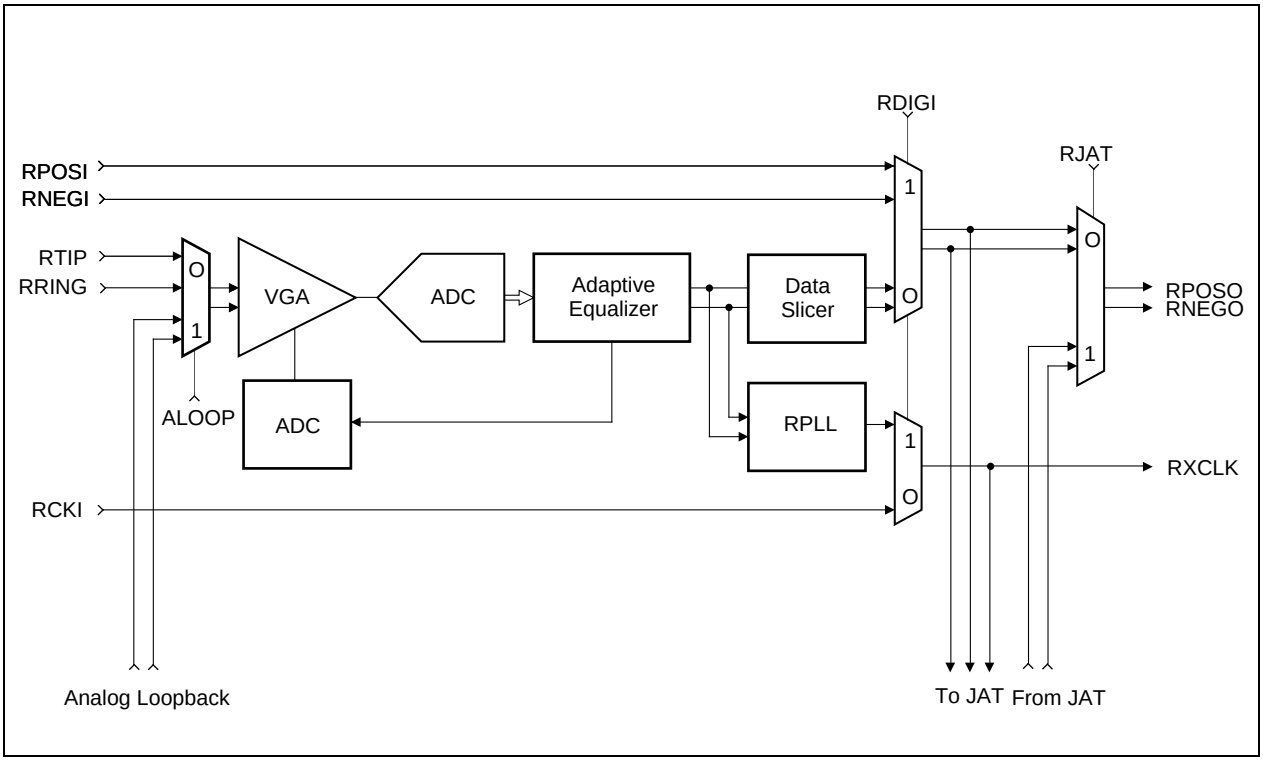
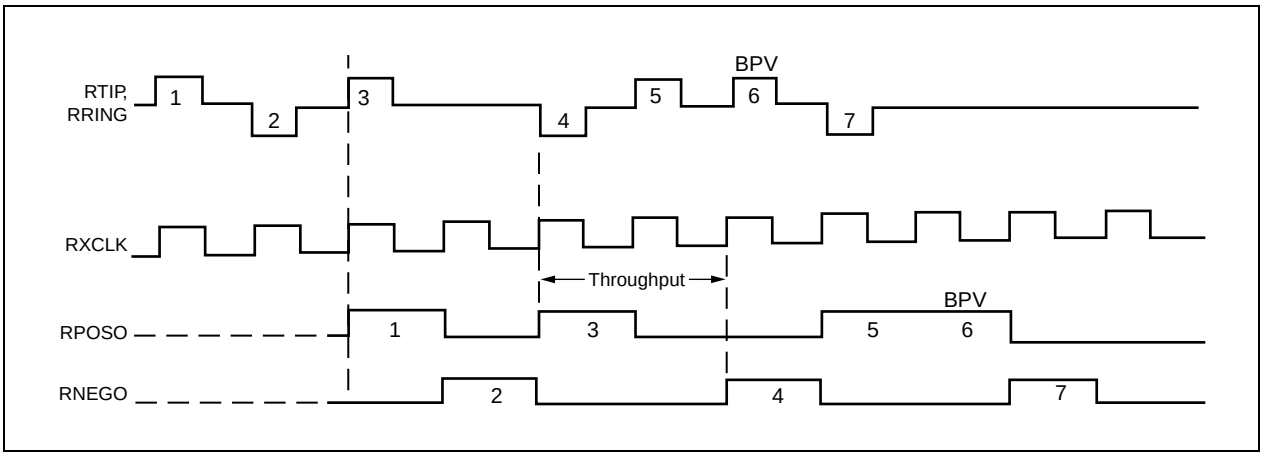
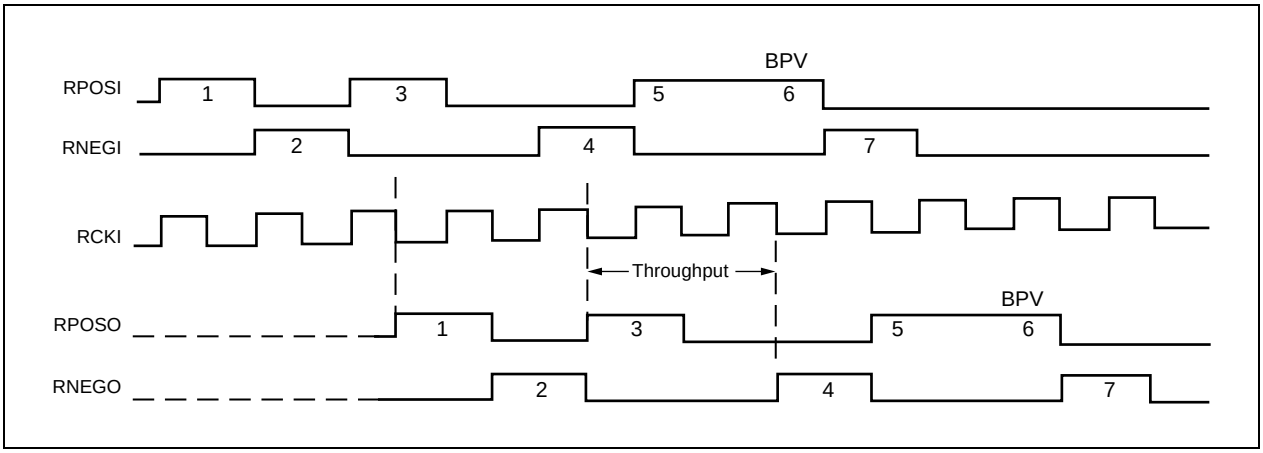


Figure 2-5. RLIU Waveforms—Bipolar Input Signal



If the RLIU functionality is not required, a bypass mode is provided [RDIGI; addr 020]. If the RLIU is bypassed, the RTIP/RRING pins are ignored, RPOSI/RNEGI P and N rail NRZ become inputs, and RCKI becomes the receive timing source. Figure 2-6 illustrates the relationship between the RLIU P and N rail NRZ data, the RLIU receive clock input, and the RCVR dual rail output.

Figure 2-6. RLIU Waveforms—P and N Rail Digital Input Signal



2.2.1 Data Recovery

The RLIU recovers data from the received analog signal by normalizing the signal with the Variable Gain Amplifier (VGA) and the Automatic Gain Control (AGC), removing distortion with the Adaptive Equalizer, and extracting the data using the Data Slicer.

2.2.1.1 Automatic Gain Control

The AGC circuit adjusts the gain of the incoming differential signal to achieve a normalized level. The normalized level ensures that the input signal to the ADC is 75% to 100% of full scale. This is done by measuring the peak voltage of the incoming signal with a peak detector, and inversely adjusting VGA gain based the peak value. The AGC can be forced to a fixed gain for test purposes or limited to a maximum value, which is the normal operating mode (see [FORCE_VGA; addr 020]).

2.2.1.2 Variable Gain Amplifier

The FORCE_VGA bit in the LIU Configuration register [LIU_CR; addr 020] selects whether the AGC operates in Gain Limit mode or Fixed Gain mode. In Gain Limit modes, the RLIU sensitivity is initially set to the maximum (approximately 43 dB), and the gain is adjusted based the peak value recorded during the AGC observation period. The AGC observation period can be set to 32, 128, 512, or 2048 symbol periods [RLIU_CR; addr 022]. A short observation period allows quick responses to pulse height variations but possible overshoots. A long observation period minimizes overshoots, but does not react quickly to pulse height variations. The real-time status of the VGA gain setting can be read in the Variable Gain Amplifier Status register [VGA; addr 029] and used to approximate the receive analog signal level.

In Fixed Gain mode, the RLIU sensitivity is set to the value stored in the Variable Gain Amplifier Maximum register [VGA_MAX; addr 024]. VGA_MAX is a 6-bit register that allows up to 64 gain settings in 1.25 dB steps.

2.2.1.3 Adaptive Equalizer

After the input amplitude has been normalized, the adaptive equalizer attempts to remove the distortion introduced by the cable. The transfer function of the equalizer is initially adjusted based on the peak value of the input signal because this value provides some indication of the line length on the input. The Adaptive Equalizer then automatically fine tunes to remove most of the signal distortion due to intersymbol interference, noise, and other cable length effects.

In certain applications the device can be connected to a DSX monitor point that has been resistively attenuated. Because this resistive attenuation adds no phase-versus-frequency distortion, the VGA gain must be adjusted. This is done by configuring the Receive Pad Resistor Compensation (ATTN[1,0]) in the LIU Configuration register [LIU_CR; addr 020]. The resistive attenuation can be configured to be either 0, –10, –20, or –30 dB.

2.2.1.4 Data Slicer

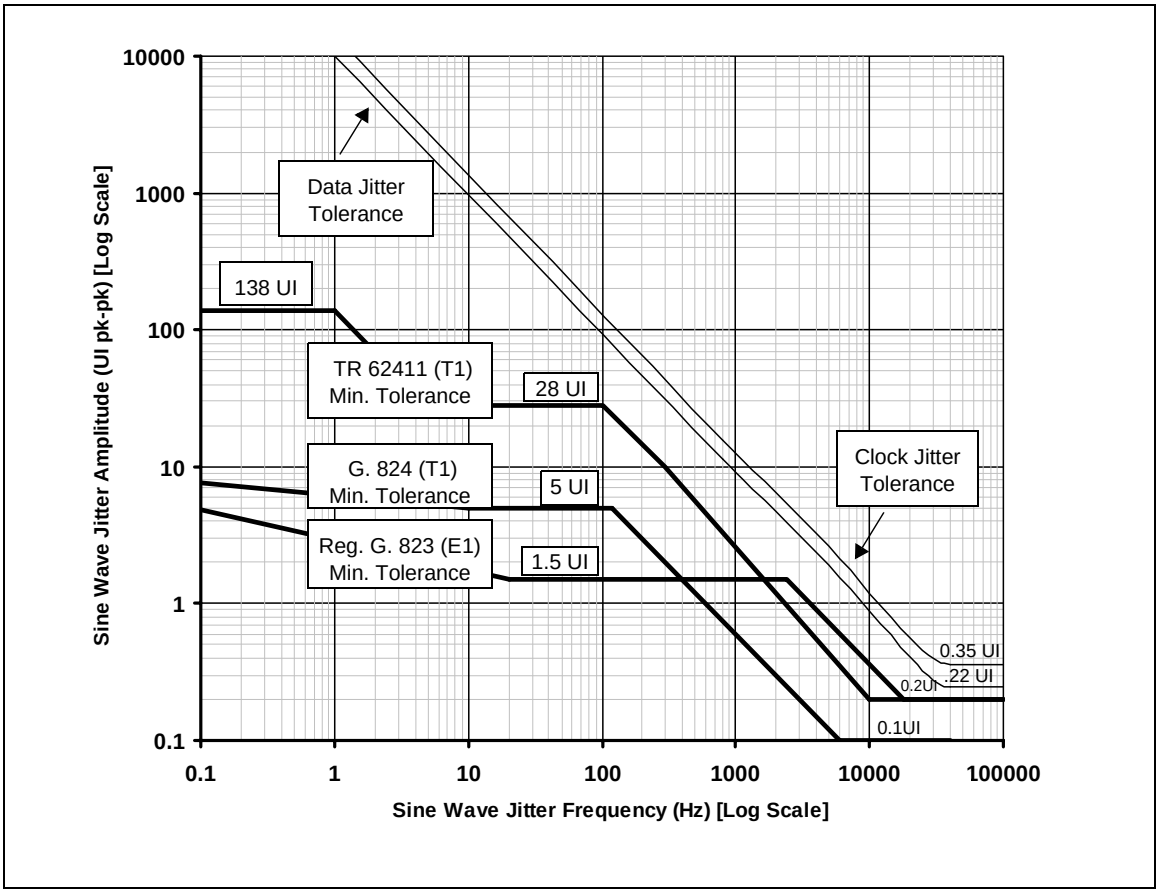
The Data Slicer extracts the data from the equalized signal by comparing the differential inputs to threshold values. The threshold values are dynamically set, based on a percentage of the peak level obtained by the peak detector. The percentage is 50% of peak for both DS1 and CEPT. Dynamically adjusting the threshold values ensures optimum signal-to-noise ratio. If the SQUELCH bit is set in the LIU Configuration register [LIU_CR; addr 020] and the input signal level is below threshold for the entire AGC observation period (EYEOPEN = 0), Data Slicer output is forced to all 0s.

2.2.2 Clock Recovery

2.2.2.1 Phase Locked Loop

The Receive Phase Locked Loop (RPLL) recovers the line rate clock from the Data Slicer dual rail outputs. The RPLL generates a recovered clock that tracks the jitter in the data from the Data Slicer, and sustains the data-to-clock phase relationship in the absence of incoming pulses. Figure 2-7 illustrates the Receive LIU's input clock and data jitter tolerance.

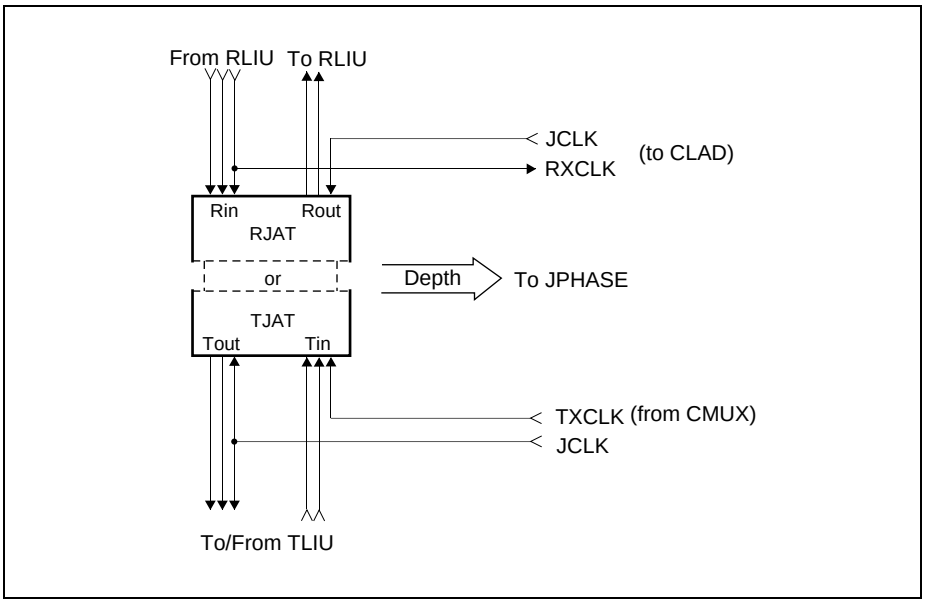
Figure 2-7. Receive Input Jitter Tolerance



2.3 Jitter Attenuator

The Jitter Attenuator (JAT), illustrated in Figure 2-8, attenuates jitter in the receive or transmit path, but not both simultaneously. In the receive configuration, the line signal is recovered by the RLIU and is dejittered before it is decoded by the RCVR. In the transmit configuration, the encoded signal from the transmit block is dejittered before it is transmitted by the Transmit Line Interface Unit (TLIU). The JAT receive/transmit configuration is done through the JDIR bit in the Jitter Attenuator Configuration register [JAT_CR; addr 002]. The JAT can also be completely disabled using the Jitter Attenuation (JEN) bit in the JAT_CR register.

Figure 2-8. Jitter Attenuator Block Diagram



2.3.1 Elastic Store

The elastic store size (RJAT or TJAT) is configurable using JSIZE[2:0] in the JAT_CR. The elastic store sizes available are 8, 16, 32, 64, and 128 bits. The 32-bit elastic store depth is sufficient to meet jitter tolerance requirements in cases where the jitter attenuator cutoff frequency is programmed at 6 Hz or below, and when the selected clock reference is frequency-locked. The larger elastic store depths allows greater accumulated phase offsets. For example, the 128-bit depth can tolerate up to ±64 bits of accumulated phase offset.

Since the elastic store is a fixed size, it can overflow and under-run. Overflow occurs when the elastic store is full; under-run occurs when the elastic store is empty. If either of these two conditions occurs, the Jitter Attenuator Elastic Store Limit Error bit (JERR) in the Error Interrupt Status register [ISR5; addr 006] is set. To determine if an overflow or under-run occurs, the Jitter Attenuator Empty/Full bit (JMPTY) must be read from the Receive LIU Status register [RSTAT; addr 021].

The elastic store is a circular buffer with independent read and write pointers. The difference between the read and write pointers is the phase error (JPHASE) between the input and output clocks of the jitter attenuator and is used to generate JCLK. The read and write pointers are initialized using JCENTER in the JAT_CR. JCENTER resets the write pointer and forces the elastic store read pointer to 1 half of the programmed JSIZE. JCENTER also resets the JMPTY status, so JMPTY must be read before JCENTER is written.

If JDIR is configured to put the jitter attenuator in the receive path, the write pointer is driven by the Receive Clock (RXCLK), and the read pointer is driven by the dejittered recovered clock (JCLK). The dejittered recovered clock output is available on the RCKO pin if the output is enabled using RCKO_OE in the Programmable Output Enable register [POE; addr 019]. The dejittering of the recovered clock is done by the Clock Rate Adapter Block (CLAD). CLAD is described later in this document.

If JDIR is configured to put the jitter attenuator in the transmit path, the write pointer is driven by the Transmit Clock (TXCLK), and the read pointer is driven by the dejittered transmit clock (JCLK). TXCLK can be slaved to four different clock sources: Transmit Clock Input (TCKI), Receive Clock Output (RCKO), Receive System Bus Clock Input (RSBCKI), or Clock Rate Adapter Output (CLADO). The dejittered transmit clock is available on the TCKO pin when the output is enabled using TCKO_OE in POE.

The receive LIU input clock and data jitter tolerance meets *TR 62411-1990*, as illustrated in Figure 2-7. The JAT input jitter tolerance is illustrated in Figure 2-9. The JAT jitter transfer function meets *TR 62411-1990*, as defined in Figure 2-10 and Table 2-1.

Figure 2-9. CLAD/JAT Input Jitter Tolerance

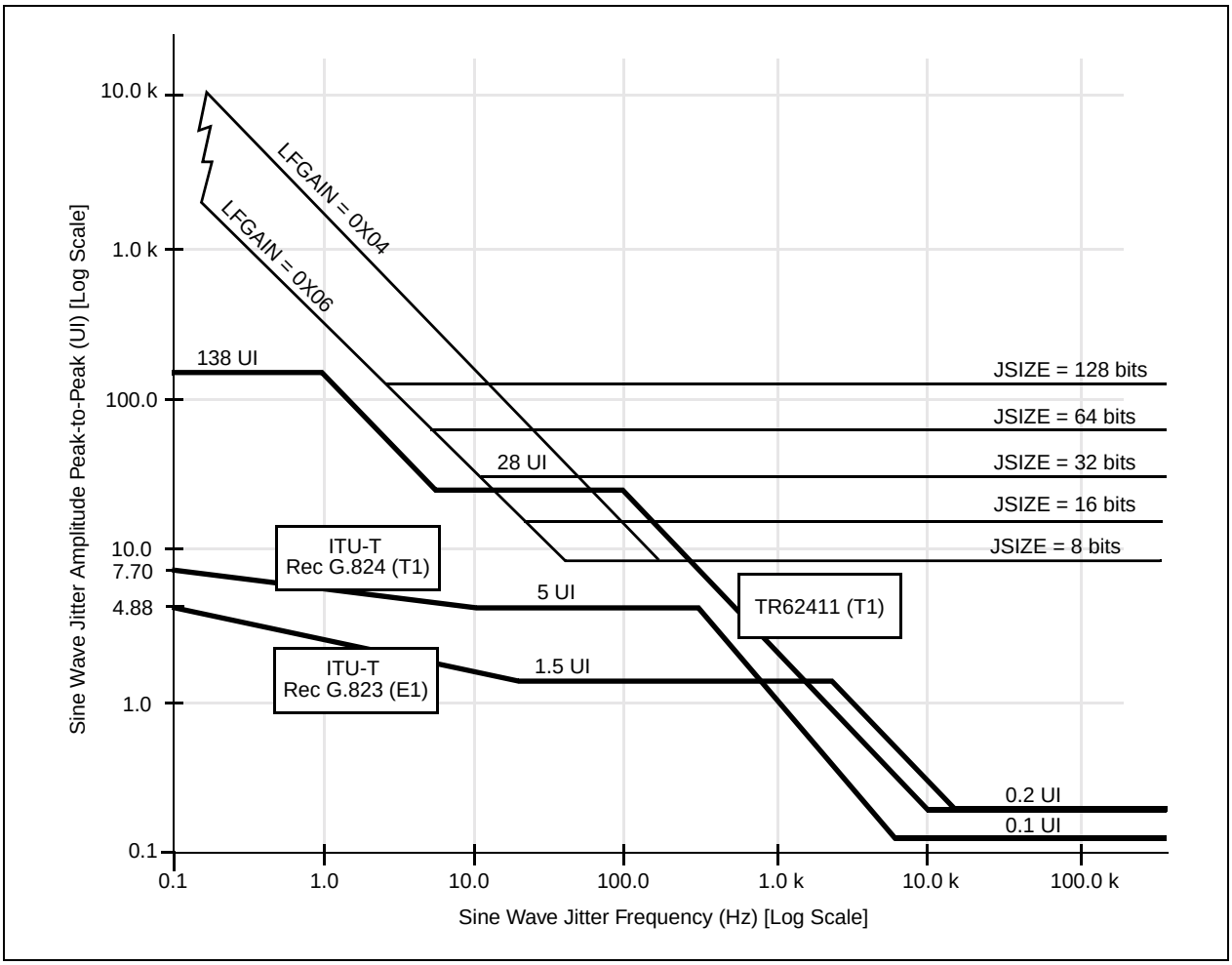


Figure 2-10. CLAD/JAT Jitter Transfer Functions

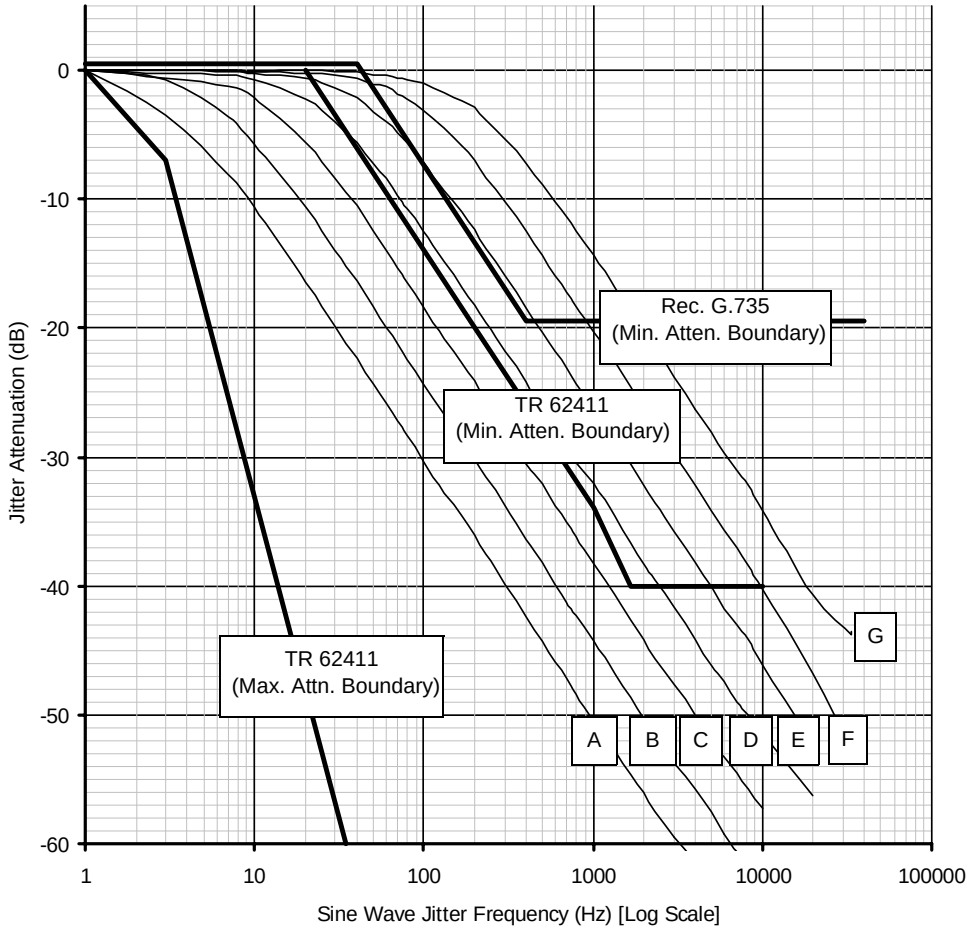


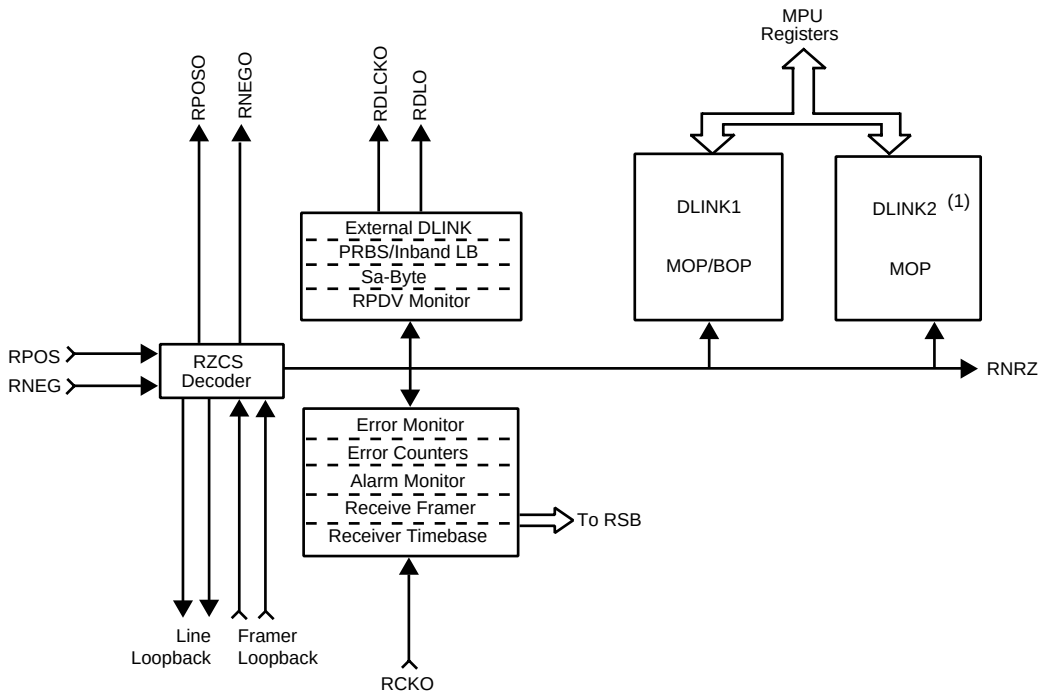
Table 2-1. CLAD/JAT Jitter Transfer Functions

Curve	JAT FIFO Size (bits)	LF Gain
A	128	0x06
B	128 64	0x05 0x06
C	128 64 32	0x04 0x05 0x06
D	64 32 16	0x04 0x05 0x06
E	32 16 8	0x04 0x05 0x06
F	16 8	0x04 0x05
G	8	0x04

2.4 Receiver

The Digital Receiver (RCVR) monitors T1/E1 overhead data and decodes positive and negative rail NRZ data from the RLIU into single rail NRZ data processed by the RSB. The RCVR, illustrated in Figure 2-11, is made up of the following elements: Zero Code Suppression (RZCS) Decoder, In-Band Loopback Code Detector, Error Counters, Error Monitor, Alarm Monitor, Test Pattern Receiver, Receive Framer, External Receive Data Link, and Receive Data Links.

Figure 2-11. RCVR Diagram



NOTE(S):
(1) DLINK2 not available in Bt8376 device.

2.4.1 ZCS Decoder

The Receive Zero Code Suppression (RZCS) decoder decodes the dual rail data (bipolar) into single rail data (unipolar). The Receive AMI bit (RAMI) in the Receiver Configuration register [RCR0; addr 040] controls whether the received signal is B8ZS/HDB3 decoded, depending on T1/E1N [addr 001] line rate selection, or depending on whether the RZCS decoder is bypassed. If the line code is unknown, the ZCSUB bit in Receive LIU Status [RSTAT; addr 021] indicates that 1 or more B8ZS/HDB3 substitution patterns have been received on the RTIP/RRING input. If the line code is B8ZS/HDB3 encoded, the RZCS bit in RCR0 must be set to keep the LCV counter from counting BPVs that are part of the B8ZS/HDB3 code.

2.4.2 In-Band Loopback Code Detection

The in-band loopback code detector circuitry detects receive data with in-band codes of configurable value and length. These codes can be used to request loopback of terminal equipment signals or other user-specified applications. The two codes are referred to as loopback-activate and loopback-deactivate, although the detectors need not be used only for loopback codes. Generally, any repeating 1–7 bit pattern can be selected. The loopback application is described in Section 9.3.1 of *ANSI T1.403-1995*. The loopback activate code is set in the Loopback Activate Code Pattern [LBA; addr 043]. The loopback deactivate code is set in the Loopback Deactivate Code Pattern [LBD; addr 044].

The sequence length for the loopback activate and deactivate codes can be programmed for 4, 5, 6, or 7 bits by setting the code length bits of the Receive Loopback Code Detector Configuration register [RLB; addr 042]. Shorter codes can be programmed by repeating the expected pattern (e.g., 3+3 bit code programmed as 6-bit code).

```
T1 In-Band Loopback Codes
      Activate 00001
      Deactivate 001
```

When a loopback code is detected, the LOOPUP or LOOPDN status bit is set in Alarm 2 register [ALM2; addr 048], and the corresponding LOOPUP or LOOPDN bit in Alarm 2 Interrupt Status register (ISR6; addr 005] is set. The loopback detection interrupt can be enabled using the Alarm 2 Interrupt Enable register [IER6; addr 00D]. When enabled, a loop-up or loop-down code detection causes the Alarm 2 Interrupt bit [ALARM2] to be set in the Interrupt Request register [IRR; addr 003] and generates an interrupt. Since loopbacks are not automatically initiated, the processor must intercept and interpret the interrupt status condition to determine when it must enable or disable the loopback control mechanism (e.g., LLOOP; addr 014).

The in-band loopback code detector circuitry is only applicable to T1 mode.

2.4.3 Error Counters

The following Performance Monitoring (PM) counters are available in the RCVR: Framing Bit Errors (FERR), CRC Errors (CERR), Line Code Violations (LCV), and Far End Block Errors (FEBE). All PM count registers are reset on read unless LATCH_CNT is set in the Alarm/Error/Counter Latch Configuration register [LATCH; addr 046]. LATCH_CNT enables the 1-second latching of counts coincident with the 1-second timer interrupt [ISR6; addr 005]. One-second latching of PM counts is required if AUTO_PRM responses are enabled. All PM counters can be disabled during RLOF, RLOS, and RAIS, using the STOP_CNT bit in the LATCH register.

NOTE: If STOP_CNT is negated, error monitoring during RLOF conditions will detect FERR, CERR, and FEBE according to the last known frame alignment.

2.4.3.1 Frame Bit Error Counter

The 12-bit Framing Bit Error Counter [FERR; addr 050 and 051] increments each time a receive Ft, Fs, T1DM, FPS, or FAS error is detected. Fs (T1) and NFAS (E1) errors can be included in the FERR count by setting FS_NFAS in Receive Alarm Signal Configuration [RALM; addr 045]. An interrupt is available to indicate that the FERR counter overflowed in the Counter Overflow Interrupt Status register [ISR4; addr 007].

2.4.3.2 CRC Error Counter

The 10-bit Cyclic Redundancy Check Error Counter [CERR; addr 052 and 053] increments each time a receive CRC4 (E1) or CRC6 (T1) error is detected. An interrupt is available to indicate that the CERR counter overflowed in ISR4.

2.4.3.3 LCV Error Counter

The 16-bit Line Code Violation Error Counter [LCV; addr 054 and 055] increments each time a receive Bipolar Violation (BPV)—not including line coding—is detected. The LCV count can include EXZ if EXZ_LCV in the Receive Alarm Signal Configuration register [RALM; addr 045] is set. EXZ can be configured [RZCS; addr 040] to be 8 or 16 successive 0s, following a 1. An interrupt is available to indicate that the LCV counter overflowed in ISR4.

2.4.3.4 FEBE Counter

The 10-bit Far End Block Error (FEBE) counter [FEBE; addr 056 and 057] increments each time the RCVR encounters an E1 far-end block error. An interrupt is available to indicate that the FEBE counter overflowed in ISR4.

2.4.4 Error Monitor

The following signal errors are detected in the RCVR: Frame Bit Error (FERR), MFAS Error (MERR), CAS Error (SERR), CRC Error (CERR), and Pulse Density Violations (PDVs). Each error type has an interrupt enable bit that allows an interrupt to occur marking the event, and has an interrupt register bit read by the interrupt service routine. All error status registers are reset on read unless the LATCH_ERR bit is set in the Alarm/Error/Counter Latch Configuration register [LATCH; addr 046]. LATCH_ERR enables the 1-second latching of alarms coincident with the 1-second timer interrupt [ISR6; addr 005]. With LATCH_ERR enabled, any error detected during the 1-second interval is latched and held during the following 1-second interval. LATCH_ERR allows the processor to gather error statistics based on the 1-second interval.

FERR is reported for the receive direction in the Error Interrupt Status register [ISR5; addr 006] and for the transmit direction in Pattern Interrupt Status [ISR0; addr 00B]. FERR indicates that 1 or more Ft/Fs/FPS frame bit errors or FAS pattern errors occurred since the last time the interrupt status was read. The FERR type is determined by the receive framer's configuration [CR0; address 001].

While CRC4 framing is enabled, MERR is reported for the receive direction in the Error Interrupt Status register [ISR5; addr 006] and for the transmit direction in Pattern Interrupt Status [ISR0; addr 00B]. MERR is only applicable in E1 mode and indicates that 1 or more MFAS pattern errors occurred since the last time the interrupt status was read.

While CAS framing is enabled, SERR is reported for the receive direction in the Error Interrupt Status register [ISR5; addr 006] and for the transmit direction in Pattern Interrupt Status [ISR0; addr 00B]. SERR is applicable only in E1 mode. In this mode, SERR indicates that 1 or more errors were received in the TS16 Multiframe Alignment Signal (MAS) since the last time the interrupt status was read.

CERR is reported for the receive direction in the Error Interrupt Status register [ISR5; addr 006] and for the transmit direction in Pattern Interrupt Status [ISR0; addr 00B]. CERR is only applicable in T1 ESF and E1 MFAS modes. In these modes, CERR indicates that 1 or more bit errors were found in the CRC4/CRC6 pattern block since the last time the interrupt status was read.

PDV is reported when the receive signal does not meet the pulse density requirements of *ANSI T1.403-1995* (Section 5.6). A PDV is declared whenever more than 15 consecutive zeros or the average ones density falls below 12.5%. RPDV is reported for the receive direction in the Alarm 1 Interrupt Status register [ISR7; addr 004].

2.4.5 Alarm Monitor

The following signal alarms are detected in the RCVR: Loss of Frame (LOF); Loss of Signal (LOS); Analog Loss of Signal (ALOS); Alarm Indication Signal (AIS); Remote Alarm Indication (RAI) or Yellow Alarm (YEL); Multiframe Yellow Alarm (MYEL); Severely Errored Frame (SEF); Change of Frame Alignment (COFA); and Multiframe AIS (MAIS). Each alarm has the following: a status register bit that reports the real-time status of the event, an interrupt enable bit that enables an interrupt to mark the event, and an interrupt register bit read by the interrupt service routine to identify the event that caused the interrupt. All alarm status registers are reset on read unless the LATCH_ALM bit is set in Alarm/Error/Counter Latch Configuration register [LATCH; addr 046]. LATCH_ALM enables the 1-second latching of alarms coincident with the 1-second timer interrupt [ISR6; addr 005]. With LATCH_ALM enabled, any alarm detected during the 1-second interval is latched and held during the following 1-second interval.

2.4.5.1 Loss of Frame

Receive Loss of Frame (RLOF) is declared when the receive data stream does not meet the framing criteria specified in the Receiver Configuration register [RCR0; addr 040].

If the line rate is E1 [T1/E1N; addr 001], RLOF is the logically OR'ed status of FAS, MFAS, and CAS alignment. These alignments, FRED, MRED and SRED, respectively, are available separately in the Alarm 3 Status register [ALM3; addr 049]. Once RLOF is declared, the LOF[1:0] bits in ALM3 report the reason for E1 loss of frame alignment. In T1 mode, RLOF is equal to FRED.

The RLOF real-time status is available in Alarm 1 Status register [ALM1; addr 047], and the interrupt status is set in the Alarm 1 Interrupt Status register [ISR7; addr 004]. The RLOF interrupt is enabled by setting RLOF in the Alarm 1 Interrupt Enable register [IER7; addr 00C].

An FRED count [FRED[3:0]; addr 05A] is also available in the SEF/LOF/COFA Alarm Counter [AERR; addr 05A]. An interrupt in Counter Overflow Interrupt Status [ISR4; addr 007] indicates that the FRED counter overflowed. COFA [1:0] is applicable to T1 modes only.

While T1 framing mode is enabled, the RLOF status and RLOF interrupt status are integrated over 2.0 to 2.5 seconds if the RLOF_INTEG bit is set in the Receive Alarm Signal Configuration register [RALM; addr 045]. The FRED count is unaffected by RLOF_INTEG.

2.4.5.2 Loss of Signal

If the line rate is T1, the criteria for Receive Loss of Signal (RLOS) is 100 contiguous 0s (consistent with the standard requirement of 175 ±75 zeros). If the line rate is E1, the criteria for RLOS is 32 contiguous 0s. RLOS is cleared upon detecting an average pulse density of at least 12.5% (occurring during a period of 114 bits starting with the receipt of a pulse, and where no occurrences of 100/32 contiguous 0s are detected).

The RLOS real-time status is available in ALM1, and the interrupt is available in ISR7. The XMTR can be configured to automatically generate an Alarm Indication Signal (AIS) in the transmit direction when RLOS is declared (see AUTO_AIS [TALM; addr 075].

2.4.5.3 Analog Loss of Signal

Receive Analog Loss of Signal (RALOS) is declared in analog receive mode, [RDIGI = 0; addr 020], when RTIP/RRING input signal amplitude is less than the programmed (VGA_MAX) threshold. In the digital receive mode, RDIGI = 1, RALOS is declared when the Receive Clock Input (RCKI) remains low for 125 µs. RALOS real-time status is available in ALM1; RALOS interrupt is available in ISR7.

2.4.5.4 Alarm Indication Signal

If the line rate is T1 [T1/E1N; addr 001], the criteria for Receive Alarm Indication Signal (RAIS) is the reception of 4 or fewer 0s in a period of 3 ms (4632 bits), and the assertion of RLOF. If the line rate is E1, RAIS is set when 2 consecutive double frames each contain 2 or fewer 0s out of 512 bits and FAS alignment is lost [FRED; addr 049]. RAIS real-time status is available in ALM1; RAIS interrupt is available in ISR7.

2.4.5.5 Yellow Alarm

The criteria for Yellow Alarm (YEL) is described in Table 3-13, *Receive Yellow Alarm Set/Clear Criteria*. YEL real-time status is available in ALM1; YEL interrupt is available in ISR7.

2.4.5.6 Multiframe YEL

The criteria for Multiframe Yellow Alarm is described in Table 3-13, *Receive Yellow Alarm Set/Clear Criteria*. MYEL real-time status is available in ALM1; MYEL interrupt is available in ISR7.

2.4.5.7 Severely Errored Frame

A SEF is reported when the receive signal does not meet the requirements of ANSI T1.231. SEF real-time status is available in ALM3. A 2-bit counter is also available [SEF; addr 05A]. An interrupt is available in ISR4 to indicate that the SEF counter overflowed.

2.4.5.8 Change of Frame Alignment

Each COFA increments a 2-bit counter [COFA; addr 05A]. An interrupt is available in ISR4 to indicate that the COFA counter overflowed.

2.4.5.9 Receive Multiframe AIS

Receive Multiframe AIS (RMAIS) is reported when the receive TS16 signal contains 3 or fewer 0s out of 128 bits in each multiframe over 2 consecutive multiframes according to the requirements of ITU–T Recommendation G.775. RMAIS is checked only in E1 CAS mode. RMAIS real-time status is available in ALM3 [addr 049].

2.4.6 Test Pattern Receiver

The test pattern receiver circuitry can sync on framed or unframed PRBS patterns and count bit errors. This feature is particularly useful for system diagnostics, production testing, and test equipment applications. The PRBS patterns available include 2E11-1, 2E15-1, 2E20-1, and 2E23-1. Each pattern can optionally include Zero Code Suppression (ZCS).

The Receive Test Pattern Configuration register [RPATT; addr 041] controls the test pattern receiver circuit. BSTART control bit (in RPATT) must be active to enable the test pattern receiver and to begin counting bit errors. RPATT controls the PRBS pattern, ZCS setting (ZLIMIT), and T1/E1 framing (FRAMED). RPATT selects which PRBS pattern the receiver should hunt for pattern sync. ZLIMIT selects the maximum number of consecutive zeros the pattern is allowed to contain. FRAMED mode informs the PRBS pattern receiver not to search for the pattern in the frame bit in T1 mode or search for the pattern in time slot 0 (and time slot 16 if CAS framing is selected) in E1 mode. CAS framing is selected by setting RFRAME[3] to 1 in the Primary Control register [CR0; addr 001]. If FRAMED is disabled, the PRBS pattern receiver searches all time slots for the test pattern.

The RESEED bit in RPATT informs the receive PRBS sync circuit to begin a PRBS pattern search. Once the search begins, any additional writes to RESEED restarts the pattern sync search at a different point in the pattern. The time to sync depends on the pattern and number of bit errors in the pattern.

Pattern sync is reported (when found) in PSYNC status of the Pattern Interrupt Status register [ISR0; addr 00B]. After pattern sync is found, the PRBS Pattern Error counter [BERR; addr 058 and 059] begins counting bit errors detected on the incoming pattern, provided that BSTART remains active. Error counting stops if the BSTART bit is cleared. BERR counter is reset to 0 after every read, or latched on every ONESEC interrupt as selected by LATCH_CNT [addr 046]. An interrupt is available to indicate the BERR counter overflowed in ISR4.

2.4.7 Receive Framing

Two framers are in the receive data stream: an offline framer and an online frame status monitor. The offline framer recovers receive frame alignment; the online framer monitors frame alignment patterns and recovers multiframe alignment in E1 modes. Frame and multiframe synchronization criteria used by the framers and monitoring criteria of the online framer are selected in RFRAME[3:0] of the Primary Control register [CR0; addr 001].

Receive frame synchronization is initiated by the online framer's activation of the Receive Loss of Frame (RLOF) status bit in the Alarm 1 Status register [ALM1; addr 047]. The RLOF criteria is set in the RLOFA, RLOFB, RLOFC, and RLOFD bits of the Receiver Configuration register [RCR01; addr 040]. The online framer supports the following LOF criteria for T1: 2 out of 4, 2 out of 5, and 2 out of 6. For E1, the online framer supports 3 out of 3, with or without 915 out of 1000 CRC errors.

Once RLOF is asserted, the offline framer automatically starts searching the receive data stream for a new frame alignment, provided that receive framing is enabled [RABORT; addr 040]. If receive framing is disabled, the offline framer does not automatically search for the frame alignment, but waits for a reframe command [RFORCE; addr 040] to start a frame alignment search. If RLOF integration is enabled [RLOF_INTEG; addr 045] the RLOF status [ALM1; addr 047] and RLOF interrupt status [ISR7; addr 004] is integrated for 2.0 to 2.5 seconds.

The online framer continuously monitors for RLOF condition [ALM1; addr 047] and searches for E1 multiframe alignment after basic frame alignment is recovered by the offline framer. Receive multiframe alignment is declared when multiframe alignment criteria are met, as shown in Table 2-2 and Table 2-3. The receive online framer reports multiframe errors, frame errors, and CRC errors in the Error Interrupt Status [ISR5; addr 006].

Table 2-2. Receive Framer Modes

T1/E1N	RFRAME[3:0]	Receive Framer Mode
0	000X	FAS Only
0	001X	FAS Only + BSLIP
0	010X	FAS + CRC
0	011X	FAS + CRC + BSLIP
0	100X	FAS + CAS
0	101X	FAS + CAS + BSLIP
0	110X	FAS + CRC + CAS
0	111X	FAS + CRC + CAS + BSLIP
1	0000	FT Only
1	0001	ESF + No CRC (FPS only)
1	0100	SF
1	0101	SF + JYEL
1	0110	SF + T1DM
1	1000	SLC + FSLOF
1	1001	SLC
1	1100	ESF + Mimic CRC
1	1101	ESF + Force CRC

Table 2-3. Criteria for Loss/Recovery of Receive Framer Alignment *(1 of 2)*

Mode	Description
FAS	Basic Frame Alignment (BFA) is recovered when the following search criteria are satisfied: • FAS pattern (0011011) is found in frame N. • Frame N+1 contains bit 2 equal to 1. • Frame N+2 also contains FAS pattern (0011011). During FAS-only modes, BFA is recovered when the following search criteria are satisfied: • FAS pattern (0011011) is found in frame N. • No mimics of the FAS pattern are present in frame N+1. • FAS pattern (0011011) is found in frame N+2. ***NOTE(S):*** If FAS pattern is not found in frame N+2, or if FAS mimic is found in frame N+1, the search restarts in frame N+2. Loss of FAS frame alignment (FRED) is declared when 1 of the following criteria is met: • Three consecutive FAS pattern errors are detected when the FAS pattern consists of a 7-bit (x0011011) pattern in FAS frames, and if FS_NFAS is also active [addr 045], the FAS pattern includes bit 2 of NFAS frames. • Loss of MFAS (MRED) is due to 915 or more CRC errors out of 1000. • Failure to locate two valid MFAS patterns within 8 ms after BFA. ***NOTE(S):*** In all cases, FRED causes next search for FAS alignment to begin 1 bit after the current FAS location.
BSLIP	FAS Bit Slip Enable. Applicable only for Dutch PTT national applications. If BSLIP is enabled, the online framer is allowed to change RX timebase by ±1 bit when a 1-bit FAS pattern slip is detected. BSLIP does not affect the offline framer's search criteria.
MFAS	CRC4 Multiframe Alignment is recovered when the following search criteria are satisfied: • BFA is recovered, identifying FAS and NFAS frames. • Within 8 ms after BFA, bit 1 of NFAS frames contains two MFAS patterns (001011xx). The second MFAS must be aligned with respect to first MFAS, but the second MFAS pattern is not necessarily received in consecutive frames. • Within 8 ms after BFA, bit 1 of NFAS frames contains the second MFAS pattern (001011xx), aligned to first MFAS. Loss of MFAS alignment (MRED) declared when 1 of the following criteria is met: • 915 or more CRC4 errors out of 1000 (submultiframe) blocks. • Loss of FAS (FRED). ***NOTE(S):*** If Disable 915 CRC Reframe is set [RLOFD; addr 040], then MRED is activated only by FRED.
CAS	CAS Multiframe Alignment is recovered when the following search criteria are satisfied: • BFA is recovered, identifying TS0 through TS31. • MAS (0000xxxx) multiframe alignment signal pattern is found in the first 4 bits of TS16, and 8 bits of TS16 in preceding frame contains non-0 value. Loss of CAS alignment (SRED) is declared when 1 of the following criteria is met: • Two consecutive MAS pattern errors are detected. • TS16 contains all 0s in 2 multiframes (32 consecutive frames). • Loss of FAS (FRED).
FT Only	Terminal frame alignment is recovered when the following occurs: The first valid Ft pattern (1010) is found in 12 alternate F-bit locations (3 ms), where F-bits are separated by 193 bits. During Ft-only mode, loss of frame alignment (FRED) is declared when the number of Ft bit errors detected meets selected loss of frame criteria [RLOFA–RLOFC; addr 040].

Table 2-3. Criteria for Loss/Recovery of Receive Framer Alignment *(2 of 2)*

Mode	Description
SF	Superframe alignment is recovered when terminal frame alignment is recovered, identifying Ft bits. Depends on SF submode: if JYEL, only Ft bits are used; Fs bits are ignored. If no JYEL, SF pattern (001110) found in Fs bits. During any SF mode, loss of frame alignment (FRED) is declared when the number of frame errors detected, either Ft or Fs bit errors, meets selected loss of frame criteria [RLOFA–RLOFC; addr 040]. FS_NFAS [addr 045] determines whether Fs bits are included in error count.
SLC	Superframe alignment is recovered when • Terminal frame alignment is recovered, identifying Ft bits. • SLC pattern (refer to Table A-3, *SLC-96 Fs Bit Contents*) is found in 16 of 36 Fs bits, according to Bellcore *TR-TSY-000008*. During SLC modes without FSLOF, loss of frame alignment (FRED) is declared when the number of Ft bit errors detected meets selected reframe criteria [RLOFA–RLOFC; addr 040].
FSLOF	FSLOF instructs the online framer to monitor 16 of 36 Fs bits (SLC multiframe pattern) for loss of frame alignment criteria. FS_NFAS [addr 045] must also be set to include Fs bits in loss of frame. FSLOF does not affect the offline framer's search criteria.
ESF	Extended Superframe alignment is recovered when A valid FPS candidate is located (001011). Candidate bits are each separated by 772 digits and are received without pattern errors. If there is only 1 valid FPS candidate and the mode is 1 of the following: No CRC mode—align to FPS, regardless of CRC6 comparison. Mimic CRC mode—align to FPS, regardless of CRC6 comparison. Force CRC mode—align to FPS, only if CRC6 is correct. If there are two or more valid FPS candidates and the mode is 1 of the following: No CRC mode—do not align (INVALID status). Mimic CRC mode—align to first FPS with correct CRC6. Force CRC mode—align to first FPS with correct CRC6. During any ESF mode, loss of frame alignment (FRED) is declared when: Number of FPS pattern errors detected meets selected loss of frame criteria [RLOFA–RLOFC; addr 040].
T1DM	During T1DM mode, frame alignment is recovered in two steps: 1. A 6-bit T1DM pattern (10111xx0) is found. 2. A valid F-bit pattern (Ft, Fs, or FPS) is found in the first six consecutive frames of the 12-frame cycle aligned to the T1DM pattern. During T1DM mode, loss of frame alignment (FRED) is declared when the number of frame errors detected, either Ft, Fs, or T1DM errors, meets selected loss of frame criteria [RLOFA–RLOFC; addr 040]. Fs_NFAS; addr 046] does not affect T1DM mode. ***NOTE(S):*** To meet Bellcore TA-TSY-000278, the processor must select SF + T1DM framer mode, RLOFC (2 of 6) reframe criteria, and FS_NFAS inactive.

The offline framer is shared between the RCVR and XMTR and can search in only one direction at any time. Consequently, the processor arbitrates which direction is searched by enabling the reframe request (RLOF and TLOF) for that direction.

The offline framer waits until the current search is complete (see [FSTAT; addr 017]) before checking for pending LOF reframe requests. If both online framers have pending reframe requests, the offline framer aligns to the direction opposite from that which was most recently searched. For example, if TLOF is pending at the conclusion of a receive search which timed out without finding alignment, the offline framer switches to search in the transmit direction. The TLOF switchover is prevented in the preceding example if the processor asserts TABORT to mask the transmit reframe request. TABORT does not affect TLOF status reporting. For applications that frame in only 1 direction, the opposite direction should be masked. If, at the conclusion of a receive search, TLOF status is asserted but masked by TABORT, the offline framer continues to search in the receive direction. For applications that frame in both directions, the processor can allow the offline framer to automatically arbitrate among pending reframe requests, or can elect to manually control reframe precedence. An example of manual control follows:

```
1   Initialize RABORT = 1 and TABORT = 1
2   Enable RLOF and TLOF interrupts
3   Read clear pending ISR interrupts
4   Release RABORT = 0
5   Call LOF Service Routine if either RLOF or TLOF interrupt;
    {
        (check current LOF status [ALM1, 2; addr 047, 048]
        If RLOF recovered and TLOF lost
        —Assert RABORT = 1
        —Release TABORT = 0
        If RLOF lost or TLOF recovered
        —Assert TABORT = 1
        —Release RABORT = 0
        }
```

The status of the offline framer can be monitored for diagnostic purposes using the Offline Framer Status register [FSTAT; addr 017]. The register reports the following:

- whether the offline framer is looking at the receive or transmit data streams (RX/TXN)
- whether the framer is actively searching for a frame alignment (ACTIVE)
- whether the framer found multiple framing candidates (TIMEOUT)
- whether the framer found frame sync (FOUND)
- whether the framer found no frame alignment candidates (INVALID)

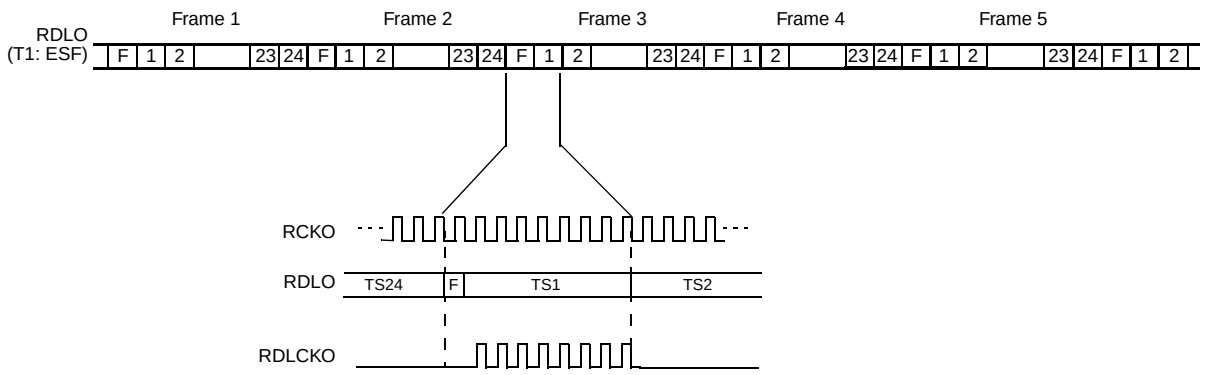
NOTE: These status bits are updated in real time and might be active for only very short (1-bit) periods of time.

2.4.8 External Receive Data Link

The External Data Link (DL3) provides signal access to any bit(s) in any time slot of all frames, odd frames, or even frames, including T1 framing bits. Pin access to the DL3 receiver is provided through RDLCKO and RDLO. These two pins serve as the DL3 clock output (RDLCKO) and data output (RDLO). The data link mode of the pins is selected using the RDL_IO bit in the Programmable Input/Output register [PIO; addr 018].

Control of DL3 is provided in two registers: External Data Link Channel [DL3_TS; add 015] and External Data Link Bit [DL3_BIT; addr 016]. RDL3 is set up by selecting the bit(s) (DL3_BIT) and time slot [TS[4:0]; addr 015] to be monitored, and then enabling the data link [DL3EN; addr 015], which starts the RDLCKO and TDLCKO gapped clock outputs that mark the selected bits, as shown in Figure 2-12.

Figure 2-12. Receive External Data Link Waveforms



NOTE(S): This waveform represents time slot 1 extraction. Any combination of bits can be selected.

2.4.9 Sa-Byte Receive Buffers

The Sa-Byte buffers give read access to the odd frame Sa bits in E1 mode. Five receive Sa-Byte buffers [RSA4 to RSA8; addr 05B to 05F] are available. As a group, the buffers are updated every multiframe from Sa-bits received in TS0. This gives the processor up to 2 ms after the receive multiframe interrupt [RMF; addr 008] occurs to read any Sa-Byte buffer before the buffer content changes.

2.4.10 Receive Data Link

The RCVR contains two independent data link controllers (DL1 and DL2) and a Bit-Oriented Protocol (BOP) transceiver. DL1 and DL2 can be programmed to send and receive HDLC formatted messages in the Message-Oriented Protocol (MOP) mode. Alternatively, unformatted serial data can be sent and received over any combination of bits within a selected time slot or F-bit channel. The BOP transceiver can preemptively receive and transmit BOP messages, such as ESF Yellow Alarm.

2.4.10.1 Data Link Controllers

The Bt8370 and Bt8375 provide two internal data link controllers, and the Bt8376 provides a single controller (DL1). DL1 and DL2 control two serial data channels operating at multiples of 4 kbps—up to the full 64 kbps time slot rate—by selecting a combination of bits from odd, even, or all frames. Both DL1 and DL2 support the following: ESF Facilities Data Link (FDL), SLC-96 Data Link, Sa Data Link, Common Channel Signaling (CCS), Signaling System #7 (SS7), ISDN LAPD channels, Digital Multiplexed Interface (DMI) Signaling in TS24, ETSI V.5.1 and V.5.2 control channels. DL1 and DL2 each contain a 64-byte receive buffer that functions as either programmable length circular buffers or full-length data FIFOs.

Both data link controllers are configured identically, except for their offset in the register map. The DL1 address range is 0A4 to 0AE, and the DL2 address range is 0AF to 0B9. From this point on, DL1 is used to describe the operation of both data link controllers.

DL1 is enabled using the DL1 Control register [DL1_CTL; addr 0A6]. DL1 does not function until it is enabled. DL1_CTL also controls the format of the data. The following data formats [DL1[1:0]; addr 0A6] are supported on the data link: Frame Check Sequence (FCS), non-FCS, Pack8, or Pack6. FCS and non-FCS are HDLC formatted messages. Pack8 and Pack6 are unformatted messages with 8 bits per FIFO access, or 6 bits per FIFO access, respectively (see Table 2-4).

Table 2-4. Commonly Used Data Link Settings

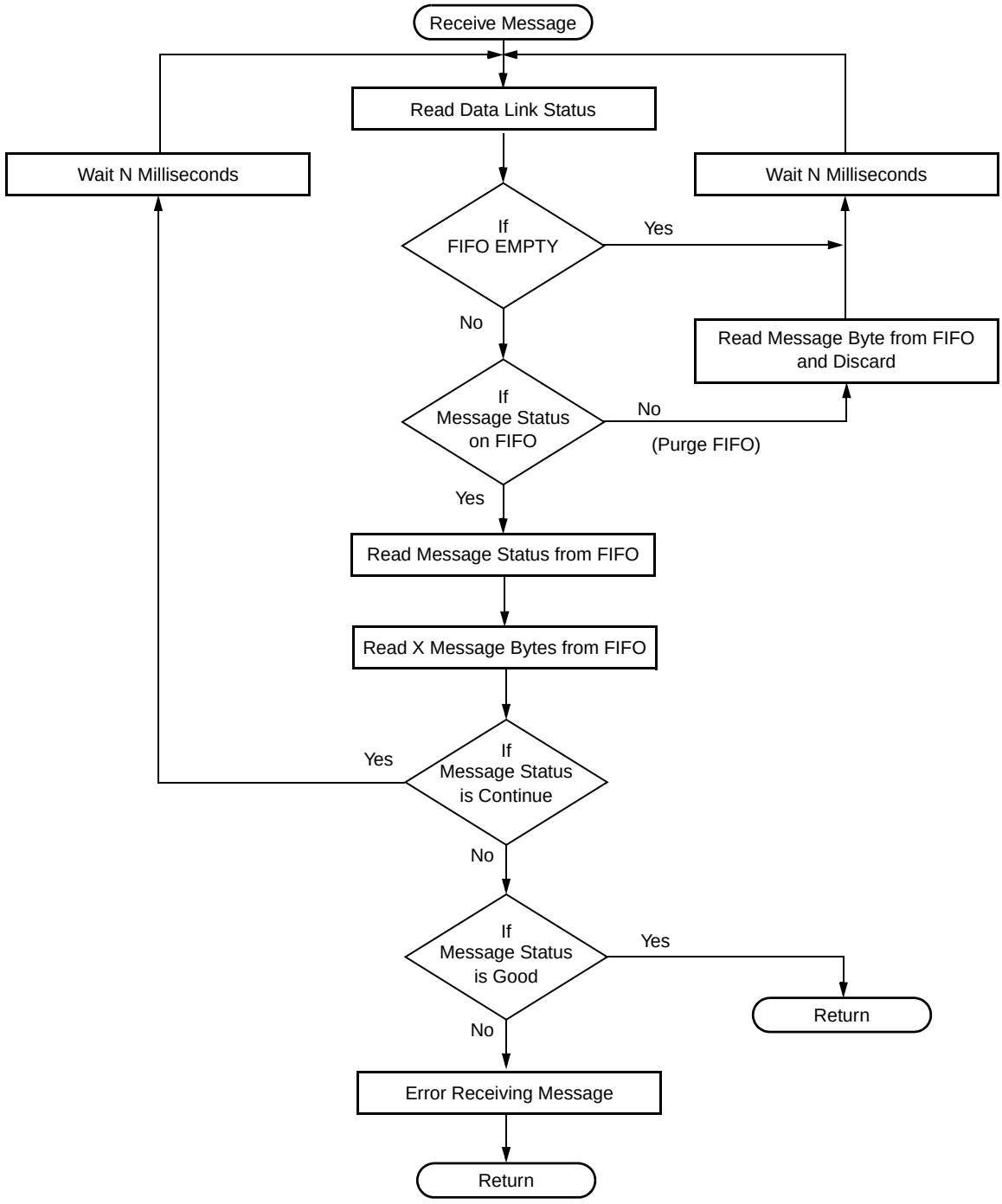
Data Link	Frame	Time Slot	Time Slot Bits	Mode
ESF FDL	Odd	0 (F-bits)	Don't Care	FCS
T1DM R Bit	All	24	00000010	FCS
SLC-96	Even	0 (F-bits)	Don't Care	Pack6
ISDN LAPD	All	N	11111111	FCS
Sa4	Odd	1	00001000	FCS
NOTE(S): N represents any T1/E1 time slot.				

The time slot and bit selection are performed through the DL1 Time Slot Enable register [DL1_TS; addr 0A4] and the DL1 Bit Enable register [DL1_BIT; addr 0A5]. The DL1 Time Slot Enable register selects the frames and time slot to extract the data link. The frame select tells the receiver to extract the time slot in all frames, odd frames, even frames. The time slot enable is a value between 0 and 31 that selects which time slot to extract. The DL1 Bit Enable register selects which bits are extracted in the selected time slot. Refer to Table 2-4 for the common frame, time slot, time slot bits, and modes used.

The Receive Data Link FIFO #1 [RDL1; addr 0A8] is 64 bytes long. The Receive FIFO is formatted differently than the transmit FIFO. The Receive FIFO contains not only received messages, but also a status byte preceding each message that specifies the size of the received message and the status of that message. The message status reports if the message was aborted, received with a correct/incorrect FCS, or continued. A continued message means the byte count represents a partial message. Once all message bytes are read, the FIFO contains another status byte. Message bytes can be differentiated from status bytes in the FIFO by reading the RSTAT1 bit in the RDL #1 Status register [RDL1_STAT; addr 0A9]. RSTAT1 reports whether the next byte read from the FIFO is a status byte or some number of message bytes.

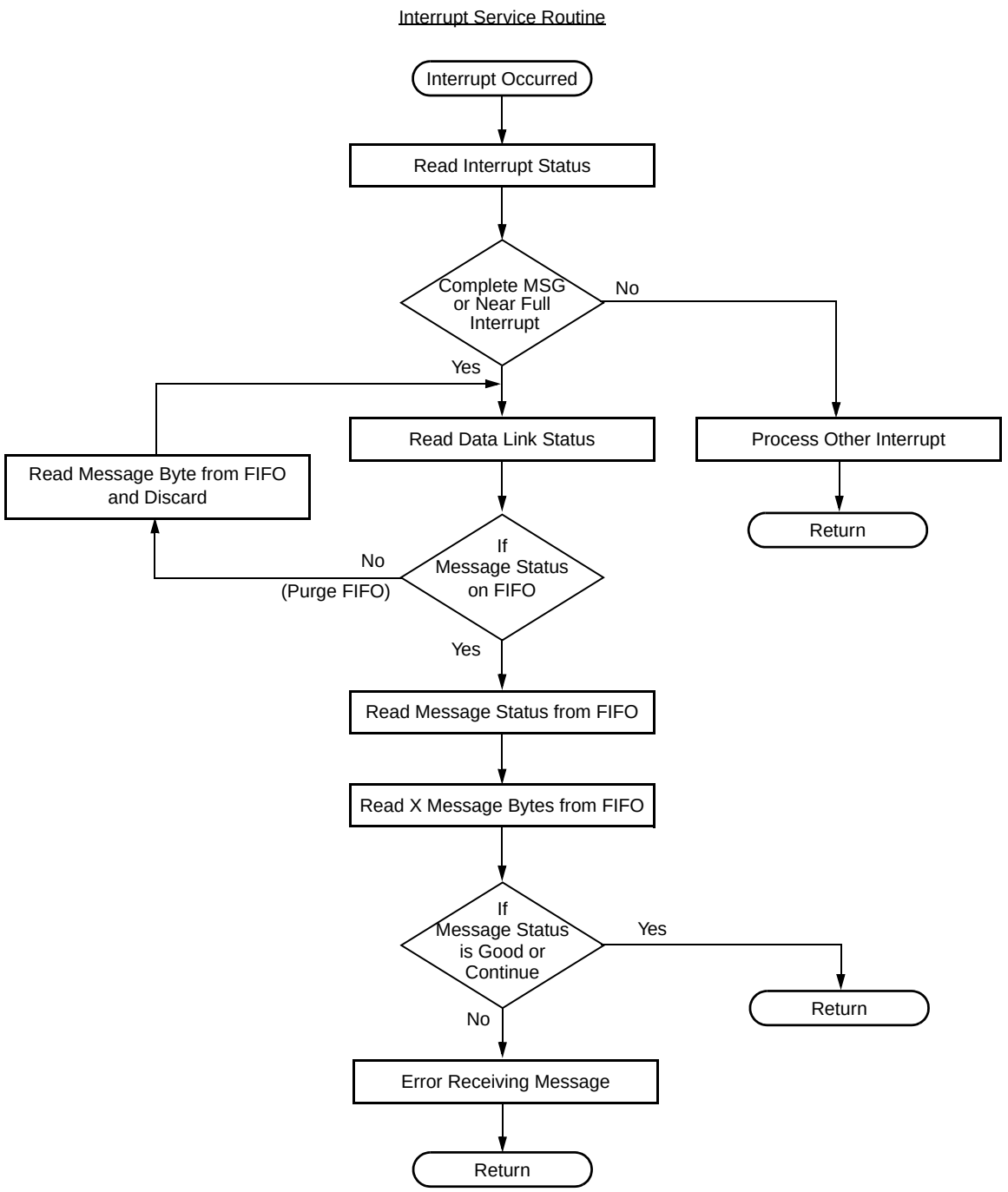
The receive data link controller has a versatile microprocessor interface that can be tuned to the system's CPU bandwidth. For systems with 1 CPU dedicated to 1 Bt8370, the data link status can be polled. For systems where a single CPU controls multiple Bt8370s, the data link can be interrupt-driven. See Figures 2-13 and 2-14 for a high-level description of polling and interrupt driven Receive Data Link Controller software.

Figure 2-13. Polled Receive Data Link Processing



NOTE(S): Message status contains number of message bytes (X) in FIFO, where (X) equals 0 during idle channel or errored message.

Figure 2-14. Interrupt Driven Receive Data Link Processing



NOTE(S): Message status contains number of message bytes (X) in FIFO where (X) equals 0 during idle channel or errored message.

Using the receive FIFO, an entire block of data can be received with very little microprocessor interrupt overhead. Block transfers from the FIFO can be controlled by the Near Full Threshold in the FIFO Fill Control register [RDL1_FFC; addr 0A7]. The Near Full Threshold is a user-programmable value between 0 and 63. This value represents the maximum number of bytes that can be placed into the receive FIFO without the near full being declared. Once the threshold is set, the Near Full Status (RNEAR1) in RDL #1 Status [RDL1_STAT; addr 0A9] is asserted when the Near Full Threshold is reached. An interrupt, RNEAR, in Data Link 1 Interrupt Status [ISR2; addr 009], is also available to mark this event.

The Bt8370/8375/8376 uses a hierarchical interrupt structure, with 1 top-level interrupt cause register directing software to the lower levels (see Interrupt Request register; addr 003). Of all the interrupt sources, the two most significant bandwidth requirements are signaling and data link interrupts. Each data link controller has a top-level interrupt status register that reports data link operations (see Data Link 1 and 2 Interrupt Status registers [ISR2, ISR1; addr 009 and 00A). The processor uses a two-step interrupt scheme for the data link:

1. It reads the Interrupt Request register.
2. It uses that register value to read the corresponding Data Link Interrupt Status register.

2.4.10.2 RBOP Receiver

The Receive Bit-Oriented Protocol (RBOP) receiver receives BOP messages, including the ESF Yellow Alarm, which consists of repeated 16-bit patterns with an embedded 6-bit codeword as shown in this example:

```
0xxxxxx0 11111111 (received right to left)

[543210] RBOP = 6-bit codeword
```

The BOP message channel is configured to operate over the same channel selected by Data Link #1 [DL1_TS; addr 0A4]. It must be configured to operate over the FDL channel so RBOP can detect priority, command, and response codeword messages according to ANSI T1.403, Section 9.4.1.

RBOP is enabled using the RBOP_START bit in Bit Oriented Protocol Transceiver register [BOP; address 0A0]. BOP codewords are received in the Receive BOP Codeword register [RBOP; addr 0A2], which contains the 6-bit codeword, a valid flag (RBOP_VALID), and a lost flag (RBOP_LOST). The valid flag is set each time a new codeword is put in RBOP, and is cleared on reading the codeword. The lost flag indicates a new codeword overwrote a valid codeword before the processor read it.

The BOP receiver can be configured to update RBOP using a message length filter and integration filter. The receive BOP message length filter [RBOP_LEN; addr 0A40] sets the number of successive identical messages required before RBOP is updated. RBOP_LEN can be set to 1, 10, and 25 messages. When enabled, the RBOP integration filter [RBOP_INTEG; add 0A0] requires receipt of two identical consecutive 16-bit patterns, without gaps or errors between patterns, to validate the first codeword. RBOP integration is needed to meet the codeword detection criteria while receiving 1 1/1000 bit error ratio.

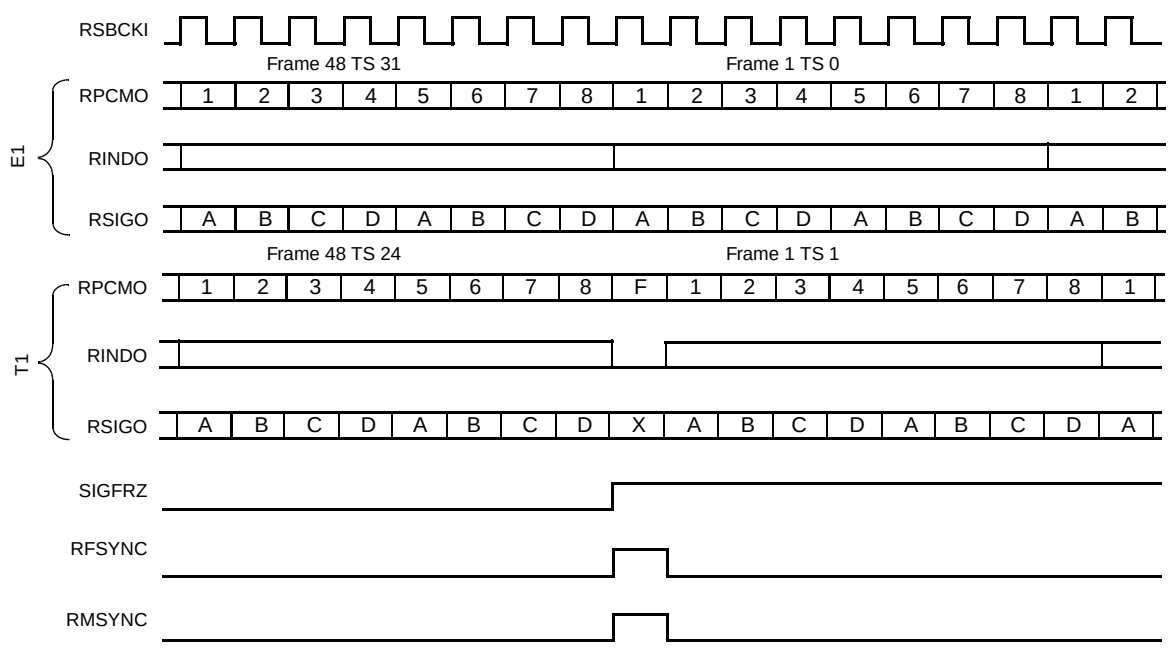
The real-time status of the codeword reception can be monitored using the RBOP_ACTIVE bit in the BOP Status register [BOP_STAT; addr 0A3]. Each time a message is put in RBOP register, an interrupt is generated, and the RBOP bit is set in the Data Link 2 Interrupt Status register [ISR1; addr 00A].

2.5 Receive System Bus

The Receive System Bus (RSB) provides a high-speed, serial interface between the RCVR and the system bus. The system bus is compatible with the Mitel ST-Bus, the Siemens PEB Bus, and the AT&T CHI Bus, and directly connects to other CONEXANT serial TDM bus devices with no need for any external circuitry.

The RSB has the following seven pins: Receive System Bus Clock (RSBCKI), Receive PCM Data (RPCMO), Receive Signaling Data (RSIGO), Receive Frame Sync (RFSYNC), Receive Multiframe Sync (RMSYNC), Receive Time Slot Indicator (RINDO), and Signaling Freeze (SIGFRZ). Figure 2-15 illustrates the relationship between these signals. (Pin definitions are provided in Table 1-1, *Hardware Signal Definitions*.) RSB data outputs can be configured to output on the rising or falling edge of RSBCKI. See the Receive System Bus Configuration register [RSB_CR; addr 0D1].

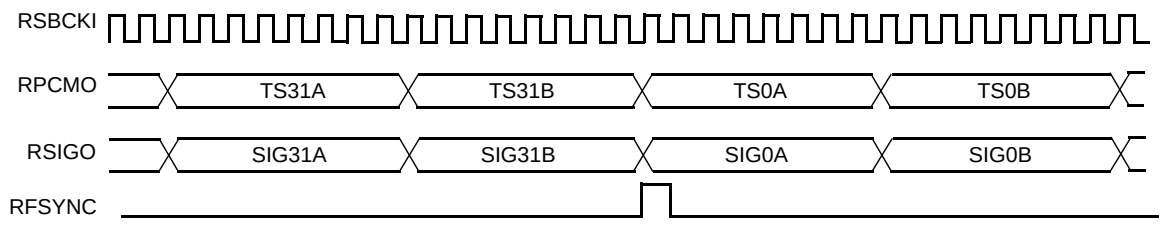
Figure 2-15. RSB Waveforms



NOTE(S): The Receive Multiframe Sync (RMSYNC) occurs every 6 ms for 48 T1 or 48 E1 frames.

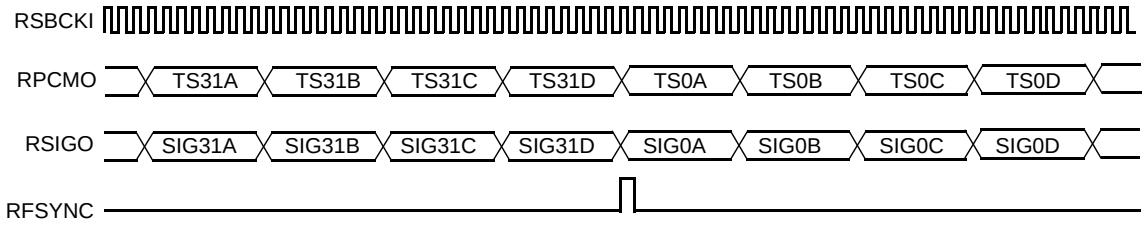
The RSB supports five system bus rates (MHz): 1.536, 1.544, 2.048, 4.096, and 8.192. The T1 rate without a framing bit is 1.536 MHz, consisting of 24 time slots. The T1 rate with a framing bit 1.544 MHz. The E1 rate is 2.048 MHz, consisting of 32 time slots. Twice the E1 rate is 4.096 MHz, consisting of 64 time slots. Four times the E1 rate is 8.192 MHz, consisting of 128 time slots. The 4.096 and 8.192 MHz bus modes contain multiple bus members (A, B, C, D) which allow multiple T1/E1 signals to share the same system bus. This is done by interleaving the time slots to a maximum of four Bt8370s without external circuitry (see Figures 2-15 and 2-17). The system bus rate is independent of the line rate and must be selected using the System Bus Interface Configuration register [SBI_CR; addr 0D0].

Figure 2-16. RSB 4.096 MHz Bus Mode Time Slot Interleaving



NOTE(S): A and B time slot data comes from different Bt8370s. Output data on rising edge clock, RCPM_NEG = 0 [addr 0D1]. Output sync on rising edge clock, RSYN_NEG = 0 [addr 0D1]. RSBCKI operates at 1 times the data rate. RSB.OFFSET equals 0.

Figure 2-17. RSB 8.192 MHz Bus Mode Time Slot Interleaving



NOTE(S): A, B, C, and D data comes from different Bt8370s. Output data on rising edge clock, RCPM_NEG = 0 [addr 0D1]. Output sync on rising edge clock, RSYN_NEG = 0 [addr 0D1]. RSBCKI operates at 1 times the data rate. RSB.OFFSET equals 0.

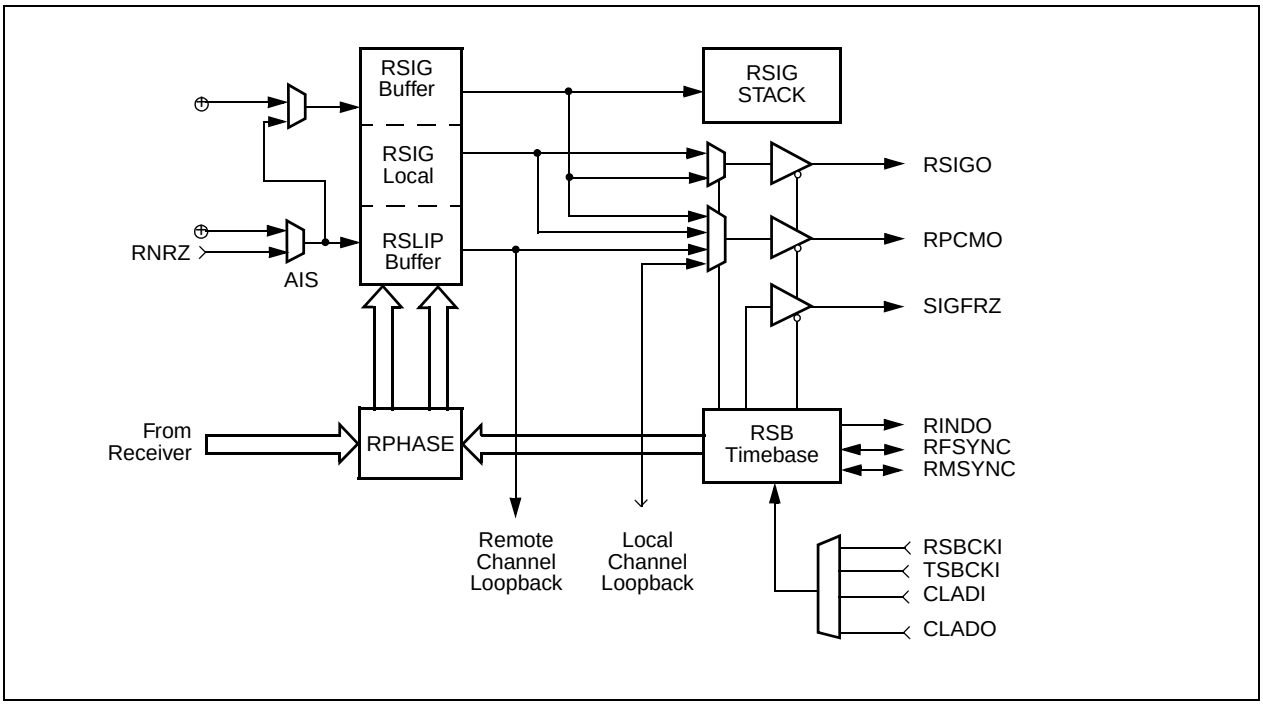
The RSB maps line rate time slots to system bus time slots. The 24- (DS1) or 32- (CEPT) line rate time slots can be mapped to 24, 32, 64, or 128 system bus time slots as listed in Table 2-5. The system bus rate must be greater than or equal to the line rate, except for 1.536 MHz bus mode.

Table 2-5. RSB Interface Time Slot Mapping

Line Rate (MHz)	Source Channels	System Bus Rate (MHz)	Destination Time Slots
1.544	24	1.536	24
	24	1.544	24
	24	2.048	32
	24	4.096	64
	24	8.192	128
2.048	32	2.048	32
	32	4.096	64
	32	8.192	128

The RSB, illustrated in Figure 2-18, consists of a timebase, slip buffer, signaling buffer, and signaling stack.

Figure 2-18. RSB Diagram



2.5.1 Timebase

The RSB timebase synchronizes RFSYNC, RMSYNC, and RINDO with the Receive System Bus Clock (RSBCKI). The RSBCKI can be slaved to 4 clock sources: Receive System Bus Clock Input (RSBCKI), Transmit System Bus Clock Input (TSBCKI), Clock Rate Adapter Input (CLADI), or Clock Rate Adapter Output (CLADO). The RSB clock selection is made through the Clock Input Mux register [CMUX; addr 01A]. The system bus clock can also be configured to run at twice the data rate by setting the X2CLK bit in the System Bus Interface Configuration register [SBI_CR; addr 0D0].

RFSYNC and RMSYNC can be individually configured as inputs or outputs [PIO; addr 018]. RFSYNC and RMSYNC must be configured as inputs when the RSB timebase is slaved to the system bus [SBI_OE; addr 0D0]. RFSYNC and RMSYNC must be configured as outputs when the RSB timebase is master of the system bus. RFSYNC and RMSYNC can also be configured as rising or falling edge outputs [RSB_CR; addr 0D1]. In addition to having RFSYNC and RMSYNC active on the frame boundary, a programmable offset is available to select the time slot and bit offset in the frame. See the Receive System Bus Sync Time Slot Offset [RSYNC_TS; addr 0D3] and the Receive System Bus Sync Bit Offset [RSYNC_BIT; addr 0D2].

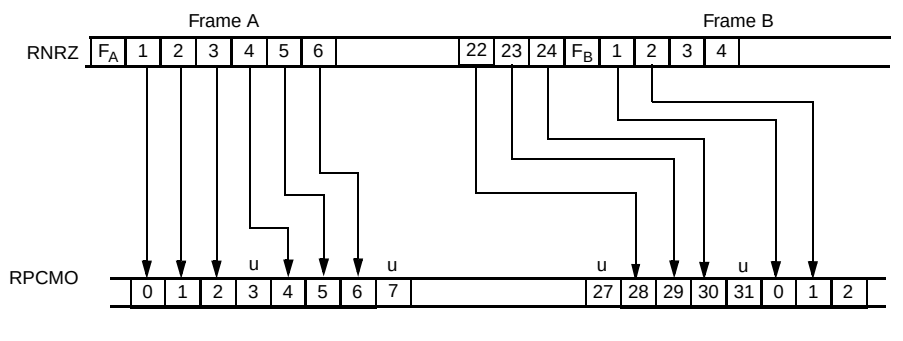
2.5.2 Slip Buffer

The 64-byte Receive PCM Slip Buffer [RSLIP; addr 1C0 to 1FF] resynchronizes the Receiver Clock (RXCLK) and data (RNRZ) to the Receive System Bus Clock (RSBCK) and data (RPCMO). RSLIP acts like an elastic store by clocking RNRZ data in with RXCLK and clocking PCM data out on RPCMO with RSBCK.

If the system bus rate is greater than the line rate (i.e., T1 line rate and E1 system bus rate), there is a mismatched number of time slots. The mapping of line rate time slots to system bus time slots is done by time slot assignments with the ASSIGN bit in the System Bus Per-Channel Control register [SBC0 to SBC31; addr 0E0 to 0FF]. ASSIGN selects which system bus time slots are used to transport line rate time slots. Time slot mapping is done by mapping the first line rate time slot to the first assigned system bus time slot. For example, T1 to E1 mapping might make every fourth time slot unassigned (i.e., 3, 7, 11, 15, 19, 23, 27, 31); see Figure 2-19. This distribution of unassigned time slots averages out the idle time slots and optimizes the slip buffer use.

NOTE: All line rate time slots must be assigned to a system bus time slot.

Figure 2-19. T1 Line to E1 System Bus Time Slot Mapping



NOTE(S):
1. u = unassigned time slots
2. F_A = T1 frame bit for frame A

RSLIP has four modes of operation: Two-Frame Normal, 64-bit Elastic, Two-Frame Short, and Bypass. RSLIP mode is set in the Receive System Bus Configuration register [RSB_CR; addr 0D1]. RSLIP is organized as a 2-frame buffer. This allows MPU access to frame data, regardless of the RSLIP mode selected. Each byte offset into the frame buffer is a different time slot: offset 0 in RSLIP is always time slot 0 (TS0), offset 1 is always TS1, and so on. The slip buffer has processor read/write access.

In Normal mode, the slip buffer total depth is two 193-bit frames (T1) or two 256-bit frames (E1). Data is written to the slip buffer using RXCLK and read from the slip buffer using RSBCK. If a slight rate difference between the clocks occurs, the slip buffer changes from its initial condition—approximately half full—by either adding or removing frames. If RXCLK writes to the slip buffer faster than RSBCK reads the data, the buffer fills up. When the slip buffer in Normal mode is full, an entire frame of data is deleted. Conversely, if RSBCK reads the slip buffer faster than RXCLK writes the data, the buffer becomes empty. When the slip buffer in Normal mode is empty, an entire frame of data is duplicated. When an entire frame is deleted or duplicated it is known as a Frame Slip (FSLIP), which is always 1 full frame of data. The FSLIP status is reported in the Slip Buffer Status register [SSTAT; addr 0D9]. In T1 mode, the F-bit is treated as part of the frame and can slip accordingly.

In 64-bit Elastic mode, the slip buffer total depth is 64 bits, and the initial throughput delay is 32 bits, half of the total depth. Similar to Normal mode, Elastic mode allows the system bus to operate at any of the programmable rates, independent of the line rate. The advantage of this mode over the Normal mode is that throughput delay is reduced from 1 frame to an average of 32 bits, and the output multiframe always retains its alignment with respect to the output data. The disadvantage of this mode is handling the full and empty buffer conditions. In Elastic mode, an empty or full buffer condition causes an Uncontrolled Slip (USLIP). Unlike an FSLIP, a USLIP is of unknown size within the range of 1 to 256 bits of data. The USLIP status is reported in SSTAT.

The Two-Frame Short mode combines the depth of the Normal mode with the throughput delay of the Elastic mode. The Two-Frame Short mode begins in the Elastic mode with a 32-bit initial throughput delay, and switches to the Normal mode when the buffer becomes empty or full; thereafter the Two-Frame Short and Normal mode perform identically. If the slip buffer is full (two frames) in the Two-Frame Short mode, an FSLIP is reported, after which the slip buffer and Two-Frame mode perform identically.

In Bypass mode, data is immediately clocked through RSLIP from the RCVR to RSB, and RCKO internally replaces the system bus clock.

2.5.3 Signaling Buffer

The 32-byte Receive Signaling Buffer [RSIG; addr 1A0 to 1BF] stores a single multiframe of signaling data. Each byte offset into RSIG contains signaling data for a different time slot: offset 0 stores TS0 signaling data, offset 1 stores TS1 signaling data and so on. The signaling data is stored in the least significant 4 bits of RSIG. The output signaling data is stored in the most significant 4 bits of RSIG. Similar to RSLIP, RSIG buffer has read/write processor access to read or overwrite signaling information. RMSYNC extracts robbed-bit signaling from RSIG onto RPCMO; RFSYNC extracts ABCD signaling from RSIG onto RSIGO.

The RSIG buffer has the following configurable features:

- transparent, robbed-bit signaling
- signaling freeze
- debounce signaling
- unicode detection

Each feature is available in the Receive Signaling Configuration register [RSIG; addr 0D7]. See the registers section for more details.

2.5.4 Signaling Stack

The Receive Signaling Stack (RSTACK) allows the processor to quickly extract signaling changes without polling every channel. RSTACK is activated on a per-channel basis by setting the Received Signaling Stack (SIG_STK) control bit in the Receive Per-Channel Control register [RPC0 to RPC31; addr 180 to 19F]. The signaling stack stores the channel and the A, B, C, and D signaling bits that changed in the last multiframe. The stack has the capacity to store signaling changes for all 24 (T1) or 30 (E1) PCM channels.

At the end of any multiframe where 1 or more ABCD signaling values have changed, an interrupt occurs with RSIG set in the Timer Interrupt Status register [ISR3; addr 008]. The processor then reads the Receive Signaling Stack [STACK; addr 0DA] twice to retrieve the channel number (WORD = 0) and the new ABCD value (WORD = 1), and continues to read from STACK until the MORE bit in STACK is cleared, indicating the RSIG stack is empty.

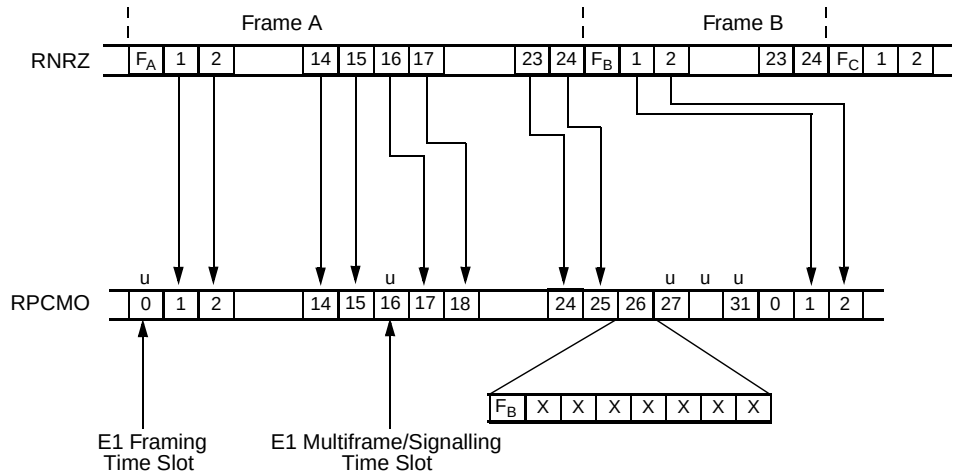
Optionally, the processor can select RSIG interrupt (SET_RSIG; addr 0D7) to occur at each multiframe boundary in T1 modes, regardless of signaling change. This mode provides an interrupt aligned to the multiframe to read the RSIG buffer rather than RSTACK.

2.5.5 Embedded Framing

Embedded Framing mode bit (EMBED; addr 0D0) instructs the RSB to embed framing bits on RPCMO while in T1 mode.

The G.802 Embedded mode supports *ITU-T Recommendation G.802*, which describes how 24 T1 time slots and 1 framing bit (193 bits) are mapped to 32 E1 time slots (256 bits). This mapping is done by leaving TS0 and TS16 unassigned, by storing the 24 T1 time slots in TS1 to TS15 and TS17 to TS25, and by storing the frame bit in bit 1 of TS26 (see Figure 2-20). TS26 through TS31 are also unassigned.

Figure 2-20. G.802 Embedded Framing



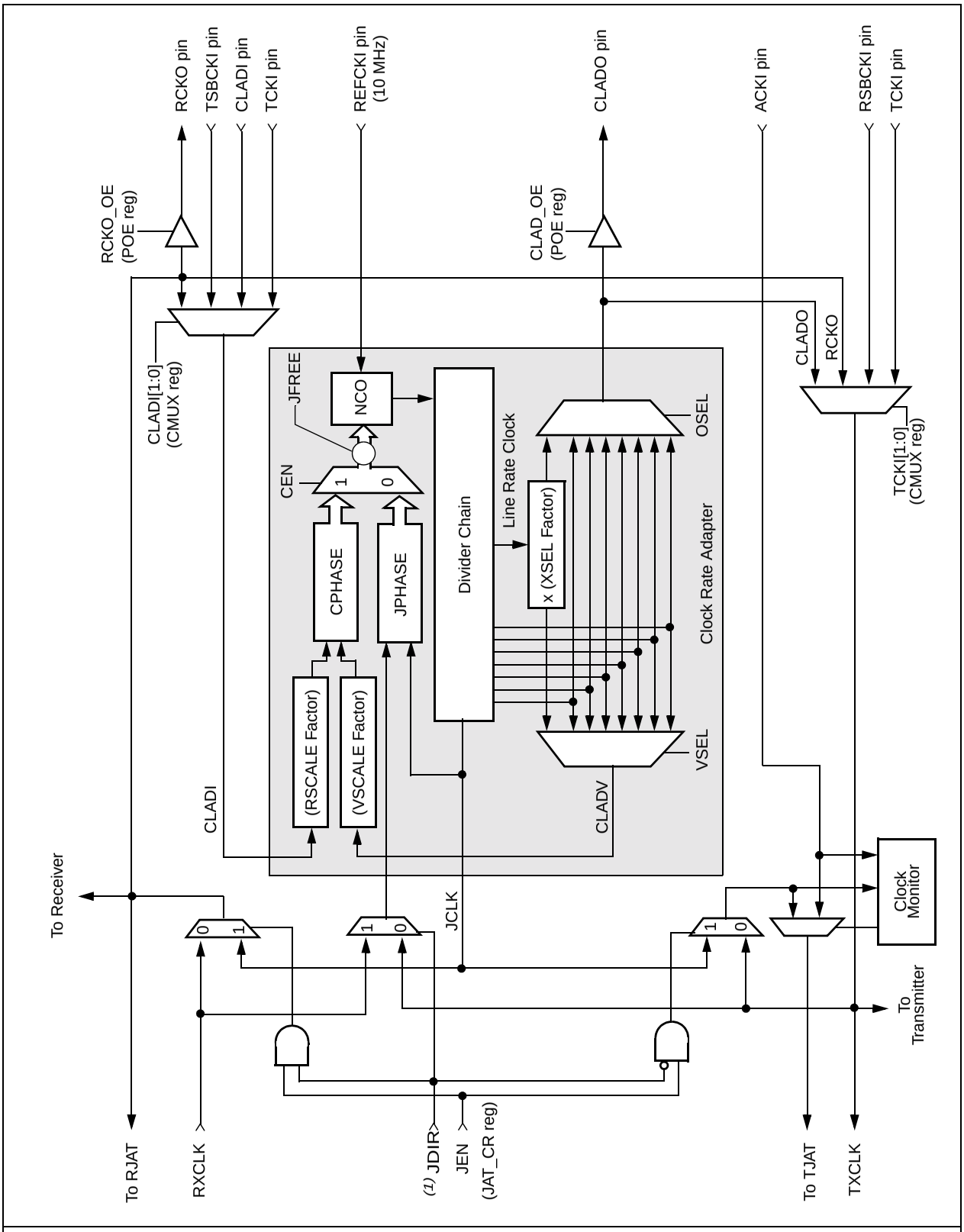
NOTE(S):
1. X = unused bits
2. u = unassigned time slot (see ASSIGN bit [addr 0E0 to 0FF])
3. F_B = T1 frame bit for frame B

2.6 Clock Rate Adapter

The full function Clock Rate Adapter is included in all Bt8370 and Bt8375 devices. In the Bt8376, the CLADO output is not implemented.

The Clock Rate Adapter (CLAD) illustrated in Figures 2-21 and 2-22 uses an input clock reference at a particular frequency (range 8 kHz to 16,384 kHz) to synthesize an output clock (CLADO and JCLK) at a different frequency (range 1024 kHz to 16,384 kHz). The CLAD also controls the read or write pointers of the elastic store by synthesizing a Jitter-attenuated Line rate Clock (JCLK); thus, it is an integral part of the Jitter Attenuator (JAT). The CLAD input clock jitter tolerance and jitter transfer functions are illustrated in Figures 2-9 and 2-10. These diagrams are illustrated for various programmed loop filter gain values (LFGAIN; addr 090).

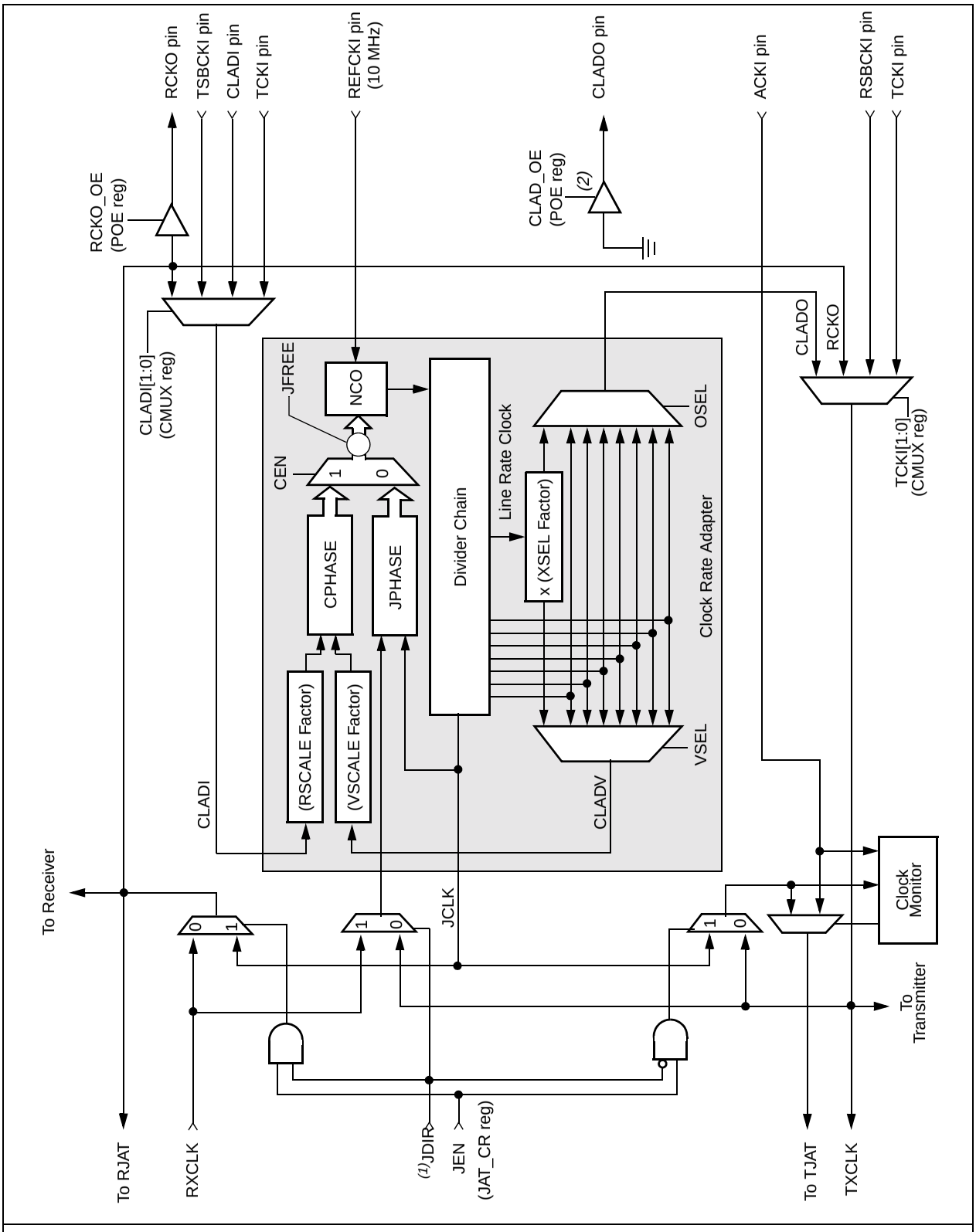
Figure 2-21. Clock Rate Adapter/Jitter Attenuator Block Diagram (Bt8370 and Bt8375 Devices)



NOTE(S):

1. JDI*R* controlled in JAT_CR [addr 002].

Figure 2-22. Clock Rate Adapter/Jitter Attenuator Block Diagram (Bt8376 Device Only)



NOTE(S):

1. JDIR controlled in JAT_CR [addr 002].
2. CLADO signal is grounded in the Bt8376 and a logical 0 is driven out on CLADO pin if enabled.

JCLK and CLADO are locked to the selected timing reference. The reference frequency can operate at T1 or E1 line rates, or at any rate supported by the clock rate adapter. See RSCALE[2:0] [addr 092] to select timing reference frequency. See Table 2-6 for the JCLK/CLADO timing reference.

Table 2-6. JCLK/CLADO Timing Reference

CEN	JEN	JFREE	JDIR	CLADO/JCLK Reference
0	0	1	X	REFCKI—Free running 10 MHz clock
0	1	1	0	REFCKI—Free running 10 MHz clock with transmit JAT
0	1	1	1	REFCKI—Free running 10 MHz clock with receive JAT
0	1	0	0	TXCLK—TCKI or ACKI per [AISCLK; addr 068]
0	1	0	1	RXCLK—RPLL or RCKI per [RDIGI; addr 020]
1	0	0	X	CLADI—System clock bypass JAT elastic store
1	1	0	0	CLADI—System clock with transmit JAT
1	1	0	1	CLADI—System clock with receive JAT

NOTE(S):
1. JCLK always operates at T1 or E1 line rate selected by [T1/E1N; addr 001]

CLAD output jitter meets jitter generation requirements of AT&T TR62411, as listed in Table 2-7.

Table 2-7. Jitter Generation Requirements

Filter Applied	Maximum Output Jitter	Measured
None (Broadband)	0.05 UI peak-peak	.015 UI
10 Hz to 40 kHz	0.025 UI peak-peak	.015 UI
8 kHz to 40 kHz	0.025UI peak-peak	.015 UI
10 Hz to 8 kHz	0.02UI peak-peak	.015 UI

CLAD modes are selected using the Clock Rate Adapter Configuration register [CLAD_CR; addr 090], the Clock Rate Adapter Frequency Select [CSEL; addr 091], and the Clock Rate Adapter Phase Detector Scale Factor [CPHASE; addr 092].

If the CLAD Phase Detector (CPHASE) is disabled [CEN; addr 090], the CLAD input timing reference is determined by the JEN and JFREE bits (addr 002).

If the CLAD Phase Detector is enabled [CEN; addr 090], the CLAD input timing reference is selected using CLADI[1:0] in the Clock Input Mux register [CMUX; addr 01A]. The input timing reference can consist of the Clock Rate Adapter Input Pin (CLADI); the Receive Clock Output (RCKO, prior to the output buffer); the Transmit Clock Input Pin (TCKI); or the Transmit System Bus Clock Input Pin (TSBCKI). (See Figures 2-21 and 2-22 for more details.)

Tables 2-8 and 2-9 list examples of program values for selecting various CLADO and CLADI frequencies. Typically, only 1 selection is needed for a given system configuration. The processor reconfigures the timing reference [CEN; addr 090] as needed to respond to system conditions where the primary reference is unavailable.

2.6.1 Configuring the CLAD Registers

Step 1 Choose a CLADO output frequency. Table 2-8 lists all possible CLADO output clock frequencies. For system bus applications, valid CLADO frequencies are 1544 kHz, 1536 kHz, 2048 kHz, 4096 kHz, and 8192 kHz.

Step 2 Configure OSEL and XSEL from Table 2-8. OSEL and XSEL together select the CLADO output frequency. In some cases, there are two options for generating the desired output signal. Selecting an option with both T1/E1 and XSEL settings equal to don't-care (X in the table) allows greater flexibility in subsequent options below, and also results in a fixed CLADO frequency when switching framer operation between T1 and E1 modes.

Table 2-8. CLADO Frequencies Selection

CLADO (kHz)	T1/$\overline{E1}$	OSEL	XSEL
1024	X	0	X
2048	X	1	X
	0	7	0
4096	X	2	X
	0	7	1
8192	X	3	X
	0	7	2
2560	X	4	X
1536	X	6	X
1544	1	7	0
	X	5	X
3088	1	7	1
6176	1	7	2
12352	1	7	3
16384	0	7	3
	X	8	X
NOTE(S): X = Don't care			

Step 3 If CLADI is the timing reference source (CEN = 1), select the desired CLAD timing reference frequency from Table 2-9. If CEN = 0, the CLAD reference is RXCLK (line rate), TXCLK (line rate), or free run (REFCKI) and Table 2-9 is not applicable.

Step 4 Configure RSCALE, VSCALE, VSEL, and XSEL from Table 2-9 which contains configuration examples. Again, in some cases, two or more configurations are possible for each frequency option. Many other RSCALE and VSCALE values are also applicable. RSCALE is a programmable frequency divider which scales the CLADI clock frequency before it is applied to the CLAD phase detector, CPHASE. Similarly, VSCALE scales the CLAD internal feedback clock, CLADV. These two clocks must have the same frequency at the phase detector's input for the CLAD loop to properly lock. The rule is

(CLADI Reference freq) ÷ (RSCALE factor) = (CLADV freq) ÷ (VSCALE factor).

Table 2-9. Common CLADI Reference Frequencies and CLAD Configuration Examples *(1 of 2)*

CLADI Reference (kHz)	RSCALE	Phase Compare Frequency (kHz)	VSCALE	CLADV (kHz)	T1/$\overline{E1}$	VSEL	XSEL
8	0	8	7	1024	X	0	X
16	0	16	6	1024	X	0	X
32	0	32	5	1024	X	0	X
64	0	64	4	1024	X	0	X
128	0	128	3	1024	X	0	X
256	0	256	2	1024	X	0	X
512	0	512	1	1024	X	0	X
1024	0	1024	0	1024	X	0	X
2048	0	2048	0	2048	X	1	X
	7	16	7	2048	X	1	X
	0	2048	0	2048	0	7	0
4096	0	4096	0	4096	X	2	X
	7	32	7	4096	X	2	X
	1	2048	1	4096	0	7	1
8192	0	8192	0	8192	X	3	X
	7	64	7	8192	X	3	X
	2	2048	2	8192	0	7	2
16384	0	16384	0	16384	X	8	X
	7	128	8	1024	X	0	X
	0	16384	0	16384	0	7	3
1536	2	384	2	1536	X	6	X
1544	2	386	2	1544	X	5	X
	2	386	2	1544	1	7	0

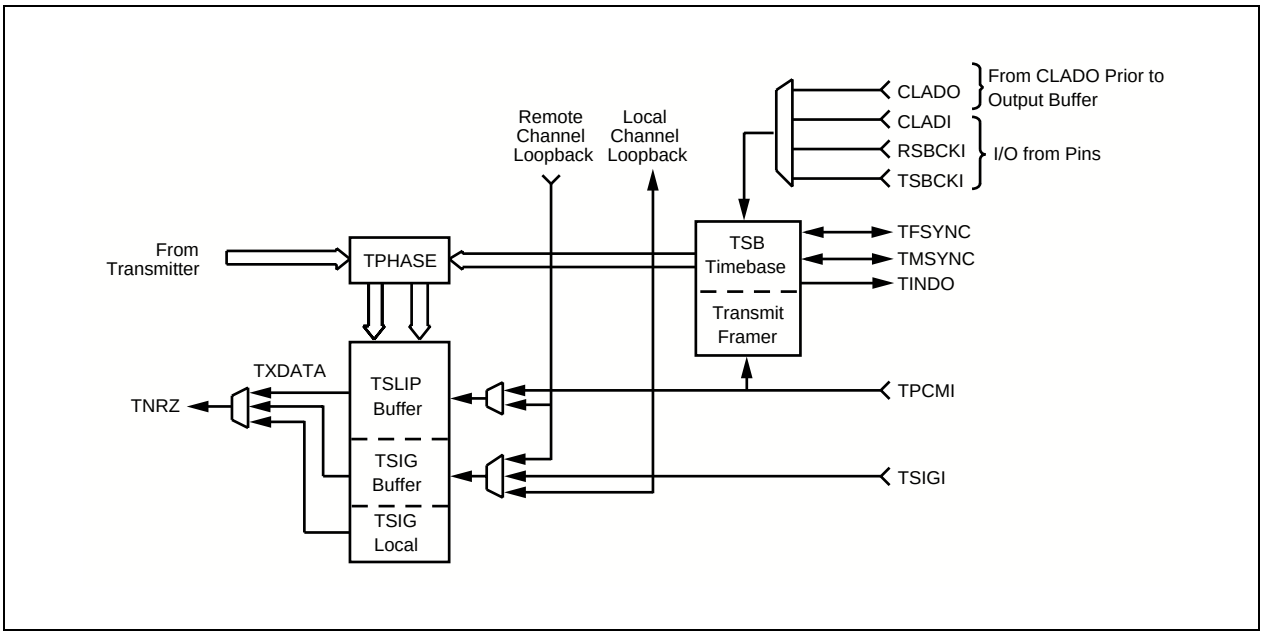
Table 2-9. Common CLADI Reference Frequencies and CLAD Configuration Examples *(2 of 2)*

CLADI Reference (kHz)	RSCALE	Phase Compare Frequency (kHz)	VSCALE	CLADV (kHz)	T1/$\overline{E1}$	VSEL	XSEL
3088	2	772	1	1544	X	5	X
	2	772	1	1544	1	7	0
6176	2	1544	0	1544	X	5	X
	2	1544	0	1544	1	7	0
12352	3	1544	0	1544	X	5	X
	3	1544	0	1544	1	7	0
NOTE(S): X = Don't care							

2.7 Transmit System Bus

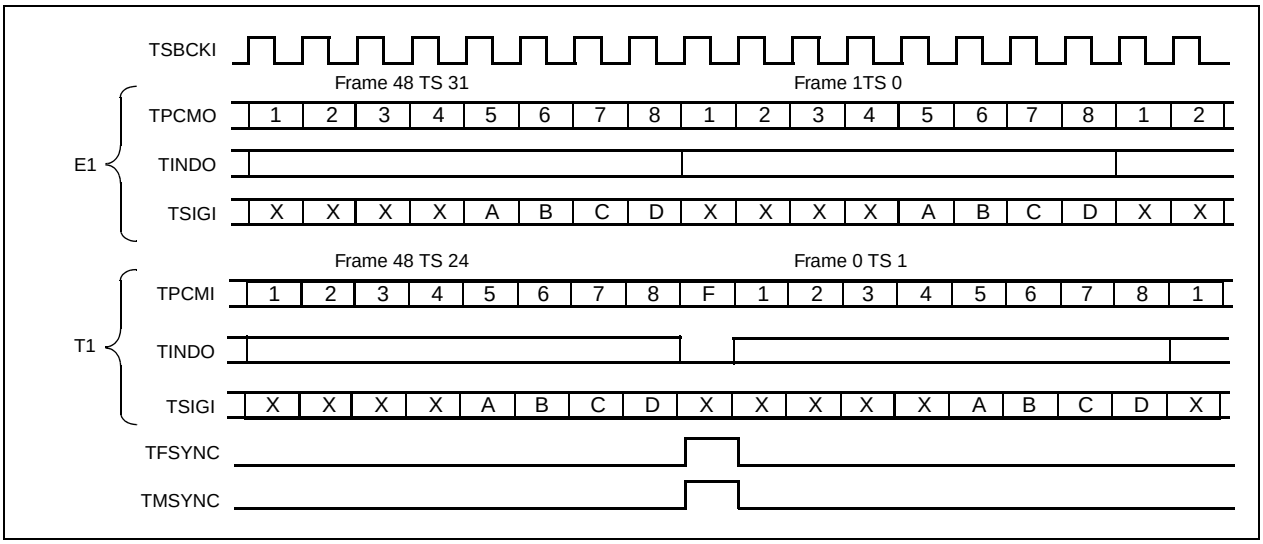
The Transmit System Bus (TSB) consists of a timebase, slip buffer, signaling buffer, and transmit framer (Figure 2-23). It provides a high-speed serial interface between the XMTR and system bus. The system bus is compatible with the Mitel ST-Bus, the PEB Bus, and the AT&T CHI Bus. TSB directly interfaces to other Conexant devices with no need for external circuitry.

Figure 2-23. TSB Interface Block Diagram



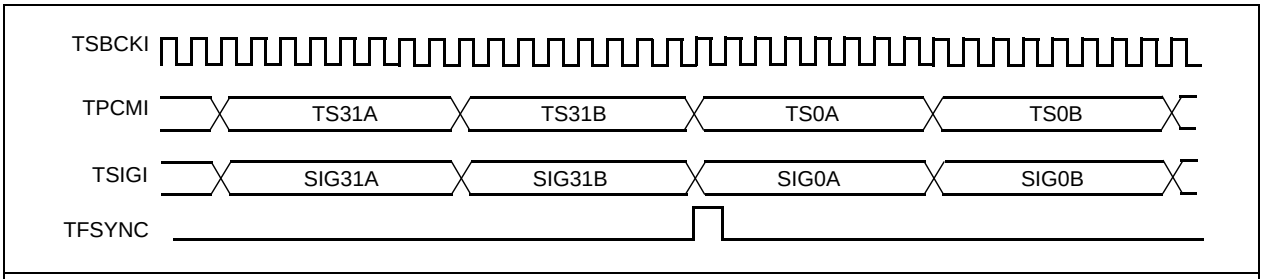
The TSB contains the following six pins: Transmit System Bus Clock (TSBCKI), Transmit PCM Data (TPCMI), Transmit Signaling Data (TSIGI), Transmit Frame Sync (TFSYNC), Transmit Multiframe Sync (TMSYNC), and Transmit time slot Indicator (TINDO). See Figure 2-24 for the relationship between these signals. These pins are further defined in Table 1-1, *Hardware Signal Definitions*.

Figure 2-24. Transmit System Bus Waveforms



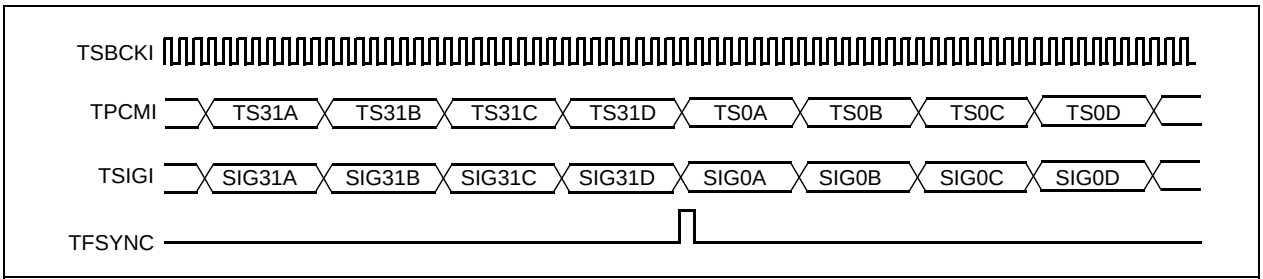
The TSB supports five system bus rates (MHz): 1.536, 1.544, 2.048, 4.096, and 8.192. The T1 rate, with 24 time slots and without framing bits, is 1.536 MHz. The T1 rate with framing bits is 1.544 MHz. The E1 rate, with 32 time slots, is 2.048 MHz. The 4.096 MHz rate is twice the E1 rate, with 64 time slots. The 8.192 MHz rate is 4 times the E1 rate, with 128 time slots. The 4.096 and 8.192 MHz bus modes contain multiple bus members (A, B, C, and D), of which 1 bus member is selected by the SBI [3:0] bits in the System Bus Interface Configuration register [SBI_CR; 0D0]. See Figures 2-25 and 2-25. The system bus rate is independent of the line rate and must be selected using the System Bus Interface Configuration register.

Figure 2-25. TSB 4.096 MHz Bus Mode Time Slot Interleaving



NOTE(S): A and B time slot data comes from different Bt8370s. TSBCKI can be operated at 1 or 2 times the data rate.

Figure 2-26. TSB 8.192 MHz Bus Mode Time Slot Interleaving



NOTE(S): A, B, C, and D time slot data comes from different Bt8370s. TSBCKI can be operated at 1 or 2 times the data rate.

2.7.1 Timebase

The TSB timebase synchronizes TPCMI, TFSYNC, TMSYNC, and TINDO with the Transmit System Bus Clock (TSBCK). The TSBCK can be slaved to five different clock sources: Transmit Clock Input (TCKI), Transmit System Bus Clock Input (TSBCKI), Receive System Bus Clock Input (RSBCKI), Clock Rate Adapter Input (CLADI), or Clock Rate Adapter Output (CLADO).

NOTE: The CLADO signal is not available in the Bt8376 device.

The TSB clock selection is made through the Clock Input Mux register [CMUX; addr 01A]. TCKI is automatically selected when the transmit slip buffer is bypassed. The system bus clock can also be configured to run at twice the data rate by setting the X2CLK bit in the System Bus Interface Configuration register [SBI_CR; addr 0D0] when TSLIP is not in Bypass mode.

TFSYNC and TMSYNC can be individually configured as inputs or outputs [PIO; addr 018]. TFSYNC and TMSYNC should be configured as inputs when the TSB timebase is slaved to the system bus, when the transmit framer is disabled [TABORT; addr 071], or when TSB carries embedded T1 framing. TFSYNC and TMSYNC should be configured as outputs when the TSB timebase is master of the system bus, or when the transmit framer is enabled. TFSYNC and TMSYNC can also be configured as rising or falling edge outputs [TSB_CR; addr 0D4]. In addition to having TFSYNC and TMSYNC active on the frame boundary, a programmable offset is available to select the time slot and bit offset in the frame. See Transmit System Bus Sync time slot Offset [TSYNC_TS; addr 0D6] and Transmit System Bus Sync Bit Offset [TSYNC_BIT; addr 0D5].

2.7.2 Slip Buffer

The 64-byte Transmit PCM Slip Buffer [TSLIP; addr 140 to 17F] resynchronizes the Transmit System Bus Clock (TSBCK) and data (TPCMI) to the Transmit Clock (TXCLK) and data (TNRZ). TSLIP acts like an elastic store by clocking PCM data in on TPCMI with TSBCK, and by clocking TNRZ data out with TXCLK. TPCMI can be configured to sample on the rising or falling edge of TSBCKI. See the Transmit System Bus Configuration register [TSB_CR; addr 0D4].

TSLIP has four modes of operation: Two-Frame Normal, 64-bit Elastic, Two-Frame Short, and Bypass. TSLIP mode is set in the Transmit System Bus Configuration register [TSB_CR; addr 0D4]. It is organized as a two-frame buffer, with high-frame and low-frame buffers. This allows MPU access to frame data, regardless of the TSLIP mode selected. Each byte offset into the frame buffer is a different time slot: offset 0 in TSLIP is always time slot 0 (TS0), offset 1 is always TS1, and so on. The slip buffer has processor read/write access.

In Normal mode, the slip buffer total depth is two 193-bit frames (T1), or two 256-bit frames (E1). Data is written to the slip buffer using TSBCK and read from the slip buffer using TXCLK. If there is a slight rate difference between the two clocks, the slip buffer changes from its initial condition—approximately half full—by either adding or removing frames. If TSBCK writes to the slip buffer faster than TCKI reads the data, the buffer becomes full. When the slip buffer in Normal mode is full, an entire frame of data is deleted. Conversely, if TXCLK is reading the slip buffer at a faster rate than TSBCK is writing the data, the buffer eventually empties. When the slip buffer in Normal mode is empty, an entire frame of data is duplicated. When an entire frame is deleted or duplicated, it is known as a Frame Slip (FSLIP). An FSLIP is always 1 full frame of data. The FSLIP status is reported in the Slip Buffer Status register [SSTAT; addr 0D9].

In 64-bit Elastic mode, the slip buffer total depth is 64 bits, and the initial throughput delay is 32 bits, or half of the total depth. Similar to Normal mode, Elastic mode allows the system bus to operate at any of the programmable bus rates, independent of the line rate. The advantage of this mode over the Two-Frame mode is that throughput delay is reduced from 1 frame to an average of 32 bits, and the transmit multiframe can retain its alignment with respect to the transmit data. The disadvantage of this mode is handling the full and empty buffer conditions. In 64-bit Elastic mode, an empty or full buffer condition causes an Uncontrolled Slip (USLIP). Unlike an FSLIP, a USLIP is of unknown size, ranging from 1 to 256 bits of data. The USLIP status is reported in SSTAT.

The Two-Frame Short mode combines the depth of the Normal mode with the throughput delay of the Elastic mode. This mode begins in Elastic mode with a 32-bit initial throughput delay, and switches to Normal modes when the buffer is empty or full; thereafter, the Two-Frame Short and Normal modes perform identically. If the slip buffer is full (two frames) in the Two-Frame Short and Normal modes, an FSLIP is reported; thereafter, the slip buffer performs exactly like Normal mode.

In Bypass mode, data is clocked through TSLIP from the TSB to the XMTR using TXCLK as selected by the TCKI input clock mux.

2.7.3 Signaling Buffer

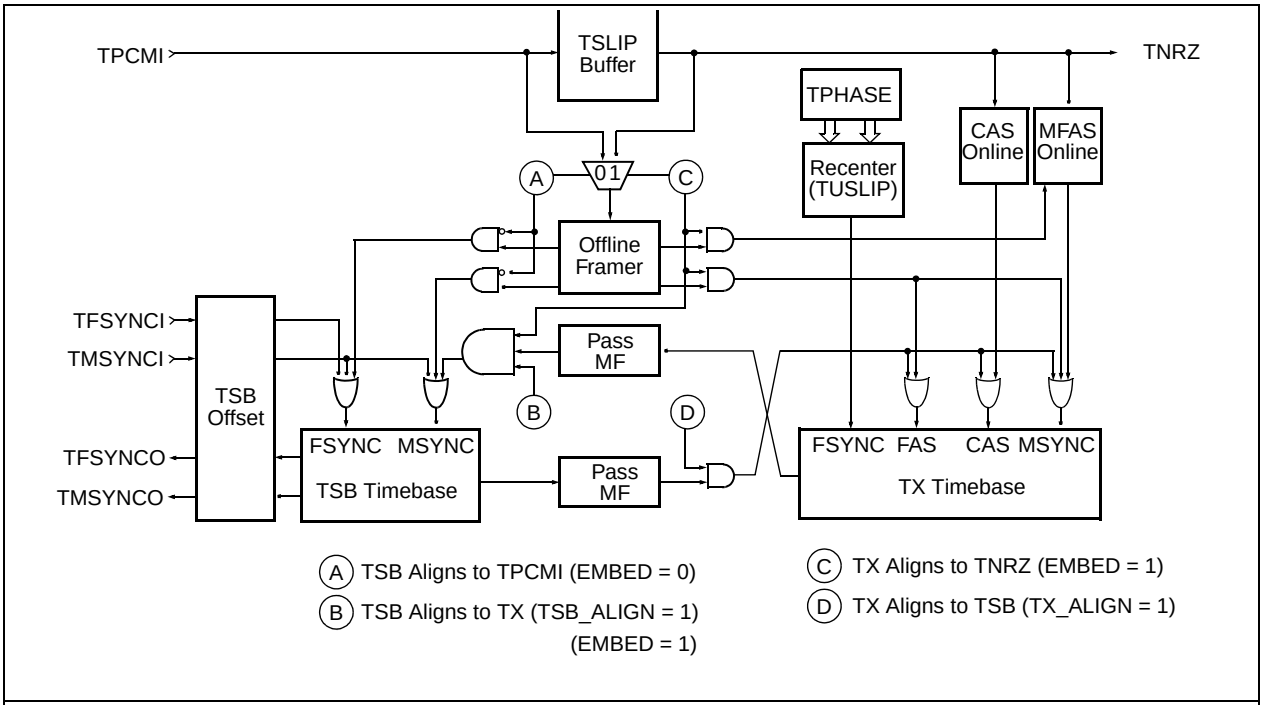
The 32-byte Transmit Signaling Buffer [TSIG; addr 120–13F] stores a single multiframe of signaling data input from the TSIGI pin and is updated as each time slot is received in every TSB frame. Each byte offset into TSIG represents a different time slot for signaling data: offset 0 stores TS0 signaling data, offset 1 stores TS1 signaling data, and so on. The signaling data is stored in the least significant 4 bits of the signaling buffer. Similar to TSLIP, TSIG has read/write processor access for accessing or overwriting signaling information. The signaling buffer uses TFSYNC to identify the frame boundaries in the TSIGI data stream.

2.7.4 Transmit Framing

The transmit data stream has two framing functions: offline framer and an online framer. Figure 2-27 illustrates these functions. The offline framer recovers the transmit frame alignment (TFSYNC). The online framer monitors the frame alignment found by the offline framer and recovers multiframe alignment (TMSYNC).

Transmit frame resynchronization is initiated by activating the Transmit Loss of Frame (TLOF) status bit in Alarm 2 status [ALM2; addr 048] register by the online framer. The TLOF criteria is set in the TLOFA, TLOFB, and TLOFC bits of the Transmitter Configuration register [TCR1; addr 071]. The online framer supports the following LOF criteria for T1: 2 frame bit errors out of 4; 2 out of 5; or 2 out of 6. For E1, it supports 3 out of 3.

Figure 2-27. Transmit Framing and Timebase Alignment Options



NOTE(S):
1. EMBED located in SBI_CR (addr 0D0).
2. TSB_ALIGN and TX_ALIGN located in TSB_CR (addr 0D4).
3. EMBED = 0 is only applicable if TPCMI is operating at the line rate.

When TLOF is asserted, the offline framer searches the transmit data stream for a new frame alignment, provided transmit framing is enabled [TABORT; addr 071]. If embedded framing is enabled [EMBED; addr 0D0], the offline framer examines the TSLIP buffer output, TNRZ, for transmit frame alignment. If embedded framing is disabled, the offline framer examines the slip buffer input (TPCMI) for transmit frame alignment. This case (EMBED = 0) is only applicable if TPCMI is configured to operate at the line rate: 2,048 kbps E1, or 1,544 kbps T1. If transmit framing is disabled, the offline framer waits for a reframe command [TFORCE; addr 071] before beginning frame alignment search.

After the offline framer recovers frame alignment, the online framer monitors TLOF and searches for multiframe alignment; the search uses the criteria defined by the Transmit Frame mode [TFRAME; addr 070]. The online framer conducts a multiframe alignment search each time the offline framer recovers transmit frame alignment, as reported by high-to-low transition of transmit loss of frame status [TLOF; addr 048]. After TLOF recovery, the online framer searches continuously for multiframe alignment until the correct pattern sequence is located, or until basic frame alignment is lost (TLOF goes active-high). After multiframe alignment recovery, the online framer checks subsequent multiframes for errored alignment patterns, but does not use those errors as part of the criteria for loss of basic frame alignment.

NOTE: The online framer's multiframe search status is not directly reported to the processor, but instead is monitored by examination of transmit error status: TMERR, TSERR, and TCERR [addr 00B]. If the system incorporates a certain number of multiframe pattern errors (or a certain error ratio) into the loss of transmit frame alignment criteria, the processor must count multiframe pattern errors to determine when to force a transmit reframe [TFORCE; addr 071].

The frame synchronization criteria used by the offline framer is set in the TFRAME[3:0] of the Transmit Framer Configuration register [TCR0; addr 070]. (Tables 3-15 and 3-16 illustrate supported transmit framing formats. Also, see Tables 3-17 and 3-18, Criteria for Loss/Recovery of Transmit Frame Alignment.)

The offline framer is shared between the RCVR and XMTR and can only search in 1 direction at a time. Consequently, the host processor can manually arbitrate between RCVR and XMTR reframe requests by manipulating the ABORT and FORCE controls, or by allowing the framer to automatically arbitrate LOF requests.

The offline framer waits until the current search is complete [FSTAT; addr 017] before checking for pending LOF reframe requests. If both online framers have pending reframe requests, the offline framer aligns to the opposite direction of that most recently searched. For example, if TLOF is pending at the conclusion of a receive search which timed out without finding alignment, the offline framer switches to search in the transmit direction. The TLOF switchover is prevented in the preceding example if the processor asserts TABORT to mask the transmit reframe request. TABORT does not affect TLOF status reporting. For applications that frame in only 1 direction, framing in the opposite direction must be masked. If, at the conclusion of a receive search timeout, TLOF status is asserted but masked by TABORT, the offline framer continues to search in the receive direction.

For applications that frame in both directions, the processor can manually arbitrate among pending reframe requests by controlling the reframe precedence. An example of manual control follows:

```
1   Initialize RABORT = 1 and TABORT = 1.
2   Enable RLOF and TLOF interrupts.
3   Read clear pending ISR interrupts.
4   Release RABORT = 0.
5   Call LOF Service Routine if either RLOF or TLOF interrupt;
    {
        (check current LOF status (ALMI, 2; addr 047, 048)
        If RLOF recovered and TLOF lost
        —Assert RABORT = 1
        —Release TABORT = 0
        If RLOF lost or TLOF recovered
        —Assert TABORT = 1
        —Release RABORT = 0
        }
```

The status of the offline framer can be monitored using the Offline Framer Status register [FSTAT; addr 017]. The register reports the following:

- whether the offline framer is looking at the receive or transmit data streams (RX/TXN)
- whether the framer is actively searching for frame alignment (ACTIVE)
- whether the framer found multiple framing candidates (TIMEOUT)
- whether the framer found frame sync (FOUND)
- whether the framer found no frame alignment candidates (INVALID)

2.7.5 Embedded Framing

Embedded framing mode [EMBED; addr 0D0] instructs the transmit framer to search TSLIP buffer output (TNRZ) for framing bits while in T1 mode, or for MFAS and CAS in E1 mode. Embedded framing allows the transmit timebase to align with the transmit framer multiframe alignment of the PCM signal transported across the system bus.

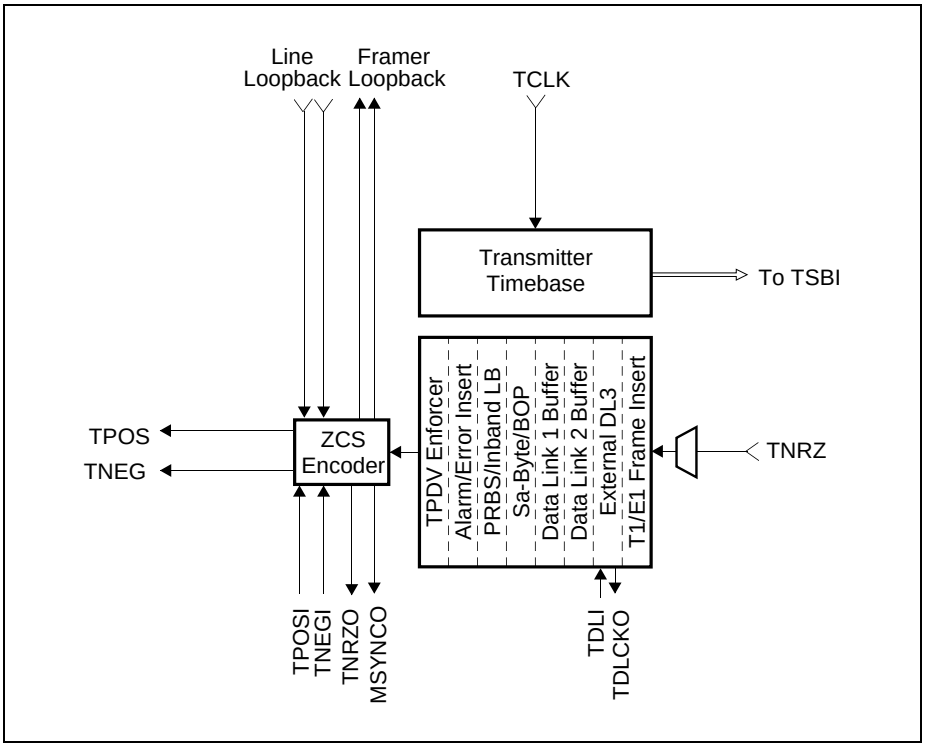
The G.802 Embedded mode supports ITU-T Recommendation G.802, which describes how 24 T1 time slots and framing bit (193 bits) are mapped to the 32 E1 time slots (256 bits): by leaving TS0 and TS16 unassigned, by storing the 24 T1 time slots in TS1 to TS15, and in TS17 to TS25, and by storing the frame bit in Bit 1 of TS26 (see Figure 2-20).

2.8 Transmitter

The Digital Transmitter (XMTR) inserts T1/E1 overhead data and encodes single rail NRZ data from the TSB into P and N rail NRZ data, suitable for transmission by the TLIU.

The XMTR, illustrated in Figure 2-28, consists of the following elements: two Transmit Data Links, Test Pattern Generator, In-Band Loopback Code Generator, Overhead Pattern Generator, Alarm Generator, Zero Code Suppression (ZCS) Encoder, External Transmit Data Link, CRC Generation, Framing Pattern Insertion, and Far End Block Error Generator.

Figure 2-28. XMTR Diagram

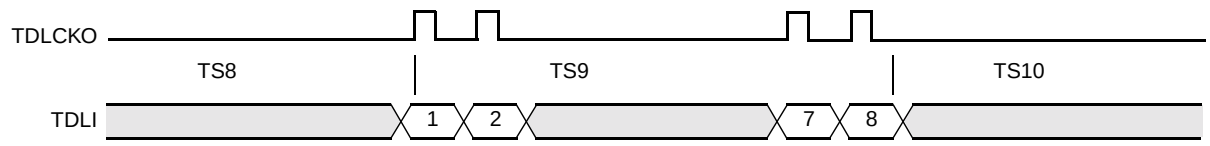


2.8.1 External Transmit Data Link

The External Data Link (DL3) allows the system to supply externally any bits in any time slot of all frames, odd frames, or even frames, including T1 framing bits. Pin access to the DL3 transmitter is provided through TDLCKO and TDLI, which serve as the TDL3 clock output (TDLCKO) and data input (TDLI). The mode of the pins is selected using TDL_IO bit in the Programmable Input/Output register [PIO; addr 018].

Control of DL3 format is provided in two registers: External Data Link Time Slot [DL3_TS; addr 015] and External Data Link Bit [DL3_BIT; addr 016]. Transmit DL3 is set up by selecting the bit(s) [DL3_BIT], and time slot [TS[4:0]; addr 015] to be overwritten, and then enabling the data link [DL3EN; addr 015]. Enabling the data link starts TDLCKO for gating the NRZ data provided on TDLI. See Figure 2-29.

Figure 2-29. Transmit External Data Link Waveforms



NOTE(S): This example shows bits 1, 2, 7, and 8 of TS9 selected. Any combination of time slot bits can be selected.

2.8.2 Transmit Data Links

The XMTR contains two independent data link controllers (DL1, DL2): a Performance Report Message (PRM) generator and a Bit-Oriented Protocol (BOP) transceiver. DL1 and DL2 can be programmed to send and receive HDLC formatted messages in the Message Oriented Protocol (MOP) mode, or unformatted serial data can be sent and received in any combination of bits within a selected time slot or F-bit channel. The PRM message generator can automatically send 1-second performance reports. The BOP transceiver can preemptively transmit BOP messages, such as ESF Yellow Alarm.

2.8.2.1 Data Link Controllers

The Bt8370 and Bt8375 provide two internal data link controllers, and the Bt8376 provides a single controller. DL1 and DL2 control the serial data channels, which operate in multiples of 4 kbps to the maximum 64 kbps time slot rate. This is done by selecting a combination of bits from either odd, even, or all frames. Both data link controllers support ESF Facilities Data Link (FDL), SLC-96 data link, Sa data link, Common Channel Signaling (CCS), Signaling System #7 (SS7); ISDN LAPD channels; Digital Multiplexed Interface (DMI) signaling in TS24; and the latest ETSI V.51 and V.52 signaling channels. DL1 and DL2 each contain a 64-byte transmit buffer which function either as programmable length circular buffers in transparent (unformatted) mode, or as full-length data FIFOs in formatted (HDLC) mode.

DL1 and DL2 are configured identically, except for their offset in the register map. The DL1 address range is 0A4 to 0AE, and the DL2 address range is 0AF to 0B9. From this point on, the DL1 is used to describe the operation of both data link controllers. Transmit Data Link 1 (TDL1) can be viewed as having a higher priority than Transmit Data Link 2 (TDL2) because TDL1 overwrites the primary rate channel after TDL2. Thus, any data that TDL2 writes to the primary rate channel can be overwritten by TDL1, if TDL1 is configured to transmit in the same time slot as TDL2.

The TDL1 is enabled using the DL1 Control register [DL1_CTL; addr 0A6]. TDL1 does not overwrite time slot data until it is enabled. DL1_CTL also controls the data format and the circular buffer/FIFO mode.

The following data formats [DL1[1,0]; addr 0A6] are supported on the data link: Frame Check Sequence (FCS), non-FCS, Pack8, or Pack6. FCS and non-FCS are HDLC-formatted messages. Pack8 and Pack6 are unformatted messages with 8 bits per FIFO access, and 6 bits per FIFO access, respectively.

The Circular Buffer/FIFO control bit [TDL1_RPT; addr 0A6] allows the FIFO to act as a circular buffer; in this mode, a message can be transmitted repeatedly. This feature is available only for unformatted transmit data link applications. The processor can repeatedly send fixed patterns on the selected channel by writing a 1- to 64- byte message into the circular buffer. The programmed message length repeats until the processor writes a new message. The first byte of each unformatted message is output automatically, aligned to the first frame of the 12-, 24-, or 16-frame transmit multiframe (SF/ESF/MFAS). This allows the processor to source overhead or data elements aligned to the TX timebase.

NOTE: Each unformatted message written is output-aligned only after the preceding message completes transmission. Therefore, data continuity is retained during the linkage of consecutive messages, provided that the contents of each message consists of a multiple of the multiframe length.

Time slot and bit selection is done through the DL1 Time Slot Enable [DL1_TS; addr 0A4] and DL1 Bit Enable [DL1_BIT; addr 0A5] registers. DL1_TS selects which frames and which time slot are overwritten. The frame select allows TDL1 to overwrite the time slot in all frames, odd frames, even frames. The time slot word enable is a value between 0 and 31 that selects which time slot is filled with data from the transmit data link buffer. DL1_BIT selects which bits are overwritten in the time slot selected. Table 2-10 lists commonly used data link settings.

Table 2-10. Commonly Used Data Link Settings

Data Link	Frame	Time Slot	Time Slot Bits	Mode
ESF FDL	Odd	0 (F-bits)	Don't Care	FCS
T1DM R Bit	All	24	00000010	FCS
SLC-96	Even	0 (F-bits)	Don't Care	Pack6
ISDN LAPD	All	N	11111111	FCS
CEPT Sa4	Odd	1	00001000	FCS
NOTE(S): N represents any T1/E1 time slot.				

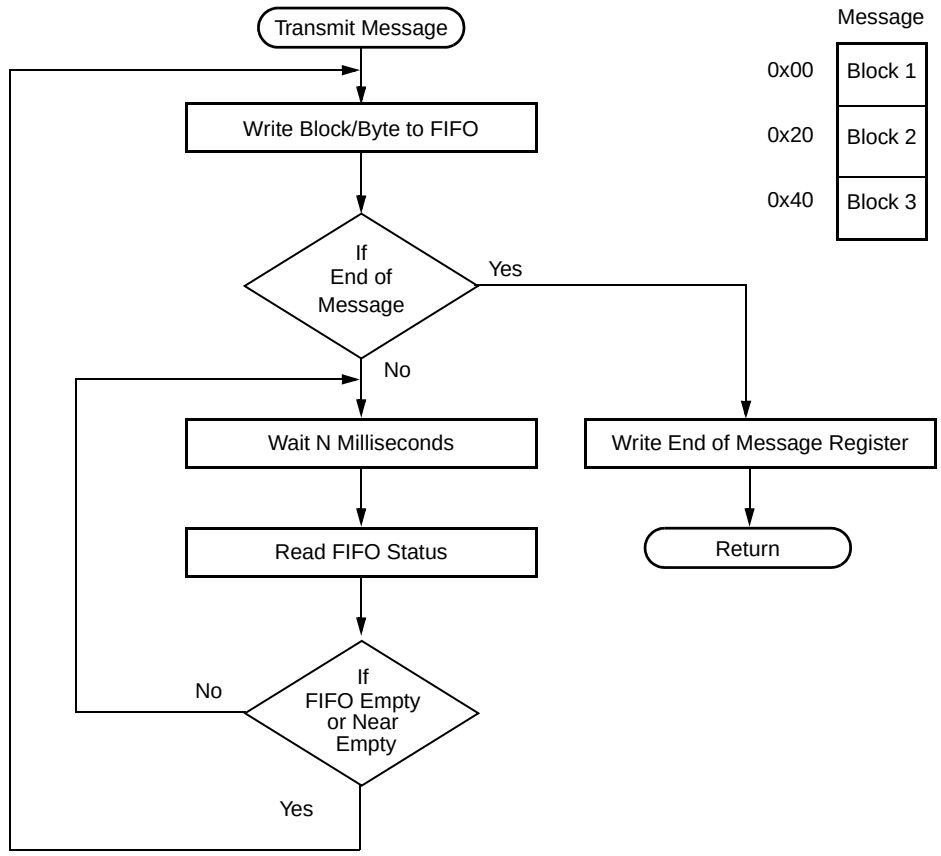
The Transmit Data Link FIFO #1 [TDL1; addr 0AD] is 64 bytes, and very versatile. It can be used as a single-byte transmit buffer or in any number of bytes, up to a maximum of 64. As a single-byte FIFO, the Transmit FIFO Empty Status (TMPTY1) in TDL #1 Status [TDL1_STAT; addr 0AE] and Transmit FIFO Empty Interrupt (TEMPTY) in Data Link 1 Interrupt Status (ISR2; addr 009] can be used for byte-by-byte transmissions.

Using the Transmit Data FIFO, an entire block of data can be transmitted with very little microprocessor-interrupt overhead. Block transfers to the FIFO can be controlled by the Near Empty Threshold in the FIFO Empty Control register [TDL1_FEC; addr 0AB]. The Near Empty Threshold is a user-programmable value between 0 and 63 that represents the minimum number of bytes that can remain in the transmit FIFO before near empty is declared. Once the threshold is set, the Near Empty Status (TNEAR1) in TDL #1 Status [TDL1_STAT; addr 0AE] is asserted whenever the Near Empty Threshold is reached. An interrupt, TNEAR in the Data Link 1 Interrupt Status register [ISR2; addr 009], is also available to mark this event.

Once an entire message is written into the transmit FIFO or circular buffer, the processor must indicate the end of message by writing any value to the TDL #1 End of Message (EOM) Control [TDL1_EOM; addr 0AC]. In FCS mode, the EOM indicates that the FCS is to be calculated and transmitted following the last byte in the FIFO; in the Circular Buffer mode, the EOM indicates the end of the transmit circular buffer.

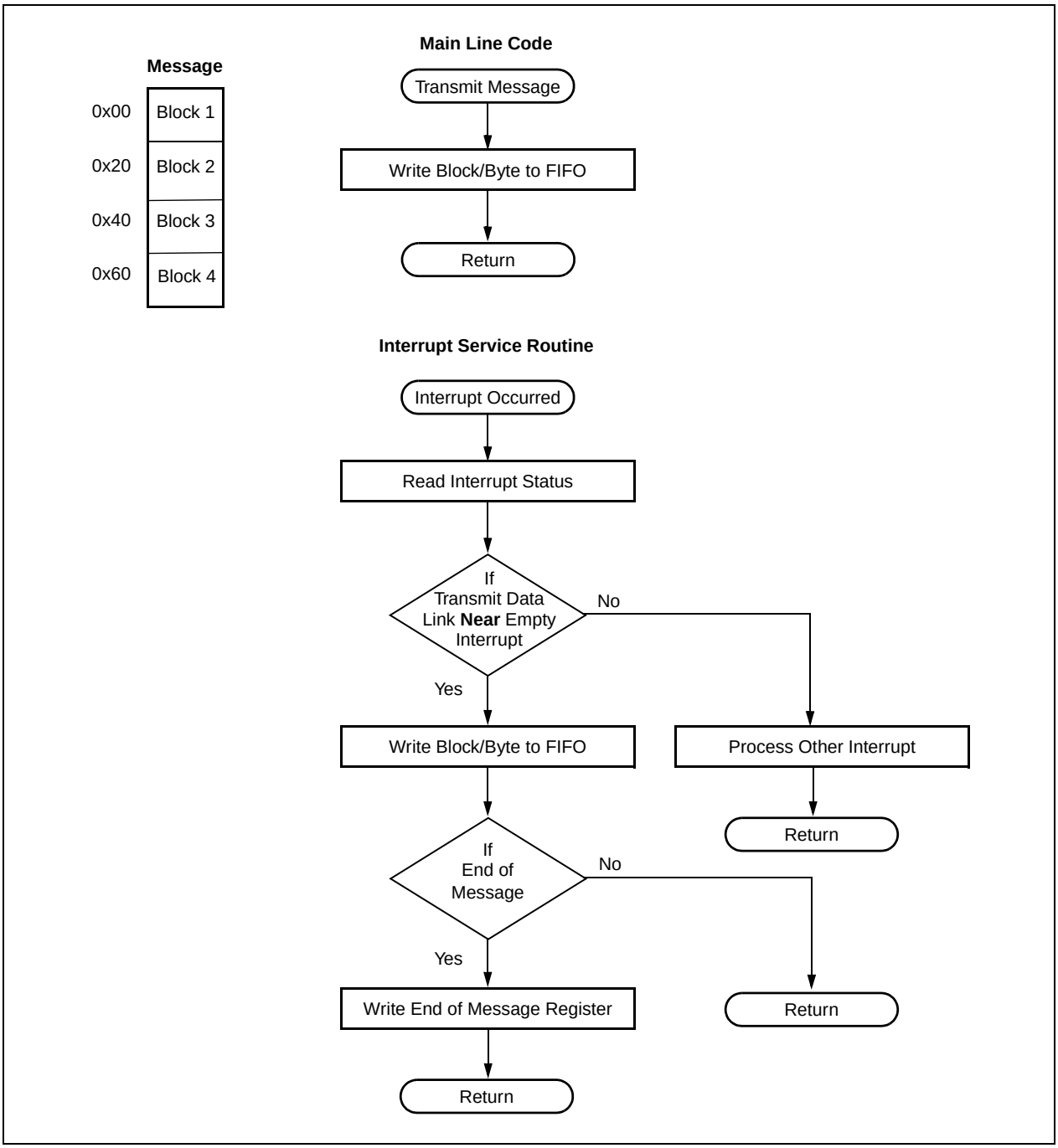
The Transmit Data Link Controller can be programmed according to the CPU bandwidth of your system. For systems with 1 CPU dedicated to 1 Bt8370, the data link status can be polled, and the 64-byte transmit FIFO can be used like a single byte transmit buffer. For systems where a single CPU controls multiple Bt8370s, the data link can be interrupt-driven and the entire 64-byte transmit FIFO can be used to store entire messages. See Figures 2-30 and 2-31 for a high-level description of polling and interrupt-driven Transmit Data Link Controller software.

Figure 2-30. Polled Transmit Data Link Processing



NOTE(S): Selected N based on the data rate of link.

Figure 2-31. Interrupt Driven Transmit Data Link Processing



Bt8370/8375/8376 uses a hierarchical interrupt structure, with 1 top-level Interrupt Request register [IRR; addr 003] directing software to the lower levels. Of all the interrupt sources, the 2 most significant bandwidth requirements are signaling and data link interrupts. Each data link controller has a top-level interrupt status register that reports data link operations (see Data Link 1 and 2 Interrupt Status registers [ISR2; addr 009, and ISR1; 00A]). The processor uses a 2-step interrupt scheme for the data link: it reads the Interrupt Request register, then uses that register value to read the corresponding Data Link Interrupt Status register.

2.8.2.2 PRM Generator

Performance Report Messages (PRMs) are HDLC messages containing path identification and performance monitoring information. If automatic performance report insertion is selected [AUTO_PRM; addr 0AA], a performance report is generated each second and begins transmitting coincident with the 1-second timer interrupt [ONESEC; addr 005]. The PRM is sent immediately if the processor sets the SEND_PRM bit in the Performance Report Message register [PRM; addr 0AA]. All performance monitoring fields of the message are automatically filled in when a PRM is generated. The remaining PRM bit fields are application-specific and can be configured using the Performance Report Message register.

For systems with a single processor and multiple Bt8370s, the automatic PRM generation can off-load a significant portion of CPU bandwidth.

TBOP Transmitter

The Transmit Bit-Oriented Protocol (TBOP) transmitter sends BOP messages, including ESF Yellow Alarm, which consists of repeated 16-bit patterns with an embedded 6-bit codeword. The TBOP is configured to operate over the same channel selected by Data Link #1 [DL1_TS; addr 0A4]. The TBOP must be configured to operate over the FDL channel. This is required for TBOP to convey Priority, Command, and Response codeword messages according to *ANSI T1.403, Section 9.4.1*. The precedence of transmitted BOP messages with respect to current DL1 transmit activity is configurable using the Transmit BOP mode bits [TBOP_MODE[1,0]; addr 0A0]. BOP messages can also be transmitted during E1 mode, although the 16-bit codeword pattern has not currently been adopted as an E1 standard. The length of the BOP message [TBOP_LEN[1,0]; addr 0A0] can be set to a single pattern, 10 patterns, 25 patterns, or continuous.

```
0xxxxxx0 11111111 (transmitted right to left)
[543210] TBOP = 6-bit codeword
```

BOP codewords are transmitted by writing to the Transmit BOP Codeword [TBOP; addr 0A1]. The real-time status of the codeword transmission can be monitored using TBOP_ACTIVE in the BOP Status register [BOP_STAT; addr 0A3]. A begin BOP transmit interrupt is available in Data Link 1 Interrupt Status [ISR2; addr 009].

2.8.3 Sa-Byte Overwrite Buffer

Five transmit Sa-Byte buffers [TSA4 to TSA8; addr 07B to 07F] are available; they insert Sa-bits into the odd frames of TS0. The entire group of 40 bits is sampled every 16 frames, coincident with the Transmit Multiframe bit interrupt boundary [TMF; addr 008]. Bit 0 from each TSA register is then inserted during frame 1, bit 1 is inserted during frame 3, bit 2 is inserted during frame 5, and so on, which gives the processor a maximum of 2 ms after TMF interrupt to write new Sa-Byte buffer values. Transmit Sa-bits maintain a fixed relationship to the transmit CRC multiframe. Each of the 5 Sa-Byte transmit buffers can be individually enabled using the Manual Sa-Byte Transmit Enable in the Transmit Manual Sa-Byte/FEBE Configuration register [TMAN; addr 074].

2.8.4 Overhead Pattern Generator

The transmit overhead generation circuitry provides the ability to insert all of the overhead associated with the Primary Rate Channel. The following types of overhead pattern generation are supported: Framing patterns, Alarm patterns, Cyclic Redundancy Check (CRC), and Far-End Block Error (FEBE).

2.8.4.1 Framing Pattern Generation

The framing pattern generation circuitry inserts the following patterns into the data stream: the 2-bit terminal framing (Ft) pattern, the 6-bit signaling frame (Fs) pattern, the 6-bit FPS pattern, the 8-bit FAS/NFAS pattern, and the 6-bit MFAS pattern.

The Ft pattern in SF, SLC-96, and T1DM is inserted into the transmit data stream by enabling the INS_FBIT in the Transmit Frame Format register [TFRM; addr 072]. The Fs pattern in SF is inserted by enabling the INS_MF bit. The FPS pattern in ESF and the FAS/NFAS pattern in E1 mode are inserted by enabling the INS_FBIT bit. The MFAS pattern is inserted by enabling the INS_MF bit.

2.8.4.2 Alarm Generator

The Transmit Alarm Generation circuitry generates Alarm Indication Signal (AIS) and Remote Alarm Indication (RAI/Yellow Alarm).

AIS Generation

AIS is defined as an unframed all-1s pattern and is normally transmitted when the data source is lost. AIS transmission can be enabled as follows:

- Manually
- Automatically upon detection of transmit loss of clock
- Automatically upon loss of received signal or loss of receive clock

Typical applications require transmission of AIS toward the line when DTE transmit data or clock is not present. In most applications, DTE data and clock are isolated from the transmitter, requiring manual AIS transmission under software control. Manual insertion of AIS is controlled by the TAIS bit in the Transmit Alarm Signal Configuration register [TALM; addr 075]. Setting this bit overwrites the currently transmitted data with the AIS pattern. If AISCLK [TLIU_CR; addr 068] is also set, AIS is transmitted using AIS Clock Input (ACKI); otherwise it uses the clock present at TCKI MUX output [CMUX; addr 01A].

Automatic transmission of AIS can be controlled by detection of transmit loss of clock [TLOC; addr 048]. This mode is enabled by setting AISCLK and providing an alternate transmit line rate clock on the ACKI clock input pin.

By setting AUTO_AIS in the TALM register, automatic transmission of AIS can also be controlled by detection of Receiver Loss of Signal [RLOS; addr 047] or Receiver Loss of Clock [RLOC; addr 047], depending on whether an analog or digital line interface option [RDIGI; addr 020] is used. This mode is typically used to transmit AIS (keep-alive) during line loopback if the received signal is lost. Setting AUTO_AIS simultaneously with setting LLOOP [LOOP; addr 014] enables this operation.

Yellow Alarm Generation

Yellow Alarm, also referred to as RAI (Remote Alarm Indication), is a bit pattern inserted into the transmit stream to alert far-end equipment that the local receiver cannot recover data. Yellow Alarm/RAI is typically transmitted during Receive Loss of Frame and is defined differently depending upon the transmit frame format configured [TFRAME; addr 070]. Table 2-11 describes the Yellow Alarm/RAI action taken for each frame format.

Table 2-11. Yellow Alarm Generation

Frame Format	Yellow Alarm Location	Mode
SF	Bit 2 of every time slot set to 0	YB2
ESF(1)	Bit 2 of every time slot set to 0	YB2
SLC-96	Bit 2 of every time slot set to 0	BY2
SF/JYEL	F-bit 12 of every superframe set to 1	YJ
T1DM	Y bit of the sync byte set to 0	Y24
E1	A bit of TS0 set to 1	Y0

NOTE(S):
(1) Yellow Alarm/RAI for T1-ESF framing is defined as a BOP priority codeword in the FDL channel. This is called T1 Multiframe Yellow Alarm in 8370. T1-ESF Multiframe Yellow Alarm/RAI(YF) is not transmitted using the procedure described below. Instead, T1- ESF Multiframe Yellow Alarm/RAI(YF) is generated by configuring DL1 to continuously transmit an all 0s BOP priority codeword. Refer to the Transmit Data Links section under TBOP Transmitter.

Transmission of Yellow Alarm(YB2) is controlled by the register bits listed in Table 2-12:

Table 2-12. Yellow Alarm Register Bits

Bit Name	Register
INS_YEL	[TFRM; addr 072]
TYEL	[TALM; addr 075]
AUTO_YEL	[TALM; addr 075]
RLOF	[ALM1; addr 047]
RLOF_INTEG	[RALM; addr 045]

The insertion of Yellow Alarm(YB2) into the transmit stream is controlled by INS_YEL. Yellow Alarm(YB2) is inserted only when INS_YEL is set. Otherwise, these bit positions are supplied by data from TPCMI. Yellow Alarm(YB2) generation can be done manually or automatically.

Manual generation of Yellow Alarm(YB2) is controlled by TYEL. Setting this bit immediately and unconditionally overwrites the Yellow Alarm signal bit(s) in the transmitted data stream with the appropriate pattern.

Automatic generation of Yellow Alarm(YB2) is controlled by AUTO_YEL, RLOF, and RLOF_INTEG. If AUTO_YEL is set, Yellow Alarm is generated during a Receive Loss of Frame alignment (RLOF = 1). Optionally, RLOF integration can be enabled by setting RLOF_INTEG. In this case, both RLOF indication and Yellow Alarm/RAI generation are delayed for approximately 2.5 seconds if a continuous out of frame condition exists. Yellow Alarm/RAI generation continues for at least 1 second after RLOF clears. Refer to Table 2-13.

Table 2-13. Multiframe Yellow Alarm Generation

Line Rate	Multiframe Yellow Alarm Action	Mode
T1	Facilitates Yellow Alarm Action (requires programming TDL1)	YF
E1	Set Y bit TS16 in frame 0 to 1	Y16

In T1 ESF framing mode, Multiframe Yellow Alarm or RAI is transmitted using BOP Codeword Transmitter [TBOP; addr 0A1] and does not depend on INS_MYEL. Transmitting Yellow Alarm/RAI toward the line can be done upon receiving Receive Loss of Frame. T1 multiframe Yellow Alarm must be generated by configuring TDL1 to transmit an all-0s BOP codeword. Optionally, RLOF integration can be enabled by setting RLOF_INTEG. In this case, both RLOF indication and Yellow Alarm/RAI generation are delayed for approximately 2.5 seconds if a continuous out of frame condition exists. Yellow Alarm/RAI generation continues for at least 1 second after RLOF clears. RLOF_INTEG does not meet the requirements of TR62411. To meet the requirements of *TR62411*, “Conditions Causing the Initiation of Carrier Failure Alarms,” the Receive Loss of Frame condition reported by FRED (addr 049) must be integrated before initiating Yellow Alarm Transmission. This can be accomplished in software by integrating FRED during an RLOF Interrupt (ISR7; addr 004), with RLOF_INTEG bit cleared.

In E1 CAS framing modes, Multiframe Yellow Alarm is inserted into the transmit stream to alert far-end equipment that local received multiframe alignment is not recovered. E1 Multiframe Yellow Alarm is transmitted by setting the Y bit in time slot 16, frame 0.

Transmission of Multiframe Yellow Alarm is controlled by the register bits listed in Table 2-14:

Table 2-14. Multiframe Yellow Alarm Register Bits

Bit Name	Register
INS_MYEL	[TFRM; addr 072]
TMYEL	[TALM; addr 075]
AUTO_MYEL	[TALM; addr 075]
SRED	[ALM3; addr 049]

The insertion of E1 Multiframe Yellow Alarm is controlled by INS_MYEL. E1 Multiframe Yellow Alarm is inserted only when INS_MYEL is set. Multiframe Yellow Alarm generation can be initiated manually or automatically.

Manual insertion of Multiframe Yellow Alarm is controlled by TMYEL. Setting this bit unconditionally overwrites the Multiframe Yellow Alarm signal bit in the transmitted data stream.

Automatic insertion of Multiframe Yellow Alarm is controlled by AUTO_MYEL in the TALM register. When set, the AUTO_MYEL mode sends a yellow alarm for the duration of a Receive Loss of CAS Multiframe Alignment [SRED; addr 049].

2.8.4.3 CRC Generation

The CRC generation circuitry computes the value of the CRC-6 code in T1 mode or the CRC-4 code in E1 mode. Once computed, it is inserted into the appropriate position of the transmitted data stream. CRC overwrite is enabled by the INS_CRC bit in Transmit Frame Format [TFRM; addr 072].

If the transmit frame format is configured as ESF, and the INS_CRC bit is active, the 2 kbps CRC sequence is inserted. (The position of the CRC-6 bits is shown in Table A-4, *Extended Superframe Format*).

If the transmit frame format is configured as E1 and the INS_CRC bit is active, the 4 kbps CRC sequence is inserted. (The position of the CRC-4 bits is shown in Table A-6, *ITU–T CEPT Frame Format Time Slot 0-Bit Allocations*.)

2.8.4.4 Far-End Block Error Generation

The Far-End Block Error (FEBE) generation circuitry inserts FEBE bits automatically or manually. Automatic FEBE generation is enabled by the INS_FE bit in TFRM. If the transmit frame format is configured as E1 and the INS_FE bit is active, a FEBE is generated in response to an incoming CRC-4 error by setting an E-bit of TS0 to 0. (Refer to Table A-7, *IRSM CEPT Frame Format Time Slot 0-Bit Allocations* for the location of the E-bits within the E1 frame.)

Manual FEBE generation is enabled by the TFEBE bit of the Transmit Manual Sa-Byte/FEBE Configuration register [TMAN; addr 074]. If the transmit frame format is configured as E1 and the TFEBE bit is active, the FEBE bits are supplied by the processor in FEBE_I and FEBE_II bits [addr 074].

2.8.5 Test Pattern Generator

The transmit test pattern generation circuitry overwrites the transmit data with various test patterns and permits logical and frame-bit error insertion. This feature is particularly useful for system diagnostics, production testing, and test equipment applications. The test pattern can be a framed or unframed PRBS pattern. The PRBS patterns available include 2E11-1, 2E15-1, 2E20-1, and 2E23-1. Each pattern can optionally include Zero Code Suppression (ZCS). Error insertion includes LCV, BPV, Ft, CRC4, CRC6, COFA, PRBS, Fs, MFAS, and CAS.

The Transmit Test Pattern Configuration register [TPATT; addr 076] controls the test pattern insertion circuit. TPATT controls the PRBS pattern (TPATT[1:0]) bits), ZCS setting (ZLIMIT bit), T1/E1 framing (FRAMED bit), and Starting and Stopping transmission (TPSTART bit).

Patterns are generated in accordance with *ITU–T O.150 (10/92)*, *O.151 (10/92)*, and *O.152 (10/92)*. Enabling ZLIMIT modifies the inserted pattern by limiting the number of consecutive 0s. For the 2E11-1 or 2E15-1 PRBS patterns, 8 or more 0s does not occur with ZLIMIT enabled. For the 2E20-1 or 2E23-1 PRBS patterns, 15 or more 0s will not occur with ZLIMIT enabled.

NOTE: The QRSS pattern is a 2E20-1 PRBS with ZLIMIT enabled. This function is performed according to ANSI T1.403 and ITU–T O.151 (10/92).

Frame bit positions can be preserved in the output pattern by enabling FRAMED. In T1 mode, this prevents the test pattern from overwriting the frame bit which occurs every 193 bits. In E1 mode with FRAMED enabled, the test pattern does not overwrite time slot 0 data (FAS and NFAS words) and time slot 16 (CAS signalling word) if CAS framing is also selected. CAS framing is selected by setting TFRAME[3] to 1 in the Transmit Configuration register [TCR0; addr 070]. The test pattern is stopped during these bit periods according to *ITU-T O.151, (10/92)*. If FRAMED is disabled, the test pattern is transmitted in all time slots.

2.8.6 Transmit Error Insertion

The Transmit Error Insert register [TERROR; addr 073] controls error insertion during pattern generation. Writing 1 to a TERROR bit injects a single occurrence of the respective error on TPOSO/TNEGO and XTIP/XRING outputs. Writing a 0 has no effect. Multiple transmit errors can be generated simultaneously. Periodic or random bit error rates can also be emulated by software control of the error control bit.

NOTE: Injected errors affect the data sent during a Framer or Analog Loopback [FLOOP or ALOOP; addr 014].

Line Code Violations (LCV) are inserted via the TVERR bit of the TERROR register. In T1 mode, if TVERR is set, a BPV is inserted between two consecutive ones. TVERR is latched until the BPV is inserted into the transmit data stream, and then it is cleared. In E1 mode with HDB3 selected, two consecutive BPVs of the same polarity are inserted. This is registered as a single LCV for the receiving E1 equipment.

Ft, FPS, and FAS bit errors are inserted using the TFERR bit in the TERROR register. TFERR commands a logical inversion of the next frame bit transmitted.

CRC4 (E1) and CRC6 (T1) bit errors are inserted using the TCERR bit in the TERROR register. TCERR commands a logical inversion of the next CRC bit transmitted.

Change of Frame Alignments (COFA) are controlled by the TCOFA and BSLIP bits in the TERROR register. TCOFA commands a 1-bit shift in the location of the transmit frame alignment by deleting (or inserting) a 1-bit position from the transmit frame. During E1 modes, BSLIP determines which direction the bit slip occurs. In T1 modes, only 1-bit deletion is provided. Note that TCOFA alters extraction rate of data from transmit slip buffer; thus, repeated TCOFAs eventually cause a controlled frame slip where 1 frame of data is repeated (T1/BSLIP = 0), or where 1 frame of data is deleted (BSLIP = 1).

PRBS test pattern errors are inserted by TBERR in the TERROR register. TBERR commands a single PRBS error by logically inverting the next PRBS generator output bit.

Fs and MFAS errors are controlled by the TMERR bit in the TERROR register. TMERR commands a single Fs bit error in T1, or MFAS bit error in E1 by logically inverting the next multiframe bit transmitted.

CAS Multiframe (MAS) errors are controlled by the TSERR bit in the TERROR register. TSERR commands a single MAS pattern error by logically inverting the first MAS bit transmitted.

2.8.7 In-Band Loopback Code Generator

The in-band loopback code generator circuitry overwrites the transmit data with in-band codes of configurable value and length. These codes are sequences with periods of 1 to 7 bits and may, in some applications, overwrite the framing bit. The Transmit Inband Loopback Code Configuration register [TLB; addr 077] controls the functions required for this operation.

A loopback code is generated in the transmit data stream by writing the loopback code to the Transmit Inband Loopback Code Pattern register [LBP; addr 078], and then by setting the Start Inband Loopback (LBSTART) and Loopback Length (LB_LEN) bits in the Transmit Inband Loopback Code Configuration register [TLB; addr 077]. The TLB register optionally allows the loopback code to overwrite framing bits using the UNFRAMED bit. The LB_LEN provides loopback code pattern lengths of 4 to 7 bits. Patterns of 2 or 3 bits can be achieved by repeating the pattern in 4- or 6-bit modes, respectively. Framed or unframed all 1s or all 0s can also be achieved by setting the pattern to all 0s or all 1s. The in-band loopback code generator is applicable only to T1 mode.

2.8.8 ZCS Encoder

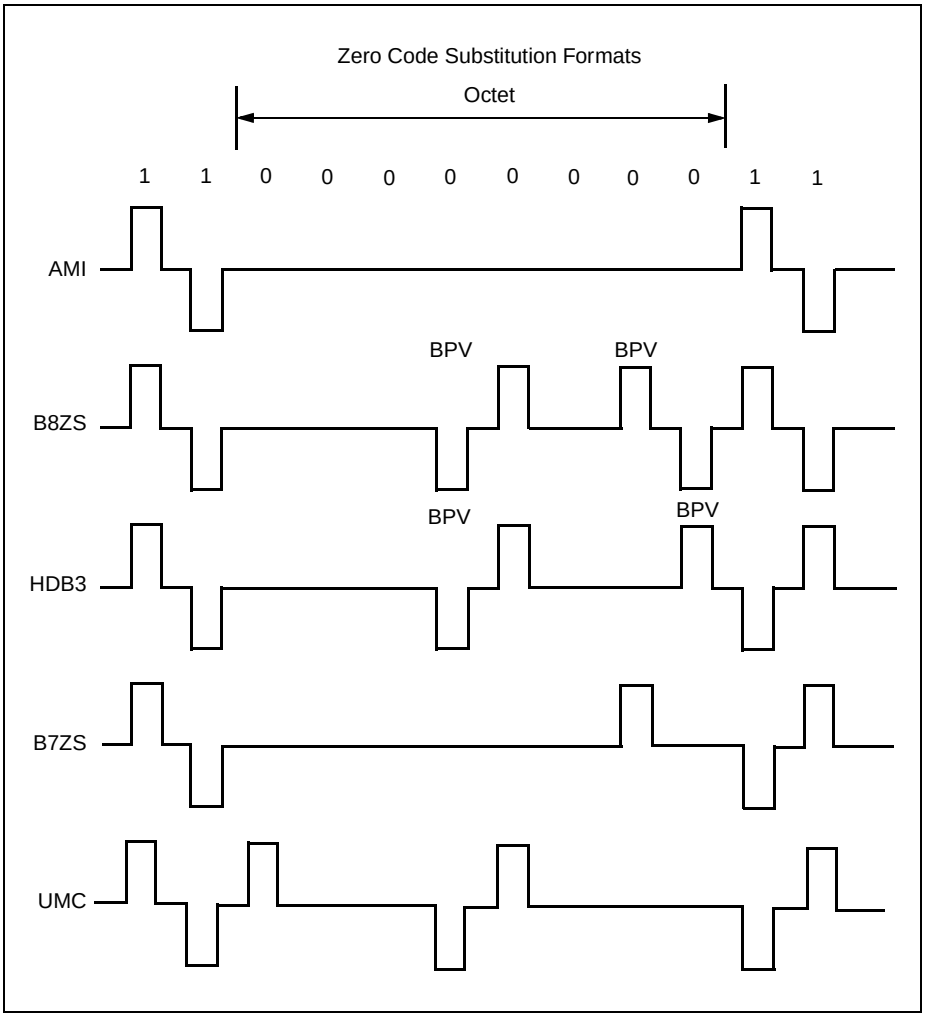
The ZCS encoder encodes the single rail clock and data (unipolar) into dual rail data (bipolar). The Transmit Zero Code Suppression Bits (TZCS[1,0]) in the Transmitter Configuration register [TCR1; addr 071] selects ZCS and Pulse Density Violation (PDV) enforcement options for XTIP/XRING and TPOSO/TNEGO output pins. TZCS supports the following: Alternate Mark Inversion (AMI), High Density Bipolar of order 3 (HDB3), Bipolar with 8 Zero Suppression (B8ZS), Pulse Density Violation (PDV), Unassigned Mux Code (UMC), and Bipolar with 7 Zero Suppression (B7ZS).

NOTE: ZCS encoding, which alters data content, is performed prior to the CRC calculation so the outgoing CRC will always be correct.

The AMI line code requires at least 12.5% average 1s density and no more than 15 consecutive 0s. A 1 is encoded as either a positive or negative pulse; a 0 is the absence of a pulse. Two consecutive pulses of the same polarity are referred to as a Bipolar Violation (BPV).

The HDB3 line code replaces 4 consecutive 0s by 000V or B00V code, where B is an AMI pulse and V is a bipolar violation (see Figure 2-32). ZCS encoder selects the code that forces the BPV output polarity opposite to the prior BPV.

Figure 2-32. Zero Code Substitution Formats



The B8ZS line code replaces strings of 8 consecutive 0s or no pulses with the B8ZS octet 000VB0VB, where B represents a normal bipolar pulse and V represents a BPV. A BPV that is not part of B8ZS octet is a BPV error.

B7ZS replaces Bit 7 of all assigned time slots with a 1 if the contents are all 0. B7ZS encoding is enabled on a per-channel basis in the Transmit Per-Channel Control register [TPC0 to TPC31; addr 100 to 11F].

PDV enforcer overwrites transmit 0s that would otherwise cause output data to fail to meet the minimum required pulse density, per ANSI T1.403 sliding window.

NOTE: The enforcer never overwrites a framing bit and is not applicable during E1 mode.

UMC forces DS0 channels containing eight 0s to be replaced with the 10011000 code, per Bellcore TA-TSY-000278.

NOTE: RCVR's ZCS decoder cannot recover original data content from a UMC or B7ZS encoded signal, or from a PDV-enforced one.

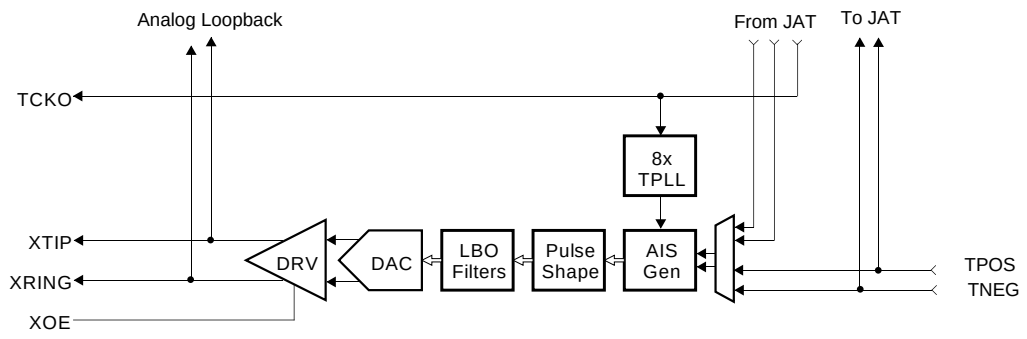
The TPOSO/TNEGO output pins provide access to the P and N rail unipolar data before it is sent to the TLIU. The output on TPOSO/TNEGO can be changed from dual rail unipolar to NRZ unipolar data (TNRZO) and to multiframe sync clock (MSYNCO), using the Transmit NRZ Data (TNRZ) bit in TCR1[addr 071]. The TNRZ setting does not affect the XTIP/XRING output.

2.9 Transmit Line Interface Unit

The Transmit Line Interface Unit (TLIU), illustrated in Figure 2-33, converts P and N rail NRZ data to AMI pulses. The P and N rail NRZ data is generated by the XMTR, converted to AMI bipolar pulses by the TLIU, and output on the transmit tip and ring pins, XTIP and XRING. The TLIU has a configurable line rate, pulse shape, Line Build Out (LBO), external termination resistor, and transformer turns ratio.

The TLIU consists of a control circuit, a pulse template ROM, a set of LBO filters, a Digital-to-Analog Converter (DAC), and a line driver.

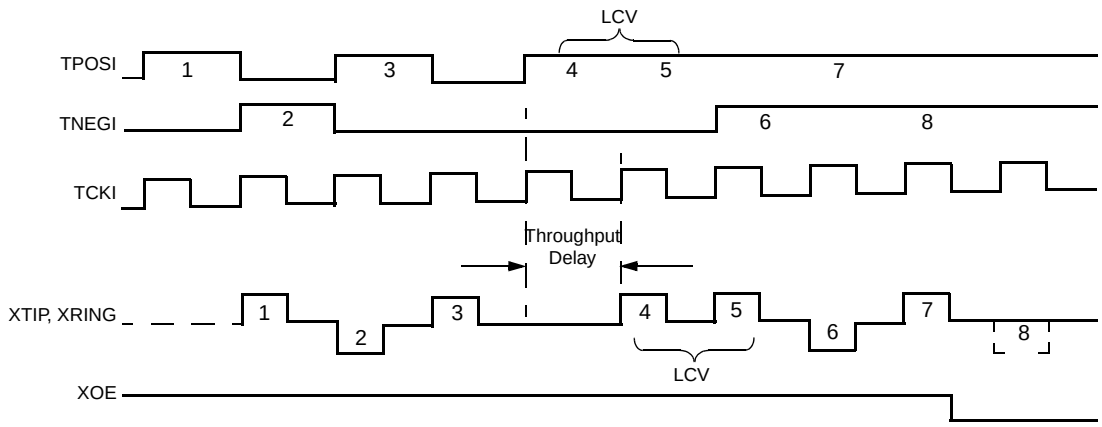
Figure 2-33. TLIU Diagram



NOTE(S): LBO filter block is not present in short haul devices: Bt8375 and Bt8376.

The TLIU can be used independently of the XMTR by applying P and N rail NRZ data to the TPOSI and TNEGI pins. Figure 2-34 shows the relationship between the P and N rail NRZ data, the transmit clock input, and XTIP/XRING. The transmit clock input can be supplied on the Transmit Clock Input pin (TCKI) or can be slaved to other clocks in the system using the Clock Input Mux register [CMUX; addr 01A]. This figure also shows the XTIP/XRING outputs being three-stated using the XOE pin.

Figure 2-34. TLIU Waveform



NOTE(S): Transmit jitter attenuation bypassed.

2.9.1 Pulse Shape

Normalized and isolated AMI output pulses fit the T1/E1 pulse templates in Figures 2-35 and 2-37 when measured in accordance with the test circuits in Figures 2-36 and 2-38. Table 2-15 through Table 2-22 list the pulse template corner points. An isolated pulse is defined as a 1 followed by seven 0s for T1, and a 1 followed by three 0s for E1. The pulse templates shown in Figures 2-35 and 2-37 come from *ANSI T1.403-1995*, *ITU-T G.703*, and *ANSI T1.102-1993*.

Figure 2-35. Standard DS1 Pulse Template

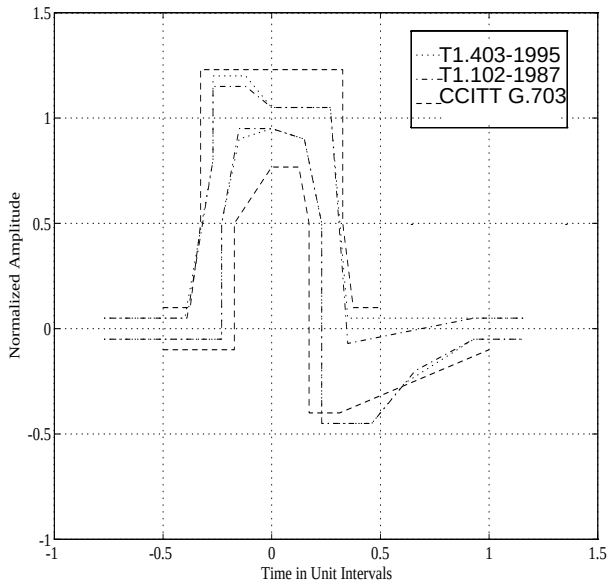
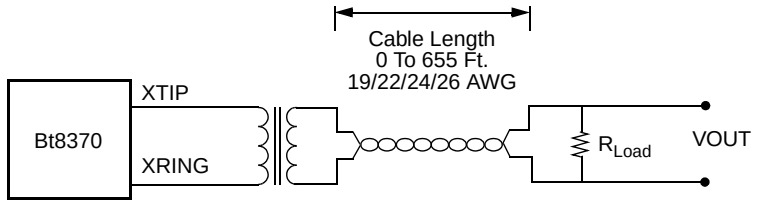


Figure 2-36. T1 Pulse Template Test Circuit



NOTE(S): R_{Load} = 100 Ω ± 5%.

Figure 2-37. Standard E1 (G.703) Pulse Template

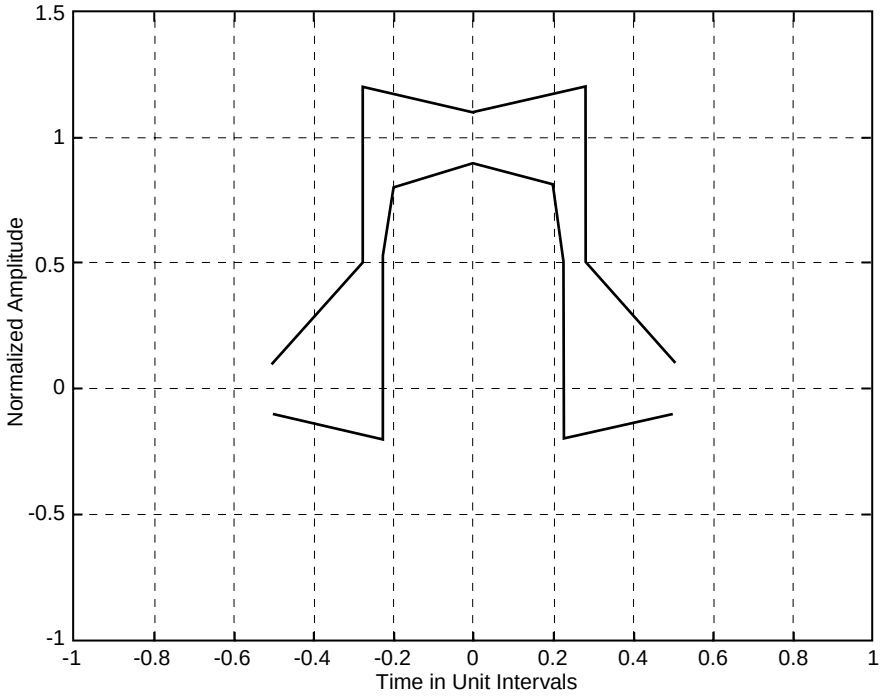
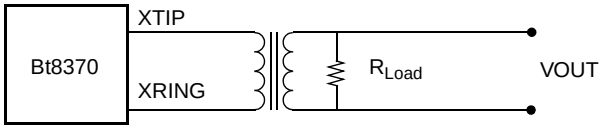


Figure 2-38. E1 (G.703) Pulse Template Test Circuit



NOTE(S):

1. For R_{Load} = 75 Ω (nominal) V_{out} (peak) = 2.37 V (nominal)
2. For R_{Load} = 120 Ω (nominal) V_{out} (peak) = 3.00 V (nominal)

Table 2-15. ANSI T1.102, 1993–DS1 Pulse Template Corner Points, Maximum Curve

Time (ns)	–400	–253	–175	–175	–75	0	175	228	602	700
Time (UI)	–0.62	–0.39	–0.27	–0.27	–0.12	0	0.27	0.35	0.93	1.08
Normalized Amplitude	0.05	0.05	0.80	1.15	1.15	1.05	1.05	–0.07	0.05	0.05

Table 2-16. ANSI T1.102, 1993–DS1 Pulse Template Corner Points, Minimum Curve

Time (ns)	–400	–150	–150	–100	0	100	150	150	300	427	602	700
Time (UI)	–0.62	–0.23	–0.23	–0.15	0	0.15	0.23	0.23	0.46	0.66	0.93	1.08
Normalized Amplitude	–0.05	–0.05	0.50	0.95	0.95	0.90	0.50	–0.45	–0.45	–0.20	–0.05	–0.05

Table 2-17. ANSI T1.403, 1995–DS1 Pulse Template Corner Points, Maximum Curve

Time (ns)	–400	–253	–175	–175	–75	0	175	228	500	700
Time (UI)	–0.62	–0.39	–0.27	–0.27	–0.12	0	0.27	0.35	0.77	1.08
Normalized Amplitude	0.05	0.05	0.80	1.20	1.20	1.05	1.05	–0.05	0.05	0.05

Table 2-18. ANSI T1.403, 1995–DS1 Pulse Template Corner Points, Minimum Curve

Time (ns)	–400	–150	–150	–100	0	100	150	150	300	396	600	700
Time (UI)	–0.62	–0.23	–0.23	–0.15	0	0.15	0.23	0.23	0.46	0.61	0.93	1.08
Normalized Amplitude	–0.05	–0.05	0.50	0.90	0.95	0.90	0.50	–0.45	–0.45	–0.26	–0.05	–0.05

Table 2-19. G.703, 1988–DS1 Pulse Template Corner Points, Maximum Curve

Time (ns)	–400	–243	–212	–212	212	212	243	700
Time (UI)	–0.62	–0.40	–0.33	–0.33	0.33	0.33	0.38	1.08
Normalized Amplitude	0.10	0.10	0.50	1.23	1.23	0.50	0.10	0.10

Table 2-20. G.703, 1988–DS1 Pulse Template Corner Points, Minimum Curve

Time (ns)	–400	–112	–112	0	81	112	112	212	700
Time (UI)	–0.62	–0.17	–0.17	0	0.13	0.17	0.17	0.33	1.08
Normalized Amplitude	–0.10	–0.10	0.50	0.77	0.77	0.50	–0.40	–0.40	–0.10

Table 2-21. G.703, 1988–Pulse Template Corner Points, Maximum Curve

Time (ns)	–244	–135	–135	0	135	135	224
Time (UI)	–0.50	0.276	–0.276	0	0.276	0.276	0.500
Normalized Amplitude	–0.10	0.0.50	1.20	1.10	1.20	0.50	0.10

Table 2-22. G.703, 1988–Pulse Template Corner Points, Minimum Curve

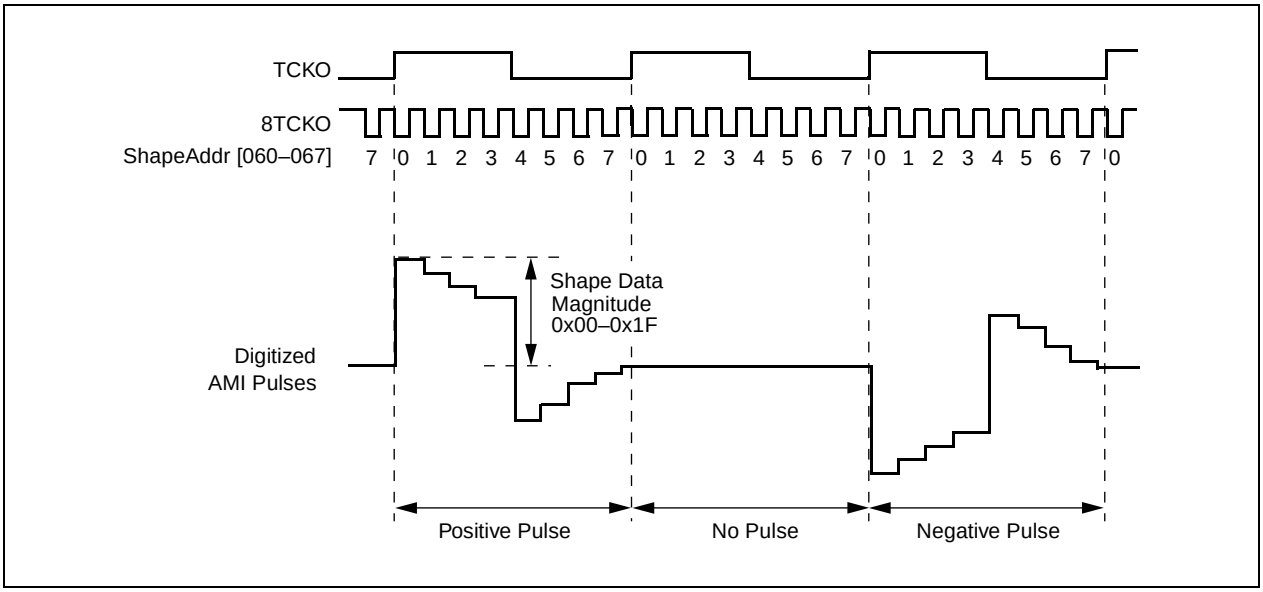
Time (ns)	–244	–110	–110	–97	0	97	110	110	244
Time (UI)	–0.500	–0.225	–0.225	–0.198	0	0.198	0.225	0.225	0.500
Normalized Amplitude	–0.10	–0.20	0.50	0.80	0.90	0.800	0.50	–0.20	–0.10

The pulse shape block receives P and N rail NRZ data. For each mark, it produces a set of eight 6-bit values which define the pulse shape to be transmitted, as illustrated in Figure 2-39. One of eight preprogrammed pulse shapes is selected via the Transmit LIU Configuration register [TLIU_CR; addr 068]. The TLIU control circuit downloads the code values associated with the selected pulse shape from the ROM to the Transmit Pulse Shape Configuration registers [SHAPE; addr 060–067], whenever the TLIU register is written to or when the device is reset. The SHAPE registers can be directly accessed via the microprocessor interface when a custom pulse shape is desired.

NOTE: Any modification to the TLIU register initiates another download to the SHAPE registers. The data stored in the pulse shape ROM and the SHAPE registers is 5-bit magnitude only.

The TLIU control circuit converts the 5-bit magnitude to 6-bit 2's complement data. The first 4 code values of the pulse (first half of the symbol) are forced to be positive, and the last 4 values (last half of the symbol) are forced to be negative, with respect to output pulse polarity.

Figure 2-39. Digitized AMI Pulse Shape



The VSET resistor not only provides a bias current to RPLL and TPLL but also controls the height of the transmit pulse. The VSET value can be fine tuned according to the total resistance on the line side. Table 2-23 shows the measured Peak value of the transmit pulse. (Please refer to Figures 4-1 through 4-4 for the recommended front-end circuitry.)

Table 2-23. Transmit Pulse

Rterm	75 Ω	VPk	2.36		2.36		2.30		2.28	
	100 Ω		LH = 2.96	SH = 3.16	LH = 2.96	SH = 3.12	LH = 2.88	SH = 3.00	LH = 2.80	SH = 3.04
	120 Ω		2.96		2.96		2.90		2.84	
PTC		No			No		One		Two	
Tx Series Resistance		No			2.1 Ω in series with XTIP and XRING		2.1 Ω in series with XTIP and XRING		2.1 Ω in series with XTIP and XRING	
VSET (Ω)		14 k			14 k		14 k		14 k	
Tx Termination (Ω)		51.1			51.1		51.1		51.1	
NOTE(S): LH refers to Long Haul, and SH refers to Short Haul.										

The minimum series resistance required with XTIP/XRING is 2.1 Ω . The two 2.1 Ω series resistors, together with the Shottky diodes, are necessary to protect the part against surge voltages of up to 50 V (please refer to Section 4, *Applications*). The line side protection circuitry should break down the voltage to 50 V so that the chip side protection circuitry (two 2.1 Ω series resistors with Shottky diodes) can protect the part for surge voltages of 50 V or below.

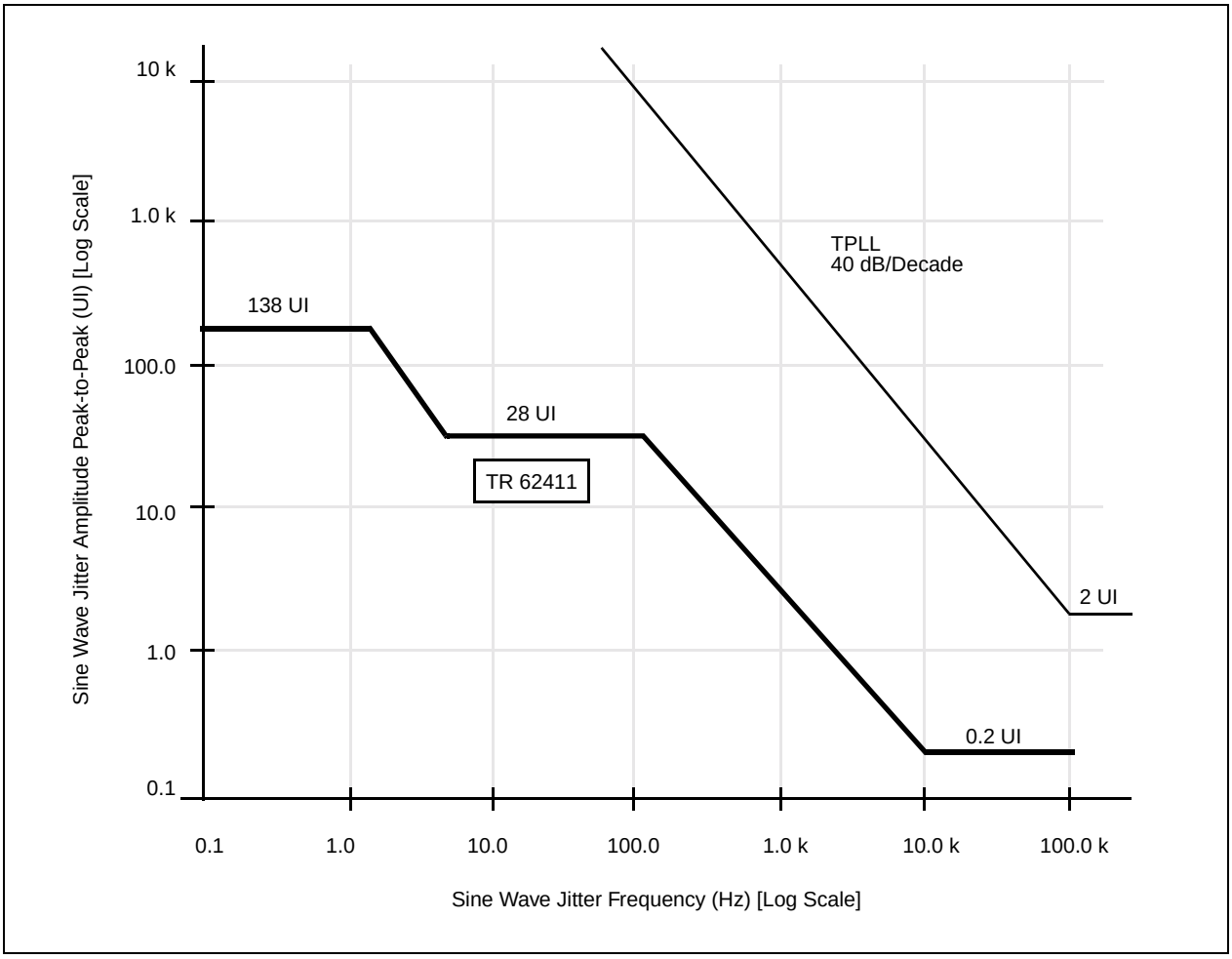
2.9.2 Transmit Phase Lock Loop

The Transmit Phase Lock Loop (TPLL) operates at a nominal rate of either 1.544 MHz or 2.048 MHz, selected by T1/E1N [CR0; addr 001]. The pull-in and hold-in range of the TPLL is ±200 ppm. The TPLL produces the transmit clock (TCKO) and an 8x clock that is used by the pulse shape block to generate the AMI pulses from TCKI clock mux, or JCLK.

2.9.2.1 Clock Reference

The TPLL reference clock is provided on the TCKO pin. If the jitter attenuator is enabled in the transmit direction [JDIR; addr 002], TCKO is the dejittered TCKI clock, or JCLK (if CLAD is enabled); otherwise, TCKO equals TCKI. The TCKI source is selected by TCKI[1:0] [CMUX; addr 01A]. TCKI can have the following selections: Recovered Receive Clock (RCKO), Receive System Bus Clock Input (RSBCKI), Clock Rate Adapter Output (CLADO), or an external clock, which is provided on the TCKI pin. The input clock jitter tolerance of the TPLL is illustrated in Figure 2-40.

Figure 2-40. TPLL Input Clock Jitter Tolerance



2.9.2.2 Output Jitter

The maximum output jitter generated on XTIP/XRING dependents on the transmit clock source selected. Refer to CLAD and JAT descriptions.

2.9.3 Line Build Out

In the Bt8370 long haul device, three LBO filter networks can be enabled in the TLIU to attenuate XTIP/XRING outputs in 7.5 dB steps, per the signal transfer function defined by FCC Part 68 Regulations. (See LBO[1:0] in TLIU_CR.) The number of LBO filters selected is based on the attached cable length. For short line lengths, larger LBO attenuation prevents far-end crosstalk. For longer line lengths, the appropriate line build-out must be selected. The following equation lists the transfer function for each of the 7.5 dB LBO filters:

$$\frac{V_{out}}{V_{in}} = \frac{n_2 S^2 + n_1 S + n_0}{d_3 S^3 + d_2 S^2 + d_1 S + d_0}$$

where:

$$n_0 = 1.6049 \times 10^{6}$$

$$n_1 = 7.9861 \times 10^{-1}$$

$$n_2 = 9.2404 \times 10^{-8}$$

$$d_0 = 2.1612 \times 10^{+6}$$

$$d_1 = 1.7223$$

$$d_2 = 4.575 \times 10^{-7}$$

$$d_3 = 3.8307 \times 10^{-14}$$

$$S = j2\pi f$$

$$f = frequency(\ Hz)$$

Pulse templates for each of the LBO settings are illustrated in Figure 2-41 through Figure 2-44.

Figure 2-41. 0 dB LBO Isolated Pulse Template

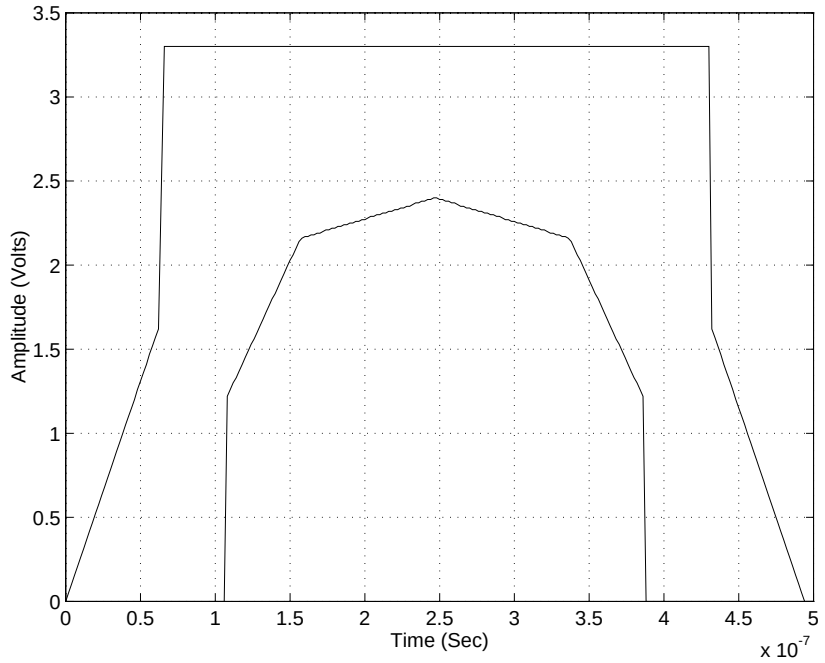


Figure 2-42. 7.5 dB LBO Isolated Pulse Template

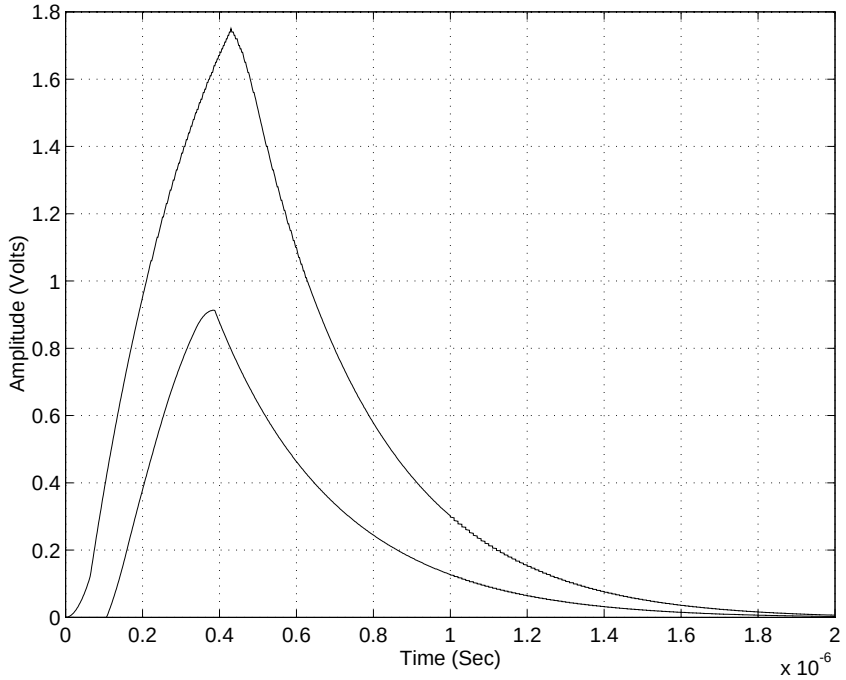


Figure 2-43. 15.0 dB LBO Isolated Pulse Template

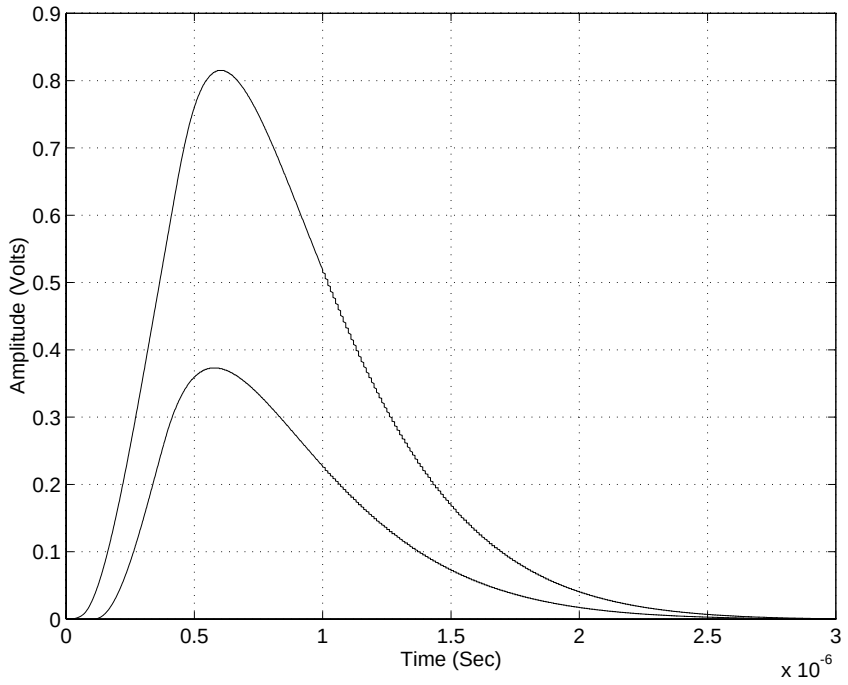
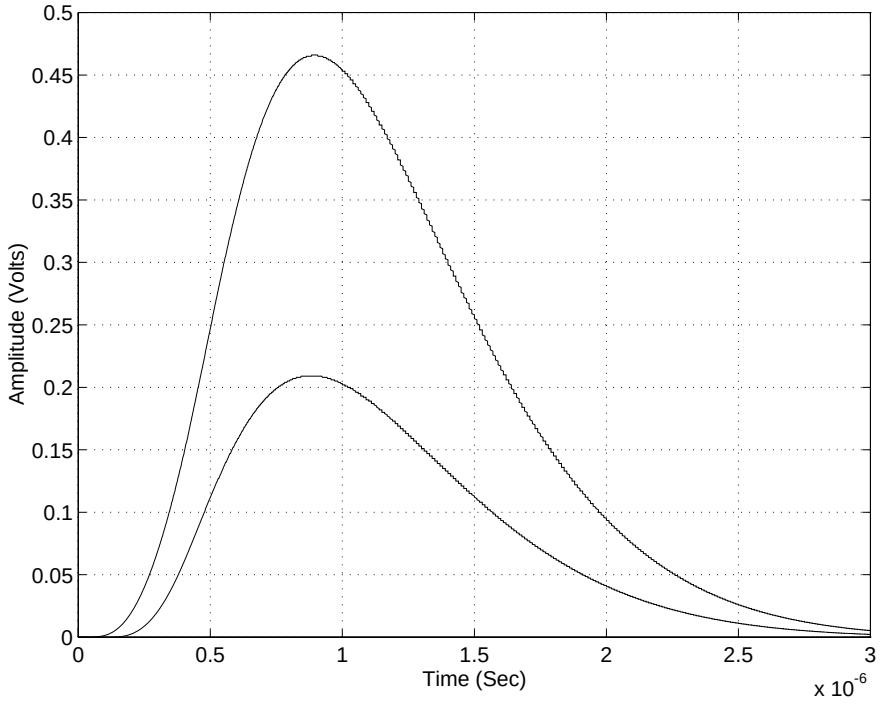


Figure 2-44. 22.5 dB LBO Isolated Pulse Template



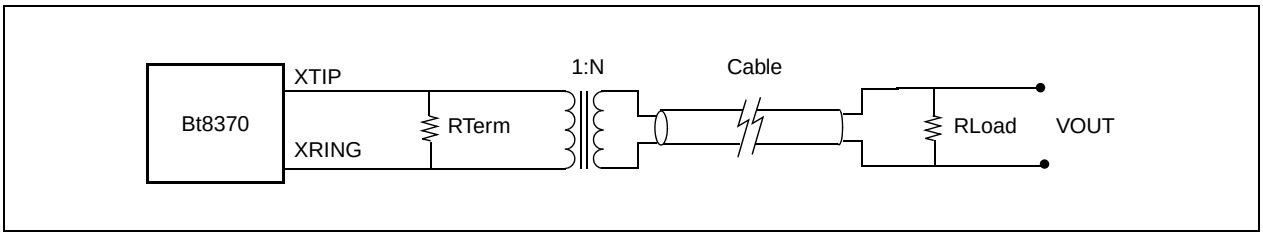
2.9.4 Line Driver

The line driver provides current drive to the low-power, bipolar analog signal from the transmit Digital-to-Analog Converter (DAC). The transmit DAC converts the coded pulse shape values to properly scaled, analog bipolar signals which drive the line transformer. The coded pulse shape values can optionally be filtered during T1 Longhaul by LBO filter options. The internal sensing circuits limit the drive current to less than 50 mA when a shorted line condition is detected for more than 48 transmitted pulses. Normal drive levels are restored when the short is removed. Typically, this is caused by a transmit cable short circuit or a transient transmission line current surge. The activation sets the TSHORT bit in Alarm 2 Status register [ALM2; addr 048].

2.9.4.1 Termination Impedance

If an external termination resistor is used, the TERM bit in TLIU_CR must be set. The transformer setting must also be set via the TURNS bit in TLIU_CR. An external termination resistor can be used only if the transformer turns ratio is 1:1.36. The external termination resistor (RTerm) is placed in parallel across XTIP/XRING, as illustrated in Figure 2-45.

Figure 2-45. External Termination Resistor Placement



2.9.4.2 Return Loss

Return loss is the measure of loss in the return path due to an impedance mismatch. To meet a –18 dB transmitter return loss, independent of the cable type, uses a 51.1 Ω termination resistor (see Figure 2-46). To see the effect of different termination resistors on the pulse height, see Figure 2-47.

Figure 2-46. Nominal Return Loss

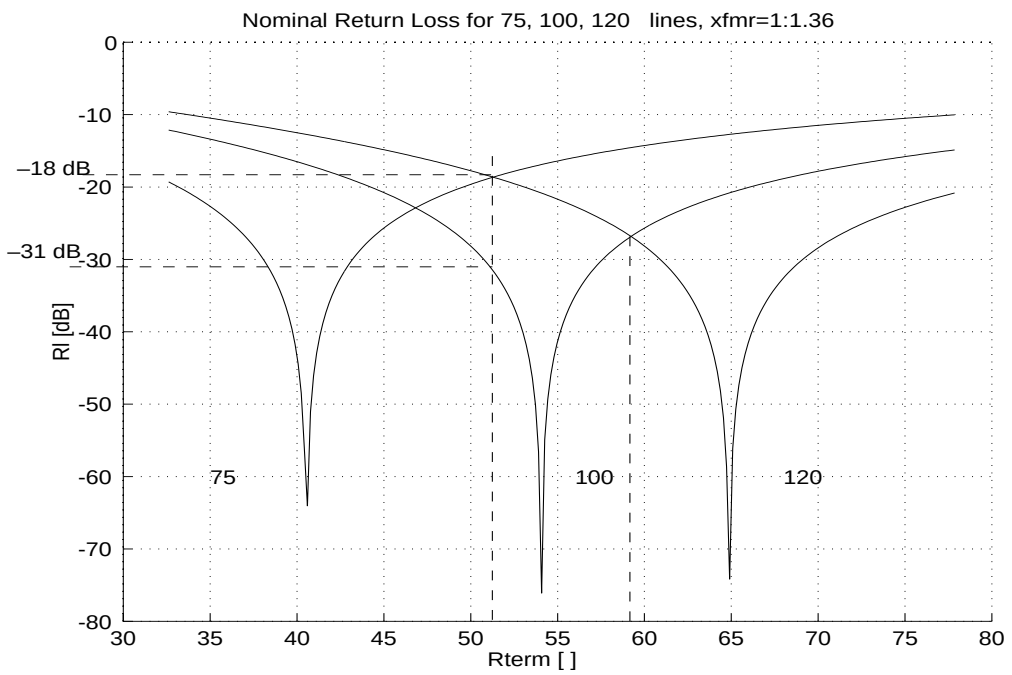
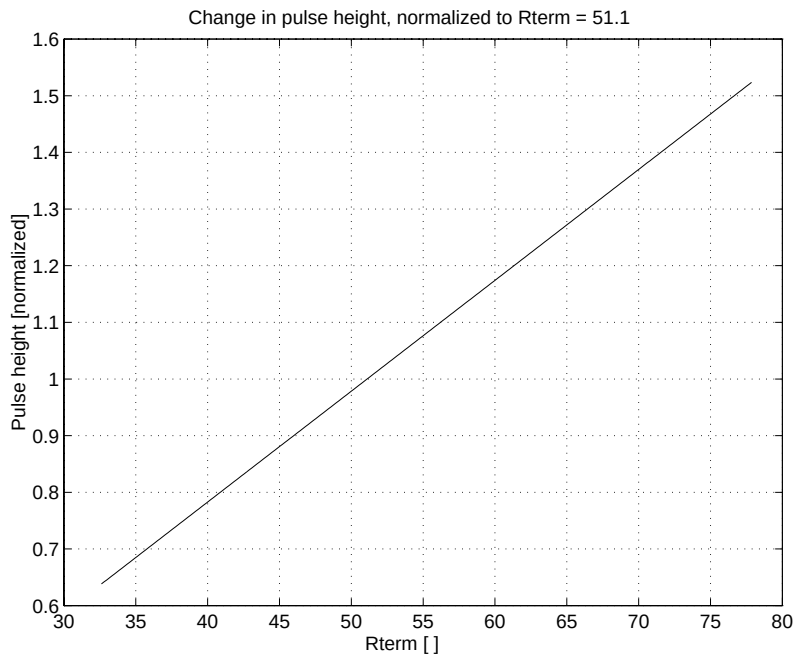


Figure 2-47. Output Pulse Height versus Transmit Termination Impedance



2.9.4.3 Output Enable

The bipolar analog output XTIP/XRING can be enabled or disabled using the XOE pin. This feature allows switching between multiple XTIP/XRING outputs that are tied together.

2.9.5 Pulse Imbalance

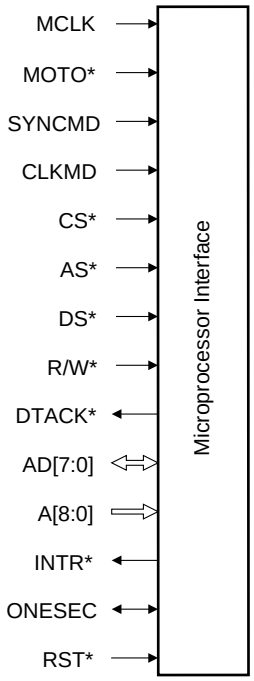
In any window of 17 consecutive primary rate cycles, the maximum variation in pulse amplitude in the absence of 60 Hz variations is <200 mV. The maximum variation in pulse width at half amplitude is <20 ns.

2.10 Microprocessor Interface

The Microprocessor Interface (MPU) provides the capability to configure the Bt8370, read status registers and counters, and respond to interrupts (see Figure 2-48). The interface supports both the Intel 8051 and Motorola 68000-type processors. In the Intel mode, the address and data are multiplexed; in the Motorola mode, the address and data are separate pins. Both synchronous and asynchronous Read and Write modes are supported. The synchronous mode is optimized for Motorola 68000-type processors with a maximum clock rate of 36 MHz. The asynchronous mode runs internally at 32 MHz, which limits the processor speed to 16 MHz for 8051 processors, and 30 MHz for 68302 processors.

The microprocessor interface consists of the following pins: MCLK, MOTO*, SYNCMD, CS*, AS*, DS*, R/W*, DTACK*, AD[7:0], A[8:0], INTR*, CLKMD, ONESEC, RST*. (A detailed description of the MPU pins is provided in Table 1-1, *Hardware Signal Definitions*.)

Figure 2-48. Microprocessor Interface Block Diagram



2.10.1 Address/Data Bus

In Non-multiplexed Address mode, A[8:0] provides the address for register access; in Multiplexed Address mode, A[8] and AD[7:0] provide the address. In both modes, the data bytes flow over the shared bidirectional, byte-wide bus, AD[7:0].

2.10.2 Bus Control Signals

Four signals control the operation of the interface port: AS*, CS*, RD*, and R/W*. An additional pin, MOTO*, selects whether the interface signals are of a Motorola or Intel flavor.

When MOTO* is low, indicating a Motorola-style interface, CS*, AS*, R/W*, and DS* signals are expected. When MOTO* is high, indicating an Intel-style interface, CS*, ALE, RD*, and WR* signals are expected.

When MOTO* is high, the address lines are multiplexed with the data. This pin is usually tied high for Intel devices, and low for Motorola devices. SYNCMD puts the interface into the Synchronous Processor Interface mode. Motorola 68000 processors typically have SYNCMD tied high if MCLK is connected to the MPU clock source, while Intel 8051 processors have SYNCMD tied low (see Table 2-24).

Table 2-24. Microprocessor Interface Operating Modes

MOTO*	SYNCMD	CLKMD	Description
0	0	0	Asynchronous Motorola, internal clock
0	1	1	Synchronous Motorola, external clock
1	0	0	Asynchronous Intel, internal clock
1	1	1	Synchronous Intel, external clock

2.10.3 Interrupt Requests

The INTR* output is an active low, open-drain type output which allows the interrupt request line from multiple devices to connect to a common microprocessor interrupt request line. All the Bt8370/8375/8376 interrupts are requested on this pin. However, each interrupt source can be individually enabled or disabled.

Interrupts are associated with three types of microprocessor interface registers:

- Interrupt Enable register—a 1 in a given bit of IER[7:0] enables the corresponding interrupt, a 0 (initial condition) disables it.
- Interrupt Status register [ISR; 7:0]—events are latched into these registers whether the corresponding interrupt enable bit is set or not. The processor must read the ISR registers to clear all latched bits.
- Interrupt Request register [IRR; addr 003]—reading this register along with the corresponding ISR register, the microprocessor can determine the cause of an interrupt. Active interrupts are indicated by bits that are high. Inactive interrupts are indicated by bits that are low. Reading from IRR clears the entire register; writing has no effect.

2.10.4 Device Reset

The Bt8370/8375/8376 contains three reset methods: internal power-on reset (POR), hardware reset which uses the RST* pin, and software reset which uses the RESET bit in register CR0 [addr 001]. All three methods result in device outputs placed in a high-impedance state and configuration registers set to default values as shown in Table 3-1, *Address Map*. In all reset methods, both REFCLK and MCLK (internal or external) must be present during the reset process for proper operation. MCLK (internal or external) performs the actual register initialization. Therefore, if the CLKMD pin is connected high to enable external MCLK, the external MCLK must be applied during reset, and if the CLKMD pin is low during reset, the internal clock (33 MHz) is used.

After hardware reset, software reset, or internal power-on reset, the microprocessor must initialize Bt8370/8375/8376 control registers and buffer memory registers to the desired state.

2.10.4.1 Power-On Reset (POR)

An internal POR process is initiated during power-up. When VDD has reached approximately 3 V, the internal reset process begins and continues for 2048 REFCLK cycles (approximately 205 µs) if REFCLK is applied. If REFCLK is not present, the Bt8370/8375/8376 remains in the reset state and does not terminate until detecting 2048 REFCLK cycles have been detected. The RESET bit in register CR0 [addr 001] can be monitored to determine when POR is complete. MCLK (internal or external) must be present during the POR concurrent with REFCLK to allow register initialization.

The LOOP register [addr 014] is not reset during power-on reset or internal reset so the device may occasionally power-on in a loopback state. If this occurs, several other registers (e.g., several IER registers) may not properly reset to their default values. To avoid this, after power-on or hardware reset, write the Loop register to 0 and then initiate a software reset using the RESET bit in the Primary Control register [CR0; addr 001]. After this procedure, all default registers have their default values. XOE needs to be disabled during the power-on reset period and re-enabled after configuring the part. The device must not be in Framer Loopback State when the software reset is written.

2.10.4.2 Hardware Reset

Hardware Reset is initiated by bringing the RST* pin active (low) for a minimum of 4 µs. If CLKMD is high (using external MCLK), external MCLK must be present while RST* is low to allow register initialization. After RST* is deactivated, the internal reset process continues for 5 µs, and register access must be avoided. The RESET bit in register CR0 [addr 001] can be monitored to determine when the reset process is complete.

2.10.4.3 Software Reset

Software Reset is initiated by writing the RESET bit [register CR0; addr 001] to 0, delaying at least 6 µs, then writing RESET to 1. Once initiated, the reset process continues for 15 µs maximum and register access must be avoided. The RESET bit can be monitored to determine when the reset process has completed. As with the other reset methods, both REFCLK and MCLK (internal or external) must be present during the reset process.

2.11 Loopbacks

Bt8370/8375/8376 provides a complete set of loopbacks for diagnostics, maintenance, and troubleshooting.

2.11.1 Remote Line Loopback

The remote line loopback loops the RCVR inputs to the XMTR outputs. The loopback provides BPV transparency and the ability to override the looped data with AIS. The RCVR data path is not affected by the activation of this loopback. Remote line loopback is activated by setting the Remote Line Loopback (LLOOP) bit in the Loopback Configuration register [LOOP; addr 014]. It is possible to operate the remote line loopback simultaneously with the local framer loopback. If receive jitter attenuator is also enabled, RJAT is placed in the line loopback path. TJAT, if enabled, is not present in the line loopback path.

2.11.2 Remote Payload Loopback

The remote payload loopback loops all DS0 channels from the RCVR input to the XMTR output. Loopback payload retains time slot integrity, such that numbered time slots from each receive frame are transferred to same numbered time slots in the transmit frame. Transmit overhead bits—F-bits in T1 mode or TS0 in E1 mode—are supplied by the transmit frame formatter or by the TSB, depending on TFRM [addr 072] settings. Existing transmit frame alignment and clock timing are not altered by [PLOOP; addr 014] activation or deactivation, allowing system operation with independent receive and transmit timing. Controlled frame slips are performed in the payload loopback path if receive and transmit clocks are asynchronous, although these slips are not reported to the processor as slip buffer errors. Multiframe integrity is not maintained during PLOOP; therefore, DS0 and signaling channel loopbacks [TPCn; addr 100–11F] must be used to implement payload loopback if transparent or forced signaling is desired. PLOOP does not override by transmit per-channel remote loopback selection (TLOOP bit in TPCn).

2.11.3 Remote Per-Channel Loopbacks

The remote per-channel loopback loops the RCVR input DS0 channel to the XMTR output DS0 channel. The remote per-channel loopback is activated by setting TLOOP in the Transmit Per-Channel Control register [TPC0 to TPC31; addr 100 to 11F].

2.11.4 Local Analog Loopback

RLIU provides a local analog loopback to internally route bipolar data from XTIP/XRING to RTIP/RRING. In the local analog loopback mode, externally applied data on RTIP/RRING inputs is ignored, and XTIP/XRING output data is unaffected. The local analog loopback is configured using the ALOOP bit in the Loopback Configuration register [LOOP; addr 014]. If RCKO is selected as the TCKI clock source [CMUX; addr 01A], an alternate transmit clock source must be provided when this loopback is activated. Possible configurations include selecting the TCKI pin or CLADO as the transmit clock source, or programming the JAT in the transmit direction and setting JFREE to enable the free-running 10 MHz reference [JAT_CR register; addr 002]. After activating or deactivating this loopback, the RLIU must be reset using RST_LIU in the LIU Configuration register [LIU_CR; addr 020]. The transmitter outputs must connect to a cable termination or a transmit termination resistor for local analog loopback to pass bipolar signals. If no cable and no resistor termination are supplied, then ALOOP cannot pass bipolar signals to RTIP/RRING.

2.11.5 Local Framer Loopback

The local framer loopback loops the transmit line encoder outputs to the receive line encoder inputs. The TLIU output is not affected by the activation of this loopback. The local framer loopback is activated by setting the Local Framer Loopback (FLOOP) bit in the Loopback Configuration register [LOOP; addr 014]. If RCKO is selected as the TCKI clock source [CMUX; addr 01A], then an alternate transmit clock source must be provided when this loopback is activated. Possible configurations include selecting the TCKI pin or CLADO as the transmit clock source, or programming the JAT in the transmit direction and setting JFREE to enable the free running 10 MHz reference [JAT_CR register; addr 002]. It is possible to operate the local framer loopback simultaneously with the remote line loopback. If transmit jitter attenuator is also enabled, TJAT is placed in the framer loopback path. RJAT, if enabled, is not present in the framer loopback path.

2.11.6 Local Per-Channel Loopback

The local per-channel loopback loops the TSB PCM and signaling inputs to the RSB PCM and signaling outputs on a per-channel basis. The local per-channel PCM loopback is activated by setting RLOOP in the System Bus Per-Channel Control registers [SBC0 to SBC31; addr 0E0 to 0FF]. The local per-channel signaling loopback is activated by setting SIG_LP in System Bus Per-Channel Control registers.

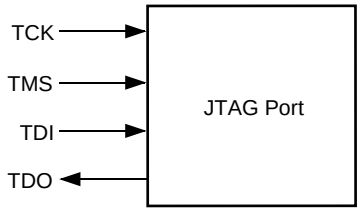
2.12 Joint Test Access Group

The Bt8370/8375/8376 incorporates printed circuit board testability circuits in compliance with IEEE Std. P1149.1a–1993, *IEEE Standard Test Access Port and Boundary–Scan Architecture*, commonly known as JTAG (Joint Test Action Group).

The JTAG includes a Test Access Port (TAP) and several data registers. The TAP provides a standard interface through which instructions and test data are communicated (see Figure 2-49). A Boundary Scan Description Language (BSDL) file for the Bt8370/8375/8376 is available from the factory upon request.

The test access port consists of the TDI, TCK, TMS, and TDO pins. An internal power on reset circuit resets the JTAG port.

Figure 2-49. JTAG Diagram



2.12.1 Instructions

In addition to the required BYPASS, SAMPLE/PRELOAD, and EXTEST instructions, IDCODE instruction is supported. There are also two private instructions. Table 2-25 lists the JTAG instructions, and their codes.

Table 2-25. JTAG Instructions

Instruction	Code
BYPASS	111 111
SAMPLE/PRELOAD	000 001
EXTEST	000 000
IDCODE	000 010
Private	xxx xxx
Private	xxx xxx

2.12.2 Device Identification Register

The JTAG ID register consists of a 4-bit version, a 16-bit part number, and an 11-bit manufacturer number (see Tables 2-26 through 2-28).

Table 2-26. Bt8370/8375/8376 Device Identification JTAG Register

Version[(1)]				Part Number																Manufacturer ID											
1	0	0	0	1	0	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0	0	1	1	0	1	0	1	1	0	1
0x8				0x8370																0x0D6											
4 bits				16 bits																11 bits											

TDO

NOTE(S):
(1) Consult factory for current version number.

Table 2-27. Bt8375 Device Identification JTAG Register

Version[(1)]				Part Number																Manufacturer ID											
0	1	0	0	1	0	0	0	0	0	1	1	0	1	1	1	0	1	0	1	0	0	0	1	1	0	1	0	1	1	0	1
0x8				0x8375																0x0D6											
4 bits				16 bits																11 bits											

TDO

NOTE(S):
(1) Consult factory for current version number.

Table 2-28. Bt8376 Device Identification JTAG Register

Version[(1)]				Part Number																Manufacturer ID											
0	1	0	0	1	0	0	0	0	0	1	1	0	1	1	1	0	1	1	0	0	0	0	1	1	0	1	0	1	1	0	1
0x8				0x8376																0x0D6											
4 bits				16 bits																11 bits											

TDO

NOTE(S):
(1) Consult factory for current version number.

3.0 Registers

Registers shown with a default setting are reset to the indicated value following power-up, software RESET (CR0; addr 001), or hardware reset (RST* pin). Refer to Table 3-1.

3.1 Address Map

Table 3-1. Address Map *(1 of 8)*

Block	Address (Hex)	Acronym	R/W	Description	Default Register Setting		
					Bt8370	Bt8375	Bt8376
Global	000	DID	R	Device Identification	08	58	68
	001	CR0	R/W	Primary Control register	00	00	00
	002	JAT_CR	R/W	Jitter Attenuator Configuration	00	00	00
	003	IRR	R	Interrupt Request register	—	—	—
Interrupt Status	004	ISR7	R	Alarm 1 Interrupt Status	—	—	—
	005	ISR6	R	Alarm 2 Interrupt Status	—	—	—
	006	ISR5	R	Error Interrupt Status	—	—	—
	007	ISR4	R	Counter Overflow Interrupt Status	—	—	—
	008	ISR3	R	Timer Interrupt Status	—	—	—
	009	ISR2	R	Data Link 1 Interrupt Status	—	—	—
	00A	ISR1	R	Data Link 2 Interrupt Status	—	—	—
	00B	ISR0	R	Pattern Interrupt Status	—	—	—

Table 3-1. Address Map *(2 of 8)*

Block	Address (Hex)	Acronym	R/W	Description	Default Register Setting		
					Bt8370	Bt8375	Bt8376
Interrupt Enable	00C	IER7	R/W	Alarm 1 Interrupt Enable register	00	00	00
	00D	IER6	R/W	Alarm 2 Interrupt Enable register	00	00	00
	00E	IER5	R/W	Error Interrupt Enable register	00	00	00
	00F	IER4	R/W	Count Overflow Interrupt Enable register	00	00	00
	010	IER3	R/W	Timer Interrupt Enable register	00	00	00
	011	IER2	R/W	Data Link 1 Interrupt Enable register	00	00	00
	012	IER1	R/W	Data Link 2 Interrupt Enable register	00	00	00
	013	IER0	R/W	Pattern Interrupt Enable register	00	00	00
Primary	014	LOOP	R/W	Loopback Configuration register	—	—	—
	015	DL3_TS	R/W	External Data Link Channel	—	—	—
	016	DL3_BIT	R/W	External Data Link Bit	—	—	—
	017	FSTAT	R	Offline Framer Status	—	—	—
	018	PIO	R/W	Programmable Input/Output	00	00	00
	019	POE	R/W	Programmable Output Enable	3F	3F	3F
	01A	CMUX	R/W	Clock Input Mux	00	00	00
	01B	TMUX	R/W	Test Mux Configuration	00	00	00
	01C	TEST	R/W	Test Configuration	00	00	00

Table 3-1. Address Map *(3 of 8)*

Block	Address (Hex)	Acronym	R/W	Description	Default Register Setting		
					Bt8370	Bt8375	Bt8376
Receive LIU (RLIU)	020	LIU_CR	R/W	LIU Configuration	00	00	00
	021	RSTAT	R	Receive LIU Status	—	—	—
	022	RLIU_CR	R/W	Receive LIU Configuration	31	31	31
	023	LPF	R/W	RPLL Low Pass Filter	33	33	33
	024	VGA_MAX	R/W	Variable Gain Amplifier Maximum	3F	2F	2F
	025	EQ_DAT	R/W	Equalizer Coefficient Data register	—	—	—
	026	EQ_PTR	R/W	Equalizer Coefficient Table Pointer	—	—	—
	027	DSLICE	R/W	Data Slicer Threshold	BA	BA	BA
	028	EQ_OUT	R/W	Equalizer Output Levels	DA	DA	DA
	029	VGA	R	Variable Gain Amplifier Status	—	—	—
	02A	PRE_EQ	R/W	Pre-Equalizer	26	26	26
	030–037	COEFF	R	LMS Adjusted Equalizer Coefficient Status	—	—	—
	038–03C	GAIN	R/W	Equalizer Gain Thresholds	16, 1F, 21, 24, 26	16, 1F, 21, 24, 26	16, 1F, 21, 24, 26
Digital Receiver (RCVR)	040	RCR0	R/W	Receiver Configuration	—	—	—
	041	RPATT	R/W	Receive Test Pattern Configuration	—	—	—
	042	RLB	R/W	Receive Loopback Code Detector Configuration	—	—	—
	043	LBA	R/W	Loopback Activate Code Pattern	—	—	—
	044	LBD	R/W	Loopback Deactivate Code Pattern	—	—	—
	045	RALM	R/W	Receive Alarm Signal Configuration	—	—	—
	046	LATCH	R/W	Alarm/Error/Counter Latch Configuration	—	—	—
	047	ALM1	R	Alarm 1 Status	—	—	—
	048	ALM2	R	Alarm 2 Status	—	—	—
	049	ALM3	R	Alarm 3 Status	—	—	—

Table 3-1. Address Map *(4 of 8)*

Block	Address (Hex)	Acronym	R/W	Description	Default Register Setting		
					Bt8370	Bt8375	Bt8376
Error/Alarm Counters	050	FERR	R	Framing Bit Error Counter LSB	—	—	—
	051	FERR	R	Framing Bit Error Counter MSB	—	—	—
	052	CERR	R	CRC Error Counter LSB	—	—	—
	053	CERR	R	CRC Error Counter MSB	—	—	—
	054	LCV	R	Line Code Violation Counter LSB	—	—	—
	055	LCV	R	Line Code Violation Counter MSB	—	—	—
	056	FEBE	R	Far End Block Error Counter LSB	—	—	—
	057	FEBE	R	Far End Block Error Counter MSB	—	—	—
	058	BERR	R	PRBS Bit Error Counter LSB	—	—	—
	059	BERR	R	PRBS Bit Error Counter MSB	—	—	—
Receive Sa-Byte	05B	RSA4	R	Receive Sa4 Byte Buffer	—	—	—
	05C	RSA5	R	Receive Sa5 Byte Buffer	—	—	—
	05D	RSA6	R	Receive Sa6 Byte Buffer	—	—	—
	05E	RSA7	R	Receive Sa7 Byte Buffer	—	—	—
	05F	RSA8	R	Receive Sa8 Byte Buffer	—	—	—
TLIU	060–067	SHAPE	R/W	Transmit Pulse Shape Configuration	15, 14, 14, 14, 6, 4, 2, 1	15, 14, 14, 14, 6, 4, 2, 1	15, 14, 14, 14, 6, 4, 2, 1
	068	TLIU_CR	R/W	Transmit LIU Configuration	01	01	01

Table 3-1. Address Map *(5 of 8)*

Block	Address (Hex)	Acronym	R/W	Description	Default Register Setting		
					Bt8370	Bt8375	Bt8376
Digital Transmitter (XMTR)	070	TCR0	R/W	Transmit Framer Configuration	—	—	—
	071	TCR1	R/W	Transmitter Configuration	—	—	—
	072	TFRM	R/W	Transmit Frame Format	—	—	—
	073	TERROR	R/W	Transmit Error Insert	—	—	—
	074	TMAN	R/W	Transmit Manual Sa-Byte/FEBE Configuration	—	—	—
	075	TALM	R/W	Transmit Alarm Signal Configuration	—	—	—
	076	TPATT	R/W	Transmit Test Pattern Configuration	—	—	—
	077	TLB	R/W	Transmit Inband Loopback Code Configuration	—	—	—
	078	LBP	R/W	Transmit In-Band Loopback Code Pattern	—	—	—
Transmit Sa-Byte	07B	TSA4	R/W	Transmit Sa4 Byte Buffer	—	—	—
	07C	TSA5	R/W	Transmit Sa5 Byte Buffer	—	—	—
	07D	TSA6	R/W	Transmit Sa6 Byte Buffer	—	—	—
	07E	TSA7	R/W	Transmit Sa7 Byte Buffer	—	—	—
	07F	TSA8	R/W	Transmit Sa8 Byte Buffer	—	—	—
CLAD	090	CLAD_CR	R/W	Clock Rate Adapter Configuration	07	07	07
	091	CSEL	R/W	CLAD Frequency Select	01	01	01
	092	CPHASE	R/W	CLAD Phase Detector Scale Factor	00	00	00
	093	CTEST	R/W	CLAD Test	00	00	00
BOP	0A0	BOP	R/W	Bit Oriented Protocol Transceiver	00	00	00
	0A1	TBOP	R/W	Transmit BOP Code Word	00	00	00
	0A2	RBOP	R	Receive BOP Code Word	—	—	—
	0A3	BOP_STAT	R	BOP Status	—	—	—

Table 3-1. Address Map *(6 of 8)*

Block	Address (Hex)	Acronym	R/W	Description	Default Register Setting		
					Bt8370	Bt8375	Bt8376
Data Link #1	0A4	DL1_TS	R/W	DL1 Time Slot Enable	00	00	00
	0A5	DL1_BIT	R/W	DL1 Bit Enable	00	00	00
	0A6	DL1_CTL	R/W	DL1 Control	00	00	00
	0A7	RDL1_FFC	R/W	RDL #1 FIFO Fill Control	00	00	00
	0A8	RDL1	R	Receive Data Link FIFO #1	—	—	—
	0A9	RDL1_STAT	R	RDL #1 Status	—	—	—
	0AA	PRM	R/W	Performance Report Message	00	00	00
	0AB	TDL1_FEC	R/W	TDL #1 FIFO Empty Control	00	00	00
	0AC	TDL1_EOM	W	TDL #1 End Of Message Control	—	—	—
	0AD	TDL1	R/W	Transmit Data Link FIFO #1	—	—	—
	0AE	TDL1_STAT	R	TDL #1 Status	—	—	—
Data Link #2	0AF	DL2_TS	R/W	DL2 Time Slot Enable	00	00	N/A
	0B0	DL2_BIT	R/W	DL2 Bit Enable	00	00	N/A
	0B1	DL2_CTL	R/W	DL2 Control	00	00	N/A
	0B2	RDL2_FFC	R/W	RDL #2 FIFO Fill Control	00	00	N/A
	0B3	RDL2	R	Receive Data Link FIFO #2	—	—	—
	0B4	RDL2_STAT	R	RDL #2 Status	—	—	—
	0B6	TDL2_FEC	R/W	TDL #2 FIFO Empty Control	00	00	N/A
	0B7	TDL2_EOM	W	TDL #2 End Of Message Control	—	—	—
	0B8	TDL2	R/W	Transmit Data Link FIFO #2	—	—	—
	0B9	TDL2_STAT	R	TDL #2 Status	—	—	—
Test	0BA	DL_TEST1	R/W	DLINK Test Configuration	00	00	00
	0BB	DL_TEST2	R/W	DLINK Test Status	00	00	00
	0BC	DL_TEST3	R/W	DLINK Test Status	00	00	00
	0BD	DL_TEST4	R/W	DLINK Test Control #1 or Configuration #2	00	00	00
	0BE	DL_TEST5	R/W	DLINK Test Control #2 or Configuration #2	00	00	00

Table 3-1. Address Map *(7 of 8)*

Block	Address (Hex)	Acronym	R/W	Description	Default Register Setting		
					Bt8370	Bt8375	Bt8376
System Bus Interface (SBI)	0D0	SBI_CR	R/W	System Bus Interface Configuration	00	00	00
	0D1	RSB_CR	R/W	Receive System Bus Configuration	00	00	00
	0D2	RSYNC_BIT	R/W	Receive System Bus Sync Bit Offset	—	—	—
	0D3	RSYNC_TS	R/W	Receive System Bus Sync Time Slot Offset	—	—	—
	0D4	TSB_CR	R/W	Transmit System Bus Configuration	00	00	00
	0D5	TSYNC_BIT	R/W	Transmit System Bus Sync Bit Offset	—	—	—
	0D6	TSYNC_TS	R/W	Transmit System Bus Sync Time Slot Offset	—	—	—
	0D7	RSIG_CR	R/W	Receive Signaling Configuration	—	—	—
	0D8	RSYNC_FRM	R/W	Signaling Reinsertion Frame Offset	—	—	—
	0D9	SSTAT	R	Slip Buffer Status	—	—	—
	0DA	STACK	R	Receive Signaling Stack	—	—	—
	0DB	RPHASE	R	RSLIP Phase Status	—	—	—
	0DC	TPHASE	R	TSLIP Phase Status	—	—	—
	0DD	PERR	R	RAM Parity Status	—	—	—
	0E0–0FF	SBCn: n = 0 to 31	R/W	System Bus Per-Channel Control	—	—	—

Table 3-1. Address Map *(8 of 8)*

Block	Address (Hex)	Acronym	R/W	Description	Default Register Setting		
					Bt8370	Bt8375	Bt8376
Buffer Memory	100–11F	TPCn: n = 0 to 31	R/W	Transmit Per-Channel Control	—	—	—
	120–13F	TSIGn: n = 0 to 31	R/W	Transmit Signaling Buffer	—	—	—
	140–15F	TSLIP_LOn: n = 0 to 31	R/W	Transmit PCM Slip Buffer	—	—	—
	160–17F	TSLIP_HIn: n = 0 to 31	R/W	Transmit PCM Slip Buffer	—	—	—
	180–19F	RPCn: n = 0 to 31	R/W	Receive Per-Channel Control	—	—	—
	1A0–1BF	RSIGn: n = 0 to 31	R/W	Receive Signaling Buffer	—	—	—
	1C0–1DF	RSLIP_LOn: n = 0 to 31	R/W	Receive PCM Slip Buffer	—	—	—
	1E0–1FF	RSLIP_HIn: n = 0 to 31	R/W	Receive PCM Slip Buffer	—	—	—

3.2 Global Control and Status Registers

Unused bits indicated by a dash (—) are reserved and should be written to 0. Writing to reserved bits has no effect.

000—Device Identification (DID)

Read only value.

7	6	5	4	3	2	1	0
DID[7]	DID[6]	DID[5]	DID[4]	DID[3]	DID[2]	DID[1]	DID[0]

DID[7:4] Device ID—A value of 0x0 indicates Bt8370.
A value of 0x5 indicates the Bt8375.
A value of 0x6 indicates the Bt8376.

DID[3:0] Device Revision—A value of 0x8 indicates the current revision. Prior revisions are obsolete.

001—Primary Control Register (CR0)

7	6	5	4	3	2	1	0
RESET	—	—	RFRAME[3]	RFRAME[2]	RFRAME[1]	RFRAME[0]	T1/E1N

RESET Device Reset—Active-high indicates a device reset is in progress. The device reset is initiated by a power-on reset, a software reset, or a hardware reset (RST* pin is active low). RESET can be monitored to determine when the reset process is complete.

To initiate a software reset, the processor must first write RESET to 0, then delay at least 6 µs, then write RESET to 1. Once initiated, the reset process continues for 15 µs maximum, and causes the Bt8370/8375/8376 to initialize certain control registers to their default settings, as shown in Table 3-1, *Address Map*. The processor must not write to these registers until RESET returns low, although other non-default registers can be processor-initialized while RESET is active.

To avoid non-compliant line rate or pulse shape transmissions during the reset process, the system can three-state the transmit line driver by holding the XOE pin inactive (low).

After the reset process, the following is true:

1. System bus outputs RSIGO, RPCMO, and SIGFRZO are three-stated.
2. Interrupt INTR* output is disabled.
3. Programmable I/O pins are configured as inputs: RFSYNC, RMSYNC, TFSYNC, TMSYNC, TNEGI/TDLCLKO, and ONESEC.
4. CONEXANT production test modes are disabled.

RFRAME[3:0] Receiver Framer mode—Establishes the offline framer's search criteria for recovery of frame alignment (reframe). Also works in conjunction with the RLOFA–RLOFD bits [addr 040] to establish the online framer's criteria for loss of frame alignment. Refer to Table A-1, *Superframe Format* through Table A-1, *Superframe Format* to find which frame bits are monitored, and refer to Table 2-3, *Criteria for Loss/Recovery of Receive Framer Alignment* for frame alignment loss/recovery criteria during the selected mode. Mode descriptions are listed in Table 3-2. The online framer's SF, SLC, CAS, and MFAS criteria for loss/recovery of multiframe alignment is also selected by RFRAME[3:0].

Table 3-2. Receive Framer Modes

RFRAME[3:0]	T1/E1N	Receive Framer Mode
000X	0	FAS Only
001X	0	FAS Only + BSLIP
010X	0	FAS + CRC
011X	0	FAS + CRC + BSLIP
100X	0	FAS + CAS
101X	0	FAS + CAS + BSLIP
110X	0	FAS + CRC + CAS
111X	0	FAS + CRC + CAS + BSLIP
0000	1	FT Only
0001	1	ESF + No CRC (FPS only)
0100	1	SF
0101	1	SF + JYEL
0110	1	SF + T1DM
1000	1	SLC + FSLOF
1001	1	SLC
1100	1	ESF + Mimic CRC
1101	1	ESF + Force CRC

T1/E1N Global T1/E1 Select—Affects all Bt8370/8375/8376 functions by enabling receive and transmit circuits to operate at either the T1 or E1 line rate. The processor must reinitialize all control register settings after changing the T1/E1N control bit. T1/E1N selects the nominal line rate (shown below), while the exact receive and transmit line rate frequencies are independently determined by their respective input clock or data references. The actual receive and transmit line frequency can vary within defined tolerances.

0 = 2.048 MHz line rate (E1)
1 = 1.544 MHz line rate (T1)

002—Jitter Attenuator Configuration (JAT_CR)

The processor writes JAT_CR register at power-up, activating the JAUTO and JCENTER bits to initialize the jitter attenuator elastic store. The processor can maximize jitter tolerance by repeating JCENTER after recovering from an error [CKERR; addr 006] on the JAT input clock reference. JAT elastic store automatically recenters upon detection of an elastic store limit error [JERR; addr 006].

7	6	5	4	3	2	1	0
JEN	JFREE	JDIR	JAUTO	JCENTER	JSIZE[2]	JSIZE[1]	JSIZE[0]

JEN Jitter Attenuator Enable—JCLK and CLADO are locked to the timing reference selected. The reference frequency can operate at T1 or E1 line rates, or at any rate supported by the clock rate adapter. See RSCALE[2:0] [addr 092] for selecting the timing reference frequency.

CEN	JEN	JFREE	JDIR	CLADO/JCLK Reference
0	0	1	X	REFCKI—Free running 10 MHz clock
0	1	1	0	REFCKI—Free running 10 MHz clock with transmit JAT
0	1	1	1	REFCKI—Free running 10 MHz clock with receive JAT
0	1	0	0	TXCLK—TCKI or ACKI per [AISCLK; addr 068]
0	1	0	1	RXCLK—RPLL or RCKI per [RDIGI; addr 020]
1	0	0	X	CLADI—System clock, bypass JAT elastic store
1	1	0	0	CLADI—System clock with transmit JAT
1	1	0	1	CLADI—System clock with receive JAT

NOTE: JCLK always operates at T1 or E1 line rate selected by [T1/E1N; addr 001].

JFREE Free-Running JCLK and CLADO—Disables both CLADI and JAT phase detectors in the clock rate adapter, which forces the Numerical Controlled Oscillator (NCO) to free-run based on the 10 MHz REFCKI input clock accuracy. When JFREE is active, JEN and JDIR select jitter attenuator direction.

0 = normal (closed loop) CLAD/JAT operation
1 = free run (open loop) NCO operation

JDIR Select JAT Direction—Applicable only when the jitter attenuator is enabled (see JEN description). JAT elastic store is placed in either the receive or transmit direction, and JCLK is placed on RCKO or TCKO pin according to JDIR selection.

0 = JAT in TX direction, JCLK output on TCKO
1 = JAT in RX direction, JCLK output on RCKO

JAUTO Enable JCLK Acceleration—When active, the jitter attenuated output clock (JCLK) phase is accelerated (added or subtracted) if the elastic store depth is within 1 Unit Interval (UI) of its limit. JCLK frequency is increased if the depth is within 1 UI of overflow, or decreased if the depth is within 1 UI of under-run. JAUTO does not affect JAT operation during other depth conditions. The amount of JCLK acceleration is proportional to the proximity of the elastic store limit, quantized in 0.125 UI steps. The JCLK phase is accelerated in 5 ns increments for each quantized step, to a total of 40 ns (maximum 0.08 UI output jitter). JAUTO expands the JAT loop bandwidth during near-limit conditions and allows JCLK to remain frequency-locked during an instantaneous reference clock switchover. Clock acceleration (±) is reported in CKERR interrupt [addr 006] and CPDERR [addr 021] status. JAUTO cannot prevent elastic store data errors [JERR; addr 006] if an invalid, out-of-frequency range clock is applied on the JAT reference input. If JCLK is programmed to free-run (JFREE), the processor must disable JAUTO. The processor can optionally disable JAUTO to prevent unnecessary clock acceleration when JCLK references CLADI, or during RLOS, RALOS, or TLOC error conditions.

0 = no acceleration
1 = enable JCLK acceleration

JCENTER Force JAT to Center (not auto clear)—Writing a 1 and then a 0 to JCENTER resets the elastic store write pointer and forces the elastic store read pointer to 1-half the programmed JSIZE. The processor writes JCENTER at power-up. Depending upon which JAT reference is selected, the processor can optionally assert JCENTER after recovery from a loss of signal (RLOS or RALOS) or in response to a transmit loss of clock (TLOC), or after recovering from a persistent clock error (CKERR).

0 = normal operation
1 = recenter JAT elastic store

JSIZE[2:0] JAT Elastic Store Size—Selects the maximum depth of JAT elastic store. The 32-bit depth is sufficient to meet jitter attenuation requirements in all cases where JAT cutoff frequency is programmed at 6 Hz and the selected clock reference is frequency-locked. However, in cases where an external reference is selected or a narrow loop bandwidth is programmed, the elastic store depth can tolerate up to ±64 Unit Intervals (128 bits) of accumulated phase offset.

JSIZE	Elastic Store Size
000	8 Bits
001	16 Bits
010	32 Bits
011	64 Bits
1xx	128 Bits

3.3 Interrupt Control Register

Unused bits indicated by a dash (—) are reserved and should be written to 0. Writing to reserved bits has no effect.

003—Interrupt Request Register (IRR)

An IRR bit is latched active (high) and the INTR* output pin is latched active (low) whenever an enabled interrupt source reports an interrupt event in the corresponding Interrupt Status register [ISR7–ISR0; addr 004–00B]. IRR and INTR* are latched until the corresponding ISR register is read by the processor. Reading ISR clears the respective IRR bit, independent of clearing ISR bits; therefore, persistently active ISR bits do not assert INTR*. All IRR bits are logically OR'ed to activate INTR*, so the processor must read IRR = 00 before exiting its interrupt service routine in order to confirm that the INTR* output has been de-asserted.

7	6	5	4	3	2	1	0
ALARM1	ALARM2	ERROR	COUNT	TIMER	DL1	DL2	PATT

ALARM1 Alarm 1 Interrupt Request—Indicates 1 or more receiver errors. The processor reads ISR7 [addr 004] to locate the specific source.
0 = no event
1 = active interrupt request

ALARM2 Alarm 2 Interrupt Request—Indicates 1-second timer expiration, or detection of 1 or more transmitter errors or inband loopback codeword. The processor reads ISR6 [addr 005] to locate the specific source.
0 = no event
1 = active interrupt request

ERROR Error Interrupt—Indicates 1 or more errors detected by the receive framer, JAT, CLAD, RSLIP, or TSLIP circuits. The processor reads ISR5 [addr 006] to locate the specific source.
0 = no event
1 = active interrupt request

COUNT Counter Overflow Interrupt—Indicates 1 or more error counts [addr 050–05A] have issued an overflow interrupt. The processor reads ISR4 [addr 007] to locate the specific source.
0 = no event
1 = active interrupt request

TIMER Timer Interrupt Request—Indicates the transmit, receive, or system bus timebase has reached a frame count terminus, or the receive signaling stack [STACK; addr 0DA] has been updated with new signaling during the prior multiframe. The processor reads ISR3 [addr 008] to locate the specific source.
0 = no event
1 = active interrupt request

DL1 Data Link Controller 1 or BOP Transmit—Indicates a transmit or receive interrupt issued by DL1 or BOP transceiver has begun transmitting a priority codeword from TBOP [addr 0A1]. The processor reads ISR2 [addr 009] to locate the specific source.
0 = no event
1 = active interrupt request

DL2 Data Link Controller 2 or BOP Receive—Indicates a transmit or receive interrupt issued by DL2 or BOP transceiver has received a valid priority codeword and updated RBOP [addr 0A2]. The processor reads ISR1 [addr 00A] to locate the specific source.

0 = no event
1 = active interrupt request

PATT PRBS Pattern or Transmit Framer Error—Indicates detection of PRBS test pattern sync, or detection of 1 or more transmit frame alignment pattern errors. The processor reads ISR0 [addr 00B] to locate the specific source.

0 = no event
1 = active interrupt request

3.4 Interrupt Status Registers

Unused bits indicated by a dash (—) are reserved and should be written to 0. Writing to reserved bits has no effect.

An Interrupt Status register (ISR) bit is latched active (high) whenever its corresponding interrupt source reports an interrupt event. The processor reads ISR to clear all latched ISR bits. If the corresponding interrupt enable is active (high), each interrupt event forces the associated IRR bit active (high) and the INTR* output pin active (low). Interrupt sources fall into two categories:

- Rising-edge source reports an interrupt event when status changes from inactive to active state. Unless specifically noted otherwise, all ISR bits are rising-edge sources.
- Dual-edge source reports an interrupt event when status changes from inactive to active (rising edge), or from active to inactive (falling edge). The processor must read the associated real-time status to determine which edge occurred.

Interrupt events are reported in real time on the INTR* output pin if the interrupt enable is active (high). Otherwise, the interrupt status is latched and reported according to the selected latching mode [LATCH; addr 046] without asserting the INTR* output pin. Table 3-3 summarizes the interrupt status registers.

Table 3-3. Interrupt Status Register Summary

Bit	004 ISR7 ALARM1	005 ISR6 ALARM2	006 ISR5 ERROR	007 ISR4 COUNT	008 ISR3 TIMER	009 ISR2 DL1	00A ISR1 DL2	00B ISR0 PATT
0	SIGFRZ	ONESEC	FERR	FERR[12]	RFRAME	TMSG	TMSG(1)	TFERR
1	RLOF	TLOF	MERR	CRC[10]	RMF	TNEAR	TNEAR(1)	TMERR
2	RLOS	—	SERR	LCV[16]	RMSYNC	TEMPTY	TEMPTY(1)	TSERR
3	RALOS	TLOC	CERR	FEBE[10]	RSIG	TDLERR	TDLERR(1)	TCERR
4	RAIS	TSHORT	JERR	BERR[12]	TFRAME	RMSG	RMSG(1)	PSYNC
5	RPDV	TPDV	CKERR	SEF[2]	TMF	RNEAR	RNEAR(1)	BSLIP
6	RYEL	LOOPUP	RSLIP	COFA[2]	TMSYNC	RFULL	RFULL(1)	—
7	RMYEL	LOOPDN	TSLIP	RLOF[4]	TSIG	TBOP	RBOP	—

NOTE(S):
(1) These bits are not active in the Bt8376 Device.

004—Alarm 1 Interrupt Status (ISR7)

All events reported in ISR7 are from dual-edge sources, except Receive Pulse Density Violation [RPDV]. Any transition of real-time status in Alarm 1 Status register [ALM1; addr 047] forces the corresponding ISR7 status bit active (high). Active-high status is latched and held according to the LATCH_ALM bit [addr 046]. Each event triggers an interrupt if the corresponding IER7 bit is enabled [addr 00C].

7	6	5	4	3	2	1	0
RMYEL	RYEL	RPDV	RAIS	RALOS	RLOS	RLOF	SIGFRZ

RMYEL Loss/Recovery of Multiframe Yellow Alarm—Reports any change in real-time status of Multiframe Yellow (E1) or ESF Yellow (T1) alarm detector.
0 = no event
1 = multiframe Yellow Alarm transition

RYEL Loss/Recovery of Yellow Alarm—Reports any change in real-time status of Remote Alarm Indication (RAI), also referred to as Yellow Alarm.
0 = no event
1 = Yellow Alarm transition

RPDV Receive Pulse Density Violation—Reports each occurrence of a receive pulse density violation, according to ANSI T1.403 sliding window criteria. RPDV is latched active upon detection of any window of 8 (N+1) bits which does not contain at least N pulses. For example, RPDV reports each occurrence of 16 consecutive 0s.
0 = no error
1 = receive pulse density violation

RAIS Loss/Recovery of Alarm Indication Signal—Reports any change in real-time status of the AIS detector.
0 = no event
1 = AIS transition

RALOS Loss/Recovery of Receive Analog Signal—Reports any change in analog receive level detector's real-time status, or receive equalizer's acquisition status (ACQUIRE; addr 021).
0 = no event
1 = receive level transition

RLOS Loss/Recovery of Receive Signal—Reports any change in real-time status of digital receive signal detector.
0 = no event
1 = receive signal transition

RLOF Loss/Recovery of Frame Alignment—Reports any change in real-time or integrated status of receive online frame status monitor.
0 = no event
1 = receive frame status transition

SIGFRZ Loss/Recovery of Signaling Freeze—Reports any change in real-time status of SIGFRZ receiver status, which is also available on the SIGFRZ output pin.
0 = no event
1 = SIGFRZ transition

005—Alarm 2 Interrupt Status (ISR6)

All events reported in ISR6 are from dual-edge sources, except the 1-second timer [ONESEC] and Transmit Pulse Density Violation [TPDV]. Any transition of real-time status in the Alarm 2 Status register [ALM2; addr 048] forces the corresponding ISR6 status bit active (high). Active-high status is latched and held according to the LATCH_ALM bit [addr 046]. Each event triggers an interrupt if the corresponding IER6 bit is enabled [addr 00D].

7	6	5	4	3	2	1	0
LOOPDN	LOOPUP	TPDV	TSHORT	TLOC	—	TLOF	ONESEC

LOOPDN Loss/Recovery of Inband Loopback Deactivate Code—Reports any change in real-time status of inband loopback deactivate code detector.
0 = no event
1 = LOOPDN code transition

LOOPUP Loss/Recovery of Inband Loopback Activate Code—Reports any change in real-time status of inband loopback activate code detector.
0 = no event
1 = LOOPUP code transition

TPDV Transmit PDV Monitor/Enforcer—Applicable only if TZCS [addr 071] enables PDV enforcement. When enabled, TPDV is latched active if 1 or more PDV-enforced 1s were output to meet ANSI T1.403 minimum pulse density requirements.
0 = no error
1 = PDV-enforced 1

TSHORT Loss/Recovery of Transmit Short Circuit—Reports any change in real-time status of transmit line driver's short circuit detector.
0 = no alarm
1 = short circuit transition

TLOC Loss/Recovery of Transmit Clock—Reports any change in real-time status of TCKI clock monitor.
0 = no alarm
1 = clock monitor transition

TLOF Loss/Recovery of Transmit Frame Alignment—Reports any change in real-time status of transmit framer's basic alignment.
0 = no alarm
1 = transmit framer transition

ONESEC 1-second Timer Event—ONESEC is derived from the internal 1-second timer or the rising edge of ONESEC input signal, according to the selected I/O mode [PIO; addr 018].
0 = no timer event
1 = ONESEC timer expired or rising edge of ONESEC input

006—Error Interrupt Status (ISR5)

All events in ISR5 are from rising edge sources. Each event is latched active-high and held according to the LATCH_ERR bit [addr 046] and triggers an interrupt if the corresponding IER5 bit is enabled [addr 00E].

7	6	5	4	3	2	1	0
TSLIP	RSLIP	CKERR	JERR	CERR	SERR	MERR	FERR

TSLIP Transmit Slip Error—Two types of TSLIP buffer errors are reported, TFSLIP or TUSLIP. The error type is reported separately in slip status [SSTAT; 0D9].
0 = no error
1 = TSLIP error

RSLIP Receive Slip Error—Two types of RSLIP buffer errors are reported, RFSLIP or RUSLIP. The error type is reported separately in slip status [SSTAT; 0D9].
0 = no error
1 = RSLIP error

CKERR CLAD Phase Detector or JCLK Acceleration Error—Reports JCLK acceleration/deceleration (enabled by JAUTO bit; addr 002).

CKERR	JAUTO	JCLK Acceleration
X	0	CKERR disabled
0	1	No error
1	1	JCLK acceleration active

JERR Jitter Attenuator Elastic Store Limit Error—Indicates the transmit (TJAT) or receive (RJAT) jitter attenuator elastic store has under-run or overflowed its programmed depth [JSIZE; addr 002]. Error type is reported separately in JMPTY [addr 021]. JAT elastic store is automatically re-centered each time JERR occurs, causing an uncontrolled data slip on the elastic store output.
0 = no error
1 = uncontrolled JAT data slip

CERR CRC6/CRC4 Block Error—Applicable to ESF and MFAS modes only; read 0 in other modes. CERR indicates 1 or more bit errors found in the received CRC-6 or CRC-4 checksum block pattern.
0 = no error
1 = CRC error

SERR CAS Pattern Error—Applicable only in E1 mode; read 0 in T1 mode. SERR indicates 1 or more bit errors found in received TS16 Multiframe Alignment Signal (MAS).
0 = no error
1 = CAS error

MERR MFAS Pattern Error—Applicable only in E1 mode; read 0 in T1 mode. Indicates 1 or more bit errors found in received MFAS alignment pattern.
0 = no error
1 = MFAS error

FERR Frame Error—Ft/Fs/T1DM/FPS/FAS Pattern Error. Indicates 1 or more Ft/Fs/FPS frame bit errors or FAS pattern errors found. Refer to Table A-1 through A-7 for a description of which frame bits are monitored according to the selected receive framer mode.
0 = no error
1 = frame error

007—Counter Overflow Interrupt Status (ISR4)

All count overflow events in ISR4 are caused by rising edge sources. Each event is latched active-high when the respective error counter [addr 050–05A] reaches its maximum count value, but only while the respective IER4 [addr 00F] interrupt enable bit is active. If the corresponding interrupt is masked, no overflow status is reported. Active overflow status bits are held until the processor read clears ISR4. Each event triggers an interrupt if the corresponding IER4 bit is enabled.

7	6	5	4	3	2	1	0
FRED[4]	COFA[2]	SEF[2]	BERR[12]	FEBE[10]	LCV[16]	CRC[10]	FERR[12]

FRED[4] Out of Frame Error Count Overflow

COFA[2] Change of Alignment Count Overflow

SEF[2] Severely Errored Frame Count Overflow

BERR[12] Test Pattern Bit Error Count Overflow

FEBE[10] FEBE Error Count Overflow

LCV[16] LCV (BPV+EXZ) Error Count Overflow

CRC[10] CRC6/CRC4 Error Count Overflow

FERR[12] Ft/Fs/FPS/FAS Error Count Overflow

008—Timer Interrupt Status (ISR3)

All events in ISR3 are caused by rising edge sources. Each event is latched active-high and held until the processor read clears ISR3. Each event triggers an interrupt if corresponding IER3 bit is enabled [addr 010].

7	6	5	4	3	2	1	0
TSIG	TMSYNC	TMF	TFRAME	RSIG	RMSYNC	RMF	RFRAME

TSIG Transmit Signaling Multiframe—Activated every 1.5 ms (SF/SLC), 3 ms (ESF), or 2 ms (CAS), coincident with the first bit of a transmit signaling multiframe.
0 = no timer event
1 = transmit signaling multiframe

TMSYNC TX System Bus MF Sync—Activated every 1.5 ms (SF/SLC), 3 ms (ESF), or 2 ms (CAS), coincident with the first bit of transmit system bus multiframe input on TPCMI.
0 = no timer event
1 = TSB multiframe

TMF Transmit Multiframe—TMF is activated every 1.5 ms (SF/SLC), 3 ms (ESF, Ft), or 2 ms (MFAS), coincident with the first bit of a transmit multiframe.
0 = no timer event
1 = transmit multiframe

TFRAME Transmit Frame—Activated every 193 bits (T1) or 256 bits (E1), coincident with first bit of a transmit frame. The processor can read TPHASE [addr ODC] to determine which TSLIP buffer half can be accessed.
0 = no timer event
1 = transmit frame

RSIG Receive Signaling Stack—Indicates 1 or more signaling bit changes were detected during the prior receive multiframe, and new ABCD (robbed bit or CAS) signaling is available on the Receive Signaling Stack register [addr 0DA]. RSIG is cleared by processor read of ISR3, independent of STACK contents. See also the SET_RSIG bit (addr 0D7).

0 = no stack update
1 = new ABCD signaling

RMSYNC Receive System Bus MF Sync—Activated every 1.5 ms (SF/SLC), 3 ms (ESF), or 2 ms (CAS), coincident with the first bit of receive system bus multiframe output on RPCMO.

0 = no timer event
1 = RSB multiframe

RMF Receive Multiframe Boundary—Activated every 3 ms for T1 (Ft, SF, SLC, ESF), or 2 ms (MFAS), coincident with the first bit of a received multiframe. If MFAS is not included in the receive framer criteria, RMF is activated at 2 ms interval.

0 = no timer event
1 = receive multiframe

RFRAME Receive Frame Boundary—Activated every 193 bits (T1) or 256 bits (E1), coincident with the first bit of a received frame. The processor can read RPHASE [addr 0DB] to determine which RSLIP buffer half can be accessed.

0 = no timer event
1 = receive frame

009—Data Link 1 Interrupt Status (ISR2)

All events in ISR2 are from rising edge sources. Each event is latched active-high and held until the processor read clears ISR2. Each event triggers an interrupt if the corresponding IER2 bit is enabled [addr 011].

7	6	5	4	3	2	1	0
TBOP	RFULL1	RNEAR1	RMSG1	TDLERR1	TEMPTY1	TNEAR1	TMSG1

TBOP BOP Codeword Transmitted—Set when a valid Bit Oriented Codeword has been transmitted and a new TBOP value can be written [TBOP; addr 0A1].

RFULL1 Receive FIFO Full—In HDLC modes, RFULL is set when the data link receiver attempts to write received data to a full FIFO causing the receive data link FIFO to overrun. In unformatted modes (Pack6 and Pack8), RFULL is set when the receive FIFO is filled to the MSG_FILL Limit selected in register RDL1_FFC [addr 0A7].

RNEAR1 Receive FIFO Near Full—Set when the receive FIFO fill level reaches the near full threshold selected in register RDL1_FFC [addr 0A7].

RMSG1 Message Received—Set when a complete message or a partial message is received and available in the receiver FIFO.

TDLERR1 Transmit FIFO Error—Set when the FIFO underruns as a result of the internal logic emptying the FIFO without encountering an end of message [TDL1_EOM; addr 0AC]. The underrun condition also forces transmission of an HDLC abort code.

TEMPTY1 Transmit FIFO Empty—Set when the FIFO overflows as a result of the processor attempting to write to a full FIFO. Overflow data is ignored by the transmit FIFO.

TNEAR1 Transmit FIFO Near Empty —Set when the transmit FIFO level falls below the threshold selected in register TDL1_FEC [addr 0AB].

TMSG1 Message Transmitted—Set when a complete message has been transmitted and the closing flag is just beginning transmission.

00A—Data Link 2 Interrupt Status (ISR1)

All events in ISR1 are from rising edge sources. Each event is latched active-high and held until the processor read clears ISR1. Each event triggers an interrupt if the corresponding IER1 bit is enabled [addr 012].

For Bt8370 and Bt8375

7	6	5	4	3	2	1	0
RBOP	RFULL2	RNEAR2	RMSG2	TDLERR2	TEMPTY2	TNEAR2	TMSG2

For Bt8376

7	6	5	4	3	2	1	0
RBOP	—	—	—	—	—	—	—

RBOP BOP Codeword Received—Set when a valid Bit Oriented Codeword is received and available in the RBOP register [addr 0A2].

RFULL2 Receive FIFO Full—In HDLC modes, RFULL is set when the data link receiver attempts to write received data to a full FIFO causing the receive data link FIFO to overrun. In unformatted modes (Pack6 and Pack8), RFULL is set when the receive FIFO is filled to the MSG_FILL limit selected in register RDL2_FFC [addr 0B2].

RNEAR2 Receive FIFO Near Full—Set when the receive FIFO fill level reaches the near full threshold selected in register RDL2_FFC [addr 0B2].

RMSG2 Message Received—Set when a complete message or a partial message is received and available in the receiver FIFO.

TDLERR2 Transmit FIFO Error—Set when the FIFO underruns as a result of the internal logic emptying the FIFO without encountering an end of message [TDL2_EOM; addr 0B7]. The underrun condition also forces transmission of an HDLC abort code.

TEMPTY2 Transmit FIFO Empty—Set when the FIFO overflows as a result of the processor attempting to write to a full FIFO. Overflow data is ignored by the transmit FIFO.

TNEAR2 Transmit FIFO Near Empty—Set when the transmit FIFO level falls below the threshold selected in register TDL2_FEC [addr 0B6].

TMSG2 Message Transmitted—Set when a complete message has been transmitted and the closing flag is just beginning transmission.

00B—Pattern Interrupt Status (ISR0)

All events in ISR0 are caused by rising edge sources. Each event is latched active-high and held until the processor read clears ISR0. Each event triggers an interrupt if the corresponding IER0 bit is enabled [addr 013].

7	6	5	4	3	2	1	0
—	—	BSLIP	PSYNC	TCERR	TSERR	TMERR	TFERR

BSLIP Online Framer Bit Slip—Active-high. Indicates that receive online framer adjusted receive frame sync by ±1 bit. When BSLIP occurs, the apparent FAS error is not reported elsewhere (not to FERR count, RLOF circuit, or SEF circuit). Applicable only to receive framer modes with BSLIP enabled (see Table 3-2, *Receive Framer Modes*).

0 = no error
1 = frame bit slip

PSYNC Receive PRBS Test Pattern Sync—Forced to inactive (low) status when the processor requests RESEED [addr 041] of the PRBS sync detector, and remains low while detector searches for test pattern sync. PRBS bit errors [BERR; addr 058, 059] are not counted while PSYNC is low. PSYNC remains low for a minimum of 128 bits following RESEED, and for as long as the received bit error ratio (BER) exceeds 1E-2. PSYNC is latched active (high) and the PRBS sync detector stops searching when no bit errors are found for a period of 96 bits. The sync detector remains disabled until the processor requests another RESEED. Therefore, any range of BER can be measured after initial pattern sync. The processor must determine criteria for loss of pattern sync based on its accumulation of bit errors over the desired time interval.

0 = no sync
1 = PRBS test pattern sync

TCERR Transmit CRC Error—Reports occurrences of CRC-6 or CRC-4 errors detected on TPCMI data according to the selected T1/E1 mode.

0 = no error
1 = CRC error

TSERR Transmit CAS Error—Reports occurrences of MAS pattern errors detected on TPCMI data if CAS transmit framer mode is selected.

0 = no error
1 = CAS error

TMERR Transmit Multiframe Error—Reports occurrences of Fs or MFAS errors detected on TPCMI data according to the selected transmit framer mode.

0 = no error
1 = transmit multiframe error

TFERR Transmit Frame Error—Reports occurrences of Ft, FPS, or FAS errors detected on TPCMI data according to the selected transmit framer mode.

3.5 Interrupt Enable Registers

Unused bits indicated by a dash (—) are reserved and should be written to 0. Writing to reserved bits has no effect.

Writing a 1 to an IER bit allows that specific interrupt source to activate its respective ISR bit, the associated IRR bit, and the INTR* output. When cleared, each IER bit allows that source to activate its respective ISR bit, but prevents activation of the INTR* output and the associated IRR bit.

00C—Alarm 1 Interrupt Enable Register (IER7)

7	6	5	4	3	2	1	0
RMYEL	RYEL	RPDV	RAIS	RALOS	RLOS	RLOF	SIGFRZ

RMYEL Enable RMYEL Interrupt

RYEL Enable RYEL Interrupt

RPDV Enable RPDV Interrupt

RAIS Enable RAIS Interrupt

RALOS Enable RALOS or RLOC Interrupt

RLOS Enable RLOS Interrupt

RLOF Enable RLOF Interrupt

SIGFRZ Enable SIGFRZ Interrupt

00D—Alarm 2 Interrupt Enable Register (IER6)

7	6	5	4	3	2	1	0
LOOPDN	LOOPUP	TPDV	TSHORT	TLOC	—	TLOF	ONESEC

LOOPDN Enable LOOPDN Interrupt

LOOPUP Enable LOOPUP Interrupt

TPDV Enable TPDV Interrupt

TSHORT Enable TSHORT Interrupt

TLOC Enable TLOC Interrupt

TLOF Enable TLOF Interrupt

ONESEC Enable ONESEC Interrupt

00E—Error Interrupt Enable Register (IER5)

7	6	5	4	3	2	1	0
TSLIP	RSLIP	CKERR	JERR	CERR	SERR	MERR	FERR

TSLIP Enable TSLIP Interrupt

RSLIP Enable RSLIP Interrupt

CKERR Enable CKERR Interrupt

JERR Enable JERR Interrupt

CERR Enable CERR Interrupt

SERR Enable SERR Interrupt

MERR Enable MERR Interrupt

FERR Enable FERR Interrupt

00F—Count Overflow Interrupt Enable Register (IER4)

7	6	5	4	3	2	1	0
LOF	COFA	SEF	BERR	FEBE	LCV	CRC	FERR

LOF Enable LOF Count Overflow Interrupt

COFA Enable COFA Count Overflow Interrupt

SEF Enable SEF Count Overflow Interrupt

BERR Enable BERR Count Overflow Interrupt

FEBE Enable FEBE Count Overflow Interrupt

LCV Enable LCV Count Overflow Interrupt

CRC Enable CRC Count Overflow Interrupt

FERR Enable FERR Count Overflow Interrupt

Table 3-4. Counter Overflow Behavior

IER4	LATCH_CNT	Count (addr 050–05A)			INTR*
Addr 00F	Addr 046	Saturate	Latch	Clear	Active
0	0	Hold all 1s	hi @rd_LSB	hi @rd_MSB	None
1	0	Rollover	hi @rd_LSB	hi @rd_MSB	@rollover
0	1	Hold all 1s	onesec	None	None
1	1	Rollover	onesec	none	@rollover

010—Timer Interrupt Enable Register (IER3)

7	6	5	4	3	2	1	0
TSIG	TMSYNC	TMF	TFRAME	RSIG	RMSYNC	RMF	RFRAME

TSIG Enable TSIG Interrupt

TMSYNC Enable TMSYNC Interrupt

TMF Enable TMF Interrupt

TFRAME Enable TFRAME Interrupt

RSIG Enable RSIG Interrupt

RMSYNC Enable RMSYNC Interrupt

RMF Enable RMF Interrupt

RFRAME Enable RFRAME Interrupt

011—Data Link 1 Interrupt Enable Register (IER2)

7	6	5	4	3	2	1	0
TBOP	RFULL1	RNEAR1	RMSG1	TDLERR1	TEMPTY1	TNEAR1	TMSG1

TBOP Enable TBOP Interrupt

RFULL1 Enable RFULL Interrupt

RNEAR1 Enable RNEAR Interrupt

RMSG1 Enable RMSG Interrupt

TDLERR1 Enable TDLERR Interrupt

TEMPTY1 Enable TEMPTY Interrupt

TNEAR1 Enable TNEAR Interrupt

TMSG1 Enable TMSG Interrupt

012—Data Link 2 Interrupt Enable Register (IER1)

7	6	5	4	3	2	1	0
RBOP	RFULL2	RNEAR2	RMSG2	TDLERR2	TEMPTY2	TNEAR2	TMSG2

7	6	5	4	3	2	1	0
RBOP	—	—	—	—	—	—	—

RBOP Enable RBOP Interrupt

RFULL2 Enable RFULL Interrupt

RNEAR2 Enable RNEAR Interrupt

RMSG2 Enable RMSG Interrupt

TDLERR2 Enable TDLERR Interrupt

TEMPTY2 Enable TEMPTY Interrupt

TNEAR2 Enable TNEAR Interrupt

TMSG2 Enable TMSG Interrupt

013—Pattern Interrupt Enable Register (IER0)

7	6	5	4	3	2	1	0
—	—	BSLIP	PSYNC	TCERR	TSERR	TMERR	TFERR

BSLIP Enable BSLIP Interrupt

PSYNC Enable PSYNC Interrupt

TCERR Enable TCERR Interrupt

TSERR Enable TSERR Interrupt

TMERR Enable TMERR Interrupt

TFERR Enable TFERR Interrupt

3.6 Primary Control and Status Registers

Unused bits indicated by a dash (—) are reserved and should be written to 0. Writing to reserved bits has no effect.

014—Loopback Configuration Register (LOOP)

7	6	5	4	3	2	1	0
—	—	—	—	PLOOP	LLOOP	FLOOP	ALOOP

PLOOP Enable Remote Payload Loopback—Payload from the receiver replaces the payload on transmitter output. The loopback payload retains the time slot and frame integrity, so numbered time slots from each receive frame transfer to same numbered time slots in the transmit frame. Transmit overhead bits—F-bits in T1 mode or TS0 in E1 mode—are supplied by the transmit frame formatter or the transmit system bus, according to TFRM [addr 072] settings. Existing transmit frame alignment and clock timing is not altered by PLOOP activation or deactivation, allowing system operation with independent receive and transmit timing. Controlled frame slips are performed in the payload loopback path if the receive and transmit clocks are asynchronous, although these slips are not reported to the processor as slip buffer errors. Multiframe integrity is not maintained during PLOOP; therefore, DS0 channel loopbacks [TPCn; addr 100–11F] must be used to implement payload loopbacks when transparent or forced signaling is desired. PLOOP does not override by the transmit per-channel selections (TPCn).

0 = no loopback
1 = payload loopback

LLOOP Enable Remote Line Loopback—Dual-rail unipolar data from RLIU (or RJAT) is internally connected to TLIU. The recovered clock from RPLL (or JCLK from RJAT) is internally connected to the transmitter. Loopback data retains BPV transparency. Data input from the transmit system bus continues to pass through the transmitter, but is ignored at ZCS encoder outputs. Data passage from RLIU block to RSB block is unaffected. LLOOP and FLOOP can be simultaneously active to support line and network loopbacks simultaneously.

0 = no loopback
1 = line loopback

FLOOP Enable Local Framer Loopback—Dual-rail unipolar data from the transmit ZCS encoder is internally connected to receive ZCS decoder inputs. The signals from the transmit clock input (TCKI) is internally connected to the receive clock output (RCKO). Externally applied data on RTIP/RRING inputs is ignored. XTIP/XRING output data is unaffected. If RCKO is selected as the TCKI clock source [CMUX; addr 01A], an alternate transmit clock source must be provided when this loopback is activated. Possible configurations include selecting the TCKI pin or CLADO as the transmit clock source, or programming the JAT in the transmit direction and setting JFREE to enable the free-running 10 MHz reference [JAT_CR register; addr 002].

0 = no loopback
1 = framer loopback

ALOOP Enable Local Analog Loopback—Bipolar data from XTIP/XRING is internally connected to RTIP/RRING inputs. Externally applied data on RTIP/RRING inputs is ignored. XTIP/XRING output data is unaffected. After ALOOP activation or deactivation, the processor must reset the receive line interface [RST_LIU; addr 020]. If RCKO is selected as the TCKI clock source [CMUX; addr 01A], an alternate transmit clock source must be provided when this loopback is activated. Possible configurations include selecting the TCKI pin or CLADO as the transmit clock source, or programming the JAT in the transmit direction and setting JFREE to enable the free-running 10 MHz reference [JAT_CR register; addr 002].

0 = no loopback
1 = analog loopback

015—External Data Link Time Slot (DL3_TS)

DL3_TS works in conjunction with the DL3_BIT register [addr 016] to determine which transmit time slots are supplied from the TDLI pin, and which receive and transmit time slots are accompanied by a gated RDLCKO and TDLCKO output. (Refer to Figure 2-29, *Transmit External Data Link Waveforms*, Transmit External Data Link Waveforms). RDLO outputs the entire receive data bit stream, and only selective digits are marked by RDLCKO.

7	6	5	4	3	2	1	0
DL3EN	FS[1]	FS[0]	TS[4]	TS[3]	TS[2]	TS[1]	TS[0]

DL3EN Enable External Data Link—Active-high enables data insertion from TDLI and enables clock gating on TDLCKO and RDLCKO outputs according to the selected external data link mode.

NOTE: PIO [addr 018] must select TDL_IO and/or RDL_IO to enable external data link signals. Bits 5 and 6 must be written to 1s for the External Data Link to operate correctly.

0 = external data link pins inactive
1 = TDLI/TDLCKO and RDLO/RDLCKO active

FS[1:0] External Data Link Frame Select—The External data link can be programmed to source and sink data bits during all frames, odd frames, or even frames. FS[1:0] controls gating of RDLCKO and TDLCKO external data link clocks.

FS[1:0]	Frame Select (T1 Mode)
00	None. Equivalent to disabling external data link.
01	Odd frames only: Frames 1, 3, 5, etc.
10	Even frames only: Frames 2, 4, 6, etc.
11	All frames.

FS[1:0]	Frame Select (E1 Mode)
00	None. Equivalent to disabling external data link.
01	Even frames only: Frames 0, 2, 4, 6, etc.
10	Odd frames only: Frames 1, 3, 5, etc.
11	All frames.

TS[4:0] External Data LinkTime Slot Select—Picks 1 8-bit time slot for input and output over the external data link pins. Any time slot can be chosen from TS0 to TS31 in E1 mode or TS1 to TS24 in T1 mode. In T1 mode, TS25 selects F-bits instead of a channel time slot.

00000	Time slot 0
00001	Time slot 1
|	|
11110	Time slot 30
11111	Time slot 31

016—External Data Link Bit (DL3_BIT)

7	6	5	4	3	2	1	0
DL3_BIT[7]	DL3_BIT[6]	DL3_BIT[5]	DL3_BIT[4]	DL3_BIT[3]	DL3_BIT[2]	DL3_BIT[1]	DL3_BIT[0]

DL3_BIT[7:0] External Data Link Bit Select—Enables receive (RDLCKO) and transmit (TDLCKO) clock pulse outputs during selected time slot bits. DL3_BIT works in conjunction with the DL3_TS register [addr 015] to select any combination of bits for input and output on the external data link pins by writing the corresponding DL3_BIT active (high). LSB enables clock pulses coincident with the first bit transmitted or received. The full T1/E1 data stream is output on RDLO as long as the RDL_IO bit [addr 018] is active, regardless of which bits are accompanied by RDLCKO clock pulses. The selected transmit data link bits are sampled from the TDLI pin on the falling edge of TDLCKO to replace normal transmitted data. DL3_BIT must be set to 0x01 when DL3_TS selects T1 F-bits.

0 = disable DL3 bit
1 = enable DL3 bit

017—Offline Framer Status (FSTAT)

Bt8370/8375/8376 contains a single offline framer that serves as a shared resource for both receive and transmit channels. Because current alignment status for receive and transmit channels is reported separately in Alarm Status registers (ALM1, ALM2; addr 047, 048), FSTAT is used primarily for diagnostic purposes to monitor the progress of an alignment search, or to verify acknowledgment of a processor-generated forced reframe request. These status bits can only be reported for a very short period of time (i.e., 1 clock cycle), because the RLOF and TLOF reframe requests can immediately request another offline framer search.

7	6	5	4	3	2	1	0
—	—	—	INVALID	FOUND	TIMEOUT	ACTIVE	RX/TXN

INVALID No Candidate—Active-high at the conclusion of a search during which no frame alignment candidates were located.

0 = search active, aborted, timed out, or found
1 = alignment not found (no candidate).

FOUND Frame Search Successful—Active-high indicates the offline framer located the frame alignment according to the selected receive or transmit framer mode. Refer to Table 3-5 for maximum average reframe time.

Upon detection of frame alignment, the following occurs:

- FOUND goes active-high
- RLOF or TLOF is cleared by the online framer, depending on RX/TX direction
- the offline framer goes inactive, if no pending reframe requests exist
- the RX, TX, or TSB timebase is realigned, depending on the RX/TX direction and the embedded framing mode.

If the reframe pulse causes the receive timebase to align to a position that differs from its existing alignment, the change of frame alignment error counter [COFA; addr 05A] increments. Changes of the transmit frame alignment are not detected.

NOTE: In E1 receive framer modes, the offline framer also reports intermediate FRED, MRED, and SRED status [ALM3; addr 049] while searching for FAS, MFAS, and CAS alignment, respectively.

0 = no candidate; search active, aborted, or timed out
1 = frame alignment found (1 and only 1 candidate)

Table 3-5. Maximum Average Reframe Time (MART) and Framer Timeout

Framer Mode	MART	TIMEOUT (addr 017)
Ft	3.5 ms	12 ms ±1 bit
Ft + T1DM	1.0 ms	12 ms ±1 bit
SF	3.5 ms	12 ms ±1 bit
SF + JYEL	4.5 ms	12 ms ±1 bit
SF + TIDM	2.0 ms	12 ms ±1 bit
SLC	15.0 ms	24 ms ±1 bit
ESF	10.0 ms	24 ms ±1 bit
ESF + CRC	15.0 ms	24 ms ±1 bit
ESF + MIMIC	15.0 ms	24 ms ±1 bit
FAS	0.5 ms	8 ms ±125 µs
CAS	2.0 ms	8 ms ±125 µs
MFAS	10.0 ms	8 ms ±125 µs

NOTE(S): MART is defined (per Bellcore TA-0278) as the difference between the time that known good pseudo-random DS1 input is applied, and the time that a valid DS0 signal is observed at the output.

TIMEOUT Framer Search Timeout—Cleared when the offline framer transitions to its ACTIVE state. If multiple frame candidates exist over the entire mode-dependent timeout interval (refer to Table 3-5), TIMEOUT is latched active-high. Processor-generated reframe requests (RFORCE or TFORCE) initiate a single search that extends to a maximum of 24 ms before TIMEOUT. After reporting TIMEOUT, the offline framer begins another search if the reframe request (RLOF or TLOF) is active.

0 = no candidate; search active, aborted, or found
1 = framer search timeout (multiple candidates)

ACTIVE Framer Active—Offline framer transitions to its ACTIVE state in response to an RFORCE or TFORCE reframe request from the processor, or in response to an RLOF or TLOF reframe request from the online framer.

The offline framer remains ACTIVE until any of the following occurs:

- alignment is found (FOUND)
- the search is aborted [see RABORT; addr 040, or TABORT; addr 071]
- the search reaches its timeout interval (TIMEOUT)
- all possible frame candidates are eliminated (INVALID)

NOTE: RFORCE or TFORCE does not change the current RLOF or TLOF status. RFORCE or TFORCE is cleared by the framer transition to ACTIVE.

0 = offline framer inactive; search completed, aborted or timed out
1 = offline framer actively searching for alignment.

RX/TXN RX/TX Reframe Operation—Indicates which direction the offline framer is actively searching or most recently searched for frame alignment. RX/TXN status is updated when the offline framer transitions to its ACTIVE state in response to a reframe request.

0 = search data from Transmit System Bus PCM Input (TPCMI)
1 = search data from receive line interface unit.

018—Programmable Input/Output (PIO)

7	6	5	4	3	2	1	0
ONESEC_IO	RDL_IO	TDL_IO	INDY_IO	RFSYNC_IO	RMSYNC_IO	TFSYNC_IO	TMSYNC_IO

ONESEC_IO Bidirectional ONESEC Input/Output mode—Selects input or output mode for ONESEC signal pin, and controls the internal timer interval used for 1-second status latching [LATCH; addr 046]. When ONESEC is an output, the JAT reference clock [JCLK; addr 002] develops the 1-second timer interval output, with an arbitrarily defined initial starting location. When ONESEC is an input, the timer/latch interval is aligned to the rising edge of ONESEC input. The system can apply ONESEC input to define any length timer/latch interval up to but not greater than 1-second.

0 = ONESEC input
1 = ONESEC output

RDL_IO Enable Receive Data Link—Selects which signals are present on bi-modal RNEGO/RDLCKO and RPOSO/RDLO pins. When active, receive data link pins RDLCKO and RDLO are enabled [see also DL3EN; addr 015]; otherwise, dual-rail RLIU data is output on RNEGO and RPOSO pins.

0 = RNEGO and RPOSO
1 = RDLCKO and RDLO

TDL_IO Enable Transmit Data Link—Selects which signals are present on bi-modal TNEGI/TDLCKO and TPOSI/TDLI pins. When active, transmit data link pins TDLCKO and TDLI are enabled [see also DL3EN; addr 015]; otherwise, TLIU data is supplied by the dual-rail TNEGI and TPOSI inputs.

0 = TNEGI and TPOSI signals
1 = TDLCKO and TDLI signals

NOTE: TDL_IO must be programmed to 1 to enable data output from the transmit frame formatter.

INDY_IO Enable Time Slot Indicators—Selects which signals are present on bi-modal TNEGO/RINDO and TPOSO/TINDO pins. When active, system bus time slot indicators RINDO and TINDO are enabled (see also [SBCn; addr 0E0–0FF]); otherwise, dual-rail TLIU data is output on TNEGO and TPOSO pins.

0 = TNEGO and TPOSO
1 = RINDO and TINDO

RFSYNC_IO Bidirectional RFSYNC Input/Output mode—Refer to system bus sync mode summary in Tables 3-6 and 3-8. When RFSYNC is an input, its low-to-high transition aligns the RSB timebase to the programmed RSB.OFFSET. Refer to RSYNC_BIT, RSYNC_TS and RSYNC_FRM offset registers [addr 0D2, 0D3, and 0D8] for a complete description of the RSB sync bit, time slot, and frame offset. Once aligned, the RSB timebase internally flywheels at 125 µs interval (8 kHz) until a new RFSYNC pulse is applied. When RFSYNC is programmed as an output, it operates continuously at 8 kHz frame rate, marking RSB sync bits and time slot offset position of each frame. Initial RFSYNC alignment and subsequent realignment depends RSB mode [RSBI; addr 0D1] and RSB manual center [RSB_CTR; addr 0D1]. RFSYNC must be programmed as an output when RSLIP is in Bypass mode or Elastic mode. RFSYNC and RMSYNC are supplied either by RSB timebase (output) or receive system bus (input) at a programmable RSB sync bit offset, time slot location, and frame offset location.

0 = RFSYNC input
1 = RFSYNC output

RMSYNC_IO Bidirectional RMSYNC Input/Output mode—Refer to system bus sync mode summary in Tables 3-6 and 3-8. When RMSYNC is an input, its low-to-high transition aligns RSB timebase to the programmed RSB.OFFSET. Once aligned, RSB timebase internally flywheels at 3 ms (T1) or at 2 ms (E1) intervals until a new RMSYNC pulse is applied.

When RMSYNC is an output, it operates continuously at a 6 ms rate (every second multiframe for T1 or every third for E1), marking the RSB.OFFSET position. Initial RMSYNC alignment and subsequent realignment depends on RSB mode [RSBI; addr 0D1] and RSB manual center [RSB_CTR; addr 0D1]. RMSYNC must be programmed as an output when RSLIP is in Bypass mode or Elastic mode. THRU bit must be set [THRU; addr 0D7] when RMSYNC is programmed as an output. RMSYNC input signal must always coincide with RFSYNC.

0 = RMSYNC input
1 = RMSYNC output

TFSYNC_IO Bidirectional TFSYNC Input/Output mode—TFSYNC_IO programming depends on transmit framer and system bus modes, as shown in Tables 3-6 and 3-7.

0 = TFSYNC input
1 = TFSYNC output

TMSYNC_IO Bidirectional TMSYNC Input/Output mode—TMSYNC_IO programming depends on transmit framer and system bus modes, as shown in Tables 3-6 and 3-7.

0 = TMSYNC input
1 = TMSYNC output

Table 3-6. System Bus Sync Mode Summary

FSYNC	MSYNC	SBI Alignment Mode
IN	IN	SBI supplies multiframe and 8 kHz frame alignment. FSYNC must be aligned with MSYNC if both are provided.
IN	IN-GND	SBI supplies 8 kHz frame alignment. Multiframe alignment is arbitrary and MSYNC is unused.
IN	OUT	SBI supplies 8 kHz frame alignment. Multiframe alignment is supplied by the framer.
IN-GND	OUT	Framer supplies multiframe alignment. FSYNC is unused.
OUT	IN	SBI supplies multiframe and frame alignment.
OUT	OUT	Framer supplies frame and multiframe alignment.

Table 3-7. Common TFSYNC and TMSYNC Configurations

Conditions	TFSYNC	TMSYNC	Explanation
Transmit framer disabled. (TABORT = 1)	IN	IN	TSB timebase slaved to system bus TFSYNC or TMSYNC.
	IN-GND	IN	TSB timebase slaved to system bus TMSYNC. TFSYNC is unused.
	IN	IN-GND	TSB timebase slaved to system bus TFSYNC. TMSYNC is unused and multiframe alignment is arbitrary.
	IN	OUT	SB timebase slaved to system bus TFSYNC. TMSYNC alignment is arbitrary.
	OUT	OUT	TSB timebase alignment is arbitrary.
	OUT	IN	TSB timebase slaved to system bus TMSYNC. TFSYNC aligns to TMSYNC input.
Transmit framer enabled to search TPCMI for embedded framing. (EMBED = 0, TABORT = 0)	OUT	OUT	TSB timebase is aligned to embedded framing on TPCMI. TPCMI must be configured to line rate for this case.
Transmit framer enabled to search TNRZ (after TSLIP buffer) for embedded framing. (EMBED = 1, TABORT = 0)	OUT	IN-GND	TSB timebase is aligned to embedded framing on TNRZ data. TMSYNC is unused. TPCMI may be configured for 1,544 kbps or a multiple of 2,048 kbps.

Table 3-8. Common RFSYNC and RMSYNC Configurations

Conditions	RFSYNC	RMSYNC	Explanation
THRU = 0 [RSIG_CR; addr 0D7]	IN	IN	RSB timebase slaved to system bus RFSYNC or RMSYNC.
	IN	OUT	RSB timebase slaved to system bus RFSYNC. RMSYNC alignment is arbitrary.
	OUT	IN	RSB timebase slaved to system bus RMSYNC. RFSYNC aligns to TMSYNC input.
	OUT	OUT	RFSYNC and RMSYNC alignment is arbitrary.
THRU = 1 [RSIG_CR; addr 0D7]	IN	OUT	RSB timebase slaved to system bus RFSYNC. RMSYNC is aligned with the RX timebase and can follow a change of RX multiframe alignment without generating an alarm indication.
	OUT	OUT	RMSYNC is aligned with the RX timebase and can follow a change of RX multiframe alignment without generating an alarm indication. RFSYNC is aligned to RMSYNC.

019—Programmable Output Enable (POE)

7	6	5	4	3	2	1	0
—	—	TDL_OE	RDL_OE	INDY_OE	TCKO_OE	CLADO_OE	RCKO_OE

TDL_OE TDLCKO Output Buffer Control—When enabled, TDLCKO is output according to DL3_TS and DL3_BIT [addr 015, 016]. Note that TDL_IO [addr 018] overrides TDL_OE when TNEGI/TDLCKO pin is configured as an input.

0 = TDLCKO output enabled
1 = TDLCKO output three-stated

RDL_OE RNEGO/RDLCKO and RPOSO/RDLO Output Buffer Control—When enabled, both bi-modal signals are output by their respective internal circuits; otherwise, both outputs are placed in high impedance state.

0 = RNEGO/RDLCKO and RPOSO/RDLO outputs enabled
1 = RNEGO/RDLCKO and RPOSO/RDLO outputs three-stated

INDY_OE TNEGO/RINDO and TPOSO/TINDO Output Buffer Control—When enabled, both bi-modal signals are output by their respective internal circuits; otherwise, both outputs are forced into high impedance state.

0 = TNEGO/RINDO and TPOSO/TINDO outputs enabled
1 = TNEGO/RINDO and TPOSO/TINDO outputs three-stated

TCKO_OE TCKO Output Buffer Control—Allows the system to connect multiple devices to a common clock bus by providing programmable three-state control over the TCKO output buffer.

0 = TCKO output enabled
1 = TCKO output three-stated

CLADO_OE CLADO Output Buffer Control—Allows the system to connect multiple devices to a common clock bus by providing programmable three-state control over the CLADO output buffer. On the Bt8376 device, enabling the CLADO output forces a low on the CLADO pin.

0 = CLADO output enabled
1 = CLADO output three-stated

RCKO_OE RCKO Output Buffer Control—Allows the system to connect multiple devices to a common clock bus by providing programmable three-state control over the RCKO output buffer.

0 = RCKO output enabled
1 = RCKO output three-stated

01A—Clock Input Mux (CMUX)

7	6	5	4	3	2	1	0
RSBCKI[1]	RSBCKI[0]	TSBCKI[1]	TSBCKI[0]	CLADI[1]	CLADI[0]	TCKI[1]	TCKI[0]

RSBCKI[1:0] RSBCKI Source Select—The internal clock mux selects 1 of four clock signals for application to the RSB timebase. RSBCKI input pin is ignored when a clock source other than RSBCKI is selected.

RSBCKI[1:0]	RSBCKI Source		Notes
00	RSBCKI	Pin	Normal RSB timebase
01	TSBCKI	Pin	RSB slaved to TSB
10	CLADI	Pin	RSB slaved to CLAD input pin
11	CLADO		Internal CLAD (before output buffer).

TSBCKI[1:0] TSBCKI Source Select—The internal clock mux selects 1 of four clock signals for application to the TSB timebase. TSBCKI input pin is ignored when a clock source other than TSBCKI is selected. If TSLIP is bypassed [TSB_CR; addr 0D4], TSBCKI is not used, and the transmit data on TPCMI must be aligned with the TCKI source selected below.

TSBCKI[1:0]	TSBCKI Source		Notes
00	TSBCKI	Pin	Normal TSB timebase
01	RSBCKI	Pin	TSB slaved to RSB
10	CLADI	Pin	TSB slaved to CLAD input
11	CLADO		Internal CLAD (before output buffer).
XX	none		When TSLIP is bypassed

CLADI[1:0] CLADI Source Select—The internal clock mux selects 1 of four clock signals. The selected clock signal acts as a CLAD input timing reference when the CLAD is enabled [CEN; addr 090]. CLADI input pin is ignored whenever a clock source other than CLADI is selected.

CLADI[1:0]	CLADI Source		Notes
00	CLADI	Pin	Normal CLAD input timing
01	RCKO		Internal RCKO (before output buffer).
10	TSBCKI	Pin	CLAD slaved to TSB
11	TCKI	Pin	CLAD slaved to transmit

TCKI[1:0] TCKI Source Select—The internal transmit clock mux selects 1 of four clock signals. The selected clock signal is applied to the transmit clock monitor and is a timing reference for the digital transmitter block. This clock signal must operate at the T1/E1 line rate. If TJAT is disabled [JDIR; addr 002], the selected clock signal also appears on TCKO pin. TCKI input pin is ignored when a clock source other than TCKI is selected.

TCKO follows TCKI during NRZ mode (framer mode only). NRZ mode is detected when TNRZ bit in TCR1 register [addr 071] is set and TPOSO/TNEGO/TCKO outputs are selected and enabled. Otherwise, during normal mode (integrated LIU and framer) TCKO follows JCLK if JAT is enabled in the Transmit direction. TCKO follows TCKI if the JAT is either in the receiver or is disabled.

TCKI[1:0]	TCKI Source		Notes
00	TCKI	Pin	Normal transmit (With TSLIP)
01	RCKO		Internal RCKO (before output buffer)
10	RSBCKI	Pin	Transmit slaved to RSB
11	CLADO		Internal CLAD (before output buffer).

01B—Test Mux Configuration (TMUX)

7	6	5	4	3	2	1	0
—	—	TMUX[5]	TMUX[4]	TMUX[3]	TMUX[2]	TMUX[1]	TMUX[0]

TMUX[5:0] Test Mux Configuration—Reserved for CONEXANT production test.

01C—Test Configuration (TEST)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	TEST[1]	TEST[0]

TEST Global Test Enable—Reserved for CONEXANT production test.

3.7 Receive LIU Registers

Unused bits indicated by a dash (—) are reserved and should be written to 0. Writing to reserved bits has no effect.

Table 3-9 details receiver LIU register settings for some typical applications. The sensitivity range values shown are the minimum range of receive signal levels for which the receiver recovers data error-free. The RALOS detect range lists the range of receive signal levels for which Analog Loss of Signal (RALOS) is declared after 1 msec. The RLOS detect threshold shows the number of continuously received zeros that cause a receiver loss of signal condition. For example, for E1 I.431 applications, the receiver declares an RALOS condition when the receive signal level is –20 dB or less. For E1 G.775 applications, an RLOS condition is declared if the received signal level remains less than –24 dB for 32 bit periods.

Table 3-9. Receive LIU Register Settings versus Application

Application		Sensitivity Range	RALOS Detect Range	RLOS Detect Threshold (No. of Continuously Received Zeros)	Receiver LIU Register Configurations					
					LIU_CR(Addr 020)	RLIU_CR (addr 022)	VGA_MAX (addr 024)	DSLICE (addr 027)(1)	EQ_OUT (addr 028)(1)	PRE_EQ (addr 02A)
E1 Modes	I.431(2)	0 to –6 dB	–6 to –20 dB	—	0x41	0xB1	0x1D	0xBA	0xDA	0xA6
	G.775(2)	0 to –6 dB	–9 to –35 dB	32 @–24 dB	0x41	0xB1	0x1D	0xBA	0xDA	0xA6
	Long Range	0 to –34 dB	≤ –43 dB	32 @–43 dB	0x41	0xB1	0x34	0xBA	0xDA	0xA6
	Extended Range	–20 to –48 dB	< –48 dB	32 @–48 dB	0x41	0xB1	0x3F	0xBA	0xDA	0xE6
T1 Modes	G.775(2)	0 to –6 dB	–9 to –35 dB	100 @–24 dB	0x41	0xB1	0x1D	0xBA	0xDA	0xA6
	T1.403, PA62411	0 to –16.5 dB	—	100 @–30 dB	0x41	0xB1	0x21	0xBA	0xDA	0xA6
	I.431	0 to –18 dB	–18 to –30 dB	100 @–30 dB	0x41	0xB1	0x21	0xBA	0xDA	0xA6
	Long Range	0 to –34 dB	≤ –43 dB	100 @–43 dB	0x41	0xB1	0x34	0xBA	0xDA	0xA6
	Extended Range	–20 to –48 dB	< –48 dB	100 @–48 dB	0x41	0xB1	0x3F	0xBA	0xDA	0xE6

NOTE(S):
(1) Default value.
(2) Register values shown for short-haul applications are also applicable for the Bt8375 and Bt8376 devices.

020—LIU Configuration (LIU_CR)

NOTE: Bits 0 and 1 are reserved and should be written to the values shown.

7	6	5	4	3	2	1	0
RST_LIU	SQUELCH	FORCE_VGA	RDIGI	ATTN[1]	ATTN[0]	0	1

RST_LIU Reset RLIU—Writing a 1 to RST_LIU resets the RLIU, reinitializes the receive equalizer, and re-attempts signal acquisition. The processor must reset the RLIU after changing ATTN, or after changing equalizer coefficients [EQ_DAT; addr 025]. Optionally, it can be reset in response to an extended alarm condition.

0 = normal
1 = reset RLIU (self clears)

SQUELCH Enable Squelch—Data slicer outputs from RLIU are forced to 0 until EYEOPEN [addr 021] = 1. SQUELCH is useful for long haul applications when near-end crosstalk may be of sufficient magnitude to prevent accurate loss of signal detection.

0 = no effect
1 = squelch data slicer output

FORCE_VGA FORCE VGA—Internal Variable Gain Amplifier (VGA) is set to equal the value programmed in VGA_MAX register (addr 024). This bit is used for test purposes only.

0 = normal operation
1 = force VGA to VGA_MAX (test mode only)

RDIGI Enable Receive Digital Inputs—When set, RDIGI bypasses RLIU and enables RPOSI/RNEGI/RCKI inputs provided by an external line interface; otherwise, bipolar RTIP/RRING inputs are enabled, RCKI input is ignored, and RPLL recovers the received clock.

0 = RTIP/RRING inputs enabled
1 = RPOSI/RNEGI/RCKI inputs enabled

ATTN[1:0] Bridge Attenuation—The receive equalizer can automatically compensate for signal level attenuation caused by placement of bridge resistors in series with the normal receive termination resistance. Bridge compensation scales the equalizer coefficients because they are loaded from internal ROM; therefore, any change to the ATTN setting must be followed by an RLIU reset command (RST_LIU).

ATTN	Bridge Attenuation	Bridge Resistance
00	0 dB	None
01	–10 dB	300 Ω
10	–20 dB	1000 Ω
11	–30 dB	1500 Ω

021—Receive LIU Status (RSTAT)

7	6	5	4	3	2	1	0
CPDERR	JMPTY	ZCSUB	EXZ	BPV	—	EYEOPEN	PRE_EQ

CPDERR CLAD Phase Detector Error—Indicates the CLAD phase detector has lost lock with respect to the selected CLADI reference clock.

JMPTY JAT Empty/Full—Indicates whether the elastic store is within two unit intervals of being empty or two unit intervals of being full. JMPTY is not updated (holds its prior value) until the elastic store is within two unit intervals of its limit. The processor reads JMPTY and CPDERR to determine what event caused JERR or CKERR [addr 006].

JMPTY	JERR	JAT Status
X	0	No error
0	1	JAT Overflow
1	1	JAT Underrun

ZCSUB Zero Code Substitution—Indicates one or more B8ZS/HDB3 substitution patterns have been detected on receiver input data, depending on T1/E1N [addr 001] line rate selection. ZCSUB is reported, regardless of whether or not ZCS decoding is enabled [RAMI; addr 040]. ZCSUB is latched active high upon detection of the first ZCS pattern, and the active high hold interval is defined by LATCH_ERR [addr 046].

ZCSUB	T1/E1N	ZCSUB Status
0	X	No ZCS patterns detected
1	0	HDB3 pattern detected
1	1	B8ZS pattern detected

EXZ Excessive Zeros—Reports one or more long strings of 0s detected on RTIP/RRING data inputs. Depending on bits RZCS [addr 040] and T1/E1N [addr 001], occurrences of 8, 10, or 16 consecutive zeros are detected. EXZ is latched active high upon detection of the first error. The active high hold interval is defined by LATCH_ERR [addr 046]. If EXZ_LCV [addr 045] is enabled, EXZ errors are also accumulated in LCV count [addr 054, 055].

EXZ	T1/E1N	RZCS	EXZ Status
0	X	X	No error
1	0	X	10 consecutive 0s
1	1	0	16 consecutive 0s
1	1	1	8 consecutive 0s

BPV Bipolar Violation—Reports one or more bipolar violations detected on RTIP/RRING data inputs. Depending on RZCS [addr 040], the BPV may include bipolar violations received as part of a B8ZS or HDB3 0 code substitution. Detection of BPV or LCV errors can be selected, regardless of whether or not receive ZCS decoding is enabled [RAMI; addr 040]. BPV is latched active high upon detection of the first error. The active high hold interval is defined by LATCH_ERR [addr 046]. BPV errors are also accumulated in LCV count [addr 054, 055].

BPV	T1/E1N	RZCS	BPV Status
0	X	X	No error
1	0	0	All BPVs, including HDB3 coded BPV
1	0	1	Code violation per ITU 0.162 (two consecutive BPVs of same polarity)
1	1	0	All BPVs, including B8ZS coded BPV
1	1	1	Only BPVs that are not part of B8ZS

EYEOPEN Equalization State—EYE OPEN indicates the real-time status of RLIU adaptive equalizer, and is intended only for diagnostic testing. Remains active as long as a valid receive AMI signal is present on RTIP/RRING. When SQUELCH [addr 020] is enabled and EYEOPEN status is 0, RLIU data outputs are forced to 0.

0= Indicates the received signal is not valid.
1= Indicates the received signal is valid and the RPLL is locked.

PRE_EQ Pre-Equalizer status. Indicates whether the pre-equalizer is enabled (on) or disabled (off).

0= PRE_EQ is off
1= PRE_EQ is on

See PRE_EQ register [addr 02A]

022—Receive LIU Configuration (RLIU_CR)

7	6	5	4	3	2	1	0
FRZ_SHORT	HI_CSLICE	AGC[1]	AGC[0]	EQ_FRZ	OOR_BLOCK	RLB0	LONG_EYE

FRZ_SHORT Freeze equalizer for short lines—When set, the equalizer is not updated when the received signal is approximately –15 dB or larger.

0 = equalizer updates for all lines
1 = enable equalizer freezing if short line

HI_CSLICE High Clock Slicer Threshold.

0 = normal operation

AGC[1:0] AGC Observation Window—Set to 0x11 for normal operation. Determines the period, in bit times, for Automatic Gain Control updates.

00 = 32 bits
01 = 128 bits
10 = 512 bits
11 = 2048 bits

EQ_FRZ Freeze EQ Coefficients.

0 = normal operation, equalizer always updates depending on FRZ_SHORT setting
1 = freeze coefficients, equalizer does not update. Does not affect AGC operation

OOR_BLOCK Disable Automatic RLBO—When active, automatic RLBO switching is disabled when the ADC is out of range.

0 = normal operation
1 = disable RLBO switching

RLBO Receiver Line Build Out—Enables receive signal attenuation.

0 = RLBO forced off (normal operation)
1 = enable automatic RLBO

LONG_EYE Eye Open Timeout

0 = 4096 bit timeout
1 = 8192 bit timeout (normal operation)

023—RPLL Low Pass Filter (LPF)

7	6	5	4	3	2	1	0
—	LPF[6]	LPF[5]	LPF[4]	LPF[3]	LPF[2]	LPF[1]	LPF[0]

LPF[6:0] RPLL Low Pass Filter Gain—Reserved for CONEXANT Production test. Determines clock recovery RPLL input jitter tolerance and the worst case signal acquisition time. The initial default value is optimized for maximum input jitter tolerance.

024—Variable Gain Amplifier Maximum (VGA_MAX)

7	6	5	4	3	2	1	0
—	—	VGA_MAX[5]	VGA_MAX[4]	VGA_MAX[3]	VGA_MAX[2]	VGA_MAX[1]	VGA_MAX[0]

VGA_MAX[5:0] VGA Maximum—The processor can limit receiver sensitivity by programming the maximum allowable input signal gain into the VGA_MAX register. This option is used for short and medium haul interfaces that must declare loss of signal when the receive level falls below a certain level. The default value is 0x3F for Bt8370 and 0x2F for Bt8375/6.

Table 3-10 contains approximate VGA_MAX settings for the receive sensitivity values. The sensitivity value is the received signal level (below nominal) at which analog loss of signal (RALOS) occurs. These values are applicable only when the RLBO and the PRE_EQ are disabled. RLBO is disabled when the receive level is less than about –8 dB, or when RLBO is forced off: RLBO = 0 (reg RLIU_CR [add 022]. The PRE_EQ is disabled when the receive level is greater than about –24 dB, or when it is forced off: register PRE_EQ [addr 02A] = (10XXXXXX).

Table 3-10. VGA Maximum Settings for Receive Sensitivity

Rx Sensitivity	0 dB	–5 dB	–10 dB	–15 dB	–20 dB	–25 dB	–30 dB	–35 dB	–40 dB	–45 dB
VGA_MAX	0x0B	0x12	0x19	0x1E	0x23	0x27	0x2C	0x2F	0x33	0x37

025—Equalizer Coefficient Data Register (EQ_DAT)

7	6	5	4	3	2	1	0
EQ_DAT[7]	EQ_DAT[6]	EQ_DAT[5]	EQ_DAT[4]	EQ_DAT[3]	EQ_DAT[2]	EQ_DAT[1]	EQ_DAT[0]

EQ_DAT[7:0] Default value is set internally during RESET or RST_LIU.

026—Equalizer Coefficient Table Pointer (EQ_PTR)

7	6	5	4	3	2	1	0
—	—	EQ_PTR[5]	EQ_PTR[4]	EQ_PTR[3]	EQ_PTR[2]	EQ_PTR[1]	EQ_PTR[0]

EQ_PTR[5:0] Default value is set internally during RESET or RST_LIU. Pointer to 48-Byte (6 sets of 8) Coefficient table.

027—Data Slicer Threshold (DSLICE)

7	6	5	4	3	2	1	0
DSLICE[7]	DSLICE[6]	DSLICE[5]	DSLICE[4]	DSLICE[3]	DSLICE[2]	DSLICE[1]	DSLICE[0]

DSLICE[7:0] Internally set to default value during RESET or RST_LIU.
DSLICE[7:6] = AGC Maximum Value
DSLICE[5:4] = AGC Minimum Value
DSLICE[3:0] = Data Slicer Threshold028—EQ Output Level (EQ_OUT)

028—Equalizer Output Levels

7	6	5	4	3	2	1	0
EQ_OUT[7]	EQ_OUT[6]	EQ_OUT[5]	EQ_OUT[4]	EQ_OUT[3]	EQ_OUT[2]	EQ_OUT[1]	EQ_OUT[0]

EQ_OUT7:0] All EQ_OUT register bits are internally set to a default value during RESET. Under normal line operating conditions, the processor should not change this default value.

7	6	5	4	3	2	1	0
M1_ERR[1:0]		M2_ERR[1:0]		EQ_OUT[3:0]			

M1_ERR[1:0] Mode1 Eyeopen Threshold—Selects equalizer error tolerance during Mode1 (ACQUISITION state), specified as a percentage of the full-scale equalizer output. The equalizer automatically restarts if the average error output exceeds the selected threshold.

00 = ± 13% error tolerance
01 = ± 19% error tolerance
10 = ± 26% error tolerance
11 = ± 32% error tolerance (default)

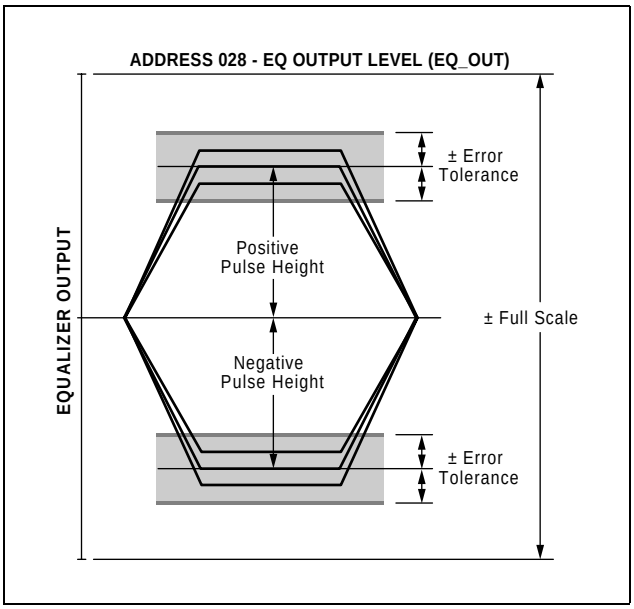
M2_ERR[1:0] Mode2 Eyeopen Threshold—Selects equalizer error tolerance during Mode2 (OPERATION state), specified as a percentage of the full-scale equalizer output. The equalizer automatically restarts if the average error output exceeds the selected threshold. During certain test situations, where the receive LIU bipolar signal level input is allowed to vary more than 15 dB without an intervening loss of signal condition, this ensures that the equalizer adapts to the modified input level.

0 = ± 13% error tolerance
01 = ± 19% error tolerance (default)
10 = ± 26% error tolerance
11 = ± 32% error tolerance

EQ_OUT[3:0] Equalizer Output Level—Selects the targeted equalizer positive/negative pulse height, specified as a percentage of the full scale equalizer output. Figure 3-1 illustrates the equalizer's eye pattern output level and its relationship to the M1_ERR and M2_ERR error tolerance thresholds.

1001 = 61% of full scale
1010 = 68% of full scale (default)
1011 = 74% of full scale
1100 = 81% of full scale

Figure 3-1. Receive Equalizer Eye Pattern Output



029—Variable Gain Amplifier Status

7	6	5	4	3	2	1	0
—	—	VGA[5]	VGA[4]	VGA[3]	VGA[2]	VGA[1]	VGA[0]

VGA[5:0] Indicates the current VGA gain level. The processor must write to this register (any value) before reading it to allow internal latches to update. The internal VGA has 64 gain values with code value 0x3F (63 dec) equal to maximum gain. The processor can estimate the line attenuation (or received signal level) in dB relative to a 3 V peak pulse level, according to the following table:

Line Attenuation	0	10	20	30	40	50	60	64dB
VGA Gain	0x0F	0x1C	0x23	0x2B	0x34	0x3A	0x3D	0x3F (max)

or:
0.77 dB/step—under 10 dB
1.25 dB/step—10–40 dB
1.67 dB/step—40–50 dB
2.80 dB/step—50 dB

02A—Pre_Equalizer (PRE_EQ)

7	6	5	4	3	2	1	0
FORCE	ON	VTHRESH[5:0]					

PRE_EQ[7:0] Internally set to default value during RESET or RST_LIU. PRE_EQ is an analog filter that resides after the VGA and which operates independently of the adaptive digital equalizer. PRE_EQ compensates for distortion introduced by long and extended long-haul lines. To configure this register, please see Table 3-9, *Receive LIU Register Settings versus Application*.

Force	ON	
0	X	Auto
1	1	Forced On
1	0	Forced Off

030–037—LMS Adjusted Equalizer Coefficient Status (COEFF)

7	6	5	4	3	2	1	0
COEFF[7]	COEFF[6]	COEFF[5]	COEFF[4]	COEFF[3]	COEFF[2]	COEFF[1]	COEFF[0]

COEFF[7:0] 8-Bit Adjusted Coefficient.

038–03C—Equalizer Gain Thresholds (GAIN)

7	6	5	4	3	2	1	0
—	—	GAIN[5]	GAIN[4]	GAIN[3]	GAIN[2]	GAIN[1]	GAIN[0]

GAIN[5:0] Default loaded from ROM after RESET or RST_LIU.

3.8 Receiver Registers

Unused bits indicated by a dash (—) are reserved and should be written to 0. Writing to reserved bits has no effect.

040—Receiver Configuration (RCR0)

7	6	5	4	3	2	1	0
RAMI	RABORT	RFORCE	RLOFD	RLOFC	RLOFB	RLOFA	RZCS

RAMI Receive AMI Encoded Inputs—Disables B8ZS/HDB3 decoding for AMI-formatted RTIP/RRING receive signals. Otherwise, the ZCS decoder replaces the 000VB0VB code (B8ZS) with 8 zeros in T1 mode, or replaces the X00V code (HDB3) with four zeros in E1 mode; where B is a normal AMI pulse, V is a bipolar violation, and X is a “don't-care.” Regardless of RAMI setting, receipt of a ZCS signature is always detected and reported in ZCSUB status [RSTAT; addr 021].

0 = receive B8ZS/HDB3 line format
1 = receive AMI line format

RABORT Abort/Disable RX Offline Framer—When set, the offline framer ignores reframe requests from the online framer (RLOF) and aborts any in-progress RLOF reframe request. Loss of Frame status [RLOF; addr 047] is not affected. While RABORT remains set, the offline framer only responds to processor forced reframes (RFORCE). This allows the processor to manually control reframe criteria and prevent changes in the current receive frame alignment. RABORT is typically set only during unframed operation.

0 = normal framer operation
1 = framer disabled

RFORCE Force RX Reframe—Forces the offline framer to perform a single reframe according to selected receive framer mode. RFORCE is automatically cleared when the offline framer acknowledges the request [FSTAT; addr 017]. The processor typically does not need to force the reframe since the online framer reframe request (RLOF) is active whenever reframe criteria (RLOFD–A) is met. However, the processor may force a reframe if the frame or CRC error ratios indicate the framer might have aligned to a duplicated frame alignment pattern.

0 = no effect
1 = force RX reframe

RLOFD–RLOFA RX Reframe Criteria—Determines the number of frame errors the online framer must detect before declaring a loss of frame alignment [ALM1; addr 047]. Refer to the Receive Framer mode in [RFRAME; addr 001] (Table 2-3, *Criteria for Loss/Recovery of Receive Framer Alignment*) to find which frame bits are monitored.

T1/E1N	RLOFD–A	Reframe Criteria
0	0100	3 Consecutive FAS or 915 CRC errors
0	1100	3 Consecutive FAS Errors
1	0001	2 out of 4 F-bit errors
1	0010	2 out of 5 F-bit errors
1	0100	2 out of 6 F-bit errors

NOTE: Other RLOFD–RLOFA combinations are invalid. RAIS and RLOF status is disabled if RLOFD–RLOFA equal all zeros.

RZCS Receive B8ZS/HDB3 Zero Code Substitution (affects only BPV/LCV/EXZ counting)—When set, the ZCS decoder does not include bipolar violations received as part of a B8ZS/HDB3 code in the LCV error count [addr 054, 055]. Otherwise, all bipolar violations are counted. EXZ detection criteria is either 8 or 16 consecutive zeros, depending on the RZCS configuration.

0 = ZCS decoder reports all occurrences of BPV;
also selects EXZ = 16 zeros
1 = ZCS decoder does not report BPVs received as part of ZCS;
also selects EXZ = 8 zeros

041—Receive Test Pattern Configuration (RPATT)

7	6	5	4	3	2	1	0
—	—	RESEED	BSTART	FRAMED	ZLIMIT	RPATT[1]	RPATT[0]

RESEED Re-seed PRBS Sync Detector (auto clear)—If BSTART is active high, writing a one to RESEED forces the PRBS sync detector to reseed and search for test pattern sync [PSYNC; addr 00B]. The reseed and search algorithm remains active until a test pattern sync is found.

0 = no effect
1 = reseed and search for test pattern sync

When inverted data mode is selected, initiating RESEED [RPATT; addr 041] while receiving all 1s will cause false pattern sync. In such cases, check receive slip buffers to see if not all 1s is being received, then re-enable RESEED.

BSTART Enable PRBS Detector and Start Counting PRBS Bit Errors—BERR [addr 058, 059] counting is enabled when BSTART is active high and a pattern sync is found [PSYNC=1; addr 00B]; otherwise, the BERR counter holds its present value until cleared by a processor read.

0 = PRBS detector disabled and BERR stops counting
1 = enable PRBS detector and BERR counter

FRAMED PRBS Framed—When set, PRBS test pattern bits are not checked during framing bit positions. In T1 mode, F-bit locations are not searched. In E1 mode, time slot 0 and time slot 16 (if CAS framing is selected) are not searched. CAS framing is selected by setting RFRAME[3] to 1 in the Primary Control register [CR0; addr 001]. If FRAMED is disabled, the PRBS pattern receiver searches all time slots for the test pattern. FRAMED, ZLIMIT, and RPATT establish the test pattern measurement type as listed in Table 3-11.

Table 3-11. Receive PRBS Test Pattern

FRAMED	ZLIMIT	RPATT	Test Pattern	Inversion
0	0	00	Unframed 2^{11}	No
0	0	01	Unframed 2^{15}	Yes
0	0	10	Unframed 2^{20}	No
0	0	11	Unframed 2^{23}	Yes
0	1	00	Unframed 2^{11} with 7 0 limit	No
0	1	01	Unframed 2^{15} with 7 0 limit (non-std)	No
0	1	10	Unframed 2^{20} with 14 0 limit (QRSS/QRS/QRTS)	No
0	1	11	Unframed 2^{23} with 14 0 limit (non-std)	No
1	0	00	Framed 2^{11}	No
1	0	01	Framed 2^{15}	Yes
1	0	10	Framed 2^{20}	No
1	0	11	Framed 2^{23}	Yes
1	1	00	Framed 2^{11} with 7 0 limit	No
1	1	01	Framed 2^{15} with 7 0 limit (non-std)	No
1	1	10	Framed 2^{20} with 14 0 limit (QRSS/QRS/QRTS)	No
1	1	11	Framed 2^{23} with 14 0 limit (non-std)	No

ZLIMIT PRBS 0 Limit—Determines the number of consecutive zeros allowed within the selected PRBS test pattern. Refer to Table 3-11 for test pattern measurement options.

RPATT[1:0] PRBS Test Pattern—Selects one of four PRBS test pattern lengths used to measure the received bit error ratio during out of service testing. Refer to Table 3-11 for test pattern measurement options. PRBS test patterns used by RPATT [addr 041] and TPATT [addr 076] are defined in the ITU standards O.151 and O.152 to use either inverted or non-inverted data. Bt8370/8375/8376 uses the standard data inversion option for the selected PRBS test pattern unless ZLIMIT is enabled, in which case the test pattern always uses non-inverted data.

042—Receive Loopback Code Detector Configuration (RLB)

7	6	5	4	3	2	1	0
—	—	—	—	DN_LEN[1]	DN_LEN[0]	UP_LEN[1]	UP_LEN[0]

DN_LEN[1:0] Loopback Deactivate Code Length—Selects the number of loopback pattern bits from LBD [addr 044] that are compared to received data to determine it a Loopback Deactivate Code [LOOPDN; addr 048] is detected. LOOPDN is recovered if the received data pattern contains fewer than 63 bit errors in a 24 ms period. LOOPDN is lost if 64 or more bit errors are detected in a subsequent 24 ms period. F-bits that overwrite or are inserted into the loopback pattern are not counted as bit errors. Accurate code detection is provided on lines with up to 1E-3 BER.

DN_LEN	LBD Length
00	4 Bits
01	5 Bits
10	6 Bits
11	7 Bits

UP_LEN[1:0] Loopback Activate Code Length—Selects the number of loopback pattern bits from LBA [addr 043] that are compared with received data to determine if a Loopback Activate Code [LOOPUP; addr 048] is detected. LOOPUP is recovered if received data pattern contains fewer than 63 bit errors in a 24 ms period. LOOPUP is lost if 64 or more bit errors are detected in a subsequent 24 ms period. F-bits that overwrite or are inserted into the loopback pattern are not counted as bit errors. Accurate code detection is provided on lines with up to 1E-3 BER.

UP_LEN	LBA Length
00	4 Bits
01	5 Bits
10	6 Bits
11	7 Bits

043—Loopback Activate Code Pattern (LBA)

7	6	5	4	3	2	1	0
LBA[1]	LBA[2]	LBA[3]	LBA[4]	LBA[5]	LBA[6]	LBA[7]	—

LBA[1] First bit expected of LOOPUP pattern

LBA[2] Second bit expected of LOOPUP pattern

LBA[3] Third bit expected of LOOPUP pattern

LBA[4] Fourth bit expected—Last bit if UP_LEN selects a 4-bit pattern.

LBA[5] Fifth bit expected—Last bit if UP_LEN selects a 5-bit pattern.

LBA[6] Sixth bit expected—Last bit if UP_LEN selects a 6-bit pattern.

LBA[7] Seventh bit expected—Last bit if UP_LEN selects a 7-bit pattern.

044—Loopback Deactivate Code Pattern (LBD)

7	6	5	4	3	2	1	0
LBD[1]	LBD[2]	LBD[3]	LBD[4]	LBD[5]	LBD[6]	LBD[7]	—

LBD[1] First bit expected of LOOPDN pattern

LBD[2] Second bit expected of LOOPDN pattern

LBD[3] Third bit expected of LOOPDN pattern

LBD[4] Fourth bit expected—Last bit if DN_LEN selects a 4-bit pattern.

LBD[5] Fifth bit expected—Last bit if DN_LEN selects a 5-bit pattern.

LBD[6] Sixth bit expected—Last bit if DN_LEN selects a 6-bit pattern.

LBD[7] Seventh bit expected—Last bit if DN_LEN selects a 7-bit pattern.

045—Receive Alarm Signal Configuration (RALM)

7	6	5	4	3	2	1	0
—	—	FS_NFAS	EXZ_LCV	YEL_INTEG	RLOF_INTEG	0[(1)]	RPCM_AIS

NOTE(S):
(1) Bit 1 must be written to 0.

FS_NFAS Include FS/NFAS in FERR and FRED—Selects whether Fs bit errors (T1) or NFAS Bit 2 errors (E1) are counted as frame errors [FERR; addr 050, 051], and loss of frame alignment [FRED; addr 049] includes Fs or NFAS bit errors as part of the detection criteria. A number of Fs bit locations checked also depends on JYEL framer mode.

0 = FERR and FRED do not include FS/NFAS
1 = FERR and FRED include FS/NFAS

EXZ_LCV Excess Zeros Included in LCV—Select line code violation error count [LCV; addr 054, 055] includes EXZ errors. Depending on RZCS bit setting [addr 040], each EXZ is equal to either 8 or 16 consecutive zeros.

0 = LCV does not include EXZ
1 = LCV includes EXZ

YEL_INTEG Enable Yellow Alarm Integration—When set, both the receive frame and multiframe Yellow Alarms [RYEL and RMYEL; addr 047] are integrated, as described in Table 3-13, *Receive Yellow Alarm Set/Clear Criteria* (per the selected framer mode). RYEL and RMYEL interrupt status [ISR7; addr 004] are similarly affected.

0 = normal RYEL and RMYEL status
1 = integrated RYEL and RMYEL status

RLOF_INTEG Enable RLOF Integration—When set, the receive loss of frame status [RLOF; addr 047] is integrated for 2.0 to 2.5 seconds during T1 framer modes (not applicable to E1 modes). RLOF interrupt status [ISR7; addr 004] is also integrated. However, receive framer status in ALM3 [addr 049], loss of frame count [FRED[3:0]; addr 05A] and RLOF counter overflow [ISR4; addr 007] are unaffected. RLOF_INTEG does not meet the requirements of TR62411. To meet the requirements of TR62411 "Conditions Causing The Initiation of Carrier Failure Alarms," the receive loss of frame condition reported by FRED (addr 049) must be integrated before initiating Yellow Alarm Transmission. This can be accomplished in software by integrating FRED during an RLOF Interrupt (ISR7; addr 004), with RLOF_INTEG bit cleared.

0 = normal RLOF status
1 = integrated RLOF [addr 047] status

RPCM_AIS Send AIS on RPCMO Output Pin—Replaces RPCMO data with a continuous series of all 1s. RPCM_AIS is useful in CSU or digital section applications, where the local interface must be able to forward an AIS to the opposing interface.

0 = normal RPCMO data
1 = RPCMO replaced with all ones

046—Alarm/Error/Counter Latch Configuration (LATCH)

7	6	5	4	3	2	1	0
—	—	—	—	STOP_CNT	LATCH_CNT	LATCH_ERR	LATCH_ALM

STOP_CNT Stop Error Count during RLOF/RLOS/RAIS—When enabled, error count registers [addr 050–057] are suspended at their present values during one of the following conditions: receive loss of frame (RLOF), loss of signal (RLOS), or all 1s (RAIS) alarm condition. STOP_CNT does not affect the counting of test pattern errors [BERR; addr 058, 059] or alarm events [AERR; addr 05A]. The occurrence of a red or AIS CGA inhibits further processing of all other performance parameters (i.e., BER, errored seconds, SLIPS). However, a CGA caused by a Yellow Alarm does not inhibit further alarm or performance monitoring.

0 = Continue error count during alarms
1 = Stop error count during alarms

LATCH_CNT Enable ONESEC Latching of Counters—Determines the interval for which error counts remain held in all count registers [addr 050–057]. LATCH_CNT must be active in T1 mode whenever automatic 1-second performance report messaging [AUTO_PRM; addr 0AA] is enabled. LATCH_CNT is active during E1 mode; the processor cannot use the RLOF counter overflow [addr 007] as a 128 ms MFAS timeout.

When the LATCH_CNT is inactive, the processor read of the LSB register reports the current LSB error count, it latches the current MSB error count to the MSB register, and then it clears LSB. Subsequently, reading the MSB register reports current latched MSB error count and then clears MSB.

LATCH_CNT	Count Latched	Count Hold Time
0	Never	Until read clear
1	ONESEC interval	ONESEC interval

LATCH_ERR Enable ONESEC Latching of Errors—Determines the interval for which latched active errors are held in error interrupt [ISR5; addr 006] and in pattern interrupt [ISR0; addr 00B] status.

IER	LATCH_ERR	ISR Latched	ISR Hold Time
0	0	Rising edge event	Until read clear
0	1	Rising edge event	ONESEC interval
1	X	Rising edge event	Until read clear

LATCH_ALM Enable ONESEC Latching of Alarms—Determines the interval for which latched active alarms remain held in alarm interrupt status [ISR7, ISR6; addr 004, 005].

IER	LATCH_ALM	ISR Latched	ISR Hold Time
0	0	Rising edge or transition	Until read clear
0	1	Rising edge or transition	ONESEC interval
1	X	Rising edge or transition	Until read clear

NOTE: Interrupt type determines rising edge or transition event.

047—Alarm 1 Status (ALM1)

ALM1 reports current status of receive alarms. Any change in the current status activates the corresponding interrupt status bit [ISR7; addr 004].

7	6	5	4	3	2	1	0
RMYEL	RYEL	—	RAIS	RALOS	RLOS	RLOF	SIGFRZ

RMYEL Receive Multiframe Yellow Alarm—Real-time or integrated RMYEL status depends on the selected framer mode and the Yellow Alarm integration mode [YEL_INTEG; addr 045]. Refer to Table 3-12 for mode summary and Table 3-13 for set/clear criteria. For YF detection, DL1 must be configured for FDL operation and RDL1_EN set to one. Also, RBOP_START must be set to one in register BOP [addr 0A0]. Refer to registers DL1_TS [addr 0A4] and DL1_CTL [addr 0A6].

0 = no alarm
1 = receive multiframe Yellow Alarm

Table 3-12. Receive Yellow Alarm

Receive Framer Mode	YEL_INTEG = 0		YEL_INTEG = 1	
	RYEL	RMYEL	RYEL	RMYEL
FT/SF/SLC	YB2	—	YB2_INT	—
JYEL	YJ	—	YJ_INT	—
T1DM	Y24	—	Y24_INT	—
ESF	YB2	YF	YB2_INT	YF_INT
FAS	Y0	—	Y0_INT	—
CAS	Y0	Y16	Y0_INT	Y16_INT

NOTE(S): Last known frame alignment is used to locate and monitor Yellow Alarms. Therefore, RYEL and RMYEL do not accurately report alarms during receive loss of frame alignment [RLOF; addr 047].

Table 3-13. Receive Yellow Alarm Set/Clear Criteria

Mode	Set/Clear Criteria
Y0	Set for 4 frames (500 µs) if 2 consecutive NFAS frames each contain TS0 bit 3 = 1. Cleared for 4 frames if 2 consecutive NFAS frames each contain TS0 bit 3 = 0.
Y0_INT	Set for 16 multiframes (32 ms) if every NFAS frame contains TS0 bit 3 = 1. Cleared for 16 multiframes if 1 or more NFAS frame contains TS0 bit 3 = 0.
Y16	Set for 2 multiframes (4 ms) if frame 0 in 2 consecutive multiframes each contain TS16 bit 6 = 1. Cleared for 2 multiframe if frame 0 in 2 consecutive multiframes each contain TS16 bit 6 = 0.
Y16_INT	Set for 16 multiframes (32 ms) if every frame 0 contains TS16 bit 6 = 1. Cleared for 16 multiframes if 1 or more frame 0 contains TS16 bit 6 = 0.
YB2	Set for 1 frame (125 µs) if all 24 time slots contain bit 2 = 0. Cleared for 1 frame if 1 or more time slots contain bit 2 = 1.
YB2_INT	Set for 192 frames (24 ms) if fewer than 15 time slots contain bit 2 = 1. Cleared for 192 frames if 15 or more time slots contain bit 2 = 1.
YJ	Set for 1 multiframe (1.5 ms) if frame 12 contains Fs bit = 1. Cleared for 1 multiframe if frame 12 contains Fs bit = 0.
YJ_INT	Set for 16 multiframes (24 ms) if each frame 12 contains Fs bit = 1. Set for 16 multiframes (24 ms) if 1 or more frame 12 contains Fs bit = 0.
Y24	Set for 1 frame (125 µs) if TS24 contains bit 6 = 0. Cleared for 1 frame if TS24 contains bit 6 = 1.
Y24_INT	Set for 192 frames (24 ms) if each TS24 bit 6 = 0. Cleared for 192 frames if 1 or more TS24 bit 6 = 1.
YF	Set for 32 frames (4 ms) if 16 FDL bits contain Yellow Alarm priority codeword pattern (00FFh). Cleared for 32 frames if 16 FDL bits do not contain a Yellow Alarm priority codeword pattern.
YF_INT	Set upon reception of 16 FDL bits matching Yellow Alarm priority codeword and remains set as long as the codeword pattern is not interrupted for greater than 100 ms. Cleared when the Yellow Alarm priority codeword is not present for more than 100 ms (26 missing codewords = 104 ms).

RYEL Receive Yellow Alarm—Real-time or integrated RYEL status depends on both the selected receive framer and Yellow Alarm integration modes [YEL_INTEG; addr 045]. Refer to Table 3-12, *Receive Yellow Alarm* for a mode summary and Table 3-13, *Receive Yellow Alarm Set/Clear Criteria* for set/clear criteria.

0 = No alarm
1 = Receive Yellow Alarm

RAIS Receive Alarm Indication Signal—Criteria for detection and clearance of RAIS, per ITU G.775 and ANSI T1.231.

Mode	RAIS	Set/Clear Criteria
E1	0	Cleared if two consecutive double frames (500 µs) each contain three or more zeros out of 512 bits, or if FAS alignment is recovered [FRED = 0; addr 049].
E1	1	Set if two consecutive double frames each contain two or fewer zeros out of 512 bits, and when FAS alignment is lost [FRED = 1; addr 049].
T1	0	Cleared if data received for a period of 3 ms contains five or more zeros out of 4,632 bits, or if the frame alignment is recovered [FRED = 0; addr 049].
T1	1	Set if data received for a period of 3 ms contains four or fewer zeros out of 4632 bits, and the frame alignment is lost [FRED = 1; addr 049].

RALOS Receive Analog Loss of Signal or RCKI Loss of Clock—Real-time RALOS status depends on the selection of receive bipolar or digital inputs [RDIGI; addr 020].

RDIGI	RALOS	Set/Clear Criteria
0	0	Cleared if AGC gain setting is less than VGA_MAX.
0	1	Set if AGC gain setting equals VGA_MAX [addr 024]. This indicates that the RTIP/RRING input signal amplitude remains below the programmed input signal threshold for more than 1 ms.
1	0	Cleared if RCKI transitions at least once in 125 µs.
1	1	Set when RCKI remains low for 125 µs.

RLOS Receive Loss of Signal—Criteria for detection and clearance of RLOS per ITU G.775 and T1.231.

Mode	RLOS	Set/Clear Criteria
T1	0	Cleared if the received data sustains an average pulse density of 12.5% over a period of 114 bits, starting with the receipt of a pulse—and no occurrence of 100 consecutive zeros.
T1	1	Set if 100 consecutive zeros are received.
E1	0	Cleared upon reception of 192 bits in which no interval of 32 consecutive zeros appears where the 192-bit window begins with receipt of a pulse.
E1	1	Set upon reception of 32 consecutive 0s.

RLOF Receive Loss of Frame Alignment—Real-time or integrated RLOF status depends on selected receive framer mode, out of frame criteria [RLOFA–RLOFD; addr 040], and integration mode [RLOF_INTEG; addr 045]. Refer to Table A-1 through A-7 in Appendix A to find which frame bits are monitored. Refer to Table 3-2, *Receive Framer Modes* for loss/recovery criteria. During E1 mode, RLOF indicates the logically OR'ed status of FAS/MFAS/CAS alignment machines from which individual alignment status is reported separately in FRED/MRED/SRED [addr 049].

0 = no alarm
1 = receive loss of frame alignment

SIGFRZ Signaling Freeze—Real-time SIGFRZ status indicates when input ABCD signaling bit updates are no longer being written to the receive signaling buffer [RSIGn; addr IA0–IBF]. Consequently, ABCD signaling on RPCMO (if signaling insertion is enabled) and RSIGO output pins are fixed to their existing buffered values. SIGFRZ remains active for 6 to 12 ms longer after COFA or RLOF clears. SIGFRZ status is also affected by manual SIGFRZ on/off controls [RSIG_CR; addr 0D7].

0 = no alarm (or FRZ_OFF)
1 = signaling freeze (or FRZ_ON)

048—Alarm 2 Status (ALM2)

Reports real-time status of transmit alarms and inband loopback codeword detectors. Any change in the current status activates the corresponding interrupt status bit [ISR6; addr 005].

7	6	5	4	3	2	1	0
LOOPDN	LOOPUP	—	TSHORT	TLOC	—	TLOF	—

LOOPDN Inband Loopback Deactivate—Reports detection or loss of an inband loopback code which matches the programmed LOOPDN code [LBD; addr 044].

0 = no inband code (or lost)
1 = LOOPDN code detected

LOOPUP Inband Loopback Activate—Reports detection or loss of an inband loopback code which matches the programmed LOOPUP code [LBA; addr 043].

0 = no inband code (or lost)
1 = LOOPUP code detected

TSHORT Transmit Short Circuit—Indicates transmit line driver output has reached its 50 mA current limit, which is typically caused by either a short circuited transmit cable or transmission line transient surge current.

0 = normal
1 = short circuit (50 mA current limited)

TLOC Transmit Loss of Clock—Clock monitor circuit reports that transmit clock (TXCLK) is lost if no signal transitions are detected for 8 clock cycles of ACKI. TXCLK is reported as present if four or more signal transitions are detected during 8 clock cycles of ACKI. When used in conjunction with AISCLK [addr 068], TLOC also identifies if ACKI is in use and AIS data transmission is enforced. TLOC status is indeterminate if the ACKI input signal is not present.

0 = transmit clock present
1 = transmit clock lost

TLOF Transmit Loss of Frame Alignment—Reports transmit framer status per selected mode [TFRAME; addr 070] and loss criteria [TLOFA–TLOFC; addr 071].

0 = recovered
1 = lost

049—Alarm 3 Status (ALM3)

Reports real-time status of the receive framer (not affected by ONESEC latch mode), and miscellaneous latched error status (SEF and RMAIS). Any change of the logical OR of FRED, MRED, or SRED status activates the RLOF interrupt [ISR7; addr 004]. Refer to Table 3-2, *Receive Framer Modes* [RFRAME; addr 001] to find the criteria for loss/recovery of frame alignment.

7	6	5	4	3	2	1	0
—	RMAIS	SEF	SRED	MRED	FRED	LOF[1]	LOF[0]

RMAIS Receive TS16 Alarm Indication Signal (CAS mode only)—RMAIS is latched active high and cleared by a processor read. The criteria for detection and clearance of RMAIS is per ITU G.775.

Mode	RMAIS Criteria
CAS	Set if TS16 contains three or fewer zeros out of 128 bits in each mutiframe over two consecutive multiframes (4 ms).
Other	Not applicable (read 0).

SEF Severely Errored Frame—SEF is latched active high and cleared by a processor read. Criteria for detection and clearance of SEF is per ANSI T1.231.

Mode	SEF Criteria
E1	Set if two or more (FAS or NFAS) errors are detected out of six frames. (FAS + NFAS, or 2 FAS, or 2 NFAS errors, etc.).
FT/SF/SLC	Set if two or more Ft errors are detected out of 3 Ft bits.
ESF	Set if two or more FPS errors detected out of 6 FPS bits.

SRED Loss of CAS Alignment—Real-time status of CAS alignment machine. SRED is applicable if CAS is enabled; otherwise SRED is 0.

0 = recovery of CAS alignment
1 = loss of CAS alignment

MRED Loss of MFAS Alignment—Real-time status of MFAS alignment machine. MRED is applicable if MFAS is enabled; otherwise MRED is 0.

0 = recovery of MFAS alignment
1 = loss of MFAS alignment

FRED Loss of T1/FAS Alignment—Real-time status of basic frame alignment machine. The FRED alarm counter [AERR; addr 05A] increments for each low-to-high FRED transition.

0 = recovery of frame alignment
1 = loss of frame alignment.

LOF[1:0] Reason for Loss of Frame Alignment—LOF status is latched whenever FRED reports a loss of frame alignment and remains held at the latched value until the next loss of frame alignment.

LOF[1:0]	LOF Criteria
00	Three consecutive FAS pattern errors
01	Three consecutive NFAS pattern errors
10	915 or more CRC4 errors out of 1000 blocks checked
11	8 ms timeout while searching for MFAS

3.9 Performance Monitoring Registers

Unused bits indicated by a dash (—) are reserved and should be written to 0. Writing to reserved bits has no effect.

If the counter overflow interrupt [IER4; addr 00F] is enabled for the respective performance monitoring counter, the counter rolls over after reaching its maximum count value. If the overflow interrupt is disabled, the counter holds maximum value upon saturation. Refer to LATCH [addr 046] for a description of 1-second latched counter operation. The processor must read the Least Significant Byte (LSB) before reading the Most Significant Byte (MSB) of each multi-byte counter.

050—Framing Bit Error Counter LSB (FERR)

7	6	5	4	3	2	1	0
FERR[7]	FERR[6]	FERR[5]	FERR[4]	FERR[3]	FERR[2]	FERR[1]	FERR[0]

FERR[7:0] Ft/Fs/T1DM/FPS/FAS Error Count

051—Framing Bit Error Counter MSB (FERR)

If LATCH_CNT [addr 046] is inactive, reading FERR [addr 051] clears the entire FERR[11:0] count value.

15	14	13	12	11	10	9	8
0	0	0	0	FERR[11]	FERR[10]	FERR[9]	FERR[8]

FERR[11:8] Ft/Fs/T1DM/FPS/FAS Error Count

052—CRC Error Counter LSB (CERR)

7	6	5	4	3	2	1	0
CERR[7]	CERR[6]	CERR[5]	CERR[4]	CERR[3]	CERR[2]	CERR[1]	CERR[0]

CERR[7:0] CRC6/CRC4 Error Count

053—CRC Error Counter MSB (CERR)

If LATCH_CNT [addr 046] is inactive, reading CERR [addr 053] clears the entire CERR[9:0] count value.

15	14	13	12	11	10	9	8
0	0	0	0	0	0	CERR[9]	CERR[8]

CERR[9:8] CRC6/CRC4 Error Count

054—Line Code Violation Counter LSB (LCV)

7	6	5	4	3	2	1	0
LCV[7]	LCV[6]	LCV[5]	LCV[4]	LCV[3]	LCV[2]	LCV[1]	LCV[0]

LCV[7:0] BPV and EXZ (if EXZ_LCV enabled) Error Count

055—Line Code Violation Counter MSB (LCV)

If LATCH_CNT [addr 046] is inactive, reading LCV [addr 055] clears the entire LCV[15:0] count value.

15	14	13	12	11	10	9	8
LCV[15]	LCV[14]	LCV[13]	LCV[12]	LCV[11]	LCV[10]	LCV[9]	LCV[8]

LCV[15:8] BPV and EXZ (if EXZ_LCV enabled) Error Count

056—Far End Block Error Counter LSB (FEBE)

7	6	5	4	3	2	1	0
FEBE[7]	FEBE[6]	FEBE[5]	FEBE[4]	FEBE[3]	FEBE[2]	FEBE[1]	FEBE[0]

FEBE[7:0] FEBE Count (applicable only in E1 mode); invalid FEBE count is reported in T1 mode.

057—Far End Block Error Counter MSB (FEBE)

If LATCH_CNT [addr 046] is inactive, reading FEBE [addr 056, 057] clears the entire FEBE[9:0] count value.

15	14	13	12	11	10	9	8
0	0	0	0	0	0	FEBE[9]	FEBE[8]

FEBE[9:8] FEBE Count (applicable only in E1 mode)

058—PRBS Bit Error Counter LSB (BERR)

Reading BERR transfers the most recent 12-bit count from the internal PRBS error counter to BERR[11:0], and clears the internal error counter without affecting the reported BERR[11:0] value. Subsequent reads of BERR MSB [addr 059] report the BERR [11:8] count value latched when the BERR LSB was last read.

7	6	5	4	3	2	1	0
BERR[7]	BERR[6]	BERR[5]	BERR[4]	BERR[3]	BERR[2]	BERR[1]	BERR[0]

BERR[7:0] BERR Count (applicable only for test pattern)

059—PRBS Bit Error Counter MSB (BERR)

15	14	13	12	11	10	9	8
0	0	0	0	BERR[11]	BERR[10]	BERR[9]	BERR[8]

BERR[11:8] BERR Count (suspended if BSTART = 0)

05A—SEF/LOF/COFA Alarm Counter (AERR)

Reading AERR clears the SEF[1:0], COFA[1:0] and FRED[3:0] count values.

7	6	5	4	3	2	1	0
FRED[3]	FRED[2]	FRED[1]	FRED[0]	COFA[1]	COFA[0]	SEF[1]	SEF[0]

FRED[3:0] Receive Loss of Frame Count—Increments for each occurrence of FRED [ALM3; addr 049]. The 4-bit count is large enough to count more than 100 ms of MFAS timeout intervals (8 ms each) during E1 modes. The processor can therefore use the FRED counter overflow interrupt to indicate that a receive MFAS alignment search has timed out.

COFA[1:0] Change of Frame Alignment Count—Increments each time the offline framer generates a reframe pulse that aligns the receiver timebase to a new bit position. Applicable to T1 modes only.

SEF[1:0] Severely Errored Frame Count—Increments for each occurrence of SEF [ALM3; addr 049].

3.10 Receive Sa-Byte Buffers

Unused bits indicated by a dash (—) are reserved and should be written to 0. Writing to reserved bits has no effect.

Five receive Sa-Byte buffers [RSA4–RSA8] are double-buffered. All five registers are updated with the Sa-bits received in TS0 of odd frames at each receive multiframe interrupt [RMF; addr 008]. Bit 0 of all RSA registers contains data from frame 1, bit 1 contains data from frame 3, bit 2 contains data from frame 5, and so on. This gives the processor a full 2 ms after RMF-interrupt to read any Sa-Byte buffer before the contents change. The processor ignores RSA buffer contents during T1 mode, and when the receiver reports a loss of FAS alignment [FRED=1; addr 049] in E1 mode.

05B—Receive Sa4 Byte Buffer (RSA4)

7	6	5	4	3	2	1	0
RSA4[7]	RSA4[6]	RSA4[5]	RSA4[4]	RSA4[3]	RSA4[2]	RSA4[1]	RSA4[0]

RSA4[7] Sa4 bit received in frame 15

RSA4[6] Sa4 bit received in frame 13

RSA4[5] Sa4 bit received in frame 11

RSA4[4] Sa4 bit received in frame 9

RSA4[3] Sa4 bit received in frame 7

RSA4[2] Sa4 bit received in frame 5

RSA4[1] Sa4 bit received in frame 3

RSA4[0] Sa4 bit received in frame 1

05C—Receive Sa5 Byte Buffer (RSA5)

7	6	5	4	3	2	1	0
RSA5[7]	RSA5[6]	RSA5[5]	RSA5[4]	RSA5[3]	RSA5[2]	RSA5[1]	RSA5[0]

RSA5[7] Sa5 bit received in frame 15

RSA5[6] Sa5 bit received in frame 13

RSA5[5] Sa5 bit received in frame 11

RSA5[4] Sa5 bit received in frame 9

RSA5[3] Sa5 bit received in frame 7

RSA5[2] Sa5 bit received in frame 5

RSA5[1] Sa5 bit received in frame 3

RSA5[0] Sa5 bit received in frame 1

05D—Receive Sa6 Byte Buffer (RSA6)

7	6	5	4	3	2	1	0
RSA6[7]	RSA6[6]	RSA6[5]	RSA6[4]	RSA6[3]	RSA6[2]	RSA6[1]	RSA6[0]

RSA6[7] Sa6 bit received in frame 15

RSA6[6] Sa6 bit received in frame 13

RSA6[5] Sa6 bit received in frame 11

RSA6[4] Sa6 bit received in frame 9

RSA6[3] Sa6 bit received in frame 7

RSA6[2] Sa6 bit received in frame 5

RSA6[1] Sa6 bit received in frame 3

RSA6[0] Sa6 bit received in frame 1

05E—Receive Sa7 Byte Buffer (RSA7)

7	6	5	4	3	2	1	0
RSA7[7]	RSA7[6]	RSA7[5]	RSA7[4]	RSA7[3]	RSA7[2]	RSA7[1]	RSA7[0]

RSA7[7] Sa7 bit received in frame 15

RSA7[6] Sa7 bit received in frame 13

RSA7[5] Sa7 bit received in frame 11

RSA7[4] Sa7 bit received in frame 9

RSA7[3] Sa7 bit received in frame 7

RSA7[2] Sa7 bit received in frame 5

RSA7[1] Sa7 bit received in frame 3

RSA7[0] Sa7 bit received in frame 1

05F—Receive Sa8 Byte Buffer (RSA8)

7	6	5	4	3	2	1	0
RSA8[7]	RSA8[6]	RSA8[5]	RSA8[4]	RSA8[3]	RSA8[2]	RSA8[1]	RSA8[0]

RSA8[7] Sa8 bit received in frame 15

RSA8[6] Sa8 bit received in frame 13

RSA8[5] Sa8 bit received in frame 11

RSA8[4] Sa8 bit received in frame 9

RSA8[3] Sa8 bit received in frame 7

RSA8[2] Sa8 bit received in frame 5

RSA8[1] Sa8 bit received in frame 3

RSA8[0] Sa8 bit received in frame 1

3.11 Transmit LIU Registers

Unused bits indicated by a dash (—) are reserved and should be written to 0. Writing to reserved bits has no effect.

060–067—Transmit Pulse Shape Configuration (SHAPE)

7	6	5	4	3	2	1	0
—	—	SHAPE[5]	SHAPE[4]	SHAPE[3]	SHAPE[2]	SHAPE[1]	SHAPE[0]

SHAPE[5:0] Initialized to default values when the processor writes to addr 068. Refer to pulse shape description in Transmit LIU section (Figure 2-39, *Digitized AMI Pulse Shape*).

068—Transmit LIU Configuration (TLIU_CR)

After writing to TLIU_CR, the processor should wait for eight MCLK-cycles before reading back TLIU_CR. This is because any write into TLIU_CR triggers an internal transfer of ROM data to update the SHAPE registers. While this internal transfer is in progress, any read or write of TLIU_CR may be blocked internally or it will return an incorrect read value.

7	6	5	4	3	2	1	0
TURNS	TERM	LBO[1]	LBO[0]	PULSE[2]	PULSE[1]	PULSE[0]	AISCLK

TURNS Transmit Transformer Turns Ratio—Transmit DAC automatically scales the XTIP/XRING outputs for the selected transformer turns ratio. The transmit DAC is current-limited and cannot source sufficient current to drive full-height output pulses when an external transmit termination resistor and 1:1.15 transformer is selected.

0 = 1:1.36 transformer
1 = 1:1.15 transformer (reduced amplitude if TERM also enabled)

TERM Transmit Termination Resistor—Transmit DAC automatically scales the XTIP/XRING output amplitude to compensate for the presence of an optional external termination resistor. The external resistor (51.1 Ω) is placed in parallel across XTIP/XRING on systems that must meet –18 dB transmitter return loss requirements. Better return loss is also possible by more closely matching transmitter and cable impedances, at the expense of higher power dissipation and lower output signal amplitude. (Refer to Figure 2-45, *External Termination Resistor Placement* for resistor placement. Refer to Table 3-14, *Return Loss Values* for return loss values.)

0 = internal transmit impedance (14.0 k Ω)
1 = external transmit termination

Table 3-14. Return Loss Values

TURNS	TERM	R_{TERM}	R_L (dB)	V_{PK} (Normalized)	Remarks
Pulse[2:0] = 75 Ω Cable Selection					
0	0	None	0	1.00	Iout scaled for 1:1.36
0	1	51.1	–18	1.00	Compromise match
0	1	40.5	–65	0.89	Impedance match
1	0	None	0	1.00	Iout scaled for 1:1.15
Pulse[2:0] = 100 Ω Cable Selection					
0	0	None	0	1.00	Iout scaled for 1:1.36
0	1	51.1	–32	1.00	Compromise match
0	1	54.1	–76	1.03	Impedance match
1	0	None	0	1.00	Iout scaled for 1:1.15
Pulse[2:0] = 120 Ω Cable Selection					
0	0	None	0	1.00	Iout scaled for 1:1.36
0	1	51.1	–18	1.00	Compromise match
0	1	64.9	–74	1.13	Impedance match
1	0	None	0	1.00	Iout scaled for 1:1.15

LBO[1:0] Select Line Build Out—Up to three LBO networks can be placed in line with the transmitter to attenuate XTIP/XRING outputs in 7.5 dB steps, per the signal transfer function defined by FCC Part 68 regulations. (Refer to Figure 2-41 through Figure 2-44 for LBO isolated pulse templates, which are applicable only while PULSE[2:0] = 111).

LBO	Attenuation @ 772 kHz	FCC Option
00	0.0 dB	Option A
01	7.5 dB	Option B
10	15.0 dB	Option C
11	22.5 dB	Final Span Target Loss

PULSE[2:0] Select Transmit Pulse Template—Each positive or negative pulse output on XTIP/XRING is shaped to meet the transmit pulse template according to the selected cable length and type. (Refer to Figure 2-34, *TLIU Waveform* and Figure 2-41, *0 dB LBO Isolated Pulse Template* for T1/E1 isolated pulse templates.) Each time the processor writes to TLIU_CR [addr 068], the default shape values are transferred from internal ROM into SHAPE registers [addr 060–067]. Custom shape programming for alternative cable types or pulse templates will be discussed in a separate Bt8370/8375/8376 application note.

PULSE	Cable Length	Cable Type	Application
000	0–133 Ft	100 Ω Twisted Pair	T1 DSX
001	133–266 Ft	100 Ω Twisted Pair	T1 DSX
010	266–399 Ft	100 Ω Twisted Pair	T1 DSX
011	399–533 Ft	100 Ω Twisted Pair	T1 DSX
100	533–655 Ft	100 Ω Twisted Pair	T1 DSX
101	ITU–T G.703	75 Ω Coaxial Cable	E1
110	ITU–T G.703	120 Ω Twisted Pair	E1
111	Long Haul FCC Part 68	100 Ω Twisted Pair	T1 CSU/NCTE

AISCLK Enable Automatic ACKI Switching—When AISCLK is active and the clock monitor reports a loss of transmit clock [TLOC; addr 048], the transmitter clock is automatically switched to reference ACKI instead of TCKI, and the transmitter is forced to send AIS (all ones) data. If both AISCLK and TAIS [addr 075] are active, AIS is transmitted using ACKI clock regardless of the clock monitor status. Set AISCLK only if the system supplies an alternate line rate clock on the ACKI pin.

Inputs			Status		Transmit	
TAIS	AUTO_AIS	AISCLK	RLOS/RLOC	TLOC	CLOCK	DATA
0	0	X	X	0	TCKI	Normal
0	0	1	X	0	TCKI	Normal
0	0	1	X	1	ACKI	AIS
0	1	X	0	0	TCKI	Normal
0	1	0	0	1	TCKI	Normal
0	1	1	X	1	ACKI	AIS
0	1	0	1	X	TCKI	AIS
1	X	1	X	X	ACKI	AIS
1	X	0	X	X	TCKI	AIS

3.12 Transmitter Registers

Unused bits indicated by a dash (—) are reserved and should be written to 0. Writing to reserved bits has no effect.

070—Transmit Framer Configuration (TCR0)

TCR0 selects the offline framer's criteria for recovery of transmit frame alignment; it determines the output of transmit frame and alarm formatters overhead bits, and works in conjunction with TCR1 [addr 071] and TFRM [addr 072]. This allows TCR0 to select the transmit online frame monitor's criteria for loss of frame alignment, and which overhead bits are supplied by the transmit frame and the alarm formatters.

7	6	5	4	3	2	1	0
—	—	—	—	TFRAME[3]	TFRAME[2]	TFRAME[1]	TFRAME[0]

TFRAME[3:0] The frame formatter generates Ft, Fs, FPS, FAS, MFAS, and CRC bits. The alarm formatter generates YB2, YJ, Y0, and Y16 bits. Frame and alarm overhead formats are selected by TFRAME[3:0] and T1/E1N settings, as listed in Tables 3-15 through 3-18. Each Yellow Alarm can be generated manually or automatically [TALM; addr 075], or can be bypassed [INS_MYEL; addr 072].

The frame formatter does not generate CAS or Sa-bit overhead; these bits are supplied by TPCMI in Bypass mode [TFRM; addr 072], or by programming TSIGn [addr 120–13F] or TSA4–TSA8 [addr 07B–07F] buffer contents. To insert CAS, the processor selects TLOCAL output signaling for time slot 0 and time slot 16 by programming transmit per-channel control registers TPC0 [addr 100] and TPC16 [addr 110]. The processor then fills ABCD local signaling value for TPC0 with the MAS pattern (ABCD = 0000) and TPC16 with XYXX pattern (ABCD = 1011).

The frame formatter does not generate SLC, T1DM, or FDL overhead; these bits are supplied either by TPCMI in Bypass mode [TFRM; addr 072] or by programming the TSLIP [addr 140–17F], TDL1 [addr 0AD], or TDL2 [addr 0B8] buffer contents.

To insert SLC concentrator, maintenance, alarm, and switch field values, the processor selects any SLC framer format and programs either the TDL1 or the TDL2 to operate in unformatted Pack6 mode over the F-bit channel during even frames. This overwrites all Fs bits inserted by the frame formatter. The data pattern to be sent in 36 Fs bit multiframe is written as six 6-bit words to the TDL1 or TDL2 circular buffer. For real-time overhead manipulation, the processor can rewrite the circular buffer with a new 36-bit pattern, as desired.

To insert T1DM, the processor enables TIDLE insertion on time slot 24 by programming the transmit per-channel control [TDC24; addr 118], and filling the TSLIP buffer location for TS24 [addr 158] with the T1DM framing pattern (TS24 = 10111YR0). If specific T1DM elements must be inserted and others bypassed, the processor configures TDL1 or TDL2 to selectively insert only the desired bits such as the T1DM sync pattern, R-bits, and/or Y-bits, by programming data link bit enables [DL1_BIT; addr 0A5 or DL2_BIT; addr 0B0].

To insert FDL, the processor configures TDL1 to operate over the F-bit channel during odd frames [DL1_TS; addr 0A4] and during Automatic Performance Report Messages [AUTO_PRM; addr 0AA], or the processor manually programs TDL1 to send each message.

Table 3-15. E1 Transmit Framer Modes (T1/E1N = 0)

TFRAME	Framer Mode	TS0 Overhead Insertion				Yellow Alarms	
		MFAS	FEBE	CRC4	FAS	YEL	MYEL
00XX	FAS Only	Ones	Ones	Ones	Yes	Y0	—
01XX	FAS + MFAS	Yes	Yes	Yes	Yes	Y0	—
10XX	FAS + CAS	Ones	Ones	Ones	Yes	Y0	Y16
11XX	FAS + MFAS + CAS	Yes	Yes	Yes	Yes	Y0	Y16

Table 3-16. T1 Transmit Framer Modes (T1/E1N = 1)

TFRAME	Framer Mode	F-bit Overhead Insertion				Yellow Alarms	
		Fs	FPS	CRC6	Ft	YEL	MYEL
0000	FT Only	Ones	—	—	Yes	YB2	—
0100	SF	Yes	—	—	Yes	YB2	—
0101	SF + JYEL	Yes	—	—	Yes	YJ	—
100X	SLC	Yes	—	—	Yes	YB2	—
0001	ESF + No CRC	—	Yes	Ones	—	YB2	YF(1)
1100	ESF + Mimic CRC	—	Yes	Yes	—	YB2	YF(1)
1101	ESF + Force CRC	—	Yes	Yes	—	YB2	YF(1)

NOTE(S):
(1) YF Yellow Alarm is generated manually using DL1 data link controller and transmitting the appropriate BOP message.

Table 3-17. Criteria for E1 Loss/Recovery of Transmit Frame Alignment

Mode	Description
FAS	Basic Frame Alignment (BFA) is recovered when the following search criteria are satisfied: • FAS pattern (0011011) is found in frame N. • Frame N+1 contains bit 2 equal to 1. • Frame N+2 also contains FAS pattern (0011011). During FAS only modes, BFA is recovered when the following search criteria is satisfied: • FAS pattern (0011011) is found in frame N. • No mimics of the FAS pattern present in frame N+1. • FAS pattern (0011011) is found in frame N+2. ***NOTE(S):*** If FAS pattern is not found in frame N+2 or FAS mimic is found in frame N+1, the search restarts in frame N+2. Transmit Loss of Frame (TLOF) alignment is declared when: Three consecutive FAS pattern errors are detected, when the FAS pattern consists of a 7-bit (x0011011) pattern in FAS frames, as well as bit 2 equaling 1 in NFAS frames.
MFAS	MFAS—CRC Multiframe Alignment is recovered when the following search criteria are satisfied: • BFA is recovered, identifying FAS and NFAS frames. • Within 6 ms after BFA, bit 1 of NFAS frames contains the first MFAS pattern (001011xx). • Within 8 ms after BFA, bit 1 of NFAS frames contains the second MFAS pattern (001011xx), aligned to first MFAS. MFAS errors do not cause Transmit Loss of Frame (TLOF) alignment.
CAS	CAS Multiframe Alignment is recovered when the following search criteria are satisfied: • BFA is recovered, identifying TS0 through TS31. • MAS (0000xxxx) Multiframe Alignment Signal pattern is found in the first 4 bits of TS16, and 8 bits of TS16 in preceding frame contains nonzero value. CAS errors do not cause Transmit Loss of Frame (TLOF) alignment.

Table 3-18. Criteria for T1 Loss/Recovery of Transmit Frame Alignment

Mode	Description
FT Only	Terminal Frame Alignment is recovered when One, and only 1 valid Ft pattern (1010) is found in 12 alternate F-bit locations (3 ms), when F-bits are separated by 193 bits. Transmit Loss of Frame (TLOF) alignment is declared when Number of Ft bit errors detected meets selected loss of frame criteria [TLOFA–TLOFC; addr 071].
SF	Superframe alignment is recovered when • Terminal frame alignment is recovered, identifying Ft bits. • Depends on SF submode. With JYEL: If SF pattern (00111x) found in Fs bits. If no JYEL: SF pattern (001110) found in Fs bits. Fs errors do not cause Transmit Loss of Frame (TLOF) alignment. Transmit loss of frame alignment (TLOF) declared when The number of Ft bit errors detected meets the selected reframe criteria [TLOFA–TLOFC; addr 071]. ***NOTE(S):*** Fs bit multiframe errors are reported in TMERR [ISR0; addr 00B], but do not cause a loss of transmit frame alignment.
SLC	Superframe alignment is recovered when • Terminal frame alignment is recovered, identifying Ft bits. • The SLC pattern (refer to Table A-3, *SLC-96 Fs Bit Contents*) is found in 16 of 32 Fs bits according to Bellcore TR-TSY-000008. Fs errors do not cause Transmit Loss of Frame (TLOF) alignment. Transmit loss of frame alignment (TLOF) declared when The number of Ft bit errors detected meets the selected reframe criteria [TLOFA–TLOFC; addr 071]. ***NOTE(S):*** Fs bit multiframe errors are reported in TMERR [ISR0; addr 00B], but do not cause a loss of transmit frame alignment.
ESF	Extended superframe alignment is recovered when A valid FPS candidate is located (001011). Candidate bits are separated by 772 digits and are received without pattern errors. • If only 1 valid FPS candidate and No CRC mode—align to FPS, regardless of CRC6 comparison. Mimic CRC mode—align to FPS, regardless of CRC6 comparison. Force CRC mode—align to FPS, only if CRC6 is correct. • If two or more valid FPS candidates and: No CRC mode—do not align (INVALID status). Mimic CRC mode—align to first FPS with correct CRC6. Force CRC mode—align to first FPS with correct CRC6. Transmit loss of frame alignment (TLOF) declared when The number of FPS pattern errors detected meets the selected loss of frame criteria [TLOFA–TLOFC; addr 071].

071—Transmitter Configuration (TCR1)

7	6	5	4	3	2	1	0
TNRZ	TABORT	TFORCE	TLOFC	TLOFB	TLOFA	TZCS[1]	TZCS[0]

TNRZ Transmit NRZ Data—Transmit dual-rail unipolar outputs TPOSO/TNEGO are replaced by non-return to 0 unipolar data (TNRZO) and transmit multiframe sync (MSYNCO). Both outputs are clocked on the rising edge of transmitter clock (TCKI). Line encoding of bipolar signals on XTIP/XRING is unaffected. MSYNCO active (high) always marks the first bit of transmit multiframe according to the selected transmit framer mode.

0 = TPOSO/TNEGO encoded per TZCS[1:0]
1 = TPOSO/TNEGO replaced by TNRZO/MSYNCO

TABORT Abort/Disable TX Offline Framer—The offline framer ignores reframe requests from the online framer (TLOF) and aborts any in progress TLOF reframe requests. The loss of frame status [TLOF; addr 048] is not affected. While TABORT remains active, the offline framer responds only to the processor force reframe request (TFORCE). This allows the processor to manually control reframe criteria or lock out changes in the current transmit frame alignment.

0 = normal framer operation
1 = framer disabled

TABORT interacts with EMBED [addr 0D0] to select which data stream is examined by online and offline transmit framer during embedded framing modes. If EMBED is active, TXDATA output from TSLIP is examined and used to align the TX timebase; otherwise, the TPCMI data stream is examined and used to align the TSB timebase, as defined in Table 3-19.

Table 3-19. Transmit Framer Position

TABORT	EMBED	TSB Alignment	Tx Alignment	Tx Framing Mode	Notes
0	0	TPCMI	Flywheel	Transmit Framing	(1–5)
0	1	TFSYNC/TMSYNC	TXDATA	Embedded Framing	(6–8)
1	X	TFSYNC/TMSYNC	Flywheel	Normal	(5, 6)

NOTE(S):
(1) TFSYNC and TMSYNC must be programmed as outputs.
(2) Offline framer examines TPCMI to supply TSB frame alignment.
(3) Online framer examines TPCMI to supply TSB multiframe alignment.
(4) SBI mode must match 2048 k or 1544 k line rate.
(5) TX timebase flywheels at initial alignment until TSB_CTR or TX_ALIGN [addr 0D4].
(6) TSB timebase flywheels if TFSYNC/TMSYNC programmed as outputs.
(7) Offline framer examines TXDATA to supply TX frame alignment.
(8) Online framer examines TXDATA to supply TX multiframe alignment.

TFORCE Force TX Reframe (auto clear)—Forces the offline framer to perform a single reframe, according to the selected transmit framer mode. TFORCE is automatically cleared when the framer acknowledges a request [ACTIVE; addr 017]. The processor typically does not need to force a reframe, because the online framer reframe request (TLOF) is active when reframe criteria TLOFC–A is met. However, the processor may attempt force a reframe if the frame or CRC bit error ratio indicates that the framer has aligned to a mimic pattern.

0 = no effect
1 = force TX reframe

TLOFC–TLOFA Transmit Loss of Frame Criteria—Determines the number of frame errors that the online framer must detect before declaring a loss of frame alignment [TLOF; addr 048]. Refer to TFRAME [addr 070] to find which frame bits are monitored during the selected framer mode.

T1/E1N	TLOFC–A	Reframe Criteria
0	100	3 consecutive FAS errors
1	001	2 out of 4 frame bit errors
1	010	2 out of 5 frame bit errors
1	100	2 out of 6 frame bit errors

NOTE(S): All other TLOFC–A combinations are invalid.

TZCS[1:0] Transmit Zero Code Suppression—Selects ZCS and Pulse Density Violation (PDV) enforcement options for XTIP/XRING and TPOSO/TNEGO outputs. B8ZS and HDB3 replace transmitted sequences of eight or four 0s with a recoverable code. These are standard T1 and E1 line code options, respectively (see Table 3-20).

Table 3-20. Transmit Zero Code Suppression

TZCS	T1/E1N	T1DM	ZCS	PDV	Zero Code Substitution (Sent left to right)
00	X	X	AMI	None	None
01	0	X	HDB3	None	000V or B00V
01	1	X	B8ZS	None	000VB0VB
10	1	X	UMC	None	10011000
11	1	X	AMI	Enforced	on PDV errors
AMI	Alternate Mark Inversion. Bipolar line code forces successive 1s to alternate their output pulse polarity. Analog and digital dual-rail outputs are always AMI encoded, although certain AMI codes are modified to include 0 suppression.				
HDB3	Prior to transmission, four consecutive 0s are substituted by 000V or B00V code, where B is an AMI pulse, and V is a bipolar violation. ZCS encoder selects the code that forces the BPV output polarity opposite that of the prior BPV.				
B8ZS	Prior to transmission, eight consecutive 0s are substituted by 000VB0VB code, where B is an AMI encoded pulse, and V is a bipolar violation.				
PDV	Enforcer overwrites transmit 0s that would otherwise cause output data to fail to meet the minimum required pulse density per ANSI T1.403 sliding window. ***NOTE(S):*** The enforcer never overwrites a framing bit and is not applicable during E1 mode. ***NOTE(S):*** Each PDV-enforced 1 causes a nonrecoverable, transmitted bit error.				
UMC	Unassigned Mux Code. DS0 channels containing eight 0s are substituted with the 10011000 code, per Bellcore TA-TSY-000278. ***NOTE(S):*** The receiver's ZCS decoder cannot recover original data content from UMC encoded signal.				
NOTE(S): PRBS, inband loopback, and YB2 alarm insertion occurs after PDV enforcement; therefore, output data might violate minimum pulse density requirements while these functions are active.					

072—Transmit Frame Format (TFRM)

TFRM controls the insertion of overhead bits generated by transmit frame and alarm formatters. Bypassed overhead bits flow transparently from TPCMI system bus input through TSLIP buffer.

7	6	5	4	3	2	1	0
—	—	INS_MYEL	INS_YEL	INS_MF	INS_FE	INS_CRC	INS_FBIT

INS_MYEL Insert Multiframe Yellow Alarm—Applicable to E1 modes only. Enables the alarm formatter to output Y16 Multiframe Yellow Alarm. Once enabled, TMYEL and AUTO_MYEL [addr 075] control the alarm output state. This bit must be set to 0 in T1 modes. In ESF framed T1 mode, the YF Multiframe Yellow Alarm is transmitted by programming the DL1 data link controller and transmitting the appropriate bit oriented code message (BOP message).

0 = bypass
1 = insert multiframe Yellow Alarm

INS_YEL Insert Yellow Alarm—The alarm formatter outputs Yellow Alarms YB2 or YJ during T1 modes, or Y0 during E1 modes. Once enabled, TYEL and AUTO_YEL [addr 075] control the Yellow Alarm output state. If the system wants to bypass JYEL (Fs bit in frame 12), it must bypass all Fs bits with INS_MF [addr 072].

0 = bypass
1 = insert Yellow Alarm.

INS_MF Insert Multiframe Alignment—The frame formatter outputs 6-bit SF alignment pattern in T1 mode, or 6-bit MFAS alignment pattern in E1 mode. INS_MF must be set while TFRAME (addr 070) selects Fs (T1) or MFAS (E1) alignment.

0 = bypass
1 = insert multiframe alignment

INS_FE Insert FEBE—During E1 mode, the alarm formatter automatically outputs TS0 bit 1 of frames 13 (FEBE13) and 15 (FEBE15) in response to received CRC4 errors. FEBE13 is active low for each received CRC4 error detected in SMF I; FEBE15 is active low for each received CRC4 error detected in SMF II. INS_FE should be set while TFRAME (addr 070) selects FEBE (E1) alignment.

0 = bypass
1 = insert FEBE

INS_CRC Insert Cyclic Redundancy Check—The frame formatter outputs the calculated CRC6 bits in T1 mode or CRC4 bits in E1 mode.

0 = bypass
1 = insert cyclic redundancy check

INS_FBIT Insert Terminal Framing—The frame formatter outputs a 2-bit Ft alignment pattern in F-bits of odd frames (SF framing) or FPS framing pattern (ESF framing) during T1 modes—or 8-bit FAS/NFAS alignment pattern during E1 modes. INS_FBIT should be set while TFRAME (addr 070) selects Ft (T1, SF), FPS (T1, ESF), or FAS (E1) alignment.

NOTE: If F-bits are bypassed while TSLIP is enabled, the system must use either embedded T1 framing or apply at least a double frame (250 µs) multiframe sync pulse (TMSYNC) to provide odd/even frame alignment.

0 = bypass
1 = insert terminal framing

073—Transmit Error Insert (TERROR)

Transmit error insertion capabilities are provided for system diagnostic, production test, and test equipment applications. Writing a 1 to any TERROR bit injects a single occurrence of the respective error on TPOSO/TNEGO and XTIP/XRING outputs. Writing a 0 has no effect. Multiple transmit errors can be generated simultaneously. Injected errors also affect data sent during either a Framer or Analog Loopback [FLOOP or ALOOP; addr 014].

7	6	5	4	3	2	1	0
TSERR	TMERR	TBERR	BSLIP	TCOFA	TCERR	TFERR	TVERR

TSERR Inject CAS Multiframe (MAS) Error—Injects a single MAS pattern error. TSERR performs a logical inversion of the first MAS bit transmitted.

0 = no effect
1 = inject MAS error

TMERR Inject Multiframe Error—Injects a single Fs (T1) or MFAS bit (E1) error. TMERR performs a logical inversion of the next multiframe bit transmitted. The processor can pace writing to TMERR to control which MFAS bit is errored.

0 = no effect
1 = inject multiframe error

TBERR Inject PRBS Test Pattern Error—Injects a single PRBS error by logically inverting the next PRBS generator output bit. The processor can pace writing to TBERR to create the desired bit error ratio (up to 5E-3 if TBERR asserted 1/192 bits at every frame interrupt).

0 = no effect
1 = inject PRBS error

BSLIP/TCOFA Inject Transmit COFA—Forces a 1-bit shift in the location of transmit frame alignment by deleting (or inserting) one bit position from the transmit frame. During E1 modes, BSLIP determines in which direction the bit slip will occur. In T1 modes, only one bit deletion is provided. Note that TCOFA alters the extraction rate of data from the transmit slip buffer; thus, repeated TCOFAs eventually cause a controlled frame slip where one frame of data is repeated (T1/BSLIP = 0) or where one frame of data is deleted (BSLIP = 1).

TCOFA	T1/E1N	BSLIP	Transmit COFA
0	X	X	No effect
1	0	0	Inhibit output of TS0 bit 1 for one frame
1	0	1	Insert 1 prior to FAS pattern for one frame
1	1	X	Inhibit output of F-bit for one frame

TCERR Inject CRC Error—Injects a single CRC6 (T1) or CRC4 (E1) bit error. TCERR logically invert the next CRC bit transmitted. The processor can pace writing to TCERR to control which CRC bit is errored.

0 = no effect
1 = inject CRC error

TFERR Inject Frame Bit Error—Injects a single Ft, FPS, or FAS bit error, depending on the selected transmit framer mode. TFERR logically invert the next frame bit transmitted. The processor can pace writing to TFERR, to control which frame bit is errored.

0 = no effect
1 = inject frame error

TVERR Inject Line Code Violation—Injects a single LCV error depending on the line mode and the selected ZCS. In T1 mode, the LCV injector waits for transmission of two consecutive pulses on the data output before performing BPV error insertion and clearing the TVERR bit. A BPV error cannot be injected into a transmit data stream that does not contain two consecutive 1s. TVERR is latched until an opportunity to inject a BPV error is presented, thus preventing the receiving end from detecting frame or multiframe bit errors, CRC errors, multiple BPV errors (due to ZCS pattern corruption), or PRBS test pattern bit errors as a consequence of error insertion. In E1 mode with HDB3 selected, the LCV injector sends two consecutive BPVs of the same polarity, which causes the receiving end to detect a single LCV error.

0 = no effect
1 = inject line code violation

074—Transmit Manual Sa-Byte/FEBE Configuration (TMAN)

7	6	5	4	3	2	1	0
INS_SA[8]	INS_SA[7]	INS_SA[6]	INS_SA[5]	INS_SA[4]	FEBE_II	FEBE_I	TFEBE

INS_SA[8] Manual Sa8-Byte Transmit (0-bypass)

INS_SA[7] Manual Sa7-Byte Transmit (0-bypass)

INS_SA[6] Manual Sa6-Byte Transmit (0-bypass)

INS_SA[5] Manual Sa5-Byte Transmit (0-bypass)

INS_SA[4] Manual Sa4-Byte Transmit (0-bypass)

FEBE_II Bit to manually transmit in FEBE bit position of Frame 15.

FEBE_I Bit to manually transmit in FEBE bit position of Frame 13.

TFEBE Manual Transmit FEBE (Overrides INS_FE; addr 072)—Provides a manual override for FEBE bits that are normally sent by the alarm formatter [INS_FE; addr 072]. When active, FEBE_I controls the data output in TS0 bit 1 of frame 13 (FEBE13), and FEBE_II controls the data output in TS0 bit 1 of frame 15 (FEBE15).

INS_FE	TFEBE	FEBE[13]	FEBE[15]	Description
0	X	TPCMI	TPCMI	Bypass FEBE
1	0	SMF I	SMF II	Automatic FEBE
1	1	FEBE_I	FEBE_II	Manual FEBE

NOTE: Automatic FEBE insertion uses two CRC4 error signals from the receiver to indicate SMF I and SMF II errors. Each error signal is latched and held for one full multiframe to compensate for phase differences between receive and transmit multiframe timing.

075—Transmit Alarm Signal Configuration (TALM)

7	6	5	4	3	2	1	0
—	—	AUTO_MYEL	AUTO_YEL	AUTO_AIS	TMYEL	TYEL	TAIS

AUTO_MYEL /TMYEL Automatic Manual Transmit Multiframe Yellow Alarm—Applicable to E1 modes only. Automatic mode sends Multiframe Yellow Alarm for the duration of a receive loss of CAS alignment [SRED; addr 049]. Manual mode sends Y16 Multiframe Yellow Alarm as long as TMYEL is active.

INS_MYEL	TMYEL	AUTO_MYEL	Transmit Multiframe Yellow
0	X	X	Inactive, supplied by TPCMI
1	0	0	Inactive, supplied by TPCMI
1	0	1	E1–Y16–follows SRED status
1	1	X	E1–Y16

AUTO_YEL/TYEL Automatic Manual Transmit Yellow Alarm—Automatic mode sends a Yellow Alarm for the duration of a receive loss of frame alignment [FRED; addr 049]. Manual mode sends the alarm as long as TYEL is active and Yellow Alarm insertion [INS_YEL; addr 072] is enabled.

INS_YEL	TYEL	AUTO_YEL	Transmit Yellow Alarm
0	X	X	Supplied by TPCMI
1	0	0	Inactive(1)
1	0	1	Follows FRED status
1	1	X	Active

NOTE(S):

(1) When Inactive, time slot data passes through transmitter without modification.

2. To transmit T1DM Yellow Alarm (Y24), the processor must program TDL1, TDL2, or TSLIP buffer to transmit Y-bit output in time slot 24.

AUTO_AIS /TAIS Automatic Manual Transmit Alarm Indication Signal—When activated manually (TAIS) or automatically (AUTO_AIS), the alarm formatter replaces all data output on TPOSO/TNEGO and XTIP/XRING with an unframed all-1s signal (AIS). This includes replacing data supplied from TPOSI/TNEGI and from the receiver during line loopback [LLOOP; addr 014]. Automatic mode sends AIS for the duration of receive loss of signal [RLOS; addr 047] or receive loss of clock [RLOC; addr 047], depending on the analog or digital line interface option [RDIGI; addr 020]. If AISCLK [addr 068] is enabled, TAIS also provides manual switch control over ACKI clock input. AUTO_AIS does not affect ACKI switching.

AIS transmission [TAIS, AUTO_AIS; addr 075, or AISCLK; addr 068] does not affect transmit data that is looped back to the receiver during framer loopback [FLOOP; addr 014]. This allows both FLOOP and LLOOP to be active simultaneously during loss of signal, without disrupting data in the framer loopback path.

TAIS	AUTO_AIS	AISCLK	Transmit Data	Transmit Clock (TCKO)
0	0	0	Normal, No AIS	TCKI
0	0	1	AIS during TLOC	ACKI while TLOC
0	1	0	AIS During RLOS/RLOC	TCKI
0	1	1	AIS During TLOC or RLOS	ACKI while TLOC
1	X	0	Manual AIS	TCKI
1	X	1	Manual AIS and ACKI	ACKI

NOTE: Systems that transmit framed all ones can utilize inband loopback code generator [TLB; addr 077] to send all ones in payload only.

076—Transmit Test Pattern Configuration (TPATT)

7	6	5	4	3	2	1	0
—	—	—	TPSTART	FRAMED	ZLIMIT	TPATT[1]	TPATT[0]

TPSTART Enable Test Pattern Transmission.

FRAMED PRBS Framed—When set, the PRBS pattern does not overwrite framing bit positions and is stopped during these bit periods. In T1 mode, the frame bit (every 193rd bit) is not overwritten. In E1 mode, the PRBS test pattern is not written to time slot 0 (FAS and NFAS words) and time slot 16 (CAS signalling word) if CAS framing is also selected. CAS framing is selected by setting TFRAME[3] to 1 in the Transmit Configuration register [TCR0; addr 070]. If FRAMED is disabled, the test pattern is transmitted in all time slots.

ZLIMIT Enable 0 Limit; 7/14 depending on pattern.

TPATT[1:0] PRBS test patterns used by RPATT [addr 041] and TPATT [addr 076] are defined in the ITU standards O.151 and O.152 to use either inverted or non-inverted data. Bt8370/8375/8376 uses standard data inversion for the selected PRBS test pattern unless ZLIMIT is enabled, in which case the test pattern uses non-inverted data (see Table 3-21).

Table 3-21. Transmit PRBS Test Pattern

FRAMED	ZLIMIT	TPATT	Test Pattern	Inversion
0	0	00	Unframed 2^{11}	No
0	0	01	Unframed 2^{15}	Yes
0	0	10	Unframed 2^{20}	No
0	0	11	Unframed 2^{23}	Yes
0	1	00	Unframed 2^{11} with 7 zero limit	No
0	1	01	Unframed 2^{15} with 7 zero limit	No
0	1	10	Unframed 2^{20} with 14 zero limit (QRSS/QRS/QRTS)	No
0	1	11	Unframed 2^{23} with 14 zero limit (non-std)	No
1	0	00	Framed 2^{11}	No
1	0	01	Framed 2^{15}	Yes
1	0	10	Framed 2^{20}	No
1	0	11	Framed 2^{23}	Yes
1	1	00	Framed 2^{11} with 7 zero limit	No
1	1	01	Framed 2^{15} with 7 zero limit (non std)	No
1	1	10	Framed 2^{20} with 14 zero limit (QRSS/QRS/QRTS))	No
1	1	11	Framed 2^{23} with 14 zero limit (non-std)	No

077—Transmit Inband Loopback Code Configuration (TLB)

7	6	5	4	3	2	1	0
—	—	—	—	LB_LEN[1]	LB_LEN[0]	UNFRAMED	LBSTART

LB_LEN[1:0] Inband Loopback Code Length (from LBP):
00 = 4 bits
01 = 5 bits
10 = 6 bits
11 = 7 bits

UNFRAMED Loopback Code Overwrites Framing

LBSTART Start Inband Loopback Code Transmission

078—Transmit Inband Loopback Code Pattern (LBP)

7	6	5	4	3	2	1	0
LBP[1]	LBP[2]	LBP[3]	LBP[4]	LBP[5]	LBP[6]	LBP[7]	—

LBP[1] First bit transmitted

LBP[2] Second bit transmitted

LBP[3] Third bit transmitted

LBP[4] Fourth bit transmitted

LBP[5] Fifth bit transmitted

LBP[6] Sixth bit transmitted

LBP[7] Seventh bit transmitted

3.13 Transmit Sa-Byte Buffers

Unused bits indicated by a dash (—) are reserved and should be written to 0. Writing to reserved bits has no effect.

Five transmit Sa-Byte buffers (TSA4–TSA8) are used to insert Sa-bits in TS0. The entire group of 40 bits is sampled every 16 frames, coincident with the TMF interrupt boundary [addr 008]. Bit 0 from each TSA register is then inserted during frame 1: bit 1 is inserted during frame 3; bit 2 is inserted during frame 5; and so on. This gives the processor a maximum of 2 ms after the TMF interrupt to write new Sa-Byte buffer values. Transmit Sa-bits maintain a fixed relationship to the transmit CRC multiframe.

07B—Transmit Sa4 Byte Buffer (TSA4)

7	6	5	4	3	2	1	0
TSA4[7]	TSA4[6]	TSA4[5]	TSA4[4]	TSA4[3]	TSA4[2]	TSA4[1]	TSA4[0]

TSA4[7] Sa4 bit transmitted in frame 15

TSA4[6] Sa4 bit transmitted in frame 13

TSA4[5] Sa4 bit transmitted in frame 11

TSA4[4] Sa4 bit transmitted in frame 9

TSA4[3] Sa4 bit transmitted in frame 7

TSA4[2] Sa4 bit transmitted in frame 5

TSA4[1] Sa4 bit transmitted in frame 3

TSA4[0] Sa4 bit transmitted in frame 1

07C—Transmit Sa5 Byte Buffer (TSA5)

7	6	5	4	3	2	1	0
TSA5[7]	TSA5[6]	TSA5[5]	TSA5[4]	TSA5[3]	TSA5[2]	TSA5[1]	TSA5[0]

TSA5[7] Sa5 bit transmitted in frame 15

TSA5[6] Sa5 bit transmitted in frame 13

TSA5[5] Sa5 bit transmitted in frame 11

TSA5[4] Sa5 bit transmitted in frame 9

TSA5[3] Sa5 bit transmitted in frame 7

TSA5[2] Sa5 bit transmitted in frame 5

TSA5[1] Sa5 bit transmitted in frame 3

TSA5[0] Sa5 bit transmitted in frame 1

07D—Transmit Sa6 Byte Buffer (TSA6)

7	6	5	4	3	2	1	0
TSA6[7]	TSA6[6]	TSA6[5]	TSA6[4]	TSA6[3]	TSA6[2]	TSA6[1]	TSA6[0]

TSA6[7] Sa6 bit transmitted in frame 15

TSA6[6] Sa6 bit transmitted in frame 13

TSA6[5] Sa6 bit transmitted in frame 11

TSA6[4] Sa6 bit transmitted in frame 9

TSA6[3] Sa6 bit transmitted in frame 7

TSA6[2] Sa6 bit transmitted in frame 5

TSA6[1] Sa6 bit transmitted in frame 3

TSA6[0] Sa6 bit transmitted in frame 1

07E—Transmit Sa7 Byte Buffer (TSA7)

7	6	5	4	3	2	1	0
TSA7[7]	TSA7[6]	TSA7[5]	TSA7[4]	TSA7[3]	TSA7[2]	TSA7[1]	TSA7[0]

TSA7[7] Sa7 bit transmitted in frame 15

TSA7[6] Sa7 bit transmitted in frame 13

TSA7[5] Sa7 bit transmitted in frame 11

TSA7[4] Sa7 bit transmitted in frame 9

TSA7[3] Sa7 bit transmitted in frame 7

TSA7[2] Sa7 bit transmitted in frame 5

TSA7[1] Sa7 bit transmitted in frame 3

TSA7[0] Sa7 bit transmitted in frame 107F—Transmit Sa8 Byte Buffer (TSA8)

07F—Transmit Sa8 Byte Buffer (TSA8)

7	6	5	4	3	2	1	0
TSA8[7]	TSA8[6]	TSA8[5]	TSA8[4]	TSA8[3]	TSA8[2]	TSA8[1]	TSA8[0]

TSA8[7] Sa8 bit transmitted in frame 15

TSA8[6] Sa8 bit transmitted in frame 13

TSA8[5] Sa8 bit transmitted in frame 11

TSA8[4] Sa8 bit transmitted in frame 9

TSA8[3] Sa8 bit transmitted in frame 7

TSA8[2] Sa8 bit transmitted in frame 5

TSA8[1] Sa8 bit transmitted in frame 3

TSA8[0] Sa8 bit transmitted in frame 1

3.14 Clock Rate Adapter Registers

Unused bits indicated by a dash (—) are reserved and should be written to 0. Writing to reserved bits has no effect.

090—Clock Rate Adapter Configuration (CLAD_CR)

7	6	5	4	3	2	1	0
CEN	XSEL[2]	XSEL[1]	XSEL[0]	LFGAIN[3]	LFGAIN[2]	LFGAIN[1]	LFGAIN[0]

CEN Enable CLAD Phase Detector—When active, the CPHASE detector compares the CLAD reference (CLADI/RSCALE) to the CLAD variable (CLADV/VSCALE), and sends the resulting phase error information to the NCO. When inactive, the CLADI signal is ignored and JEN or JFREE [addr 002] selects the input timing reference.

CEN	JEN	JFREE	JDIR	CLAD Input Timing Reference
0	0	1	X	REFCKI = Free running 10 MHz clock
0	1	1	0	REFCKI = Free running 10 MHz clock with transmit JAT
0	1	1	1	REFCKI = Free running 10 MHz clock with receive JAT
0	1	0	0	TXCLK = TCKI or ACKI per AISCLK [addr 068]
0	1	0	1	RXCLK = RPLL or RCKI per RDIGI [addr 020]
1	0	0	X	CLADI = System clock, bypass JAT elastic store
1	1	0	0	CLADI = System clock, with transmit JAT
1	1	0	1	CLADI = System clock, with receive JAT

NOTE: JCLK always operates at T1 or E1 line rate selected by T1/E1N.

XSEL[2:0] Line Rate Multiple Select—The CLAD divider chain outputs (CLADO and CLADV) can be programmed to operate at 2^0 to 2^3 times (1 X to 32 X) the T1/E1 line rate. XSEL chooses the multiplier. This is applicable only when OSEL or VSEL [addr 091] selects the multiplier output.

XSEL	Output (kHz) T1/E1N = 0	Output (kHz) T1/E1N = 1	Line Rate Multiplier
0	2048	1544	1X
1	4096	3088	2X
2	8192	6176	4X
3	16384	12352	8X
4, 5, 6, 7	—	—	Reserved

LFGAIN[3:0] Loop Filter Gain—Determines CLAD jitter tolerance and jitter attenuation characteristics by selecting the NCO loop filter's proportional phase error gain. Lower gain values improve jitter tolerance by reducing phase response time, but provide less jitter attenuation. Higher gain values increase the phase response time and improve jitter attenuation at the expense of loop acquisition time.

NOTE: Loop instability or acquisition failures may result from incorrectly programmed LFGAIN values. Typically, LFGAIN is programmed to provide a minimum 3 Hz loop bandwidth and 20 dB/decade jitter attenuation with 6 Hz filter cutoff frequency. LFGAIN values of 5 or 6 are typically chosen to meet jitter requirements.

LFGAIN	Proportional Gain
0000	$1/2^0$
|	|
1111	$1/2^{15}$

091—CLAD Frequency Select (CSEL)

7	6	5	4	3	2	1	0
VSEL[3]	VSEL[2]	VSEL[1]	VSEL[0]	OSEL[3]	OSEL[2]	OSEL[1]	OSEL[0]

VSEL[3:0] CLADV Frequency Select—Applicable only if CEN [addr 90] is active. Picks one of eight CLAD divider chain frequencies to feed back to the CPHASE detector. (Refer to Tables 2-8 through 2-9 for programming examples.) The selected CLADV frequency passes to VSCALE for further division before phase detector comparison.

VSEL	CLADV Frequency (kHz)
0000	1024
0001	2048
0010	4096
0011	8192
0100	2560
0101	1544
0110	1536
0111	T1/E1 line rate x 2^{XSEL} (addr 090)
1xxx	16,384

OSEL[3:0] CLADO Frequency Select—Picks one of eight CLAD divider chain frequencies to output on the CLADO pin. (Refer to Table 2-8, *CLADO Frequencies Selection* through 2-9 for programming examples with various input timing references.)

OSEL	CLADO Frequency (kHz)
0000	1024
0001	2048
0010	4096
0011	8192
0100	2560
0101	1544
0110	1536
0111	Multiplier = T1/E1 line rate x 2^{XSEL} (addr 090)
1xxx	16,384

092—CLAD Phase Detector Scale Factor (CPHASE)

7	6	5	4	3	2	1	0
—	RSCALE[2]	RSCALE[1]	RSCALE[0]	—	VSCALE[2]	VSCALE[1]	VSCALE[0]

RSCALE[2:0] CLAD Reference Scale Factor—Divides CLADI signal by $2^{[RSCALE]}$ to form CLADR input to CPHASE detector. Applicable only if CEN [addr 090] is active. Allows the system to supply CLADI frequency, up to a maximum of 128 times the desired CLADR reference frequency.

RSCALE	Scale Factor	CLADR Reference
000	1	CLADR = CLADI
001	2	CLADR = CLADI/2
010	4	CLADR = CLADI/4
011	8	CLADR = CLADI/8
100	16	CLADR = CLADI/16
101	32	CLADR = CLADI/32
110	64	CLADR = CLADI/64
111	128	CLADR = CLADI/128

VSCALE[2:0] CLAD Variable Scale Factor—Divides CLADV signal by $2^{[VSCALE]}$ before use in the CPHASE detector. Applicable only if CEN [addr 090] is active. Allows the system to select CLADV frequency that is up to 128 times CLADR.

VSCALE	Scale Factor	CPHASE Variable Input
000	1	CLADV selected by VSEL [addr 091]
001	2	CLADV/2
010	4	CLADV/4
011	8	CLADV/8
100	16	CLADV/16
101	32	CLADV/32
110	64	CLADV/64
111	128	CLADV/128

093—CLAD Test (CTEST)

For Conexant test purposes only. Set to 0 for normal operation.

7	6	5	4	3	2	1	0
—	—	—	PNSEL	D20A	TBUS	RWINI	JINIT

3.15 Bit-Oriented Protocol Registers

Unused bits indicated by a dash (—) are reserved and should be written to 0. Writing to reserved bits has no effect.

The Bit Oriented Protocol (BOP) transceiver sends and receives BOP messages, including ESF Yellow Alarm, which consists of repeated 16-bit patterns with an embedded 6-bit codeword. The BOP message channel is configured to operate over the same channel selected by the DL1 Time Slot Enable register [DL1_TS; addr 0A4]. Therefore, DL1 must be configured and enabled to allow BOP operation, as described in Table 3-22.

Table 3-22. (Datalink Configuration Register Description)

Datalink Configuration Registers	Value	Description
DL1_TS [addr 0A4]	0x40	Enabling odd frames, Fbit(T1)
DL1_BIT [addr 0A5]	0x00	Select bits to use in time slot.
DL1_CTL [addr 0A6]	0x03	Select normal FIFO mode, FCS, Tx enabled, Rx enabled.
RDL1_FFC [addr 0A7]	00######	###### is the threshold for receiver FIFO near full.
TDL1_FEC [addr 0AB]	00######	###### is the threshold for transmit FIFO near empty.

The BOP message channel must be configured to operate over the FDL channel for BOP messages to convey Priority, Command, and Response codeword messages according to *ANSI T1.403*, Section 9.4.1. The precedence of transmitted BOP messages with respect to current DL1 transmit activity is configurable [TBOP_MODE; addr 0A0]. BOP messages can also be transmitted during E1 mode, although the 16-bit codeword pattern has not been adopted as an E1 standard. BOP message format:

```
0xxxxxx011111111 (transmitted right to left)
[543210]6-bit codeword
```

0A0—Bit Oriented Protocol Transceiver (BOP)

7	6	5	4	3	2	1	0
RBOP_START	RBOP_INTEG	RBOP_LEN[1]	RBOP_LEN[0]	TBOP_LEN[1]	TBOP_LEN[0]	TBOP_MODE[1]	TBOP_MODE[0]

RBOP_START BOP Receiver Enable—When active, the BOP receiver searches the FDL channel for data that matches a 16-bit pattern in the form of 0xxxxxx011111111, where xxxxxx equals a 6-bit codeword. Otherwise, the BOP receiver is disabled.

0 = disabled
1 = BOP receiver enable

RBOP_INTEG RBOP Integration—Requires receipt of two identical, consecutive 16-bit patterns (without errors or gaps between patterns) to validate a single codeword. In this case, an errored codeword does not increment the pattern count. RBOP integration must be enabled to meet codeword detection criteria while receiving a 1E-3 bit error ratio. RBOP_INTEG adds at least one to the number of successive 16-bit patterns needed to qualify receipt of BOP message (2 in a row counts as 1 pattern; 11 in a row counts as 10; and 26 in a row counts as 25).

0 = no integration

1 = RBOP integrationRBOP_LEN[1:0]

RBOP Message Length—Selects the number of successive identical 16-bit patterns needed to qualify receipt of a single BOP message and update RBOP [addr 0A2] with the received codeword. During this time, the RBOP interrupt [ISR1; addr 00A] is also activated. Successive patterns can be separated by any number of bits, as long as they do not contain a different valid codeword.

RBOP_LEN	Successive Patterns	Notes
00	1	Single 16-bit pattern updates RBOP
01	10	Minimum command, response length
10	25	Preferred command, response length
11	Change	RBOP updates on receipt of each new pattern

TBOP_LEN[1:0] TBOP Message Length—Selects the number of repeated 16-bit patterns sent as a single message when a TBOP [addr 0A1] codeword is written. Another message with the same or different codeword value can be written to TBOP as soon as prior message start is acknowledged, via activation of a TBOP interrupt [ISR2; addr 009]. If no new message is written, the FDL channel returns to TDL1 output control upon completion of message transmission. The processor changes TBOP_LEN to end transmission of a continuously repeating message.

TBOP_LEN	Repeated Patterns	Message Length (ms)	Notes
00	1	4	Single message sends 16 FDL bits
01	10	40	Minimum command, response length
10	25	100	Preferred command
11	Continuous	Continuous	Required for ESF Yellow Alarm

TBOP_MODE[1:0] Transmit BOP mode—Enables the BOP transmitter and establishes priority of TBOP [addr 0A1] output in relation to TDL1 [addr 0AD] output. When TBOP messages are given output priority, any write to TBOP aborts TDL1 output within the next 8 FDL bit times and suspends TDL1 data output until TBOP has completed transmission. The processor can check TMSG1 status [addr 0AE] before writing TBOP to determine if TDL1 output is idle. The TDL1 buffer can be written while TBOP is granted priority.

When TDL1 messages are given output priority, TBOP output is suspended when the TDL1 buffer becomes non-empty. In case of multiple pending messages, PRM messages have highest priority, then BOP, and then TDL1. Furthermore, TBOP is forced to wait until the TDL1 buffer is empty and the TDL1 output is in the idle state before TBOP output is granted priority. If TBOP_LEN is continuous, and TDL1/PRM message output is pending, then TBOP is suspended at the next 16-bit pattern boundary. TDL1 priority is used to transmit PRM, DS1 Idle (ISID), or optional path maintenance (PID, TSID) messages, which are separated by ESF Yellow Alarm codewords, as defined in Annex D of ANSI T1.403.

TBOP_MODE	Mode Description
0X	Disabled: TBOP writes are ignored
10	TBOP output priority
11	TDL1 output priority

0A1—Transmit BOP Codeword (TBOP)

Writing a codeword into TBOP transmits a BOP message. The LSB is transmitted first.

7	6	5	4	3	2	1	0
—	—	TBOP[5]	TBOP[4]	TBOP[3]	TBOP[2]	TBOP[1]	TBOP[0]

TBOP[5] Sixth bit transmitted

TBOP[4] Fifth bit transmitted

TBOP[3] Fourth bit transmitted

TBOP[2] Third bit transmitted

TBOP[1] Second bit transmitted

TBOP[0] Transmit BOP codeword; first bit transmitted

0A2—Receive BOP Codeword (RBOP)

7	6	5	4	3	2	1	0
RBOP_LOST	RBOP_VALID	RBOP[5]	RBOP[4]	RBOP[3]	RBOP[2]	RBOP[1]	RBOP[0]

RBOP_LOST Previous Message Overwritten—Activated when RBOP is updated and RBOP_VALID is already set, indicating the previous codeword was never read by the processor.
0 = no error
1 = prior codeword lost

RBOP_VALID RBOP Message Valid—Set each time RBOP[5:0] is updated with a codeword value. Reading from RBOP clears RBOP_VALID.
0 = no message or message read
1 = new RBOP message received

RBOP[5] Sixth bit received

RBOP[4] Fifth bit received

RBOP[3] Fourth bit received

RBOP[2] Third bit received

RBOP[1] Second bit received

RBOP[0] Receive BOP codeword, first bit received

0A3—BOP Status (BOP_STAT)

Real-time status of the BOP transmitter and receiver are reported primarily for diagnostic purposes.

7	6	5	4	3	2	1	0
TBOP_ACTIVE	RBOP_ACTIVE	—	—	—	—	—	—

TBOP_ACTIVE TBOP Active—Remains set for the entire length of a message as defined by TBOP_LEN[1:0] [addr 0A0].

RBOP_ACTIVE RBOP Active—If RBOP_LEN [addr 0A0] is programmed to 10 or 25, RBOP_ACTIVE is set at the end of the first pattern and held active until the desired number of patterns is detected. The RBOP interrupt is then generated. RBOP_ACTIVE does not toggle when RBOP_LEN is programmed to 1.

3.16 Data Link Registers

Unused bits indicated by a dash (—) are reserved and should be written to 0. Writing to reserved bits has no effect.

The Bt8370 and Bt8375 contain two independent Data Link Controllers (DL1, DL2) that are programmed to send and receive HDLC formatted or unformatted serial data over any combination of bits within a selected time slot. The serial data channels operate at a multiple of 4 kbps, up to the full 64 kbps time slot rate, by selecting a combination of time slot bits from odd, even, or all frames. DL1 and DL2 each contain a 64-byte receive and 64-byte transmit buffer which function as programmable length circular buffers or as full-length data FIFOs. The Bt8376 device contains only a single controller, DL1.

0A4—DL1 Time Slot Enable (DL1_TS)

7	6	5	4	3	2	1	0
DL1_TS[7]	DL1_TS[6]	DL1_TS[5]	DL1_TS[4]	DL1_TS[3]	DL1_TS[2]	DL1_TS[1]	DL1_TS[0]

DL1_TS[7] Unchannelized—Test mode only, all time slots selected. Zero for normal operation.

DL1_TS[6, 5] Frame Select—Transmit and receive data link 1 operates on data only during specified T1/E1 frames. Frame select options give the processor access to different types of data link channels and overhead channels. Overhead bit insertion is performed after TDL1, so internal transmitter overhead insertion must be bypassed [TFRM; addr 072] before processor-supplied overhead can be output from TDL1.

00 = all frames
01 = even frames only
10 = odd frames only
11 = reserved

DL1_TS[4:0] Time Slot Word Enable—Transmit and receive data link 1 operates on data only during the specified time slot. During T1 mode, selecting time slot 0 enables data link operation on the F-bit positions.

DL1_TS[4:0]	Time slot Enable
00000	F-bit (T1) or TS0 (E1)
00001	TS1
|	|
11110	TS30
11111	TS31

0A5—DL1 Bit Enable (DL1_BIT)

7	6	5	4	3	2	1	0
DL1_BIT[7]	DL1_BIT[6]	DL1_BIT[5]	DL1_BIT[4]	DL1_BIT[3]	DL1_BIT[2]	DL1_BIT[1]	DL1_BIT[0]

DL1_BIT[7:0] DL1 Bit Select—Works in conjunction with DL1_TS [addr 0A4] to select one or more time slot bits for data link input and output. Any combination of bits can be enabled by writing the corresponding DL1_BIT active (high). The LSB enables first bit transmitted or received, and MSB enables eighth bit transmitted or received. DL1_BIT has no effect when DL1_TS selects T1 F-bits.

0 = disable data link bit
1 = enable data link bit

0A6—DL1 Control (DL1_CTL)

7	6	5	4	3	2	1	0
—	—	—	TDL1_RPT	DL1[1]	DL1[0]	TDL1_EN	RDL1_EN

TDL1_RPT The Circular Buffer/FIFO control bit [TDL1_RPT; addr 0A6] allows the FIFO to act as a circular buffer; in this mode, a message can be transmitted repeatedly. This feature is available only for unformatted transmit data link applications. The processor can repeatedly send fixed patterns on the selected channel by writing a 1- to 64-byte message into the circular buffer. The programmed message length repeats until the processor writes a new message. The first byte of each unformatted message is output automatically, aligned to the first frame of a 24-, or 16-frame transmit multiframe (SF/ESF/MFAS). This allows the processor to source overhead or data elements aligned to the TX timebase. In both SF and ESF T1 modes, unformatted messages are aligned on 24-frame boundaries. Therefore, in SF applications, the repeating message must be designed to span two SF multiframes. Each unformatted message written is output-aligned only after the preceding message completes transmission. Therefore, data continuity is retained during the linkage of consecutive messages, provided that the contents of each message consist of a multiple of the multiframe length.

DL1[1: 0] Data Link 1 mode—Selects either HDLC-formatted Frame Check Sequence (FCS) or Non-FCS transmit and receive data link message mode or unformatted (Pack8 or Pack6) message mode. During HDLC modes, the transmit/receive circuits perform zero insertion/removal after each occurrence of five consecutive 1s contained in the message bits, FLAG (0x7E) character insertion/removal during idle channel conditions, and ABORT (0xFF) code insertion/detection upon errored channel conditions. Refer to *ITU-T Recommendation Q.921* for complete details of the HDLC link-layer protocol. FCS mode automatically generates, inserts, and checks the 16-bit FCS without passing FCS bits through transmit and receive FIFOs. Non-FCS mode passes all message bits that exist between the opening and closing FLAG characters through the FIFOs, without generating or checking FCS bits. Non-FCS mode allows the processor to generate and check the entire contents of each HDLC frame.

Unformatted data link modes provide transparent channel access, in which every data link bit transmitted is supplied by the processor through TDL1, and each bit received is passed to the processor through RDL1 [addr 0A8]. Pack8 and Pack6 unformatted mode options select the number of bits per byte that are stored in transmit/receive FIFOs—8 or 6 bits, respectively.

In T1 modes, only Pack6 is applicable. In E1, unformatted mode cannot be used if FAS_MFAS_CAS receive framing is configured. The only data processing performed during unformatted mode is the alignment of transmitted data bits with respect to the receive and transmit multiframe. Please see the valid modes for Pack8 and Pack6 in the table shown below.

00 = HDLC with FCS
01 = HDLC without FCS
10 = Unformatted Pack8
11 = Unformatted Pack6

The following initializations are required when Pack8 or Pack6 is selected:

```
If (Dlink mode == Pack8 or PACK6)
  {
    DL_TEST[1]   = 0x03      ** The value DL_TEST[1] = 0x2 is for DLINK#1,
                             and 0x3 is for DLINK#2.
    TEST         = 0x02
    DL_TEST[5]   = 0x60      ** DL_TEST[4] is for DLINK #1
    DL_TEST[5]   = 0x10      ** DL_TEST[5] is for DLINK #2
    TDL2         = 0x0
    TDL2_EOM     = 0x0
    TEST         = 0x0
  }
```

PACK8 and PACK6 would be applicable for the following applications:

Configuration	1	2	3
CR0.T_E1N	E1	E1	T1
CR0.RFRAME	FAS FAS_MFAS FAS_CAS	FAS FAS_MFAS FAS_CAS	Any
DL1_1CTL.DL	PACK8	PACK8	PACK6
DL1_TS.FRAME	ODD, EVEN	ALL FRAMES	ALL FRAMES ODD, EVEN, EVERY_ OTHER_ Even
DL1_TS, DL_TS	Any	Any	Any
DL1_BIT, DL_BIT	Two bits or more	Any	Any

TDL1_EN Transmit Data Link 1 Enable—When enabled, the transmitter begins to empty and format the contents of the transmit data link FIFO for output during the selected time slot bits according to the selected DL1[1:0] mode. It enables generation of transmitter data link interrupt events.

0 = disabled
1 = enable transmit data link

RDL1_EN Receive Data Link 1 Enable—When enabled, the receiver begins to format data from the selected time slot bits and fills the receive data link FIFO according to the selected DL1[1:0] mode. It also enables generation of receiver data link interrupt events.

0 = disabled
1 = enable receive data link

0A7—RDL #1 FIFO Fill Control (RDL1_FFC)

7	6	5	4	3	2	1	0
MSG_FILL[1]	MSG_FILL[0]	FFC[5]	FFC[4]	FFC[3]	FFC[2]	FFC[1]	FFC[0]

MSG_FILL[1:0] Unformatted Message Fill Limit—Applicable only for Pack8 and Pack6 modes, the message fill limit selects how many receive FIFO locations [RDL1; addr 0A8] are filled before the receive data link generates an RFULL interrupt [ISR2; addr 009] and generates a corresponding RDL1 Partial message status word entry. Fill limit determines how many bytes constitute an unformatted message, and also gives the processor an alternative to using RNEAR interrupts to signal the end of a received unformatted message.

The number of bits per unformatted message must divide evenly by the number of bits monitored per multiframe. For example, SLC applications monitor Fs-bits during even frames for a total of 36 bits monitored out of 72 frames. Using Pack6 mode, that group of 36 Fs-bits from each SLC multiframe can be chosen to constitute one unformatted message by selecting a message fill limit which equals 6 bytes (of 6 bits/byte). In the SLC example, an RFULL interrupt would be generated every 9 ms on each SLC multiframe boundary. Fill limits provided for T1 cases are multiples of 6 bytes (i.e., 6, 12 or 18 FIFO locations) to hold one or more multiframes of monitored data. In E1 mode, fill limits are specified in multiples of 8 bytes to correspond with the 16-frame multiframe lengths (i.e., monitoring CRC4 in MFAS framing mode, or monitoring TS16 in CAS framing mode).

T1/E1N	MSG_FILL[1:0]	Message Fill Limit
X	00	Disabled
0	01	8 bytes
0	10	16 bytes
0	11	24 bytes
1	01	6 bytes
1	10	12 bytes
1	11	18 bytes

FFC[5:0] Near Full FIFO Threshold—Selects FIFO depth of near full interrupt [RNEAR; addr 009] and near full level status [RNEAR1; addr 0A9]. The RNEAR interrupt and RNEAR1 indicator are both activated when the number of empty FIFO locations equals the selected threshold. The threshold controls how many data and/or status bytes (64 minus threshold value) that the processor must read from RDL1 after the RNEAR interrupt so it can clear the RNEAR1 indicator. The threshold also determines how much time remains (in bytes) for the processor to read RDL1 before the receive FIFO is full. If a receive message is in progress when the near full threshold is reached, the receiver issues a message interrupt [RMSG; addr 009] and places a Partial message in the receive FIFO.

FFC[5:0]	Empty @ RNEAR	Filled @ RNEAR
00 0000	none	64 = RFULL
00 0001	1 empty FIFO location	63 filled
00 0010	2 empty FIFO locations	62 filled
|	|	|
11 1110	64 empty FIFO locations	1 filled
11 1111	63 empty FIFO locations	0 filled = empty

0A8—Receive Data Link FIFO #1 (RDL1)

Two different read byte values are supplied: WORD0 equals message status, and WORD1 equals message data. The processor determines which byte value is located in the FIFO by reading the receiver data link status [RDL1_STAT; addr 0A9]. In some cases, multiple consecutive status bytes can be placed in the FIFO, so the processor must always read RDL1_STAT before reading RDL1. This allows it to distinguish between WORD0 and WORD1 byte values. However, each time a non-0 byte count [RDL1_CNT] status is read, the processor is guaranteed that the next byte read from RDL1 will be message data [WORD1], not message status. Status byte and a message data byte each occupy 1 byte of FIFO space.

WORD0: Message Status

7	6	5	4	3	2	1	0
EOM[1]	EOM[0]	RDL1_CNT[5]	RDL1_CNT[4]	RDL1_CNT[3]	RDL1_CNT[2]	RDL1_CNT[1]	RDL1_CNT[0]

EOM[1, 0] End of Message—Receive data link reports an End of Message status for each occurrence of a complete (Good), a continued (Partial), an errored (FCS/Non-integer), or an aborted (Abort) message.

Properly received unformatted messages are reported with a Partial end of message status. The processor responds to Good or Partial status by reading the indicated number of data bytes [RDL1_CNT] from RDL1. For abort or error cases, RDL1_CNT equals 0 to indicate all that received data from that message was discarded.

A Good status with RDL1_CNT=0 is reported if the processor reads RDL1 while the receiver is in progress of filling the FIFO (in which case RDL1_STAT contains RSTAT1=1 and RMSG1=1). If an abort or error status with zero byte count is reported after the processor has already buffered a prior HDLC partial message, that partial buffered processor data should be discarded.

Abort status is reported if the receiver detects a string of 7 or more consecutive 1s during an HDLC message. FCS error status is reported if FCS mode is enabled, and the checksum calculated over the received HDLC message does not match the received 16-bit FCS. Non-integer error status is reported if the receiver detects a closing FLAG character that yields an HDLC message length that is not an integer number of 8-bit octets.

00 = Good
01 = FCS/Non-integer
10 = Abort
11 = Partial

RDL1_CNT[5:0] Byte Count [5:0]—Indicates the number of Message Data [WORD1] bytes stored in subsequent consecutive FIFO locations and which constitute one received message. The reported byte count is the actual number of bytes, from 0 to 63 bytes, where 0 indicates 0 bytes for the processor to read. The processor can either read the specified number of message data bytes consecutively from RDL1, or poll RDL1_STAT after reading each data byte until RDL1_STAT reports an end of message (i.e., RMPTY1=1 or RSTAT1=1).

WORD1: Message Data

7	6	5	4	3	2	1	0
RDL1[7]	RDL1[6]	RDL1[5]	RDL1[4]	RDL1[3]	RDL1[2]	RDL1[1]	RDL1[0]

RDL1[7:0] Receive Message Data—Filled by the receiver data link, from LSB to MSB, with bits from the selected channel. The processor reads 8-bit FIFO data during HDLC and Pack8 modes. During Pack6 mode, only the six least significant bits RDL1[5:0] are filled.

0A9—RDL #1 Status (RDL1_STAT)

7	6	5	4	3	2	1	0
—	—	—	RMSG1	RSTAT1	RMPTY1	RNEAR1	RFULL1

RMSG1 In-Progress Receive Message—Real time status of receive message sequencer is provided mostly for processor-polled applications. During HDLC modes, RMSG1 is high for the interval between opening and closing FLAG characters to indicate that the receiver is filling FIFO locations (in which case RSTAT1 is also held high). RMSG1 is low while the channel receives FLAG or abort characters. During unformatted modes, RMSG1 is high continuously.

0 = channel idle
1 = channel actively filling FIFO

RSTAT1 Next, FIFO Read Equals Message Status—For non-empty FIFO conditions (RMPTY1=0), RSTAT1 indicates that the next byte read from RDL1 returns WORD0 message status or WORD1 message data. RSTAT1 equals zero if the FIFO is empty and no message is in-progress. The processor polls RSTAT1 before reading RDL1 to determine how to interpret RDL1 read byte value, or the processor checks RSTAT1 in response to RMSG interrupt [ISR2; addr 009].

0 = RDL1 byte equals Message Data (or empty FIFO, if RMTPY1=1)
1 = RDL1 byte equals Message Status (if RMPTY1=0)

RMPTY1 Receive FIFO Empty—Indicates no data or status bytes are present in the receive data link FIFO.

0 = FIFO contains data or status as indicated by RSTAT1
1 = FIFO empty

RNEAR1 Receive FIFO Near Full—Indicates the data link has filled the receive FIFO to the near full threshold level specified in FFC[5:0]. Upon reaching that level, the receiver updates the message status byte [WORD0] placed on top of the FIFO and reports the current in-progress message with a Partial end of message status. The processor must read those filled FIFO locations to clear the RNEAR1 status indicator and enable the next RNEAR interrupt.

0 = FIFO depth is below the near full level
1 = FIFO is filled to the near full level

RFULL1 Receive FIFO Full—Indicates the data link has completely filled 64 byte locations in the receive FIFO. In all cases, RFULL1 is an error indicating that the processor did not keep pace with the receiver and that one or more received messages were discarded after the FIFO became full. The FIFO can still contain one or more Good received messages, and the processor can still process all receive FIFO contents as usual. However, any message in progress when FIFO reached full is discarded and reported with a Partial end of message status and a 0 byte count (which distinguishes a full end of message status from a normal abort or error message status).

0 = FIFO is less than full
1 = FIFO has been completely filled

0AA—Performance Report Message (PRM)

7	6	5	4	3	2	1	0
AUTO_PRM	PRM_CR	PRM_R	PRM_U1	PRM_U2	PRM_SL	AUTO_SL	SEND_PRM

AUTO_PRM Automatic PRM Insertion—AUTO_PRM instructs the data link transmitter to format and send a Performance Report Message on the selected transmit channel after each occurrence of the ONESEC interrupt. To meet PRM requirements specified in ANSI T1.403-1995, both FCS mode [DL1_CTL; addr 0A6] and 1-second error count latching [LATCH_CNT; addr 046] must be enabled, and the data link channel must be selected to output on Facility Data Link (FDL) framing bits [DL1_TS=0x40; addr 0A4]. Octets 1–14 of the transmit PRM message contents are automatically encoded (as shown in Figure A-5, *Performance Report Message Structure*), based on the number of received CRC, FPS, LCV, SEF, and FRED errors [addr 050-05A]. RFSLIP errors [SSTAT; addr 0D9] are also automatically encoded if AUTO_SL (described below) is enabled. The remaining PRM message contents typically remain fixed and are supplied by the processor from other bits that follow in the PRM register. BOP priority codeword transmissions are interrupted by AUTO_PRM, if TDL1 is granted output priority [TBOP_MODE=11; addr 0A0].

AUTO_PRM messages take up no space in the transmit data link FIFO, but are inserted on the transmit channel only after the FIFO is empty. Therefore, if the processor needs to transmit another type of FDL message between PRM messages, the processor must write that message after AUTO_PRM has begun sending (i.e., after ONESEC interrupt).

0 = no automatic PRM
1 = send PRM automatically every ONESEC

PRM_CR Transmit CR Message Bit—The processor writes the selected C/R bit value to send in each PRM.

PRM_R Transmit R Message Bit—The processor writes the selected R bit value to send in each PRM.

PRM_U1 Transmit U1 Message Bit—The processor writes the selected U1 bit value to send in each PRM.

PRM_U2 Transmit U2 Message Bit—The processor writes the selected U2 bit value to send in each PRM.

PRM_SL Transmit SL Message Bit—The processor writes the selected SL bit value to send in each PRM.

AUTO_SL Automatic SL Bit Insertion—RFSLIP error status is encoded into the transmit PRM contents, or the PRM_SL bit value supplied by the processor is sent.

0 = send PRM_SL value in SL bit
1 = send RFSLIP error status in SL bit

SEND_PRM Immediately Generate and Send PRM—Similar to AUTO_PRM mode, SEND_PRM instructs the data link transmitter to format and send a Performance Report Message according to ANSI T1.403-1995. SEND_PRM executes immediately rather than waiting for an ONESEC interrupt. Thus, SEND_PRM gives processor control over PRM transmit timing. This is easier for the processor to manage if other FDL message types must also be transmitted.

0AB—TDL #1 FIFO Empty Control (TDL1_FEC)

7	6	5	4	3	2	1	0
—	—	FEC[5]	FEC[4]	FEC[3]	FEC[2]	FEC[1]	FEC[0]

FEC[5:0] Near Empty Transmit FIFO Threshold—Selects FIFO depth of near empty interrupt [TNEAR; addr 009] and near empty level status [TNEAR1; addr 0AE]. The TNEAR interrupt is activated when the number of data bytes remaining to be transmitted from the FIFO falls below the selected threshold. The TNEAR1 indicator is active as long as the number of processor-filled FIFO locations is below the selected threshold. Thus, TNEAR1 is active-high when the transmit FIFO is empty, and remains active until the processor writes the selected threshold number of bytes to TDL1 [addr 0AD]. Assuming the processor writes 64 bytes to fill an empty FIFO, a TNEAR interrupt occurs after the transmitter has sent the number of bytes required to bring the FIFO level back down below the selected threshold. Hence, the processor can consecutively write 64 - FEC[5:0] number of bytes to the transmit FIFO in response to a TNEAR interrupt. The interrupt also signifies time remaining (in bytes) for the processor to write TDL1 before transmit FIFO is emptied. Typically, FEC[5:0] is set to a small value (below 10-byte threshold) to minimize the number of TNEAR interrupts and maximize the time between TNEAR interrupts.

FEC[5:0]	Byte threshold @ TNEAR	Empty @ TNEAR
00 0000	disabled	disabled
00 0001	1 byte threshold	63 empty
00 0010	2 byte threshold	62 empty
|	|	|
11 1110	62 byte threshold	2 empty
11 1111	63 byte threshold	1 empty

0AC—TDL #1 End Of Message Control (TDL1_EOM)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—

TDL1_EOM End of Transmit Message—Writing any data value to TDL1_EOM marks the last byte of data written into the transmit FIFO as the end of an HDLC message (FCS or non-FCS mode), or the end of a transmit circular buffer. The processor must write TDL1_EOM after writing a complete message or after writing the last byte of a circular buffer into TDL1 [addr 0AD]. The written data value is ignored and cannot be read back. Multiple HDLC messages are allowed to be queued in the transmit FIFO simultaneously. The transition from one circular buffer to another occurs only after the end of message byte of the current circular buffer has been sent.

0AD—Transmit Data Link FIFO #1 (TDL1)

7	6	5	4	3	2	1	0
TDL1[7]	TDL1[6]	TDL1[5]	TDL1[4]	TDL1[3]	TDL1[2]	TDL1[1]	TDL1[0]

TDL1[7:0] Transmit Message Data—Output by the transmitter data link, from LSB to MSB, and sent on the selected time slot bits. The processor writes 8-bit FIFO data during HDLC and Pack8 modes. During Pack6 mode, only the six least significant bits TDL1[5:0] are used.

0AE—TDL #1 Status (TDL1_STAT)

7	6	5	4	3	2	1	0
—	—	—	—	TMSG1	TMPTY1	TNEAR1	TFULL1

TMSG1 In-Progress Transmit Message—The real-time status of the transmit message sequencer is provided mostly for diagnostic purposes. During HDLC modes, TMSG1 is high for the interval between opening and closing FLAG characters to indicate the transmitter is actively pulling data bytes from transmit FIFO locations. TMSG1 is low while the channel transmits FLAG or Abort characters. During Unformatted and Circular Buffer modes, TMSG1 is high continuously.

0 = channel idle
1 = channel actively emptying FIFO

TMPTY1 Transmit FIFO Empty—Indicates no message data is present in transmit data link FIFO. This is typically checked by the processor in response to a TMSG or TNEAR interrupt. If a TMSG interrupt occurs, the processor checks TMPTY1 to determine whether all queued messages were sent (TMPTY1=1) or more queued messages remain to be sent (TMPTY1=0). If TNEAR interrupt occurs, the processor confirms TMPTY1=0 to verify that the partial transmit message was not aborted by a FIFO underrun.

0 = FIFO contains data to be transmitted
1 = FIFO empty

TNEAR1 Transmit FIFO Near Empty—Indicates that the data link has emptied the transmit FIFO to below the near empty threshold specified in FEC[5:0]. After sending the byte that occupied the near empty FIFO threshold level, TNEAR1 goes active-high, which generates a TNEAR interrupt. The processor must write data to TDL1 to fill the transmit FIFO beyond the near empty threshold. This is necessary to clear TNEAR1 status, and enable the next TNEAR interrupt event.

0 = FIFO depth is below the near empty level
1 = FIFO has been emptied past the near empty level

TFULL1 Transmit FIFO Full—Indicates that the processor has completely filled 64 byte locations in transmit FIFO. While TFULL1 remains active, any subsequent processor-writes to TDL1 are ignored. If the processor inadvertently writes to TDL1 while TFULL1 is active, the processor must allow FIFO to become completely empty without writing to TDL1_EOM. This is necessary to force the transmitter to send an abort character.

0 = FIFO is less than full
1 = FIFO has been completely filled

0AF—DL2 Time Slot Enable (DL2_TS)

NOTE: Not available in Bt8376 device.

7	6	5	4	3	2	1	0
DL2_TS[7]	DL2_TS[6]	DL2_TS[5]	DL2_TS[4]	DL2_TS[3]	DL2_TS[2]	DL2_TS[1]	DL2_TS[0]

DL2_TS[7] Unchannelized—Test mode only, all time slots selected. Zero for normal operation.

DL2_TS[6, 5] Frame Select—Transmit and receive data link 2 operates on data only during specified T1/E1 frames. Frame select options give the processor access to different types of data link channels and overhead channels. Overhead bit insertion is performed after TDL1, so internal transmitter overhead insertion must be bypassed [TFRM; addr 072] before the processor-supplied overhead can be output from TDL2.

00 = all frames
01 = even frames only
10 = odd frames only
11 = reserved

DL2_TS[4:0] Time Slot Word Enable—Transmit and receive data link 2 operates on data only during the specified time slot. During T1 mode, selecting time slot 0 enables data link operation on the F-bit positions.0B0—DL2 Bit Enable (DL2_BIT)

DL2_TS[4:0]	Time Slot Enable
00000	F-bit (T1) or TS0 (E1)
00001	TS1
|	|
11110	TS30
11111	TS31

0B0—DL2 Bit Enable (DL2_BIT)

NOTE: Not available in Bt8376 device.

7	6	5	4	3	2	1	0
DL2_BIT[7]	DL2_BIT[6]	DL2_BIT[5]	DL2_BIT[4]	DL2_BIT[3]	DL2_BIT[2]	DL2_BIT[1]	DL2_BIT[0]

DL2_BIT[7:0] DL2 Bit Select—Works in conjunction with DL2_TS [addr 0AF] to select 1 or more time slot bits for data link input and output. Any combination of bits can be enabled by writing the corresponding DL2_BIT active (high). Where the LSB enables first bit transmitted or received, and MSB enables eighth bit transmitted or received, DL2_BIT has no effect when DL2_TS selects T1 F-bits.

0 = disable data link bit
1 = enable data link bit

0B1—DL2 Control (DL2_CTL)

NOTE: Not available in Bt8376 device.

7	6	5	4	3	2	1	0
—	—	—	TDL2_RPT	DL2[1]	DL2[0]	TDL2_EN	RDL2_EN

TDL2_RPT The Circular Buffer/FIFO control bit [TDL2_RPT; addr 0B1] allows the FIFO to act as a circular buffer; in this mode, a message can be transmitted repeatedly. This feature is available only for unformatted transmit data link applications. The processor can repeatedly send fixed patterns on the selected channel by writing a 1- to 64-byte message into the circular buffer. The programmed message length repeats until the processor writes a new message. The first byte of each unformatted message is output automatically, aligned to the first frame of a 24-, or 16-frame transmit multiframe (SF/ESF/MFAS). This allows the processor to source overhead or data elements aligned to the TX timebase. In both SF and ESF T1 modes, unformatted messages are aligned on 24-frame boundaries. Therefore, in SF applications, the repeating message must be designed to span two SF multiframes. Each unformatted message written is output-aligned only after the preceding message completes transmission. Therefore, data continuity is retained during the linkage of consecutive messages, provided that the content of each message consists of a multiple of the multiframe length.

DL2[1: 0] Data Link 2 mode—Selects either HDLC formatted (FCS or non-FCS) transmit and receive data link message mode or unformatted (Pack8 or Pack6) message mode. During HDLC modes, the transmit/receive circuits perform zero insertion/removal after each occurrence of five consecutive 1s contained in the message bits, FLAG (0x7E) character insertion/removal during idle channel conditions, and ABORT (0xFF) code insertion/detection, upon errored channel conditions. Refer to *ITU-T Recommendation Q.921* for complete details of the HDLC link-layer protocol. FCS mode automatically generates, inserts, and checks the 16-bit FCS without passing FCS bits through transmit and receive FIFOs. Non-FCS mode passes all message bits that exist between the opening and closing FLAG characters through the FIFOs without generating or checking FCS bits. Non-FCS mode allows the processor to generate and check the entire contents of each HDLC frame.

Unformatted data link modes provide transparent channel access in which every data link bit transmitted is supplied by the processor through TDL2, and each bit received is passed to the processor through RDL2 [addr 0B3]. Pack8 and Pack6 unformatted mode options select the number of bits per byte that are stored in transmit/receive FIFOs, 8 or 6 bits, respectively. In T1 modes, only Pack6 is applicable. In E1, unformatted mode cannot be used if FAS_MFAS-CAS receive framing is configured. The only data processing performed during unformatted mode is the alignment of transmitted data bits with respect to the receive and transmit multiframe. Please see the valid modes for Pack8 and Pack6 in the table shown below.

00 = HDLC with FCS
01 = HDLC without FCS
10 = Unformatted Pack8
11 = Unformatted Pack6

The following initializations are required when Pack8 or Pack6 is selected:

```
If (Dlink mode == Pack8 or PACK6)
  {
    DL_TEST[1]   = 0x03      ** The value DL_TEST[1] = 0x2 is for DLINK#1,
                             and 0x3 is for DLINK#2.
    TEST         = 0x02
    DL_TEST[5]   = 0x60      ** DL_TEST[4] is for DLINK #1
    DL_TEST[5]   = 0x10      ** DL_TEST[5] is for DLINK #2
    TDL2         = 0x0
    TDL2_EOM     = 0x0
    TEST         = 0x0
  }
```

PACK8 and PACK6 would be applicable for the following applications:

Configuration	1	2	3
CR0.T_E1N	E1	E1	T1
CR0.RFRAME	FAS FAS_MFAS FAS_CAS	FAS FAS_MFAS FAS_CAS	Any
DL1_1CTL.DL	PACK8	PACK8	PACK6
DL1_TS.FRAME	ODD, EVEN	ALL FRAMES	ALL FRAMES ODD, EVEN, EVERY_ OTHER_ Even
DL1_TS, DL_TS	Any	Any	Any
DL1_BIT, DL_BIT	Two bits or more	Any	Any

TDL2_EN Transmit Data Link 2 Enable—When enabled, the transmitter begins to empty and format the contents of the transmit data link FIFO for output during the selected time slot bits, according to the selected DL2[1:0] mode. It also enables generation of transmitter data link interrupt events.

0 = disabled
1 = enable transmit data link

RDL2_EN Receive Data Link 2 Enable—When enabled, the receiver begins to format data from the selected time slot bits and fill the receive data link FIFO according to the selected DL2[1:0] mode. It also enables generation of receiver data link interrupt events.

0 = disabled
1 = enable receive data link

0B2—RDL #2 FIFO Fill Control (RDL2_FFC)

NOTE: Not available in Bt8376 device.

7	6	5	4	3	2	1	0
MSG_FILL[1]	MSG_FILL[0]	FFC[5]	FFC[4]	FFC[3]	FFC[2]	FFC[1]	FFC[0]

MSG_FILL[1:0] Unformatted Message Fill Limit—Applicable only for Pack8 and Pack6 modes, the message fill limit selects how many receive FIFO locations [RDL2; addr 0B3] are filled before the receive data link generates an RFULL interrupt [ISR1; addr 00A] and before the data link generates a corresponding RDL2 Partial message status word entry. Fill limits determine how many bytes constitute an unformatted message, and give the processor an alternative to using RNEAR interrupts to signal the end of a received unformatted message.

The number of bits per unformatted message must divide evenly by the number of bits monitored per multiframe. For example, SLC applications monitor Fs-bits during even frames, for a total of 36 bits monitored out of 72 frames. Using Pack6 mode, that group of 36 Fs-bits from each SLC multiframe can be chosen to constitute one unformatted message by selecting a message fill limit which equals 6 bytes (of 6 bits/byte). In the SLC example, an RFULL interrupt would be generated every 9 ms on each SLC multiframe boundary. Fill limits provided for T1 cases are multiples of 6 bytes (i.e., 6, 12 or 18 FIFO locations) to hold one or more multiframes of monitored data. In E1 mode, fill limits are multiples of 8 bytes to correspond with the 16 frame multiframe lengths (i.e., monitoring CRC4 in MFAS framing mode, or monitoring TS16 in CAS framing mode).

T1/E1N	MSG_FILL[1:0]	Message Fill Limit
X	00	Disabled
0	01	8 bytes
0	10	16 bytes
0	11	24 bytes
1	01	6 bytes
1	10	12 bytes
1	11	18 bytes

FFC[5:0] Near Full FIFO Threshold—Selects FIFO depth of near full interrupt [RNEAR; addr 00A] and near full level status [RNEAR2; addr 0B4]. The RNEAR interrupt and RNEAR2 indicator are both activated when the number of empty FIFO locations equals the selected threshold. The threshold controls how many data and/or status bytes (64 minus threshold value) the processor

must read from RDL2 after RNEAR interrupt to clear the RNEAR2 indicator, and how much time remains (in bytes) for the processor to read RDL2 before receive FIFO is full. If a receive message is in progress when the near full threshold is reached, the receiver issues a message interrupt [RMSG; addr 00A] and places a Partial message in the receive FIFO.

FFC[5:0]	Empty @ RNEAR	Filled @ RNEAR
00 0000	none	64 = RFULL
00 0001	1 empty FIFO location	63 filled
00 0010	2 empty FIFO locations	62 filled
|	|	|
11 1110	62 empty FIFO locations	1 filled
11 1111	63 empty FIFO locations	0 filled = empty

0B3—Receive Data Link FIFO #2 (RDL2)

NOTE: Not available in Bt8376 device.

Two different read byte values are supplied: WORD0 equals message status, and WORD1 equals message data. The processor determines which byte value is located in the FIFO by first reading the receiver data link status [RDL2_STAT; addr 0B4]. In some cases, multiple consecutive status bytes can be placed in the FIFO, so the processor must always read RDL2_STAT before reading RDL2 to distinguish between WORD0 and WORD1 byte values. However, each time a non-0 byte count [RDL2_CNT] status is read, the processor is guaranteed that the next byte read from RDL2 is message data [WORD1], not message status. Status byte and a message data byte each occupies 1 byte of FIFO space.

WORD0: Message Status

7	6	5	4	3	2	1	0
EOM[1]	EOM[0]	RDL2_CNT[5]	RDL2_CNT[4]	RDL2_CNT[3]	RDL2_CNT[2]	RDL2_CNT[1]	RDL2_CNT[0]

EOM[1, 0] End of Message—The receive data link reports an End of Message status for each occurrence of a complete (Good), a continued (Partial), an errored (FCS/Non-integer), or an aborted (Abort) message. Properly received unformatted messages are reported with a Partial end of message status. The processor responds to Good or Partial status by reading the indicated number of data bytes [RDL2_CNT] from RDL2. For abort or error cases, RDL2_CNT equals 0 to indicate all received data from that message was discarded.

Note that A Good status with RDL2_CNT=0 is reported if the processor reads RDL2 while the receiver is in progress of filling the FIFO (in which case RDL2_STAT contains RSTAT2=1 and RMSG2=1). If an abort or error status with 0 byte count is reported after the processor has buffered a prior HDLC Partial message, that partial buffered processor data must be discarded. Abort status is reported if the receiver detects a string of 7 or more consecutive 1s during an HDLC message. FCS error status is reported if FCS mode is enabled and the checksum calculated over the received HDLC message does not match the received 16-bit FCS. Non-integer error status is reported if the receiver detects a closing FLAG character that yields an HDLC message length which is not an integer number of 8-bit octets.

00 = Good
01 = FCS/Non-integer
10 = Abort
11 = Partial

RDL2_CNT[5:0] Byte Count [5:0]—Indicates the number of Message Data [WORD1] bytes stored in subsequent consecutive FIFO locations, constituting one received message. The reported byte count is the actual number of bytes from 0 to 63, where 0 indicates 0 bytes for the processor to read. The processor can read either the specified number of message data bytes consecutively from RDL2, or poll RDL2_STAT after reading each data byte until RDL2_STAT reports an end of message (i.e., RMPTY2=1 or RSTAT2=1).

WORD1: Message Data

7	6	5	4	3	2	1	0
RDL2[7]	RDL2[6]	RDL2[5]	RDL2[4]	RDL2[3]	RDL2[2]	RDL2[1]	RDL2[0]

RDL2[7:0] Receive Message Data—Filled by the receiver data link, from LSB to MSB, with bits from the selected channel. The processor reads 8-bit FIFO data during HDLC and Pack8 modes. During Pack6 mode, only the 6 least significant bits RDL2[5:0] are filled.

0B4—RDL #2 Status (RDL2_STAT)

NOTE: Not available in Bt8376 device.

7	6	5	4	3	2	1	0
—	—	—	RMSG2	RSTAT2	RMPTY2	RNEAR2	RFULL2

RMSG2 In-Progress Receive Message—The real-time status of the receive message sequencer is provided mostly for processor-polled applications. During HDLC modes, RMSG2 is high for the interval between opening and closing FLAG characters to indicate the receiver is actively filling FIFO locations (in which case RSTAT2 is also held high). RMSG2 is low while the channel receives FLAG or abort characters. During unformatted modes, RMSG2 is continuously high.

0 = channel idle
1 = channel actively filling FIFO

RSTAT2 Next, FIFO Read Equals Message Status—For non-empty FIFO conditions (RMPTY2=0), RSTAT2 indicates that the next byte read from RDL2 is WORD0 message status or WORD1 message data. RSTAT2 equals 0 if the FIFO is empty, with no message in-progress. The processor polls RSTAT2 before reading RDL2 to determine how to interpret the RDL2 read byte value, or checks RSTAT2 in response to an RMSG interrupt [ISR1; addr 00A].

0 = RDL2 byte equals Message Data (or empty FIFO, if RMTPY2=1)
1 = RDL2 byte equals Message Status (if RMPTY2=0)

RMPTY2 Receive FIFO Empty—Indicates no data or status bytes are present in receive data link FIFO.

0 = FIFO contains data or status as indicated by RSTAT2
1 = FIFO empty

RNEAR2 Receive FIFO Near Full—Indicates the data link has filled the receive FIFO to the near full threshold level specified in FFC[5:0]. Upon reaching the near full level, the receiver updates the message status byte [WORD0] placed on top of the FIFO and reports the current in-progress message with a Partial end of message status. The processor must read those filled FIFO locations to clear RNEAR2 status indicator and enable the next RNEAR interrupt.

0 = FIFO depth is below the near full level
1 = FIFO has been filled to the near full level

RFULL2 Receive FIFO Full—Indicates the data link has completely filled 64 byte locations in the receive FIFO. In all cases, RFULL2 is an error indicating the processor did not keep pace with the receiver, and one or more received messages were discarded after the FIFO became full. The FIFO can still contain one or more Good received messages, and the processor can still process all receive FIFO contents as usual. However, any message that was in progress when FIFO reached full is discarded and reported with Partial end of message status and a 0 byte count (which distinguishes a full end of message status from a normal abort or error message status).

0 = FIFO is less than full
1 = FIFO has been completely filled

0B6—TDL #2 FIFO Empty Control (TDL2_FEC)

NOTE: Not available in Bt8376 device.

7	6	5	4	3	2	1	0
—	—	FEC[5]	FEC[4]	FEC[3]	FEC[2]	FEC[1]	FEC[0]

FEC[5:0] Near Empty Transmit FIFO Threshold—Selects a FIFO depth of near empty interrupt [TNEAR; addr 00A] and near empty level status [TNEAR2; addr 0B9]. The TNEAR interrupt is activated when the number of data bytes remaining to be transmitted from the FIFO falls below the selected threshold. The TNEAR2 indicator is active as long as the number of processor-filled FIFO locations is below the selected threshold. Thus, TNEAR2 is active-high when the transmit FIFO is completely empty. It remains active until the processor writes the selected threshold number of bytes to TDL2 [addr 0B8].

Assuming the processor writes 64 bytes to fill an empty FIFO, the TNEAR interrupt occurs after the transmitter has sent the number of bytes required to bring the FIFO level below the selected threshold. Hence, the processor is guaranteed to consecutively write 64 – FEC[5:0] number of bytes to the transmit FIFO in response to a TNEAR interrupt. The interrupt signifies time remaining (in bytes) for the processor to write TDL2 before the transmit FIFO is emptied. Typically, FEC[5:0] is set to a small value (approximately 5- to 10-byte threshold) minimize the number of TNEAR interrupts and to maximize the time between TNEAR interrupts.

FEC[5:0]	Byte threshold @ TNEAR	Empty @ TNEAR
00 0000	disabled	disabled
00 0001	1-byte threshold	63 empty
00 0010	2-byte threshold	62 empty
|	|	|
11 1110	62-byte threshold	2 empty
11 1111	63-byte threshold	1 empty

0B7—TDL #2 End Of Message Control (TDL2_EOM)

NOTE: Not available in Bt8376 device.

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—

TDL2_EOM End of Transmit Message—Writing any data value to TDL2_EOM marks the last byte of data written into the transmit FIFO as the end of an HDLC message (FCS or Non-FCS mode), or end of a transmit circular buffer. The processor must write TDL2_EOM after writing a complete message, or after writing the last byte of a circular buffer into TDL2 [addr 0B8]. The written data value is ignored and cannot be read back. Multiple HDLC messages are allowed to be queued in the transmit FIFO simultaneously. Transition from one circular buffer to another occurs only after the current circular buffer has been sent.

0B8—Transmit Data Link FIFO #2 (TDL2)

NOTE: Not available in Bt8376 device.

7	6	5	4	3	2	1	0
TDL2[7]	TDL2[6]	TDL2[5]	TDL2[4]	TDL2[3]	TDL2[2]	TDL2[1]	TDL2[0]

TDL2[7:0] Transmit Message Data—Output by the transmitter data link from LSB to MSB sent on selected time slot bits. The processor writes 8-bit FIFO data during HDLC and Pack8 modes. During Pack6 mode, only the 6 least significant bits TDL2[5:0] are used.

0B9—TDL #2 Status (TDL2_STAT)

NOTE: Not available in Bt8376 device

7	6	5	4	3	2	1	0
—	—	—	—	TMSG2	TMPTY2	TNEAR2	TFULL2

TMSG2 In-Progress Transmit Message—The real-time status of the transmit message sequencer is provided mostly for diagnostic purposes. During HDLC modes, TMSG2 is high for the interval between opening and closing FLAG characters to indicate the transmitter is actively pulling data bytes from transmit FIFO locations. TMSG2 is low while the channel transmits FLAG or abort characters. During Unformatted and Circular Buffer modes, TMSG2 is continuously high.

0 = channel idle
1 = channel actively emptying FIFO

TMPTY2 Transmit FIFO Empty—Indicates that no message data is present in the transmit data link FIFO. This is typically checked by the processor in response to a TMSG or TNEAR interrupt. If a TMSG interrupt occurs, the processor checks TMPTY2 to verify that all queued messages were sent (TMPTY2=1) or that more queued messages remain to be sent (TMPTY2=0). If TNEAR interrupt occurs, the processor confirms TMPTY2=0 to verify that the partial transmit message was not aborted by a FIFO underrun.

0 = FIFO contains data to be transmitted
1 = FIFO empty

TNEAR2 Transmit FIFO Near Empty—Indicates that the data link has emptied the transmit FIFO to below the near empty threshold as specified in FEC[5:0]. After sending the byte that occupied the near empty FIFO threshold level, TNEAR2 goes active-high, which generates a TNEAR interrupt. The processor must write data to TDL2 to fill the transmit FIFO beyond the near empty threshold to clear TNEAR2 status and enable the next TNEAR interrupt event.

0 = FIFO depth is below the near empty level
1 = FIFO has been emptied past the near empty level

TFULL2 Transmit FIFO Full—Indicates the processor has filled 64 byte locations in the transmit FIFO. While TFULL2 remains active, subsequent processor writes to TDL2 are ignored. If the processor inadvertently writes to TDL2 while TFULL2 is active, the processor must allow FIFO to become completely empty without writing to TDL2_EOM, to force the transmitter to send an Abort character.

0 = FIFO is less than full
1 = FIFO has been completely filled

0BA—DLINK Test Configuration (DL_TEST1)

Data link test registers [addr 0BA-0BE] are for CONEXANT production test. Set to 0 for normal operation.

7	6	5	4	3	2	1	0
—	—	—	—	DL_TEST1[3]	DL_TEST1[2]	DL_TEST1[1]	DL_TEST1[0]

DL_TEST1[3] Clock Test—Zero for normal operation, where clocks are controlled by DL1_CTL and DL2_CTL [addr 0A6, 0B1]. When active-high, clocks are enabled.

DL_TEST1[2] Shadow Select—Report shadow pointers instead of normal read/write pointers.

DL_TEST1[1, 0] FIFO Select: 00 = RDL1; 01 = RDL2; 10 = TDL1; 11 = TDL2

0BB—DLINK Test Status (DL_TEST2)

7	6	5	4	3	2	1	0
—	—	DL_TEST2[5]	DL_TEST2[4]	DL_TEST2[3]	DL_TEST2[2]	DL_TEST2[1]	DL_TEST2[0]

DL_TEST2[5:0] Read or Shadow Read Pointer—Reports selected FIFO read pointer current address.

0BC—DLINK Test Status (DL_TEST3)

7	6	5	4	3	2	1	0
—	—	DL_TEST3[5]	DL_TEST3[4]	DL_TEST3[3]	DL_TEST3[2]	DL_TEST3[1]	DL_TEST3[0]

DL_TEST3[5:0] Write or Shadow Write Pointer—Specifies selected FIFO write pointer address.

0BD—DLINK Test Control #1 or Configuration #2 (DL_TEST4)

7	6	5	4	3	2	1	0
—	DL_TEST4[6]	DL_TEST4[5]	DL_TEST4[4]	DL_TEST4[3]	DL_TEST4[2]	DL_TEST4[1]	DL_TEST4[0]

DL_TEST4[6] TFIFO1 Read Clear—Force transmit FIFO read pointer to empty.

DL_TEST4[5] TFIFO1 Write Clear—Force transmit FIFO write pointer to empty.

DL_TEST4[4] TFIFO1 Write—MPU data goes to specified write pointer address.

DL_TEST4[3] RFIFO1 Read Clear—Force receive FIFO read pointer to empty state (flush).

DL_TEST4[2] RFIFO1 Write Clear—Force receive FIFO write pointer to empty state (flush).

DL_TEST4[1] RFIFO1 Write—MPU data goes to specified write pointer address.

DL_TEST4[0] RFIFO1 Bypass—Pipe receive data.

0BE—DLINK Test Control #2 or Configuration #2 (DL_TEST5)

7	6	5	4	3	2	1	0
—	DL_TEST5[6]	DL_TEST5[5]	DL_TEST5[4]	DL_TEST5[3]	DL_TEST5[2]	DL_TEST5[1]	DL_TEST5[0]

DL_TEST5[6] TFIFO2 Read Clear—Force transmit FIFO read pointer to empty.

DL_TEST5[5] TFIFO2 Write Clear—Force transmit FIFO write pointer to empty.

DL_TEST5[4] TFIFO2 Write—MPU data goes to specified write pointer address.

DL_TEST5[3] RFIFO2 Read Clear—Force receive FIFO read pointer to empty state (flush).

DL_TEST5[2] RFIFO2 Write Clear—Force receive FIFO write pointer to empty state (flush).

DL_TEST5[1] RFIFO2 Write—MPU data goes to specified write pointer address.

DL_TEST5[0] RFIFO2 Bypass—Pipe receive data.

3.17 System Bus Registers

Unused bits indicated by a dash (—) are reserved and should be written to 0. Writing to reserved bits has no effect.

0D0—System Bus Interface Configuration (SBI_CR)

7	6	5	4	3	2	1	0
X2CLK	SBI_OE	EMF	EMBED	SBI[3]	SBI[2]	SBI[1]	SBI[0]

X2CLK Enable Times 2 Clocks—X2CLK modifies the number of RSB/TSB clock cycles used to clock a single data bit onto RSB and TSB. When X2CLK is active, two RSBCKI/TSBCKI clock cycles occur for each RPCMO, RSIGO, SIGFRZ, TPCMI, and TSIGI bit. The FSYNC and MSYNC signals remain at the full 1x RSBCKI/TSBCKI clock rate.

0 = RSB/TSB signals at RSBCKI/TSBCKI
1 = Two SBCKI clock cycles per SBI bit (except FSYNC and MSYNC).

SBI_OE Enable System Bus Outputs—Places RPCMO, RSIGO, RINDO, and SIGFRZ output buffers under the control of the RSB timebase. SBI_OE also places the TINDO output buffer under the control of TSB timebase. Inactive (low) forces SBI output buffers to a high-impedance state. Power-on and RESET [addr 001] force SBI_OE to an inactive state to avoid bus contention on devices that share system bus connections.

0 = SBI outputs forced to high-impedance state
1 = SBI outputs controlled by respective RSB or TSB timebase

EMF Embedded Framing—During T1 mode, EMF controls placement of T1 framing bits on RPCMO and the sampling of T1 framing bits from TPCMI. EMF supports system buses that carry T1 frames but operate above T1 line rate. EMF allows the system bus to transport and maintain 193-bit frame integrity while T1 data is passed through RSLIP and/or TSLIP buffers.

0 = G.802 embedded format
1 = Reserved

EMBED

EMBED instructs the transmit framer (refer to [TABORT; addr 071] to align TX timebase with respect to frame and multiframe alignment embedded in TXDATA, the transmit line rate data output from TSLIP. If TSLIP is enabled, EMBED is inactive, and overhead is bypassed, TX timebase is not guaranteed to align to TXDATA, and bypassed overhead cannot reliably pass through TSLIP. EMBED is applicable to all system bus modes.

EMBED	T1/E1N	Embedded Framing Mode
0	x	Transmit framer searches TPCMI
1	0	TS0 Embedded; search TXDATA
1	1	G.802; search TXDATA

NOTE(S): Embedded F-bits reach TX output only if frame formatter [TFRM; addr 072] is in Bypass or Transparent mode.

TS0 Embedded — The offline framer examines TXDATA to align TX timebase to the embedded FAS pattern. If MFAS is also enabled [TFRAME; addr 070], the transmit online framer examines TXDATA to align TX timebase to the embedded MFAS pattern. While EMBED is active, TXDATA output is monitored, and transmit frame errors are reported in ISR0 [addr 00B]. Embedded TS0 supports E1 overhead bypass options for applications where TSLIP buffer is enabled.

G.802 Embedded — Automatically supports *ITU–T Recommendation G.802*, which defines frame format conversion between T1 and E1 line rates by locating T1 F-bits in Bit 1 of time slot 26 of each system bus frame. G.802 embedded mode is applicable for system buses that are 1x, 2x, or 4x multiples of the E1 line rate. Full implementation of G.802 also requires the processor to program TS0, TS16, and TS26–TS31 as unassigned system bus time slots [SBCn; addr 0E0–0FF].

SBI[3:0]

System Bus Interface mode—Defines transmit and receive system bus data format. System buses operate in one of nine basic formats which differ in the number of total available data time slots and the associated system bus clock rate. If the total time slots are a multiple of 32, SBI also defines which bus group of 32 byte-interleaved time slots are assigned to the respective device.

SBI[3:0]	Mode	Clock (Kobe)	Total Time Slots	Bus Group
0000	128A	8192	128	Group 0
0001	128B	8192	128	Group 1
0010	128C	8192	128	Group 2
0011	128D	8192	128	Group 3
0100	64A	4096	64	Group 0
0101	64B	4096	64	Group 1
0110	32	2048	32	—
0111	24	1544	24 + F-bit	—
1000	24	1536	24	—

0D1—Receive System Bus Configuration (RSB_CR)

7	6	5	4	3	2	1	0
BUS_RSB	SIG_OFF	RPCM_NEG	RSYN_NEG	BUS_FRZ	RSB_CTR	RSBI[1]	RSBI[0]

BUS_RSB Enable Bussed RSB Outputs—Applicable only if the system bus outputs are controlled by SBI timebases [SBI_OE = 1; addr 0D0]. When BUS_RSB is active, RPCMO, RSIGO, and RINDO outputs from multiple devices are allowed to share common receive system bus connections. Unused time slots are three-stated during those bus groups not selected by SBI mode [addr 0D0]; otherwise, unused time slots repeat their output data value for all bus groups.

0 = RSB time slot value repeated for all bus groups
1 = three-state RSB outputs during unused bus groups

SIG_OFF Inhibit RPCMO Signaling Reinsertion—Disables insertion of ABCD signaling for all time slots on the receive system bus PCM output (RPCMO); otherwise, ABCD signaling is reinserted on RPCMO, as controlled by System Bus Per-Channel [SBCn; addr 0E0–0FF] and RX Per-Channel [RPCn; addr 180–19F] controls.

0 = enable insertion of signaling onto RPCMO
1 = inhibit RPCMO signaling

RPCM_NEG Output Data on Falling Edge Clock—Selects RSBCKI rising or falling edge clock signal to output RPCMO, RSIGO, RINDO, and SIGFRZ.

0 = RSB rising edge outputs
1 = RSB falling edge outputs

RSYN_NEG Output Sync on Falling Edge Clock—Selects RSBCKI rising or falling edge clock signal for RFSYNC or RMSYNC outputs. Opposite RSBCKI edge is used if RFSYNC or RMSYNC is programmed as input.

0 = RFSYNC or RMSYNC rising edge output (falling edge input)
1 = RFSYNC or RMSYNC falling edge output (rising edge input)

When RFSYNC or RMSYNC is an input and configured for rising edge sampling, RFSYNC or RMSYNC must be sampled low during the previous falling clock edge, then sampled high at the rising clock edge. (Refer to *Figure 5-5, SBI Timing: Setup and Hold Time for RFSYNC/RMSYNC and TFSYNC/TMSYNC Input Signals* and *Table 5-6, Input Data Setup and Hold Timing.)*

BUS_FRZ Enable Bused SIGFRZ Output—Enables SIGFRZ from multiple devices to share a common receive system bus connection. When active, SIGFRZ three-states during bus group time slots unused by the selected SBI mode [addr 0D0].

0 = SIGFRZ repeats for all bus groups
1 = three-state SIGFRZ during unused bus groups

RSB_CTR Force RSLIP to Center—Writing a one to RSB_CTR forces RSLIP read buffer pointer to its initial delay condition. If RFSYNC or RMSYNC is programmed as an output, RSB_CTR forces a change of system bus sync alignment. The processor must assert RSB_CTR after configuration of the receive slip buffer. Centering RSLIP does not effect RSLIP status reported in ISR.5 [addr 006]. RSB_CTR must be written to a 1, then to a 0. This bit is not self-clearing.

0 = no effect
1 = force RSLIP to center

RSBI[1:0] Receive Slip Buffer Interface mode—Selects configuration of RSLIP buffer. RSBI determines total buffer depth and initial delay conditions. While RSLIP is bypassed, RCKO clocks RSB outputs and RSBCKI is ignored. RFSYNC and RMSYNC are also ignored in Bypass mode if they are programmed as inputs. RFSYNC and RMSYNC must be programmed as outputs if RSB [1:0] selects either bypass or Elastic buffer mode.

RSBI	Mode	Total Depth	Initial Delay	Conditions
00	Normal	2 Frame	1 Frame	When RFSYNC is output
			0.5 to 1.5 Frames	When RFSYNC is input
01	Short	2 Frame	32 Bits	Reverts to normal upon slip
10	Elastic	64 Bits	32 Bits	Recenters automatically upon slip
11	Bypass	0 Bits	0 Bits	RSBCKI ignored

NOTE(S): To guarantee the pointer in the slip buffer is initialized properly during Elastic Mode, the following procedure can be applied:

1. Disable slip buffer — RSBI[1:0] = 11, RSB_CTR = 0
2. Center slip buffer — RSBI[1:0] = 11, RSB_CTR = 0
3. Set the slip buffer to Elastic Mode. — RSBI[1:0] = 10, RSB_CTR = 0

0D2—RSB Sync Bit Offset (RSYNC_BIT)

7	6	5	4	3	2	1	0
—	—	—	—	—	OFFSET[2]	OFFSET[1]	OFFSET[0]

OFFSET[2:0] RSB Sync Bit Offset—Selects which RSB bit number coincides with RFSYNC and RMSYNC sync pulses. Sync pulses are programmed to align to 1 bit in relation to RPCMO, RSIGO, RINDO, and SIGFRZ time slots. If the sync pulses are desired to coincide with location of T1 F-bit or time slot 0 Bit 1, OFFSET is programmed to equal 0. Sync bit offset is added to time slot offset [RSYNC_TS; addr 0D3] to form a 10-bit OFFSET value that applies to RFSYNC location, which is then added to frame offset [RSYNC_FRM; addr 0D8]. This forms a 15-bit OFFSET value that applies to the RMSYNC location. Both RFSYNC and RMSYNC offsets are expressed as RSB.OFFSET, allowing the system to generate or accept sync pulses at any bit location within the RSB multiframe.

OFFSET[2:0]	RSYNC Location
000	Bit 1 or F-bit
001	Bit 2
|	|
110	Bit 7
111	Bit 8

0D3—RSB Sync Time Slot Offset (RSYNC_TS)

7	6	5	4	3	2	1	0
—	OFFSET[9]	OFFSET[8]	OFFSET[7]	OFFSET[6]	OFFSET[5]	OFFSET[4]	OFFSET[3]

OFFSET[9:3] RSB Sync Time Slot Offset—Selects which RSB time slot number coincides with RFSYNC and RMSYNC sync pulses, in the range of time slots 0–127. If the sync pulses coincide with location of T1 F-bit or TS0, OFFSET is programmed to equal 0. Refer also to RSYNC_BIT and RSYNC_FRM [addr 0D2, 0D8].

2048, 1544, and 1536 kbps SBI Mode

OFFSET[9:3]	RSYNC Time Slot
0000000	0 or F-bit
0000001	1
|	|
0011110	30
0011111	31

4096 kbps SBI Mode

OFFSET[9:4]	OFFSET[3]	RSYNC Time Slot	Group
000000	0	0	A
000000	1	0	B
000001	0	1	A
000001	1	1	B
|	|	|	|
011110	0	30	A
011110	1	30	B
011111	0	31	A
011111	1	31	B

8192 kbps SBI Mode			
OFFSET[9:5]	OFFSET[4:3]	RSYNC Time Slot	Group
00000	00	0	A
00000	01	0	B
00000	10	0	C
00000	11	0	D
00001	00	1	A
00001	01	1	B
00001	10	1	C
00001	11	1	D
|	|	|	|
11110	00	30	A
11110	01	30	B
11110	10	30	C
11110	11	30	D
11111	00	31	A
11111	01	31	B
11111	10	31	C
11111	11	31	D

NOTE(S): Offsets outside the RSB timebase range result in no pulses on RFSYNC and RMSYNC outputs.

0D4—Transmit System Bus Configuration (TSB_CR)

7	6	5	4	3	2	1	0
BUS_TSB	TX_ALIGN	TPCM_NEG	TSYN_NEG	TSB_ALIGN	TSB_CTR	TSBI[1]	TSBI[0]

BUS_TSB Enable Bussed TSB Output—Applicable only if system bus outputs are controlled by SBI timebases [SBI_OE = 1; addr 0D0]. When BUS_TSB is active, TINDO outputs from multiple devices are allowed to share a common transmit system bus connection. Unused time slots are three-stated during bus groups not selected by SBI mode [addr 0D0]; otherwise, unused time slots repeat their TINDO value for all bus groups.

0 = TINDO repeated for all bus groups
1 = three-state TINDO during unused time slots

TX_ALIGN Transmitter Output Multiframe Aligns to TSB Timebase—Allows multiframe alignment located at TSB (from TMSYNC or TFRAMER) to pass across TSLIP buffer and force the corresponding multiframe alignment onto the transmitter timebase. Used primarily to pass TMSYNC from system bus.

0 = Transmitter multiframe does not follow TSB
1 = Transmitter multiframe follows TSB multiframe

TPCM_NEG Output Data on Falling Edge Clock—Selects TSBCKI rising or falling edge clock signal to output TINDO and the opposite TSBCKI edge to sample TPCMI and TSIGI inputs.

0 = TINDO rising edge output (TPCMI and TSIGI falling edge inputs)
1 = TINDO falling edge outputs (TPCMI and TSIGI rising edge inputs)

TSYN_NEG Output Sync on Falling Edge Clock—Selects TSBCKI rising or falling edge clock signal for TFSYNC or TMSYNC outputs. Opposite TSBCKI edge is used if TFSYNC or TMSYNC is programmed as input.

0 = TFSYNC or TMSYNC rising edge output (falling edge input)
1 = TFSYNC or TMSYNC falling edge output (rising edge input)

When TFSYNC or TMSYNC is an input and configured for rising edge sampling, TFSYNC or TMSYNC must be sampled low during the previous falling clock edge, then sampled high at the rising clock edge. (Refer to *Figure 5-5, SBI Timing: Setup and Hold Time for RFSYNC/RMSYNC and TFSYNC/TMSYNC Input Signals* and Table 5-6, *Input Data Setup and Hold Timing*.)

TSB_ALIGN Transmit System Bus Multiframe Aligns to Transmit Timebase—Allows multiframe alignment located at TX timebase to pass across TSLIP and forces the corresponding multiframe alignment onto the TSB timebase. Used primarily to pass CAS or MFAS alignment located by the transmit online framer onto the TMSYNC output.

0 = TSB multiframe does not follow XMTR
1 = TSB multiframe aligned by XMTR

TSB_CTR Force TSLIP to Center—Writing a 1 to TSB_CTR forces TSLIP read buffer pointer to its initial delay condition, possibly forcing a change of transmit frame alignment if TSLIP is configured in Elastic or Bypass modes. Writing a 0 has no effect. The processor must assert TSB_CTR after configuration of the transmit slip buffer, after which, Bt8370/8375/8376 automatically recenters TSLIP buffer according to the configured mode. Centering TSLIP does not effect TSLIP status reported in ISR5[addr 006].

0 = no effect
1 = force TSLIP to center

TSBI[1:0] Transmit Slip Buffer Interface mode—Selects the configuration of the TSLIP buffer. The TSBI determines the total buffer depth and initial delay conditions. While TSLIP is bypassed, TCKI clocks the TSB input/output, and TSBCKI is ignored.

TSBI	Mode	Total Depth	Initial Delay	Conditions
00	Normal	2 Frame	0.5 to 1.5 Frames	Dependent on present depth, no change of output frame.
01	Short	2 Frame	32 Bits	Reverts to normal upon slip
10	Elastic	64 Bits	32 Bits	Recenters automatically upon slip
11	Bypass	0 Bits	0 Bits	TSBCKI ignored

NOTE(S): Bypass requires system bus equal to line rate.

To guarantee the pointer is initialized properly in the slip buffer during Elastic Mode, the following procedure can be applied:

1. Disable Slip Buffer TSBI[1:0] = 11, TSB_CTR = 0
2. Center Slip Buffer TSBI[1:0] = 11, TSB_CTR = 1
3. Set the Slip Buffer to Elastic mode TSBI[1:0] = 10, TSB_CTR = 0

0D5—TSB Sync Bit Offset (TSYNC_BIT)

7	6	5	4	3	2	1	0
—	—	—	—	—	OFFSET[2]	OFFSET[1]	OFFSET[0]

OFFSET[2:0] TSB Sync Bit Offset—Selects which TSB bit number coincides with TFSYNC and TMSYNC sync pulses. Sync pulses are programmed to align to 1 bit in relation to TPCMI, TSIGI, and TINDO time slots. If the sync pulses are desired to coincide with location of T1 F-bit or time slot zero bit 1, OFFSET is programmed to equal 0. Sync bit offset is added to time slot offset [TSYNC_TS; addr 0D6] to form a 10-bit OFFSET value that applies to TFSYNC and TMSYNC location. Both TFSYNC and TMSYNC offsets are expressed as TSB.OFFSET, allowing the system to generate or accept sync pulses at any bit location within the TSB frame.

OFFSET[2:0]	TSYNC Location
000	Bit 1 or F-bit
001	Bit 2
|	|
110	Bit 7
111	Bit 8

0D6—TSB Sync Time Slot Offset (TSYNC_TS)

7	6	5	4	3	2	1	0
—	OFFSET[9]	OFFSET[8]	OFFSET[7]	OFFSET[6]	OFFSET[5]	OFFSET[4]	OFFSET[3]

OFFSET[9:3] TSB Sync Time Slot Offset—Selects which TSB time slot number coincides with TFSYNC and TMSYNC sync pulses, in the range of time slots 0–127. If the sync pulses coincide with location of T1 F-bit or TS0, OFFSET is programmed to equal 0.

2048, 1544, and 1536 kbps SBI Mode	
OFFSET[9:3]	TSYNC Time Slot
0000000	0 or F-bit
0000001	1
|	|
0011110	30
0011111	31

4096 kbps SBI Mode

OFFSET[9:4]	OFFSET[3]	TSYNC Time Slot	Group
000000	0	0	A
000000	1	0	B
000001	0	1	A
000001	1	1	B
|	|	|	|
011110	0	30	A
011110	1	30	B
011111	0	31	A
011111	1	31	B

8192 kbps SBI Mode

OFFSET[9:5]	OFFSET[4:3]	TSYNC Time Slot	Group
00000	00	0	A
00000	01	0	B
00000	10	0	C
00000	11	0	D
00001	00	1	A
00001	01	1	B
00001	10	1	C
00001	11	1	D
|	|	|	|
11110	00	30	A
11110	01	30	B
11110	10	30	C
11110	11	30	D
11111	00	31	A
11111	01	31	B
11111	10	31	C
11111	11	31	D

NOTE(S): Offsets outside the TSB timebase range result in no pulses on TFSYNC and TMSYNC outputs.

0D7—Receive Signaling Configuration (RSIG_CR)

7	6	5	4	3	2	1	0
—	SET_RSIG	SET_SIG	UNICODE	DEBOUNCE	FRZ_OFF	FRZ_ON	THRU

SET_RSIG Force RSIG Interrupt—Allows the processor to receive an interrupt on RSIG [addr 008] at every multiframe boundary. Applicable only to T1 mode. Overrides STACK interrupt.

0 = RSIG interrupt on signaling STACK change
1 = RSIG interrupts on T1 multiframe boundary

SET_SIG Overwrite Robbed-Bit Signaling—Applicable only during T1 mode and function dependent on RIDLE. When RIDLE is inactive, SET_SIG forces receive robbed-bit signaling to one before updating the RSLIP time slot value. Bit 8 of each time slot received during signaling frames 6, 12, 18, and 24 is replaced with a 1. This function is particularly useful in cross-connect and exchange systems that strip robbed-bit signaling, or in systems that use different signaling frame alignment on inbound and outbound ports.

0 = no change to receive signaling
1 = replace robbed-bit signaling

UNICODE Inband Signaling Freeze (applicable to T1 modes only)—If UNICODE is enabled, received ABCD signaling on all channels is searched on a per-channel basis for the 4-bit UNICODE pattern. UNICODE pattern detection inhibits STACK and RSIG buffer updates for that channel as long as UNICODE is present, but does not affect SIGFRZ output. It is not reported to the processor. This function is described in *Bellcore TR-TSY-000303, Section 4.4.9, Revision 2, July 1989*.

0 = no effect
1 = enable UNICODE detection and per-channel signaling freeze

DEBOUNCE Debounce Receive ABCD Signaling—Applicable only to those channels where the signaling stack is enabled (SIG_STK; addr 180–19F). The signaling buffer (RSIG) output updates for these channels are evaluated after D-bit signaling is received. New signaling is placed into RSIG and STACK buffers only if the RSIG input and output values differ. The DEBOUNCE function filters single bit errors in ABCD signaling by comparing incoming bits, buffered bits from the previous multiframe, and output bits on a bit-by-bit basis. A signaling error is detected if the new input signaling and current output signaling are the same but differ from the current buffered signaling. When this occurs, the current buffered signaling is rejected, and the output signaling does not change. Therefore, output signaling is updated only when the current buffered signaling and the input signaling are equal. At the end of each multiframe, the entire input ABCD value is copied to the output ABCD value.

0 = no effect
1 = debounce receive ABCD signaling

Signaling State During Current Multiframe			Signaling State Updated at the End of Current Multiframe		
New Input Signaling Bit	Buffered Input Signaling Bit from Previous Multiframe (RSIGn[3:0])	Buffered Output Signaling Bit (RSIGn[7:4])	Buffered Input Signaling Bit is Updated from Input Signaling Bit (RSIGn[3:0])	Buffered Output Signaling Bit (RSIGn[7:4])	Notes
0	0	0	0	0	
1	0	0	1	0	
1	1	0	1	1	Change Output
0	1	0	0	0	Debounce
1	1	1	1	1	
0	1	1	0	1	
0	0	1	0	0	Change Output
1	0	1	1	1	Debounce

NOTE(S): Non-Debounced signaling always transfers buffered ABCD input to buffered ABCD output coincident with the D-bit update.

FRZ_OFF/FRZ_ON Manual Signaling Update and SIGFRZ Output—Allows the processor to manually control updates of the receive signaling buffer [RSIGn; addr 1A0–1BF], the signaling stack [addr 0DA], and the SIGFRZ output pin. FRZ_ON and FRZ_OFF control the SIGFRZ pin's output state, but do not affect normal operations of the SIGFRZ interrupt [ISR7; addr 004]. The receive ABCD input signaling is placed into the STACK and RSIG buffers according to the modes shown below. Stack updates are individually enabled on a per-channel basis according to SIG_STK [addr 180–19F].

FRZ_ON	FRZ_OFF	SIG_STK	SIGFRZ Interrupt	SIGFRZ Pin	STACK	RSIGn
0	0	0	0	0	No update	All ABCD
0	0	X	1	1	No update	No update
0	0	1	0	0	ABCD Changes	All ABCD
X	1	0	X	0	No Update	All ABCD
X	1	1	X	0	ABCD Changes	All ABCD
1	0	X	X	1	No update	No Update

THRU Enable Transparent Robbed-Bit Signaling—RMSYNC is forced to align with respect to RX timebase and follow each change of receiver's multiframe alignment, plus any frame offset caused by RSLIP buffer delay. In this manner, RMSYNC is able to retain its signaling multiframe alignment with respect to RPCMO output data frames. THRU mode is required when RSLIP is configured in Bypass mode. It is also useful for ADPCM transcoder systems that utilize robbed-bit signaling during frames other than normal (modulo 6) signaling frames, and therefore cannot utilize RPCMO signaling reinsertion in ADPCM coded channels. During THRU mode, RMSYNC must be programmed as an output [PIO; addr 018]. RMSYNC can follow a change of RX multiframe alignment without generating an alarm indication (e.g., receiver change of SF alignment without accompanying loss of basic frame alignment).

0 = no effect

1 = transparent robbed-bit signaling

0D8—Signaling Reinsertion Frame Offset (RSYNC_FRM)

7	6	5	4	3	2	1	0
—	—	—	OFFSET[14]	OFFSET[13]	OFFSET[12]	OFFSET[11]	OFFSET[10]

OFFSET[14:10] RSB Sync Frame Offset—Selects which RSB frame number coincides with an RMSYNC pulse in the range of frame 0–23. OFFSET specifies the frame in which RMSYNC is applied as an input, or in which RMSYNC appears as an output—consequently locating RPCMO signaling frames used for T1 robbed-bit (frames 6,12,18, and 24), or E1 CAS signaling reinsertion. The only RPCMO channels affected are those with signaling insertion enabled [INSERT; addr 0E0–0FF].

T1/E1N	OFFSET[14:10]	RMSYNC Pulse
0	X0000	RSB Frame 0
0	X0001	RSB Frame 1
|	|	|
0	X1110	RSB Frame 14
0	X1111	RSB Frame 15
1	00000	RSB Frame 1
1	00001	RSB Frame 2
|	|	|
1	10110	RSB Frame 23
1	10111	RSB Frame 24

0D9—Slip Buffer Status (SSTAT)

SSTAT[7:0] is updated at the start of each respective receive/transmit internal frame boundary (i.e., 125 µs interval). Each bit in SSTAT is latched upon event detection and held until cleared by a processor read.

7	6	5	4	3	2	1	0
TSDIR	TFSLIP	TUSLIP	—	RSDIR	RFSLIP	RUSLIP	—

TSDIR Transmit Slip Direction—TSDIR is updated each time a TSLIP error is latched in TFSLIP, and TSDIR indicates which direction the slip occurred.

0 = TSLIP error deleted 1 frame on TX data output
1 = TSLIP error repeated 1 frame on TX data output

TFSLIP Controlled TSLIP Event—TUSLIP and TFSLIP event status are latched active-high when transmit slip error is detected. Either event reports a TSLIP error in ISR5 [addr 006]. Active-high hold interval is defined by LATCH_ERR [addr 046].

Two types of errors are detected:

1. FSLIP = Controlled ±frame slip on TX data output. FSLIP affects transmit time slot data, but does not change the transmit timebase or frame alignment.
2. USLIP = Uncontrolled ±1 to ±256 bit slip on TX data. USLIP affects both time slot data and frame alignment. TUSLIP and TFSLIP status depends on the transmit system bus configuration [TSB_CR; addr 0D4].

TSBI Mode	TUSLIP	TFSLIP	TSLIP Event
Normal	0	0	none
	0	1	FSLIP
	1	0	USLIP
	1	1[(1)]	Both FSLIP and USLIP
Short	0	0	none
	0	1	FSLIP
	1	0	USLIP
Elastic	0	N/A	none
	1	N/A	USLIP
Bypass	N/A	N/A	—

NOTE(S):

(1) Most recent slip error direction is reported in TSDIR.

2. TFSLIP not applicable (read zero value) if TSLIP bypassed or configured as elastic store. TUSLIP not applicable if TSLIP bypassed. In Short-Delay mode, if the bus clock is faster than the receive clock, the system bus resynchronizes and USLIP is be reported. If the receive clock is faster, RSLIP reverts to Normal mode and reports FSLIP errors.

TUSLIP Uncontrolled TSLIP Event—See TFSLIP description.

RSDIR Receive Slip Direction—RSDIR is updated each time an RSLIP error is latched in RFSLIP or RUSLIP, and indicates which direction the slip occurred.

0 = RSLIP error deleted 1 frame on RPCMO or SBI resync detected

1 = RSLIP error repeated 1 frame on RPCMO or SBI time slot reassigned

RFSLIP Controlled RSLIP Event—RUSLIP and RFSLIP event status are latched active-high when receive slip error is detected. Either event reports RSLIP error in ISR5 [addr 006]. Active-high hold interval is defined by LATCH_ERR [addr 046]. Two types of errors are detected:

1. FSLIP = Controlled ±1 frame slip on RPCMO data output. FSLIP affects RPCMO, but does not change the alignment of system bus RFSYNC or RMSYNC signals.
2. USLIP = Uncontrolled ±1 to ±256 bit slip on RPCMO. USLIP affects both system bus data and sync outputs. RUSLIP and RFSLIP status depends on the receive system bus configuration [RSB_CR; addr 0D1].

RSBI Mode	RUSLIP	RFSLIP	RSLIP Event	Notes
Normal	0	0	none	—
	0	1	FSLIP	Most recent slip error direction is reported in RSDIR.
	1	0	USLIP	An uncontrolled slip can occur in Normal mode due to a resync of the SBI or, in T1 rate converted applications, the active time slots are reassigned. The former sets RSDIR = 0; the latter sets RSDIR = 1.
Short	0	0	none	—
	0	1	FSLIP	—
	1	0	USLIP	In Short-Delay mode, if the bus clock is faster than receive clock, the system bus resynchronizes and USLIP is reported. If the receive clock is faster, RSLIP reverts to Normal mode and reports FSLIP errors.
Elastic	0	0	none	—
	1	0	USLIP	RFSLIP is not applicable (read zero value) while the RSLIP buffer is bypassed or configured as elastic store. FSLIP or USLIP errors reported upon Bypass mode initialization should be ignored.
Bypass	—	—	—	—

RUSLIP Uncontrolled RSLIP Event—See RFSLIP description.

0DA—Receive Signaling Stack (STACK)

STACK contains new signaling information from those channels with SIG_STK [addr 180–19F] enabled. STACK allows the processor to monitor only changed ABCD signaling values from the selected channels. RSIG interrupt [addr 008] is triggered at the end of any multiframe where one or more ABCD signaling values have changed. The processor reads the STACK address twice to retrieve the channel number (Word 0) and to retrieve the new ABCD value (Word 1). The processor continues to read from STACK until empty. An empty Stack is indicated when either MORE = 0 in Word 1 or no Word 1 exists (the last two STACK reads are Word 0).

Internal STACK read/write pointers are initialized by RESET [addr 001]. STACK contents are updated for each channel in which the stack is enabled [SIG_STK; addr 180–19F]. STACK contents are updated with new output signaling if the buffered RSIGn input and output ABCD signaling values differ. STACK is evaluated on a channel-by-channel basis after the D-bit is updated. The processor must poll the RSIG interrupt to determine when STACK has new information.

Word 0: Channel Number (first read)

7	6	5	4	3	2	1	0
WORD	MORE	—	CH[4]	CH[3]	CH[2]	CH[1]	CH[0]

WORD Stack Word ID (always 0 in Word 0)

MORE More Stack Contents (always 1 in Word 0)

CH[4:0] Channel Number (E1 range 0–31; T1 range 1–24)

Word 1: New Signaling Value (second read)

7	6	5	4	3	2	1	0
WORD	MORE	—	—	SIG_BITA	SIG_BITB	SIG_BITC	SIG_BITD

WORD Stack Word ID (always 1 in Word 1)

WORD	MORE	MPU Response
0	0	First word, get channel
0	1	Never used
1	0	No change or last change, stop
1	1	New signaling, keep reading

MORE More Stack Contents equals 1 if more available.

SIG_BITA–D Signaling Bit A–D—Processor reads new ABCD signaling value from this location. The ABCD value is also present in RSIGn (addr 1A0–1BF) output signaling buffer, so the processor need not store a local copy of each channel's signaling status.

0DB—RSLIP Phase Status (RPHASE)

7	6	5	4	3	2	1	0
RDELAY[5]	RDELAY[4]	RDELAY[3]	RDELAY[2]	RDELAY[1]	RDELAY[0]	RSLIP_WR	RSLIP_RD

RDELAY[5:0] RSLIP Buffer Delay—The difference between the RX and RSB timebase in time slot intervals, reported once per frame, coincident with RFRAME interrupt [ISR3; addr 008]. Actual delay may vary significantly, depending on which time slots are assigned.

000000 = RX to RSB delay in the range of 0–7 bits
|
111111 = RX to RSB delay in the range of 504–511 bits

RSLIP_RD Active Receiver Slip Buffer Half—Indicates which half of the receive slip buffer is currently receiving data from the receiver (0 = RSLIP_LO, 1 = RSLIP_HI). The processor can read data from the opposite buffer half.

RSLIP_WR Active RSB Slip Buffer Half—Indicates which half of the receive slip buffer is currently supplying data to the Receive System Bus (0 = RSLIP_LO, 1 = RSLIP_HI). The processor can write data to the opposite buffer half.

0DC—TSLIP Phase Status (TPHASE)

7	6	5	4	3	2	1	0
TDELAY[5]	TDELAY[4]	TDELAY[3]	TDELAY[2]	TDELAY[1]	TDELAY[0]	TSLIP_WR	TSLIP_RD

TDELAY[5:0] TSLIP Buffer Delay—The difference between the TSB and TX timebase in time slot intervals, reported once per frame, coincident with the TFRAME interrupt [ISR3; addr 008]. The actual delay may vary significantly, depending on which time slots are assigned.

000000 = TSB to TX delay in the range of 0–7 bits
|
111111 = TSB to TX delay in the range of 496–503 bits

TSLIP_WR Active Transmitter Slip Buffer Half—Indicates which half of the transmit slip buffer is currently supplying data to the transmitter (0 = TSLIP_LO, 1 = TSLIP_HI). The processor can write data to the opposite buffer half.

TSLIP_RD Active TSB Slip Buffer Half—Indicates which half of the transmit slip buffer is currently receiving data from the Transmit System Bus (0 = TSLIP_LO, 1 = TSLIP_HI). The processor can read data from the opposite buffer half.

0DD—RAM Parity Status (PERR)

All Bt8370/8375/8376 system bus data, signaling, and controls are transferred through a set of internal RAMs with parity error detection capabilities. Any parity error detected during RAM access is reported in PERR. Each error event is latched active-high and held until the processor read clears PERR. Parity errors are indicative of system clock glitches (REFCKI, TSBCKI, or RSBCKI), a failing or excessively noisy power supply, or general circuit failure.

7	6	5	4	3	2	1	0
—	—	—	—	—	PERR_TPC	PERR_RPC	PERR_SBC

PERR_TPC TPC (Transmit) RAM Parity Error

PERR_RPC RPC (Receive) RAM Parity Error

PERR_SBC SBC (Control) RAM Parity Error

0E0–0FF—System Bus Per-Channel Control (SBCn; n = 0 to 31)

7	6	5	4	3	2	1	0
—	INSERT	SIG_LP	RLOOP	RINDO	TINDO	TSIG_AB	ASSIGN

INSERT Insert RX Signaling on RPCMO—Enables per-channel signaling insertion on RPCMO output, where ABCD signaling is supplied by RLOCAL signaling (RPCn; addr 180–19F) or buffered signaling [RSIGn; addr 1A0–IBF]. INSERT is a lower priority than no signaling (SIG_OFF; addr 0D1). RSB signaling frame locations are specified by RMSYNC signal in conjunction with the programmed frame offset [OFFSET; addr 0D8].

SIG_OFF	INSERT	RLOCAL	RPCMO Inserted Signal
1	X	X	None
0	1	0	ABCD from RSIGn output buffer
0	1	1	ABCD from RPCn local buffer

SIG_LP Local Signaling Loopback—Instructs the receiver output signaling on RSIGO to be supplied from TSIGn buffer contents. Signaling in RPCMO (T1-robbed bit or E1-CAS) is not affected.
0 = normal
1 = local signaling loopback

RLOOP Local Loopback—RPCMO output data supplied from TSLIP buffer contents.
0 = normal
1 = local loopback

RINDO Activate RINDO Time Slot Indicator—Receive system bus time slots are individually marked (active-high for 8 bits) by RINDO. SBI_OE (addr 0D0) overrides RINDO.
0 = RINDO signal inactive (low)
1 = RINDO signal active (high)

TINDO Activate TINDO Time Slot Indicator—Transmit system bus time slots are individually marked (active-high for 8 bits) by TINDO.
0 = TINDO inactive
1 = TINDO active

TSIG_AB TSIG_AB—AB Signaling. In T1 mode, only AB signaling bits are updated from TSIGI to the TSIGn buffer. If SIGFRZ is active, the output CD signaling bits are copied from the buffered output AB bits, respectively. In E1 mode, setting TSIG_AB forces C = 0 and D = 1 when updating the TSIGn buffer.

0 = ABCD Signaling
1 = AB Signaling

ASSIGN Assign System Bus Time Slot—During T1 line applications where the system bus group consists of 32 time slots, or a multiple of 32, any 24 out of 32 time slots can be assigned. The only time SBC [1:24] must be assigned is during 1536K or 1544K bus modes. The number of assigned system bus time slots must equal the number of line time slots; therefore, ASSIGN must be active in all 32 SBCn locations during E1 modes. The receiver does not update unassigned time slots as it fills the RSLIP buffer. T1 time slots are filled sequentially from RSLIP 1 to 24. Time slots 0 and 25 to 31 are reserved for unassigned values. Values are read from either assigned or unassigned locations in a sequential fashion based on the ASSIGN bit. System bus output data for unassigned time slots is taken from the RSLIP buffer, which the processor can fill with any desired 16-bit fixed value (8 bits in RSLIP_LO, plus 8 bits in RSLIP_HI).

0 = unassigned system bus time slot
1 = assigned system bus time slot

100–11F—Transmit Per-Channel Control (TPCn; n = 0 to 31)

7	6	5	4	3	2	1	0
TB7ZS/EMFBIT	TLOOP	TIDLE	TLOCAL	TSIGA/TSIGO	TSIGB/RSIGO	TSIGC	TSIGD

TB7ZS/EMFBIT Bit 7 Zero Code Substitution/Embedded F-bit Value (Applicable in T1 mode only)—For assigned system bus time slots [ASSIGN; addr 0E0-0FF], TB7ZS replaces bit 7 of the time slot with a one if examination of 8-bit output detects all zeros. For an unassigned time slot where TIDLE is active, EMFBIT replaces all embedded F-bit outputs with the programmed EMFBIT value.

0 = no effect or force embedded F-bit (low)
1 = enable B7ZS or force embedded F-bit (high)

TLOOP Remote DS0 Channel Loopback—Transmits data supplied from RSLIP buffer contents. TLOOP works in conjunction with other TPCn control bits to select the source of transmitted data and signaling (see Table 3-23).

Table 3-23. Remote DS0 Channel Loopback

TLOOP	TIDLE	TLOCAL	TSIGO	RSIGO	Sig Source	Data Source	Channel Mode
0	0	0	0	0	None	TPCMI	Clear Channel
0	0	0	0	1	RSIGn	TPCMI	Rx Signaling
0	0	0	1	0	TSIGn	TPCMI	Tx Signaling
0	0	1	X	X	TSIGA–D	TPCMI	Local Signaling
0	1	0	0	0	None	TSLIP_LO	Idle Code
0	1	0	0	1	RSIGn	TSLIP_LO	Idle Code Rx Signaling
0	1	0	1	0	TSIGn	TSLIP_LO	Idle Code Tx Signaling
0	1	1	X	X	TSIGA–D	TSLIP_LO	Idle Code Local Signaling
1	X	0	0	0	None	RXDATA	Remote Loop
1	X	0	0	1	RSIGn	RXDATA	Remote Loop Rx Signaling
1	X	0	1	0	TSIGn	RXDATA	Remote Loop Tx Signaling
1	X	1	X	X	TSIGA–D	RXDATA	Remote Loop Local Signaling

NOTE(S): If RX Signaling, RSIGn output buffer supplies transmit signaling.

TIDLE Transmit Idle—Transmit data supplied from TSLIP_LO buffer contents. The processor writes an 8-bit idle pattern to TSLIP_LO for output on the selected time slot, or optionally writes real-time data output to TSLIP_LO after each TFRAME interrupt [ISR3; addr 008]. Only TSLIP_HI buffer is updated from TPCMI to allow continued local DS0 channel loopback.

0 = normal data output
1 = transmit idle data output

TLOCAL Transmit Local Signaling—When active, TLOCAL transmits TSIGA–TSIGD values in output ABCD signaling bits.

0 = TSIGO or RSIGO control output signaling
1 = transmit signaling from TSIGA–TSIGD

In E1, when it is attempted to merge signaling embedded in the TPCMI datastream with signaling inserting by TLOCAL [TPCn; addr 100-11F], the signaling inserted by TLOCAL appears two time slots early with TX_ALIGN bit set in [TSB_CR; addr 0D4]. Therefore, signaling intended for TS1 would instead be inserted into TS31. TX_ALIGN needs to be set. This offset does not occur during local signaling insertion for all 32 time slots. In T1, transmitting local signaling should be synchronized with Transmit Multiframe interrupt [TMF_IER3; addr 010]. This would avoid transmitting intermediate values.

TSIGA–TSIGD Transmit Local Signaling—Holds the 4-bit ABCD signaling value, which is output when TLOCAL is active. In AB only applications, such as T1/SF framing, TSIGC and TSIGD must also be written with the same data as TSIGA and TSIGB. In E1 modes, TS0 and TS16 local signaling value determines CAS multiframe alignment signal (MAS) and XYXX output.

TSIGO Transmit Signaling Output—Applicable only if TLOCAL is inactive. ABCD signaling from TSIGn buffer is transmitted.

0 = no effect
1 = transmit signaling from TSIGn buffer

RSIGO Receive Signaling Output—Applicable only if TLOCAL is inactive. Forces transmit ABCD signaling to be supplied from RSIGn buffer, affecting a remote signaling loopback.

0 = no effect
1 = transmit signaling from RSIGn buffer

120–13F—Transmit Signaling Buffer (TSIGn; n = 0 to 31)

Transmit signaling from the TSIGI pin is automatically placed into the TSIGn buffer. The processor controls TSIGn insertion into the transmitter output by selecting TSIGO [in TPCn]. The processor can monitor TSIGn from system supplied signaling or use TSIGn for inter-processor communication. During E1 modes, TSIG0 and TSIG16 buffer locations hold the CAS multiframe alignment signal (MAS.1 through MAS.4), extra bits (X.1 through X.4), and multiframe Yellow Alarm (MYEL) bits supplied from TSIGI.

7	6	5	4	3	2	1	0
—	—	—	—	TSIGn[3]	TSIGn[2]	TSIGn[1]	TSIGn[0]

		TSIG0 (E1)	TSIG16 (E1 mode)
TSIGn.3	Input Signaling A Bit	MAS.1	X.1
TSIGn.2	Input Signaling B Bit	MAS.2	MYEL
TSIGn.1	Input Signaling C Bit	MAS.3	X.3
TSIGn.0	Input Signaling D Bit	MAS.4	X.4

140–15F—Transmit PCM Slip Buffer (TSLIP_LOn; n = 0 to 31)

7	6	5	4	3	2	1	0
TPCM[1]	TPCM[2]	TPCM[3]	TPCM[4]	TPCM[5]	TPCM[6]	TPCM[7]	TPCM[8]

TPCM[1] First bit

TPCM[2] Second bit

TPCM[3] Third bit

TPCM[4] Fourth bit

TPCM[5] Fifth bit

TPCM[6] Sixth bit

TPCM[7] Seventh bit

TPCM[8] Eighth bit received on TPCMI

160–17F—Transmit PCM Slip Buffer (TSLIP_HIn; n = 0 to 31)

7	6	5	4	3	2	1	0
TPCM[1]	TPCM[2]	TPCM[3]	TPCM[4]	TPCM[5]	TPCM[6]	TPCM[7]	TPCM[8]

TPCM[1] First bit

TPCM[2] Second bit

TPCM[3] Third bit

TPCM[4] Fourth bit

TPCM[5] Fifth bit

TPCM[6] Sixth bit

TPCM[7] Seventh bit

TPCM[8] Eighth bit received on TPCMI

180–19F—Receive Per-Channel Control (RPCn; n = 0 to 31)

7	6	5	4	3	2	1	0
RSIG_AB/ EMFBIT	RIDLE	SIG_STK	RLOCAL	RSIGA	RSIGB	RSIGC	RSIGD

RSIG_AB/EMFBIT AB Signaling (Per-Channel RSIG_AB [without DEBOUNCE])—In E1 mode, received signaling is placed into RSIGn, but RSIGO output duplicates the buffered AB bit value in the CD output bits, thus sending ABAB on RSIGO instead of ABCD. In T1 mode, RSIG_AB instructs the receiver to use the available RSIGn buffer space to meet PUB43801 and TR-170—which require three SF multiframes of receive signaling buffer storage before output. Every 24 frames, the received ABCD signaling value is transferred from the RSIGn input buffer space to the RSIGn output buffer space, regardless of whether the receiver operates in SF, SLC, or ESF mode. In SF mode, the ABCD value contains AB = AB(N–1), and CD = AB(N) from two multiframes. Since multiframe N–1 is the older sample, AB(N–1) replaces AB(N) in the event of signaling freeze. RSIGO and RPCMO signaling bit output values are always taken from RSIGn output buffer according to RSB frame number.

0 = normal ABCD and embedded F-bit throughput
1 = AB signaling and embedded F-bit replacement

AB Signaling (Per-Channel RSIG_AB [with DEBOUNCE])—Debounce affects RSIGn input buffer update mechanism by comparing—on a bit-by-bit basis—the present received input signaling bit value with the current buffered signaling bit values from two prior multiframes. If signaling from prior multiframe (N) differs from input and input equals buffered value from two multiframes prior (N–1), the signaling bit value from multiframe N is inverted when the input buffer is updated.

Sig Input	Buffer N, N-1	Update N, N-1	Notes
0	00	00	—
0	01	00	Change Update
0	10	00	Debounce
0	11	01	—
1	00	10	—
1	01	11	Debounce
1	10	11	Change Update
1	11	11	—

When RIDLE is active in an unassigned time slot defined to carry embedded F-bits, EMFBIT replaces all embedded F-bit outputs on RPCMO with the programmed value.

RIDLE Time Slot Idle—When RIDLE is active, the incoming RX time slot data is only updated in RSLIP_HIn buffer, and the RSB time slot data output is only extracted from RSLIP_LOn buffer. Thus, the processor can write an 8-bit idle code pattern in RSLIP_LOn buffer for output during RSB time slot.

0 = no effect
1 = RSB time slot replaced by contents of RSLIP_LOn

SIG_STK Receive Signaling Stack—Selects whether changes detected in the ABCD signaling value are reported in the signaling stack [addr 0DA]. Signaling for all time slots is continuously updated in RSIGn buffer, regardless of the SIG_STK setting.

0 = no effect
1 = signaling stack

RLOCAL Enable Local Signaling Output—Determines whether the RSIGO output signaling and RPCMO inserted signaling [INSERT; addr 0E0-0FF] are supplied from the RSIGn output buffer or processor-supplied local signaling from RSIGA–RSIGD.

0 = RSIGn buffer signaling
1 = RSIGA-RSIGD local signaling

RSIGA–RSIGD Local Receive Signaling—When RLOCAL is active, these four bits are inserted into RSIGO instead of the buffered signaling from RSIGn. If both RLOCAL and INSERT are active, they are also inserted into RPCMO during system bus signaling frames.

0 = output signaling bit equals 0
1 = output signaling bit equals 1

1A0–1BF—Receive Signaling Buffer (RSIGn; n = 0 to 31)

The Receive Signaling Buffer (RSIGn) contains all ABCD signaling inputs from all channels, regardless of whether signaling is active [SIG_STK; addr 180–19F]. RSIGn is not updated during signaling freeze conditions, or when the receive framer is configured in a non-signaling mode. Normal signaling buffer operation transfers ABCD input to ABCD output, coincident with the D-bit update (in T1 mode), or coincident with the receipt of the respective channel's ABCD signaling during TS16 (in E1 mode). When DEBOUNCE is active, output signaling for active channels is updated coincident with the sampling of each input signaling bit. This may cause the buffered output value to transition in the middle of the received multiframe.

7	6	5	4	3	2	1	0
RSIGn[7]	RSIGn[6]	RSIGn[5]	RSIGn[4]	RSIGn[3]	RSIGn[2]	RSIGn[1]	RSIGn[0]

RSIGn[7] Output Signaling A Bit

RSIGn[6] Output Signaling B Bit

RSIGn[5] Output Signaling C Bit

RSIGn[4] Output Signaling D Bit

		RSIG0 (E1)	RSIG16 (E1 Mode)
RSIGn[3]	Input Signaling A Bit	MAS.1	X.1
RSIGn[2]	Input Signaling B Bit	MAS.2	MYEL
RSIGn[1]	Input Signaling C Bit	MAS.3	X.3
RSIGn[0]	Input Signaling D Bit	MAS.4	X.4

1C0–1DF—Receive PCM Slip Buffer (RSLIP_LOn; n = 0 to 31)

7	6	5	4	3	2	1	0
RPCM[1]	RPCM[2]	RPCM[3]	RPCM[4]	RPCM[5]	RPCM[6]	RPCM[7]	RPCM[8]

RPCM[1] First bit

RPCM[2] Second bit

RPCM[3] Third bit

RPCM[4] Fourth bit

RPCM[5] Fifth bit

RPCM[6] Sixth bit

RPCM[7] Seventh bit

RPCM[8] Eighth bit received from receiver

1E0–1FF—Receive PCM Slip Buffer (RSLIP_HIn; n = 0 to 31)

7	6	5	4	3	2	1	0
RPCM[1]	RPCM[2]	RPCM[3]	RPCM[4]	RPCM[5]	RPCM[6]	RPCM[7]	RPCM[8]

RPCM[1] First bit

RPCM[2] Second bit

RPCM[3] Third bit

RPCM[4] Fourth bit

RPCM[5] Fifth bit

RPCM[6] Sixth bit

RPCM[7] Seventh bit

RPCM[8] Eighth bit received from receiver

3.18 Register Summary

Table 3-24. Global Control and Status Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
000	DID	R	DID[7]	DID[6]	DID[5]	DID[4]	DID[3]	DID[2]	DID[1]	DID[0]
001	CR0	R/W	RESET	—	—	RFRAME[3]	RFRAME[2]	RFRAME[1]	RFRAME[0]	T1/E1N
002	JAT_CR	R/W	JEN	JFREE	JDIR	JAUTO	JCENTER	JSIZE[2]	JSIZE[1]	JSIZE[0]

Table 3-25. Interrupt Request Register

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
003	IRR	R	ALARM1	ALARM2	ERROR	COUNT	TIMER	DL1	DL2	PATT

Table 3-26. Interrupt Status Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
004	ISR7	R	RMYEL	RYEL	RPDV	RAIS	RALOS	RLOS	RLOF	SIGFRZ
005	ISR6	R	LOOPDN	LOOPUP	TPDV	TSHORT	TLOC	—	TLOF	ONESEC
006	ISR5	R	TSLIP	RSLIP	CKERR	JERR	CERR	SERR	MERR	FERR
007	ISR4	R	FRED[4]	COFA[2]	SEF[2]	BERR[12]	FEBE[10]	LCV[16]	CRC[10]	FERR[12]
008	ISR3	R	TSIG	TMSYNC	TMF	TFRAME	RSIG	RMSYNC	RMF	RFRAME
009	ISR2	R	TBOP	RFULL1	RNEAR1	RMSG1	TDLERR1	TEMPTY1	TNEAR1	TMSG1
00A	ISR1	R	RBOP	RFULL2	RNEAR2	RMSG2	TDLERR2	TEMPTY2	TNEAR2	TMSG2
00B	ISR0	R	—	—	BSLIP	PSYNC	TCERR	TSERR	TMERR	TFERR

Table 3-27. Interrupt Enable Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
00C	IER7	R/W	RMYEL	RYEL	RPDV	RAIS	RALOS	RLOS	RLOF	SIGFRZ
00D	IER6	R/W	LOOPDN	LOOPUP	TPDV	TSHORT	TLOC	—	TLOF	ONESEC
00E	IER5	R/W	TSLIP	RSLIP	CKERR	JERR	CERR	SERR	MERR	FERR
00F	IER4	R/W	LOF	COFA	SEF	BERR	FEBE	LCV	CRC	FERR
010	IER3	R/W	TSIG	TMSYNC	TMF	TFRAME	RSIG	RMSYNC	RMF	RFRAME
011	IER2	R/W	TBOP	RFULL1	RNEAR1	RMSG1	TDLERR1	TEMPTY1	TNEAR1	TMSG1
012	IER1	R/W	RBOP	RFULL2	RNEAR2	RMSG2	RDLERR2	TEMPTY2	TNEAR2	TMSG2
013	IER0	R/W	—	—	BSLIP	PSYNC	TCERR	TSERR	TMERR	TFERR

Table 3-28. Primary Control and Status Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
014	LOOP	R/W	—	—	—	—	PLOOP	LLOOP	FLOOP	ALOOP
015	DL3_TS	R/W	DL3EN	FS[1]	FS[0]	TS[4]	TS[3]	TS[2]	TS[1]	TS[0]
016	DL3_BIT	R/W	DL3_BIT[7]	DL3_BIT[6]	DL3_BIT[5]	DL3_BIT[4]	DL3_BIT[3]	DL3_BIT[2]	DL3_BIT[1]	DL3_BIT[0]
017	FSTAT	R	—	—	—	INVALID	FOUND	TIMEOUT	ACTIVE	RX/TXN
018	PIO	R/W	ONESEC_IO	RDL_IO	TDL_IO	INDY_IO	RFSYNC_IO	RMSYNC_IO	TFSYNC_IO	TMSYNC_IO
019	POE	R/W	—	—	TDL_OE	RDL_OE	INDY_OE	TCKO_OE	CLADO_OE	RCKO_OE
01A	CMUX	R/W	RSBCKI[1]	RSBCKI[0]	TSBCKI[1]	TSBCKI[0]	CLADI[1]	CLADI[0]	TCKI[1]	TCKI[0]
01B	TMUX	R/W	—	—	TMUX[5]	TMUX[4]	TMUX[3]	TMUX[2]	TMUX[1]	TMUX[0]
01C	TEST	R/W	—	—	—	—	—	—	TEST[1]	TEST[0]

Table 3-29. Receive LIU Registers *(1 of 2)*

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
020	LIU_CR	R/W	RST_LIU	SQUELCH	FORCE_VGA	RDIGI	ATTN[1]	ATTN[0]	—	1
021	RSTAT	R	CPDERR	JMPTY	ZCSUB	EXZ	BPV	—	EYEOPEN	PRE_EQ
022	RLIU_CR	R/W	FRZ_SHORT	HI_CSLICE	AGC[1]	AGC[0]	EQ_FRZ	OOR_BLOCK	RLB0	LONG_EYE
023	LPF	R/W	—	LPF[6]	LPF[5]	LPF[4]	LPF[3]	LPF[2]	LPF[1]	LPF[0]
024	VGA_MAX	R/W	—	—	VGA_MAX[5]	VGA_MAX[4]	VGA_MAX[3]	VGA_MAX[2]	VGA_MAX[1]	VGA_MAX[0]
025	EQ_DAT	R/W	EQ_DAT[7]	EQ_DAT[6]	EQ_DAT[5]	EQ_DAT[4]	EQ_DAT[3]	EQ_DAT[2]	EQ_DAT[1]	EQ_DAT[0]
026	EQ_PTR	R/W	—	—	EQ_PTR[5]	EQ_PTR[4]	EQ_PTR[3]	EQ_PTR[2]	EQ_PTR[1]	EQ_PTR[0]

***Table 3-29. Receive LIU Registers** (2 of 2)*

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
027	DSLICE	R/W	DSLICE[7]	DSLICE[6]	DSLICE[5]	DSLICE[4]	DSLICE[3]	DSLICE[2]	DSLICE[1]	DSLICE[0]
028	EQ_OUT	R/W	EQOUT[7]	EQOUT[6]	EQOUT[5]	EQOUT[4]	EQOUT[3]	EQOUT[2]	EQOUT[1]	EQOUT[0]
029	VGA	R	—	—	VGA[5]	VGA[4]	VGA[3]	VGA[2]	VGA[1]	VGA[0]
02A	PRE_EQ	R/W	FORCE	ON	VTHRESH[5]	VTHRESH[4]	VTHRESH[3]	VTHRESH[2]	VTHRESH[1]	VTHRESH[0]
030–037	COEFF	R	COEFF[7]	COEFF[6]	COEFF[5]	COEFF[4]	COEFF[3]	COEFF[2]	COEFF[1]	COEFF[0]
038–03C	GAIN	R/W	—	—	—	GAIN[4]	GAIN[3]	GAIN[2]	GAIN[1]	GAIN[0]

Table 3-30. Receiver Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
040	RCR0	R/W	RAMI	RABORT	RFORCE	RLOFD	RLOFC	RLOFB	RLOFA	RZCS
041	RPATT	R/W	—	—	RESEED	BSTART	FRAMED	ZLIMIT	RPATT[1]	RPATT[0]
042	RLB	R/W	—	—	—	—	DN_LEN[1]	DN_LEN[0]	UP_LEN[1]	UP_LEN[0]
043	LBA	R/W	LBA[1]	LBA[2]	LBA[3]	LBA[4]	LBA[5]	LBA[6]	LBA[7]	—
044	LBD	R/W	LBD[1]	LBD[2]	LBD[3]	LBD[4]	LBD[5]	LBD[6]	LBD[7]	—
045	RALM	R/W	—	—	FS_NFAS	EXZ_LCV	YEL_INTEG	RLOF_INTEG	0	RPCM_AIS
046	LATCH	R/W	—	—	—	—	STOP_CNT	LATCH_CNT	LATCH_ERR	LATCH_ALM
047	ALM1	R	RMYEL	RYEL	—	RAIS	RALOS	RLOS	RLOF	SIGFRZ
048	ALM2	R	LOOPDN	LOOPUP	—	TSHORT	TLOC	—	TLOF	—
049	ALM3	R	—	RMAIS	SEF	SRED	MRED	FRED	LOF[1]	LOF[0]

Table 3-31. Performance Monitoring Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
050	FERR	R	FERR[7]	FERR[6]	FERR[5]	FERR[4]	FERR[3]	FERR[2]	FERR[1]	FERR[0]
051	FERR	R	0	0	0	0	FERR[11]	FERR[10]	FERR[9]	FERR[8]
052	CERR	R	CERR[7]	CERR[6]	CERR[5]	CERR[4]	CERR[3]	CERR[2]	CERR[1]	CERR[0]
053	CERR	R	0	0	0	0	0	0	CERR[9]	CERR[8]
054	LCV	R	LCV[7]	LCV[6]	LCV[5]	LCV[4]	LCV[3]	LCV[2]	LCV[1]	LCV[0]
055	LCV	R	LCV[15]	LCV[14]	LCV[13]	LCV[12]	LCV[11]	LCV[10]	LCV[9]	LCV[8]
056	FEBE	R	FEBE[7]	FEBE[6]	FEBE[5]	FEBE[4]	FEBE[3]	FEBE[2]	FEBE[1]	FEBE[0]
057	FEBE	R	0	0	0	0	0	0	FEBE[9]	FEBE[8]
058	BERR	R	BERR[7]	BERR[6]	BERR[5]	BERR[4]	BERR[3]	BERR[2]	BERR[1]	BERR[0]
059	BERR	R	0	0	0	0	BERR[11]	BERR[10]	BERR[9]	BERR[8]
05A	AERR	R	FRED[3]	FRED[2]	FRED[1]	FRED[0]	COFA[1]	COFA[0]	SEF[1]	SEF[0]

Table 3-32. Receive Sa-Byte Buffers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
05B	RSA4	R	RSA4[7]	RSA4[6]	RSA4[5]	RSA4[4]	RSA4[3]	RSA4[2]	RSA4[1]	RSA4[0]
05C	RSA5	R	RSA5[7]	RSA5[6]	RSA5[5]	RSA5[4]	RSA5[3]	RSA5[2]	RSA5[1]	RSA5[0]
05D	RSA6	R	RSA6[7]	RSA6[6]	RSA6[5]	RSA6[4]	RSA6[3]	RSA6[2]	RSA6[1]	RSA6[0]
05E	RSA7	R	RSA7[7]	RSA7[6]	RSA7[5]	RSA7[4]	RSA7[3]	RSA7[2]	RSA7[1]	RSA7[0]
05F	RSA8	R	RSA8[7]	RSA8[6]	RSA8[5]	RSA8[4]	RSA8[3]	RSA8[2]	RSA8[1]	RSA8[0]

Table 3-33. Transmit LIU Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
060–067	SHAPE	R/W	—	—	SHAPE[5]	SHAPE[4]	SHAPE[3]	SHAPE[2]	SHAPE[1]	SHAPE[0]
068	TLIU_CR	R/W	TURNS	TERM	LBO[1]	LBO[0]	PULSE[2]	PULSE[1]	PULSE[0]	AISCLK

Table 3-34. Transmitter Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
070	TCR0	R/W	—	—	—	—	TFRAME[3]	TFRAME[2]	TFRAME[1]	TFRAME[0]
071	TCR1	R/W	TNRZ	TABORT	TFORCE	TLOFC	TLOFB	TLOFA	TZCS[1]	TZCS[0]
072	TFRM	R/W	—	—	INS_MYEL	INS_YEL	INS_MF	INS_FE	INS_CRC	INS_FBIT
073	TERROR	R/W	TSERR	TMERR	TBERR	BSLIP	TCOFA	TCERR	TFERR	TVERR
074	TMAN	R/W	INS_SA[8]	INS_SA[7]	INS_SA[6]	INS_SA[5]	INS_SA[4]	FEBE_II	FEBE_I	TFEBE
075	TALM	R/W	—	—	AUTO_MYEL	AUTO_YEL	AUTO_AIS	TMYEL	TYEL	TAIS
076	TPATT	R/W	—	—	—	TPSTART	FRAMED	ZLIMIT	TPATT[1]	TPATT[0]
077	TLB	R/W	—	—	—	—	LB_LEN[1]	LB_LEN[0]	UNFRAMED	LBSTART
078	LBP	R/W	LBP[1]	LBP[2]	LBP[3]	LBP[4]	LBP[5]	LBP[6]	LBP[7]	—

Table 3-35. Transmit Sa-Byte Buffers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
07B	TSA4	R/W	TSA4[7]	TSA4[6]	TSA4[5]	TSA4[4]	TSA4[3]	TSA4[2]	TSA4[1]	TSA4[0]
07C	TSA5	R/W	TSA5[7]	TSA5[6]	TSA5[5]	TSA5[4]	TSA5[3]	TSA5[2]	TSA5[1]	TSA5[0]
07D	TSA6	R/W	TSA6[7]	TSA6[6]	TSA6[5]	TSA6[4]	TSA6[3]	TSA6[2]	TSA6[1]	TSA6[0]
07E	TSA7	R/W	TSA7[7]	TSA7[6]	TSA7[5]	TSA7[4]	TSA7[3]	TSA7[2]	TSA7[1]	TSA7[0]
07F	TSA8	R/W	TSA8[7]	TSA8[6]	TSA8[5]	TSA8[4]	TSA8[3]	TSA8[2]	TSA8[1]	TSA8[0]

Table 3-36. CLAD Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
090	CLAD_CR	R/W	CEN	XSEL[2]	XSEL[1]	XSEL[0]	LFGAIN[3]	LFGAIN[2]	LFGAIN[1]	LFGAIN[0]
091	CSEL	R/W	VSEL[3]	VSEL[2]	VSEL[1]	VSEL[0]	OSEL[3]	OSEL[2]	OSEL[1]	OSEL[0]
092	CPHASE	R/W	—	RSCALE[2]	RSCALE[1]	RSCALE[0]	—	VSCALE[2]	VSCALE[1]	VSCALE[0]
093	CTEST	R/W	—	—	—	PNSEL	D20A	TBUS	RWINI	JINIT

Table 3-37. Bit-Oriented Protocol Registers

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0A0	BOP	R/W	RBOP_START	RBOP_INTEG	RBOP_LEN[1]	RBOP_LEN[0]	TBOP_LEN[1]	TBOP_LEN[0]	TBOP_MODE[1]	TBOP_MODE[0]
0A1	TBOP	R/W	—	—	TBOP[5]	TBOP[4]	TBOP[3]	TBOP[2]	TBOP[1]	TBOP[0]
0A2	RBOP	R	RBOP_LOST	RBOP_VALID	RBOP[5]	RBOP[4]	RBOP[3]	RBOP[2]	RBOP[1]	RBOP[0]
0A3	BOP_STAT	R	TBOP_ACTIVE	RBOP_ACTIVE	—	—	—	—	—	—

Table 3-38. Data Link Registers *(1 of 2)*

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0A4	DL1_TS	R/W	DL1_TS[7]	DL1_TS[6]	DL1_TS[5]	DL1_TS[4]	DL1_TS[3]	DL1_TS[2]	DL1_TS[1]	DL1_TS[0]
0A5	DL1_BIT	R/W	DL1_BIT[7]	DL1_BIT[6]	DL1_BIT[5]	DL1_BIT[4]	DL1_BIT[3]	DL1_BIT[2]	DL1_BIT[1]	DL1_BIT[0]
0A6	DL1_CTL	R/W	—	—	—	TDL1_RPT	DL1[1]	DL1[0]	TDL1_EN	RDL1_EN
0A7	RDL1_FFC	R/W	MSG_FILL[1]	MSG_FILL[0]	FFC[5]	FFC[4]	FFC[3]	FFC[2]	FFC[1]	FFC[0]
0A8	RDL1	R	EOM[1]	EOM[0]	RDL1_CNT[5]	RDL1_CNT[4]	RDL1_CNT[3]	RDL1_CNT[2]	RDL1_CNT[1]	RDL1_CNT[0]
			RDL1[7]	RDL1[6]	RDL1[5]	RDL1[4]	RDL1[3]	RDL1[2]	RDL1[1]	RDL1[0]
0A9	RDL1_STAT	R	—	—	—	RMSG1	RSTAT1	RMPTY1	RNEAR1	RFULL1
0AA	PRM	R/W	AUTO_PRM	PRM_CR	PRM_R	PRM_U1	PRM_U2	PRM_SL	AUTO_SL	SEND_PRM

Table 3-38. Data Link Registers *(2 of 2)*

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0AB	TDL1_FEC	R/W	—	—	FEC[5]	FEC[4]	FEC[3]	FEC[2]	FEC[1]	FEC[0]
0AC	TDL1_EOM	W	—	—	—	—	—	—	—	—
0AD	TDL1	R/W	TDL1[7]	TDL1[6]	TDL1[5]	TDL1[4]	TDL1[3]	TDL1[2]	TDL1[1]	TDL1[0]
0AE	TDL1_STAT	R	—	—	—	—	TMSG1	TMPTY1	TNEAR1	TFULL1
0AF	DL2_TS	R/W	DL2_TS[7]	DL2_TS[6]	DL2_TS[5]	DL2_TS[4]	DL2_TS[3]	DL2_TS[2]	DL2_TS[1]	DL2_TS[0]
0B0	DL2_BIT	R/W	DL2_BIT[7]	DL2_BIT[6]	DL2_BIT[5]	DL2_BIT[4]	DL2_BIT[3]	DL2_BIT[2]	DL2_BIT[1]	DL2_BIT[0]
0B1	DL2_CTL	R/W	—	—	—	TDL2_RPT	DL2[1]	DL2[0]	TDL2_EN	RDL2_EN
0B2	RDL2_FFC	R/W	MSG_FILL[1]	MSG_FILL[0]	FFC[5]	FFC[4]	FFC[3]	FFC[2]	FFC[1]	FFC[0]
0B3	RDL2	R	EOM[1]	EOM[0]	RDL2_CNT[5]	RDL2_CNT[4]	RDL2_CNT[3]	RDL2_CNT[2]	RDL2_CNT[1]	RDL2_CNT[0]
			RDL2[7]	RDL2[6]	RDL2[5]	RDL2[4]	RDL2[3]	RDL2[2]	RDL2[1]	RDL2[0]
0B4	RDL2_STAT	R	—	—	—	RMSG2	RSTAT2	RMPTY2	RNEAR2	RFULL2
0B6	TDL2_FEC	R/W	—	—	FEC[5]	FEC[4]	FEC[3]	FEC[2]	FEC[1]	FEC[0]
0B7	TDL2_EOM	W	—	—	—	—	—	—	—	—
0B8	TDL2	R/W	TDL2[7]	TDL2[6]	TDL2[5]	TDL2[4]	TDL2[3]	TDL2[2]	TDL2[1]	TDL2[0]
0B9	TDL2_STAT	R	—	—	—	—	TMSG2	TMPTY2	TNEAR2	TFULL2
0BA	DL_TEST1	R/W	—	—	—	—	DL_TEST1[3]	DL_TEST1[2]	DL_TEST1[1]	DL_TEST1[0]
0BB	DL_TEST2	R/W	—	—	DL_TEST2[5]	DL_TEST2[4]	DL_TEST2[3]	DL_TEST2[2]	DL_TEST2[1]	DL_TEST2[0]
0BC	DL_TEST3	R/W	—	—	DL_TEST3[5]	DL_TEST3[4]	DL_TEST3[3]	DL_TEST3[2]	DL_TEST3[1]	DL_TEST3[0]
0BD	DL_TEST4	R/W	—	DL_TEST4[6]	DL_TEST4[5]	DL_TEST4[4]	DL_TEST4[3]	DL_TEST4[2]	DL_TEST4[1]	DL_TEST4[0]
0BE	DL_TEST5	R/W	—	DL_TEST5[6]	DL_TEST5[5]	DL_TEST5[4]	DL_TEST5[3]	DL_TEST5[2]	DL_TEST5[1]	DL_TEST5[0]

Table 3-39. System Bus Registers *(1 of 2)*

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0D0	SBI_CR	R/W	X2CLK	SBI_OE	EMF	EMBED	SBI[3]	SBI[2]	SBI[1]	SBI[0]
0D1	RSB_CR	R/W	BUS_RSB	SIG_OFF	RPCM_NEG	RSYN_NEG	BUS_FRZ	RSB_CTR	RSBI[1]	RSBI[0]
0D2	RSYNC_BIT	R/W	—	—	—	—	—	OFFSET[2]	OFFSET[1]	OFFSET[0]
0D3	RSYNC_TS	R/W	—	OFFSET[9]	OFFSET[8]	OFFSET[7]	OFFSET[6]	OFFSET[5]	OFFSET[4]	OFFSET[3]
0D4	TSB_CR	R/W	BUS_TSB	TX_ALIGN	TPCM_NEG	TSYN_NEG	TSB_ALIGN	TSB_CTR	TSBI[1]	TSBI[0]
0D5	TSYNC_BIT	R/W	—	—	—	—	—	OFFSET[2]	OFFSET[1]	OFFSET[0]
0D6	TSYNC_TS	R/W	—	OFFSET[9]	OFFSET[8]	OFFSET[7]	OFFSET[6]	OFFSET[5]	OFFSET[4]	OFFSET[3]
0D7	RSIG_CR	R/W	—	SET_RSIG	SET_SIG	UNICODE	DEBOUNCE	FRZ_OFF	FRZ_ON	THRU
0D8	RSYNC_FRM	R/W	—	—	—	OFFSET[14]	OFFSET[13]	OFFSET[12]	OFFSET[11]	OFFSET[10]
0D9	SSTAT	R	TSDIR	TFSLIP	TUSLIP	—	RSDIR	RFSLIP	RUSLIP	—
0DA	STACK	R	WORD	MORE	—	CH[4]	CH[3]	CH[2]	CH[1]	CH[0]
			WORD	MORE	—	—	SIG_BITA	SIG_BITB	SIG_BITC	SIG_BITD
0DB	RPHASE	R	RDELAY[5]	RDELAY[4]	RDELAY[3]	RDELAY[2]	RDELAY[1]	RDELAY[0]	RSLIP_WR	RSLIP_RD
0DC	TPHASE	R	TDELAY[5]	TDELAY[4]	TDELAY[3]	TDELAY[2]	TDELAY[1]	TDELAY[0]	TSLIP_WR	TSLIP_RD
0DD	PERR	R	—	—	—	—	—	PERR_TPC	PERR_RPC	PERR_SBC
0E0–0FF	SBCn; n = 0 to 31	R/W	—	INSERT	SIG_LP	RLOOP	RINDO	TINDO	TSIG_AB	ASSIGN
100–11F	TPCn; n = 0 to 31	R/W	TB7ZS/EMFBIT	TLOOP	TIDLE	TLOCAL	TSIGA/TSIGO	TSIGB/RSIGO	TSIGC	TSIGD
120–13F	TSIGn; n = 00 to 31	R/W	—	—	—	—	TSIGn[3]	TSIGn[2]	TSIGn[1]	TSIGn[0]

Table 3-39. System Bus Registers *(2 of 2)*

ADDR (hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
140–15F	TSLIP_LOn; n = 0 to 31	R/W	TPCM[1]	TPCM[2]	TPCM[3]	TPCM[4]	TPCM[5]	TPCM[6]	TPCM[7]	TPCM[8]
160–17F	TSLIP–HIn; n = 0 to 31	R/W	TPCM[1]	TPCM[2]	TPCM[3]	TPCM[4]	TPCM[5]	TPCM[6]	TPCM[7]	TPCM[8]
180–19F	RPCn; n = 0 to 31	R/W	RSIG_AB/ EMFBIT	RIDLE	SIG_STK	RLOCAL	RSIGA	RSIGB	RSIGC	RSIGD
1A0–1BF	RSIGn; n = 0 to 31	R/W	RSIGn[7]	RSIGn[6]	RSIGn[5]	RSIGn[4]	RSIGn[3]	RSIGn[2]	RSIGn[1]	RSIGn[0]
1C0–1DF	RSLIP_LOn; n = 0 to 31	R/W	RPCM[1]	RPCM[2]	RPCM[3]	RPCM[4]	RPCM[5]	RPCM[6]	RPCM[7]	RPCM[8]
1E0–1FF	RSLIP_HIn; n = 0 to 31	R/W	RPCM[1]	RPCM[2]	RPCM[3]	RPCM[4]	RPCM[5]	RPCM[6]	RPCM[7]	RPCM[8]

4.0 Applications

4.1 External Component Specifications

Table 4-1. Transformer Specifications

Parameter	TX Low Power	RX	TX Better R_L
	Value	**Value**	**Value**
Turns Ratio	1:1.15	1:1	1:1.36
Pulse Engineering Part Numbers: Temp. 0 to 70 °C. Dual– SMT (small) 1500 Vrms Dual– SMT 3 KVrms	 — —	 T1190 T1038/T1035	
Pulse Engineering Part Numbers: Temp. 0 to 70 °C. Dual– SMT Dual– SMT (small) Dual– Thru Hole	 PE–68865[(1)] PE–65865 PE–65567		 — — —
Serial Resistance	1 Ω maximum		
Primary Inductance	OCL 1.2 mH @ 25 °C.		
Isolation Voltage	1500 Vrms/3 KVrms		
Leakage Inductance	0.6 µH		

NOTE(S):
(1) Contact Pulse Engineering for other part numbers.
Phone: (619) 674-8100.
WEB: http://www.pulseeng.com

Table 4-2. REFCKI (10 MHz) Crystal Oscillator Specifications

Parameter	Value
Nominal Frequency	10 MHz
Frequency Accuracy (E1)	±50 ppm
Frequency Accuracy (T1)	± 32 ppm
Output Level	CMOS or TTL
Aging	2 ppm/year, 10 ppm maximum

Figure 4-1. Option A: Long Haul Application with Ground Reference on the Line Side *(1 of 2)*

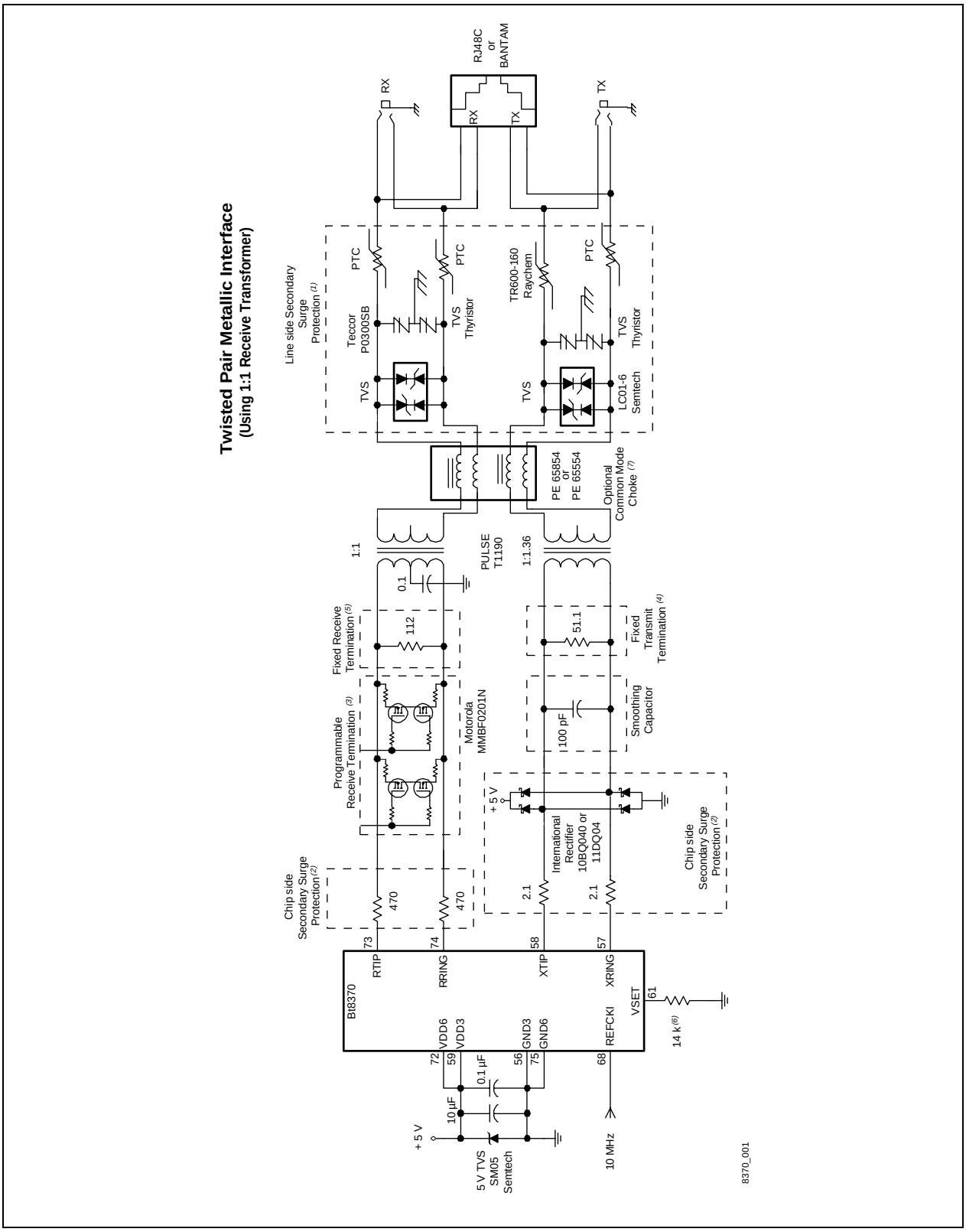


Figure 4-1. Option A: Long Haul Application with Ground Reference on the Line Side *(2 of 2)*

NOTE(S):

(1) Line side secondary surge protection to meet FCC Part 68, Bellcore TR-NWT-001089, and IEC 1000-4-5 requirements. These components are: 1. TVS-LC01-6 Semtech, 2. PTC-TR600-160 Raychem, 3. TVS Thyristor—Teccor P3100SB. A thyristor device (crow bar device) is used to protect against common mode (longitudinal) surges. A Thyristor device with 275 V breakover voltage rated to handle 100A (tp = 10X100Us) is required. A LC01-6 device provides protection during the metallic high surge lightning tests. It is designed to shunt the surge current with a maximum clamping voltage of 16 V below the transformer saturation point. The low capacitance characteristic of LC01-6 (50 pF) is required to avoid signal degration of the high speed digital pulse. A PTC device is used for AC power cross faults, meeting the requirements of Bellcore 1089 and UL1459.

(2) Chip side Secondary surge protection. Diodes should be low capacitance, fast turn-on Schottky or surge protection diodes. These components are: 1. Schottky Diode—10BQ040(surface mount) or 11DQ04(discrete) International Rectifier or one 20CJQ04 with two 10BQ040 2. two 2.1 Ω, 1/4 W, 1% Resistors. The two 470 Ω resistors in series with RTIP/RRING are used to limit the current going into the device while the power is off and T1/E1 lines are connected.

(3) Optional programmable receive termination –75/100/120 Ω.

(4) Optional fixed transmit termination. The value shown provides acceptable transmit return loss for T1 and E1 applications.

(5) Required fixed receive termination. The parallel combination of the fixed termination and programmable termination plus series value of the primary surge protection line feed resistor (PTC) should match the line impedance required.

(6) VSET Resistor. The VSET resistance value controls the transmit signal amplitude and depending on the line feed resistance (PTC) in the primary surge protection circuit, its value can be fine-tuned. Use R (VSET) = 14 k if total line series resistance is 0 to 12 Ω.

(7) The Physical area between the connector and chokes should be kept small in order to avoid high frequency coupling and to improve emissions test. Another good option is to place chokes between PTC and the Line side surge protection device. If common mode noise is a concern then use the through hole package (PE65854) at the connector.

Figure 4-2. Option B: Long Haul with No Ground Reference *(1 of 2)*

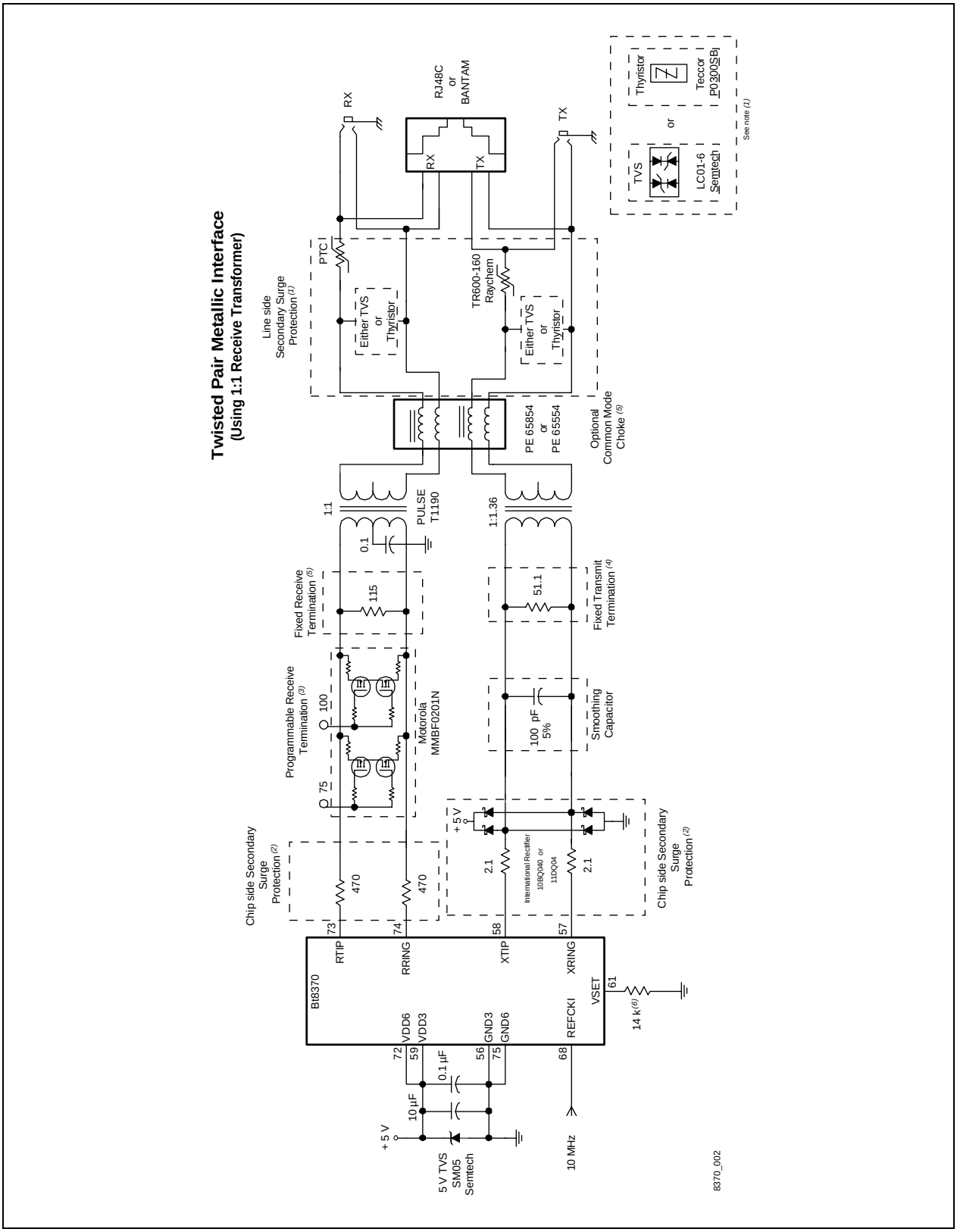


Figure 4-2. Option B: Long Haul with No Ground Reference *(2 of 2)*

NOTE(S):

(1) Line side secondary surge protection to meet FCC Part 68, Bellcore TR-NWT-001089, and IEC 1000-4-5 requirements. These components are: 1. TVS-LC01-6 Semtech, 2. PTC-TR600-160 Raychem, or 1. Thyristor (Sidactor)—Teccor P0300SB, 2. PTC-TR600-160 Raychem can be used.
An LC01-6 device provides protection during high surge lightning tests. It is designed to shunt the surge current with a maximum clamping voltage of 16 V maximum, below the transformer saturation point.
A Thyristor (Sidactor—Teccor P0300SB) clamps the voltage at 40 V maximum.
A PTC device is used for power cross faults, meeting the requirements of Bellcore 1089 and UL1459.

(2) Chip side Secondary surge protection. Diodes should be low capacitance, fast turn-on Schottky or surge protection diodes. These components are: 1. Schottky Diode—11DQ04 (disrete) or 10BQ040 (surface mount) International Rectifier, 2. two 2.1 Ω, 1/4 W, 1% Resistors. The two 470 Ω resistors in series with RTIP/RRING are used to limit the current going into the device while the power is off and T1/E1 lines are connected.

(3) Optional programmable receive termination –75/100/120 Ω.

(4) Optional fixed transmit termination. The value shown provides acceptable transmit return loss for T1 and E1 applications.

(5) Required fixed receive termination. The parallel combination of the fixed termination and programmable termination plus the primary surge protection line feed resistor (PTC) must match the line impedance.

(6) VSET Resistor. The VSET resistance value controls the transmit signal amplitude and depending on the line feed resistance (PTC) in the primary surge protection circuit, its value can be fine-tuned. Use R (VSET) = 14 k if total line feed resistance is 0 to 12 Ω.

(7) The Physical area between the connector and chokes should be kept small in order to avoid high frequency coupling and to improve emissions test. Another good option is to place chokes between PTC and Line side surge protection device. If common mode noise is a concern then use the through hole package (PE65854) at the connector.

Figure 4-3. Option C: Long Haul Application with No Ground Reference on the Line *(1 of 2)*

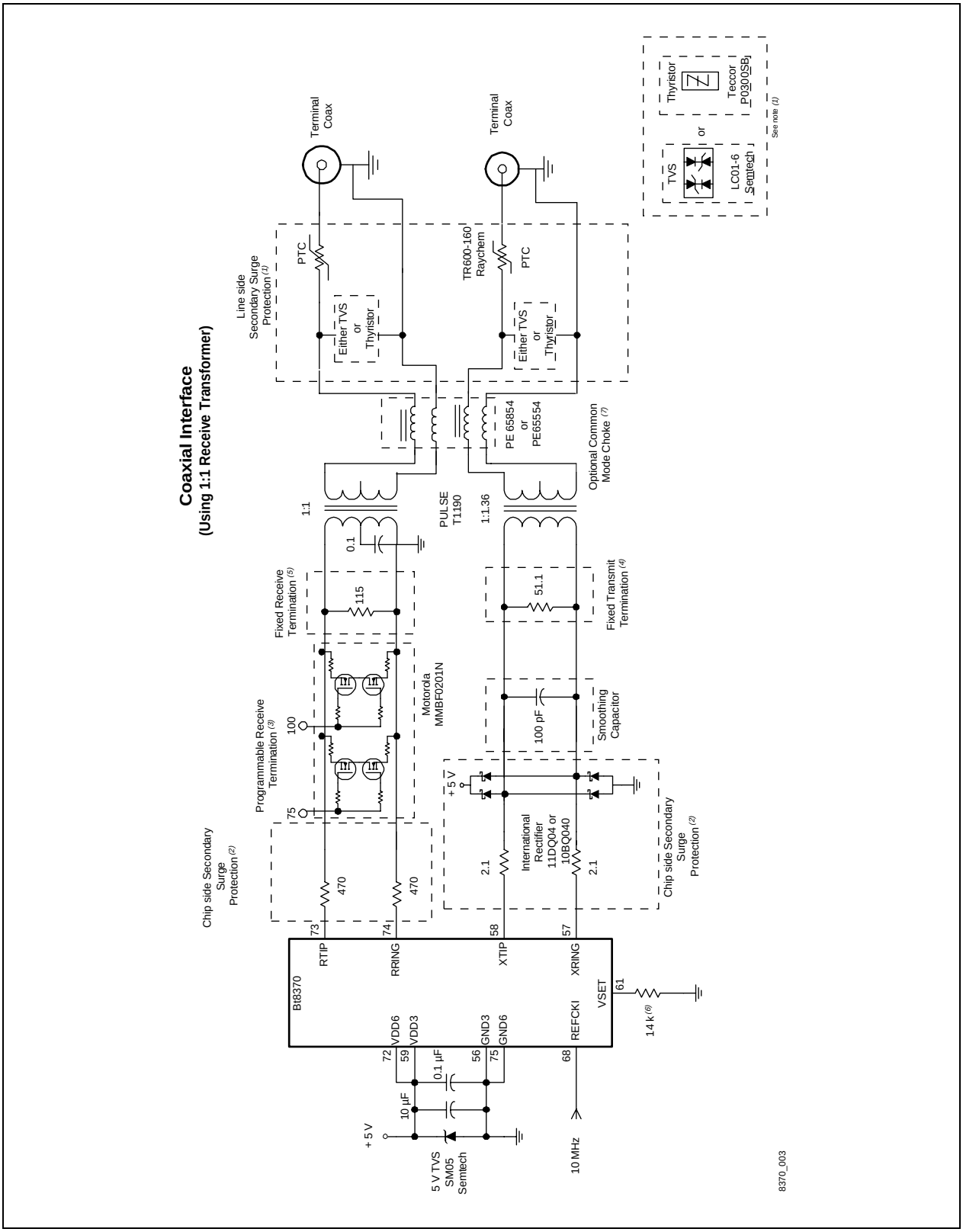


Figure 4-3. Option C: Long Haul Application with No Ground Reference on the Line *(2 of 2)*

NOTE(S):

(1) Line side secondary surge protection to meet FCC Part 68, Bellcore TR-NWT-001089, and IEC 1000-4-5 requirements. These components are: 1. TVS-LC01-6 Semtech, 2. PTC- TR600-160 Raychem, or 1. Thyristor (Sidactor)—Teccor P0300SB, 2. PTC-TR600-160 Raychem can be used.
A LC01-6 device provides protection during high surge lightning tests. It is designed to shunt the surge current with a maximum clamping voltage of 16 V maximum, below the transformer saturation point. A Thyristor (Sidactor—Teccor P0300SB) clamps the voltage at 40 V maximum. A PTC device is used for power cross faults, meeting the requirements of Bellcore 1089 and UL1459.

(2) Chip side Secondary surge protection. Diodes should be low capacitance, fast turn-on Schottky or surge protection diodes. These components are: 1. Schottky Diode—10BQ040 (surface mount) or 11DQ04 (discrete) International Rectifier or one 20CJQ04 with two 10BQ040 2. two 2.1 Ω, 1/4 W, 1% Resistors. The two 470 Ω resistors in series with RTIP/RRING are used to limit the current going into the device and the power are off and T1/E1 lines are connected.

(3) Optional programmable receive termination –75/100/120 Ω.

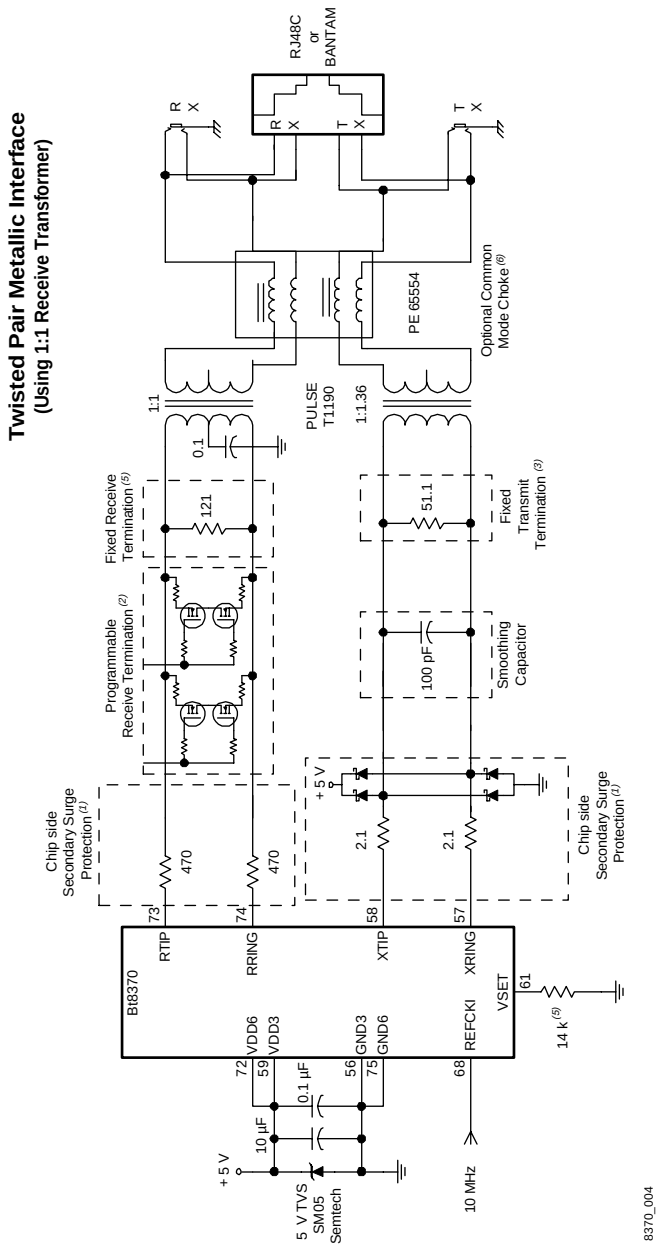
(4) Optional fixed transmit termination. The value shown provides acceptable transmit return loss for T1 and E1 applications.

(5) Required fixed receive termination. The parallel combination of the fixed termination and programmable termination plus the primary surge protection line feed resistor (PTC) must match the line impedance.

(6) VSET Resistor. The VSET resistance value controls the transmit signal amplitude and depending on the line feed resistance (PTC) in the primary surge protection circuit, its value can be fine-tuned. Use R (VSET) = 14 k if total line series resistance is 0 to 12 Ω.

(7) The Physical area between the connector and chokes should be kept small in order to avoid high frequency coupling and to improve emissions test. Another good option is to place chokes between PTC and the Line side surge protection device. If common mode noise is a concern then use the through hole package (PE65854) at the connector.

Figure 4-4. Option D: Short Haul Interface Application



NOTE(S):

(1) Chip side secondary surge protection. Diodes should be low capacitance, fast turn-on Schottky or surge protection diodes. These components are: 1. Schottky Diode—11DQ04 (disrete) or 10BQ040 (surface mount) International Rectifier, 2. two 2.1 Ω, 1/4 W, 1% Resistors. The two 470 Ω resistors in series with RTIP/RRING are used to limit the current going into the device while the power is off and T1/E1 lines are connected.

(2) Optional programmable receive termination –75/100/120 Ω.

(3) Optional fixed transmit termination. The value shown provides acceptable transmit return loss for T1 and E1 applications.

(4) Required fixed receive termination. The parallel combination of the fixed termination and programmable termination must match the line impedance.

(5) VSET Resistor. The VSET resistance value controls the transmit signal amplitude.

(6) The Physical area between the connector and chokes should be kept small in order to avoid high frequency coupling and to improve emissions test

5.0 Electrical/Mechanical Specifications

5.1 Absolute Maximum Ratings

Table 5-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
V_{DD}	Power Supply (measured to GND)	–0.5	7	V
ΔV_{DD}	Voltage Differential (between any 2 V_{DD} pins)		0.5	V
V_i	Constant Voltage on any Signal Pin	–1.0	V_{DD} + 0.5	V
ESD	Transient Voltage on any Signal Pin HBM rating CDM rating MMM rating	—	 ±2 ±700 ±200	 kV V V
I_i	Constant Current on any Signal Pin	–10	+10	mA
LATCHUP	Transient Current on any Signal Pin Digital Pins Analog Pins (TIP,RING)	 –350 –350	 +400 +400	 mA mA
T_s	Storage Temperature	–65	150	°C
T_j	Junction Temperature: (θ_{jA} x V_{DD} x I_{DD}) + T_{amb}	–40	125	°C
T_{vsol}	Vapor Phase Soldering Temperature (1 minute)	—	220	°C
θ_{jA}	Thermal Resistance (80MQFP), Still Air	—	43	°C/W

NOTE(S): Stresses above those listed as Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

Table 5-2. Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{DD}	Supply Voltage	4.75	5.25	V
T_{amb}	Ambient Operating Temperature Bt8370KPF, Bt8375KPF, Bt8376KPF Bt8370EPF, Bt8375EPF, Bt8376EPF	 0 –40	 70 85	 °C °C
V_{ih}	Input High Voltage (except TCK)	2.0	V_{DD} + 0.5	V
V_{ih}	TCK	2.2	V_{DD} + 0.5	V
V_{il}	Input Low Voltage	–0.5	0.8	V

5.3 Electrical Characteristics

Table 5-3. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
I_{DD}	Supply Current	—	125	175	mA
V_{oh}	Output High Voltage (I_{oh} = –400 µA)	3.5	—	—	V
V_{ol}	Output Low Voltage (I_{ol} = 4 mA)	—	—	0.4	V
I_{od}	Open Drain Output Current Sink	—	—	4	mA
I_{pr}	Resistive Pullup Current	40	100	500	µA
I_l	Input Leakage Current	–10	1	10	µA
I_{oz}	Three-state Leakage Current	–10	1	10	µA
C_{in}	Input Capacitance (f = 1 MHz, Vin = 2.4 V)	—	2	5	pF
C_{io}	I/O Capacitance (PIO, AD[7:0] pins)	—	5	10	pF
C_{out}	Output Capacitance	—	2	5	pF
C_{ld}	Capacitive Loading (Test Condition)	—	70	85	pF
I_{osc}	Short Circuit Output Current	37	50	160	mA

Table 5-4. Line Interface Unit (RLIU, TLIU) Performance Characteristics

Parameter	Minimum	Typical	Maximum	Units
T1 Receiver Sensitivity (Attenuation @ 772 kHz)*(1)*	+3	—	–36	dB
E1 Receiver Sensitivity (Attenuation @ 1024 kHz)*(1)*	+3	—	–43	dB
T1/E1 Short-Haul Receiver Sensitivity *(2)*	+3	—	–20	dB
Transmitter XTIP, XRING Outputs:				
Output Impedance (XOE = 0, high impedance)	10	100	—	kΩ
Output Impedance (XOE = 1, unterminated)	—	1	2	kΩ
T1 Pulse Amplitude, 100 Ω UTP	2.4	3.0	3.6	V
E1 Pulse Amplitude, 75 Ω Coax	2.14	2.37	2.6	V
E1 Pulse Amplitude, 120 Ω UTP	2.7	3.0	3.3	V
Space/Mark Peak Voltage Ratio	–10	—	+10	%
Receiver RTIP, RRING Inputs:				
Input Impedance (unterminated)	—	10	12	kΩ
Peak-to-Peak Voltage (measured deferentially)	—	6	7.2	V
Receiver Phase-Lock Loop (RPLL)				
Tolerable consecutive 0s before frequency lost	23	75	100	bits
T1 Frequency Lock Range	–0.3	1544	+0.3	kHz
E1 Frequency Lock Range	–0.4	2048	+0.4	kHz
Transmitter Phase-Lock Loop (TPLL):				
T1 Frequency Lock Range	–0.7	1544	+0.7	kHz
E1 Frequency Lock Range	–1.0	2048	+1.0	kHz
Longitudinal Balance, Impedance to GND:				
T1 (50 kHz < f < 1544 kHz)	35	42	—	dB
E1 (50 kHz < f < 2048 kHz)	35	40	—	dB
Receiver Noise Immunity (SNR):				
Near-End Crosstalk (2^{15} PRBS)	—	15	18	dB
60 Hz Longitudinal	—	18	20	dB
Transmitter Signal Power Level (3 kHz band):				
Power @ 772 kHz	12	15	+19	dBm
Power @ 1544 kHz (versus Power @ 772 kHz)	–25	–36	—	dB

NOTE(S):
(1) Bt8370/8375/8376 receiver sensitivity includes 3 dB margin for 6000 feet (22 AWG) or 3.0 km (0.6 mm) cable.
(2) Bt8375 and Bt8376 receiver sensitivity is limited to –20 dB in both T1 and E1 modes.

5.4 AC Characteristics

Table 5-5. Input Clock Timing

Symbol	Parameter	Minimum	Maximum	Units
1	MCLK Frequency	8.0	35.7	MHz
	REFCKI Frequency	9.999	10.001	MHz
	RCKI, TCKI, ACKI Frequency	1.5	2.1	MHz
	RSBCKI, TSBCKI Frequency	1.5	8.2	MHz
	CLADI Frequency	8	16,384	kHz
	TCK Frequency	0	5.0	MHz
2	Clock Width High RCKI, TCKI, ACKI, CLADI MCLK, REFCKI, RSBCKI, TSBCKI	 0.2 x t(1) 0.4 x t(1)	 0.8 x t(1) 0.6 x t(1)	 ns ns
3	Clock Width Low RCKI, TCKI, ACKI, CLADI MCLK, REFCKI, RSBCKI, TSBCKI	 0.2 x t(1) 0.4 x t(1)	 0.8 x t(1) 0.6 x t(1)	 ns ns
4	Clock Rise Time	—	20	ns
5	Clock Fall Time	—	20	ns

Figure 5-1. Minimum Clock Pulse Widths

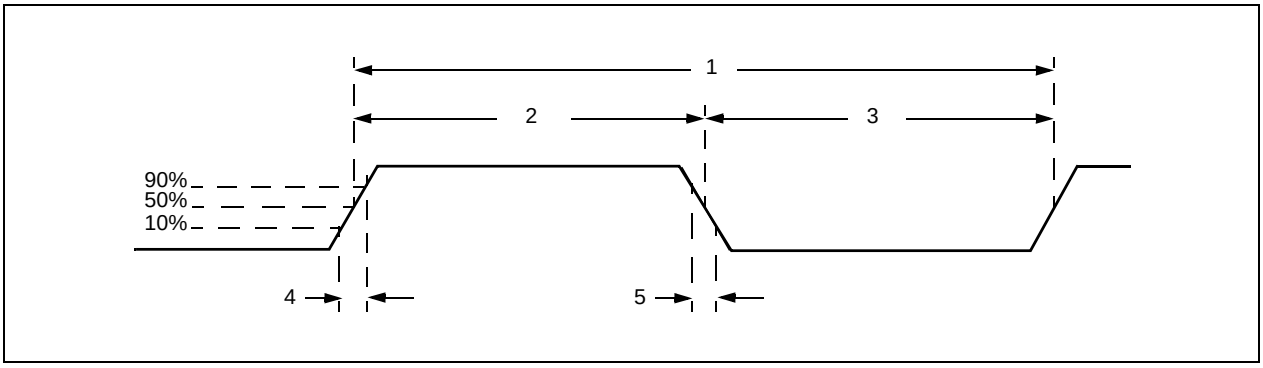


Table 5-6. Input Data Setup and Hold Timing

Symbol	Clock	Edge	Input Data	Minimum	Maximum	Units	Figure
1	MCLK	Rising	ONESEC	5	—	ns	5-2
			RST*	5	—	ns	5-2
	RCKI	Falling	RPOSI	5	—	ns	5-2
			RNEGI	5	—	ns	5-2
	TDLCKO	Falling	TDLI	5	—	ns	5-2
	RSBCKI	RSYN_NEG (addr 0D1)	RMSYNC	5	—	ns	5-2, 5-5
			RFSYNC	5	—	ns	5-5
	TSBCKI	TPCM_NEG (addr 0D4)	TPCMI	5	—	ns	5-2
			TSIGI	5	—	ns	5-2
		TSYN_NEG (addr 0D4)	TFSYNC	5	—	ns	5-5
			TMSYNC	5	—	ns	5-2, 5-5
2	MCLK	Rising	ONESEC	5	—	ns	5-2
			RST*	5	—	ns	5-2
	RCKI	Falling	RPOSI	5	—	ns	5-2
			RNEGI	5	—	ns	5-2
	TCKI	Falling	TPOSI	5	—	ns	5-2
			TNEGI	5	—	ns	5-2
	TDLCKO	Falling	TDLI	5	—	ns	5-2
	RSBCKI	RSYN_NEG (addr 0D1)	RMSYNC	5	—	ns	5-2, 5-5
			RFSYNC	5	—	ns	5-5
	TSBCKI	TPCM_NEG (addr 0D4)	TPCMI	5	—	ns	5-2
			TSIGI	5	—	ns	5-2
		TSYN_NEG (addr 0D4)	TFSYNC	5	—	ns	5-5
			TMSYNC	5	—	ns	5-2, 5-5
3	RSBCKI	RSYN_NEG	RMSYNC	5	—	ns	5-5
			RFSYNC	5	—	ns	5-5
	TSBCKI	TSYN_NG	TMSYNC	5	—	ns	5-5
			TFSYNC	5	—	ns	5-5
4	RSBCKI	RSYN_NEG	RMSYNC	5	—	ns	5-5
			RFSYNC	5	—	ns	5-5
	TSBCKI	TSYN_NEG	TMSYNC	5	—	ns	5-5
			TFSYNC	5	—	ns	5-5

Table 5-7. Output Data Delay Timing

Symbol	Clock	Edge	Output Data	Minimum	Maximum	Units	Figure
1	MCLK	Rising	ONESEC	0	10	ns	5-3
			INTR	0	10	ns	5-3
	RCKI	—	RCKO	0	20	ns	5-3
	RCKO	Rising	RPOSO	0	20	ns	5-3
			RNEGO	0	20	ns	5-3
		Falling	RDLO	0	20	ns	5-3
		—	RDLCKO	0	20	ns	5-3
	TCKI or ACKI	—	TCKO	0	20	ns	5-3
		—	TDLCKO	0	20	ns	5-3
		Rising	TNRZO	0	20	ns	5-3
			MSYNCO	0	20	ns	5-3
	TCKO	Rising	TPOSO	0	20	ns	5-3
			TNEGO	0	20	ns	5-3
	RDLCKO	Rising	RDLO	–5	15	ns	5-3
	RSBCKI	RPCM_NEG (addr 0D1)	RPCMO	0	30	ns	5-3
			RSIGO	0	30	ns	5-3
			RINDO	0	30	ns	5-3
			SIGFRZ	0	20	ns	5-3
		RSYN_NEG (addr 0D1)	RFSYNC	0	20	ns	5-3
			RMSYNC	0	20	ns	5-3
	TSBCKI	TPCM_NEG (addr 0D4)	TINDO	0	20	ns	5-3
		TSYN_NEG (addr 0D4)	TFSYNC	0	20	ns	5-3
			TMSYNC	0	20	ns	5-3

Table 5-8. 1-Second Input/Output Timing

Symbol	Parameter	Minimum	Maximum	Units
1	Input Pulse Width	1/MCLK	1 sec–125 µs	As shown
2	Output Pulse Width	125	250	µs

Figure 5-2. Input Data Setup/Hold Timing

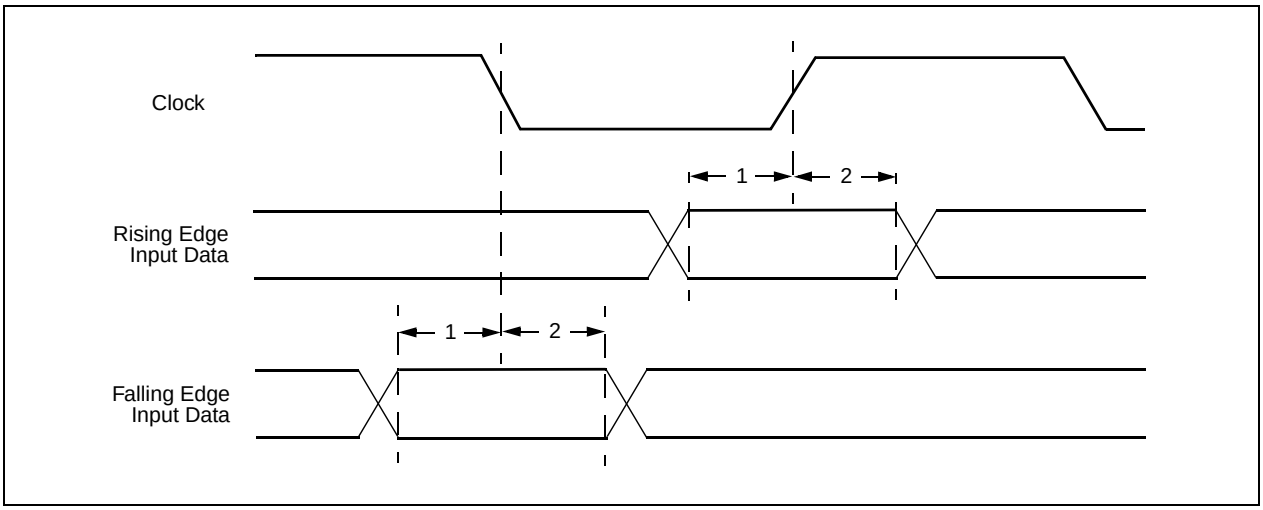


Figure 5-3. Output Data Delay Timing

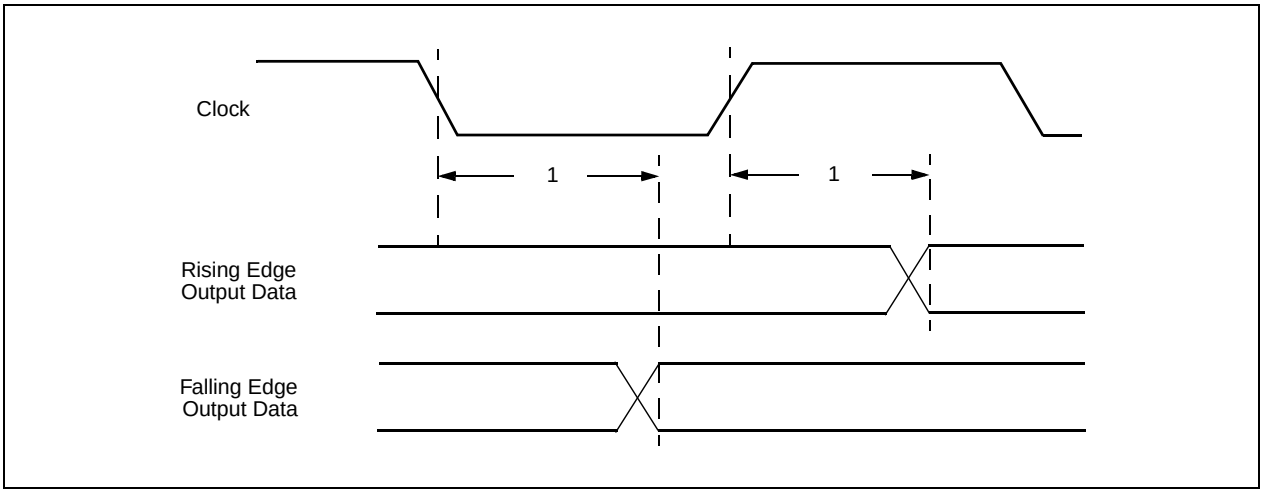
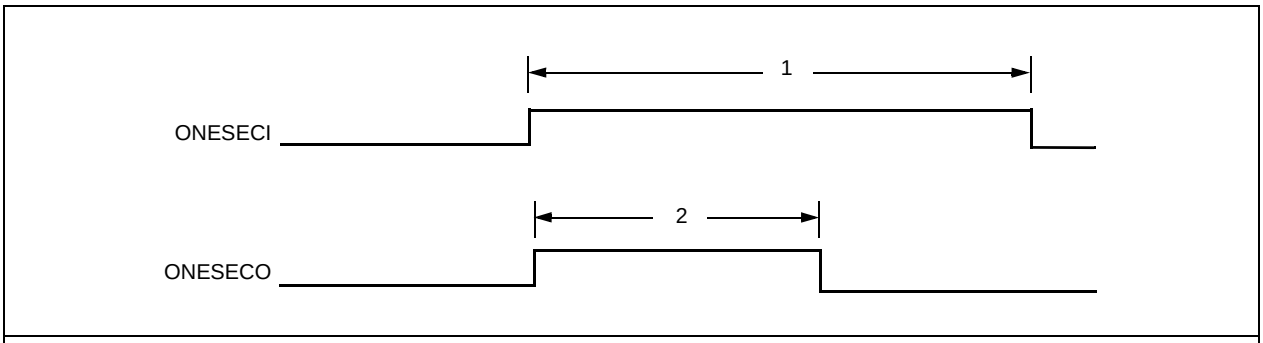
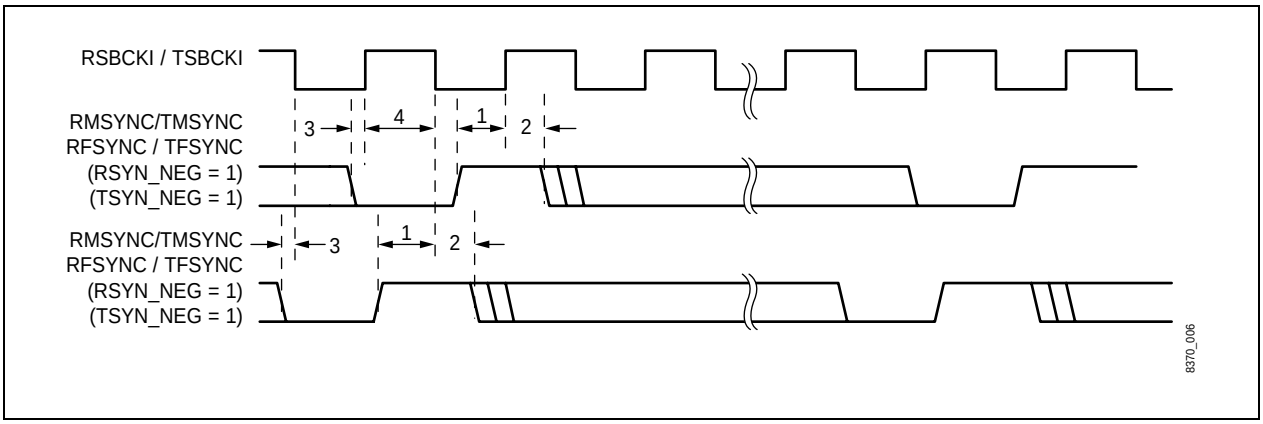


Figure 5-4. 1-Second Input/Output Timing



NOTE(S): ONESEC pin can be either an input (ONESECI) or an output (ONESECO).

Figure 5-5. SBI Timing: Setup and Hold Time for RFSYNC/RMSYNC and TFSYNC/TMSYNC Input Signals



5.5 MPU Interface Timing

Figure 5-6. Motorola Asynchronous Read Cycle

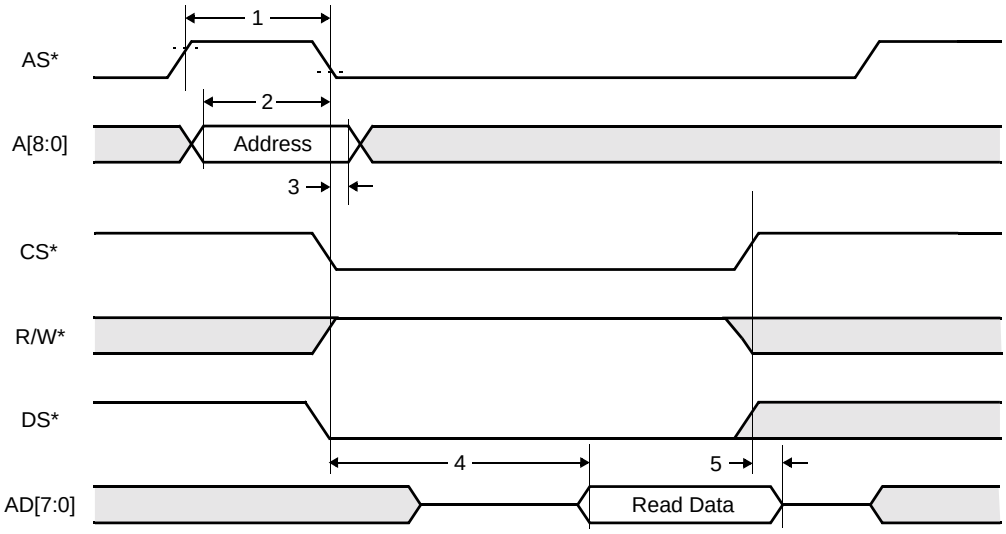


Table 5-9. Motorola Asynchronous Read Cycle

Symbol	Parameter	Minimum	Maximum	Units
1	AS* high pulse width	15	—	ns
2	A[8:0] Address setup to AS* low	5	—	ns
3	A[8:0] Address hold after AS* low	10	—	ns
4	CS* low and R/W* high, and DS* low to AD[7:0] valid	—	80	ns
5	CS* high and DS* high, and R/W* low to AD[7:0] invalid/three-state	5	20	ns

Figure 5-7. Motorola Asynchronous Write Cycle

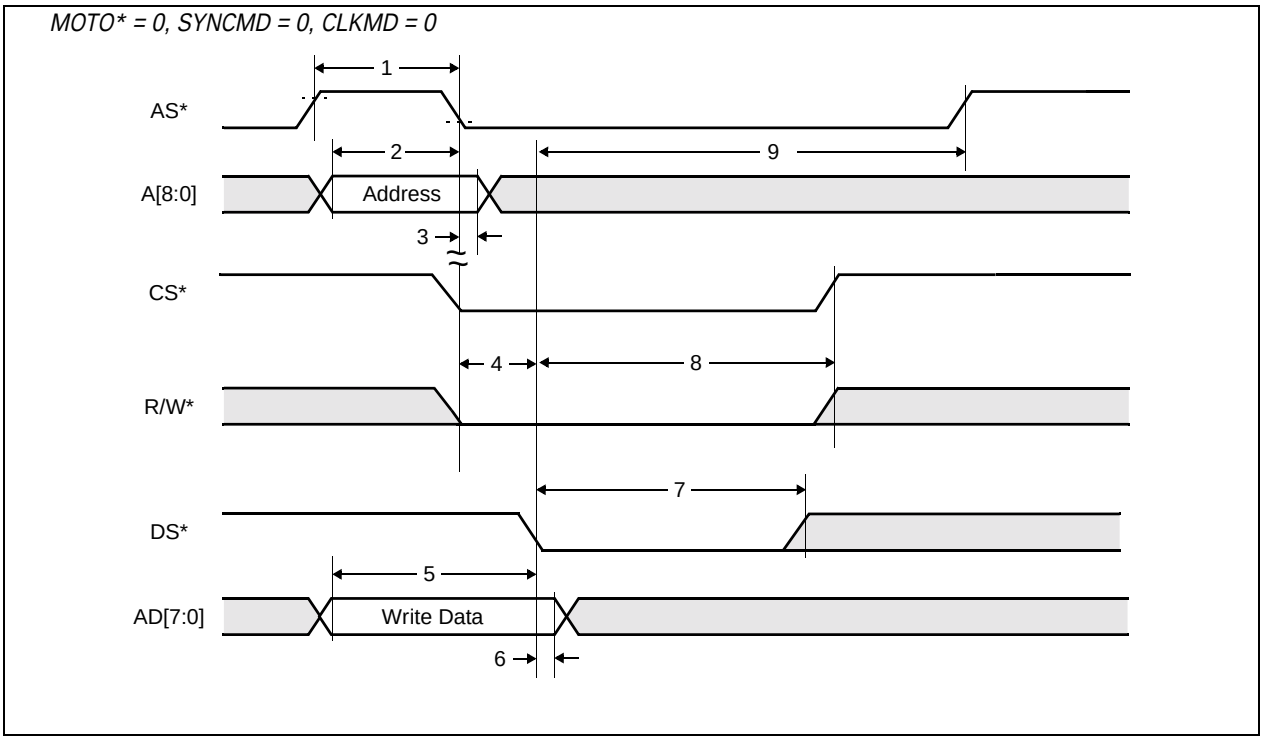


Table 5-10. Motorola Asynchronous Write Cycle

Symbol	Parameter	Minimum	Maximum	Units
1	AS* high pulse width	15	—	ns
2	A[8:0] Address setup to AS* low	5	—	ns
3	A[8:0] Address hold after AS* low	2	—	ns
4	CS* low and R/W* low to DS* low	5	—	ns
5	AD[7:0] setup to DS* low	0	—	ns
6	AD[7:0] hold after DS* low	15	—	ns
7	DS* low pulse width	38	—	ns
8	CS*, R/W* hold after DS* low	38	—	ns
9	DS* low to AS* high	70	—	ns

Figure 5-8. Intel Asynchronous Read Cycle

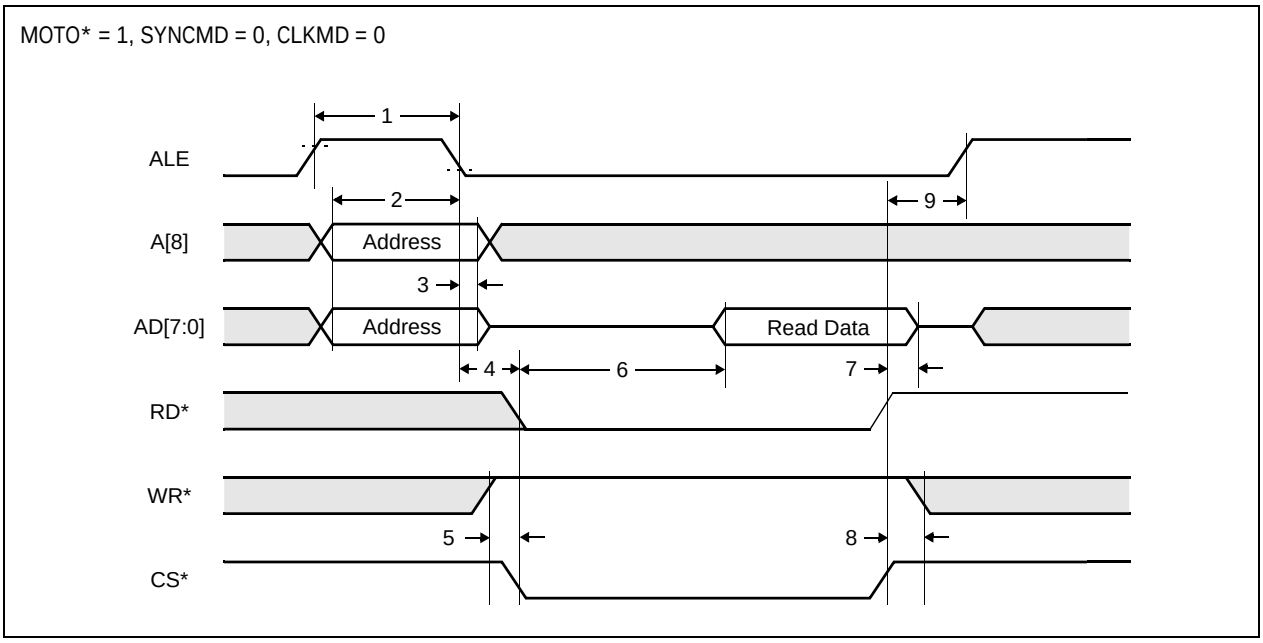


Table 5-11. Intel Asynchronous Read Cycle

Symbol	Parameter	Minimum	Maximum	Units
1	ALE high pulse width	15	—	ns
2	A[8], AD[7:0] Address setup to ALE low	5	—	ns
3	A[8], AD[7:0] Address hold after ALE low	10	—	ns
4	ALE low to RD* and CS* both low	0	—	ns
5	WR* high setup to RD* and CS* both low	0	—	ns
6	RD* and CS* both low to AD[7:0] valid	—	80	ns
7	RD* or CS* high to AD[7:0] invalid/three-state	0	15	ns
8	WR* high hold after RD* or CS* high	0	—	ns
9	RD* or CS* high to next ALE	0	—	ns

Figure 5-9. Intel Asynchronous Write Cycle

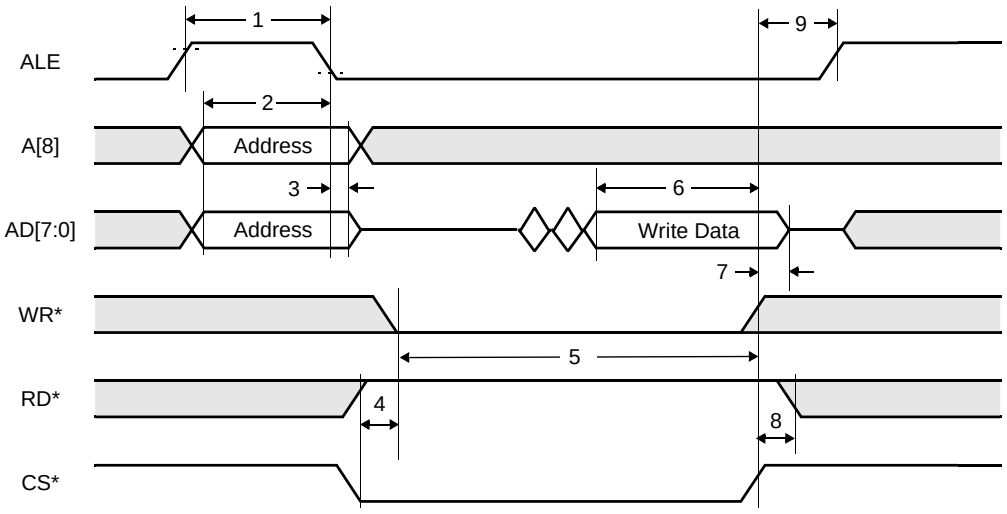


Table 5-12. Intel Asynchronous Write Cycle

Symbol	Parameter	Minimum	Maximum	Units
1	ALE high pulse width	15	—	ns
2	A[8], AD[7:0] Address setup to ALE low	5	—	ns
3	A[8], AD[7:0] Address hold after ALE low	10	—	ns
4	CS*, RD* setup to WR* low	0	—	ns
5	WR* pulse width low	38	—	ns
6	AD[7:0] input data setup to WR* or CS* high	0	—	ns
7	AD[7:0] input data hold after WR* or CS* high	15	—	ns
8	RD* hold after WR* or CS* high	0	—	ns
9	End write cycle to next ALE high	55	—	ns

Figure 5-10. Motorola Synchronous Read Cycle

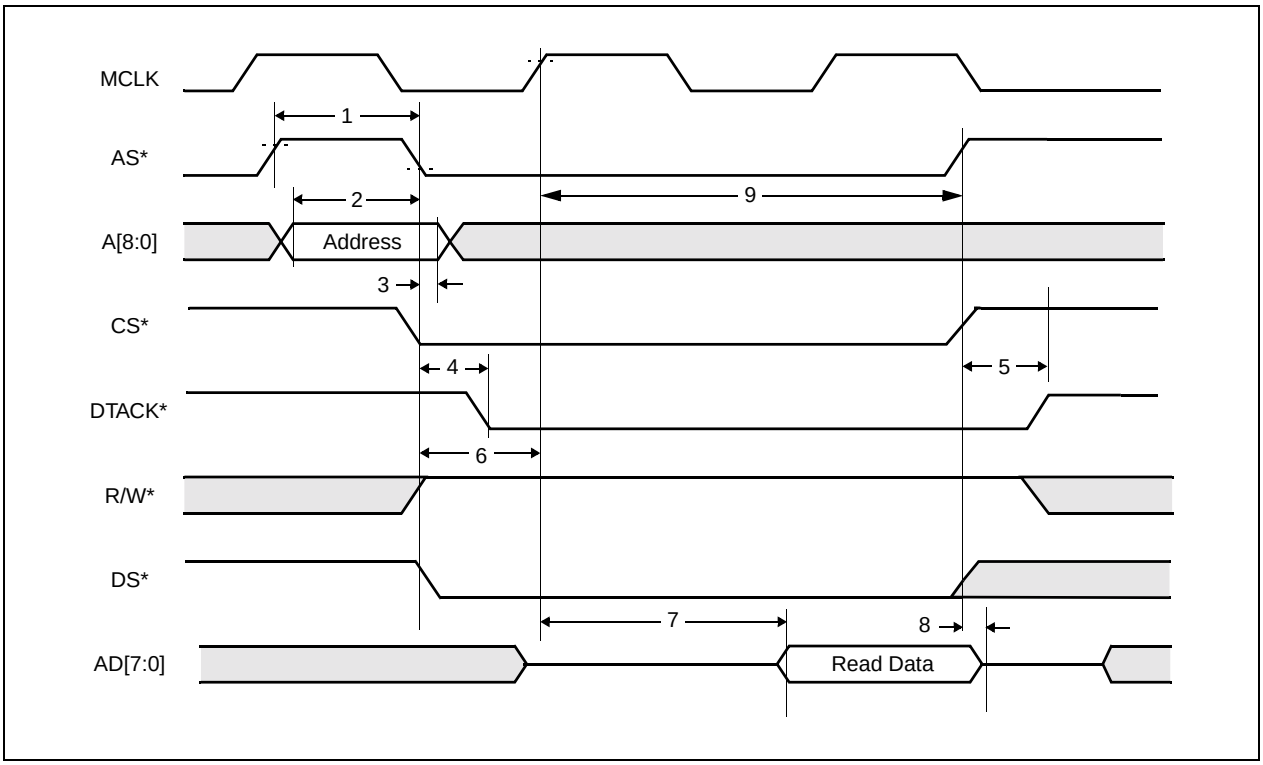


Table 5-13. Motorola Synchronous Read Cycle

Symbol	Parameter	Minimum	Maximum	Units
1	AS* high pulse width	15	—	ns
2	A[8:0] Address setup to AS* low	5	—	ns
3	A[8:0] Address hold after AS* low	10	—	ns
4	AS* and CS* low to DTACK* low	0	15	ns
5	AS* or CS* high to DTACK* high	0	10	ns
6	AS*, DS*, CS*, R/W* setup to MCLK high	15	—	ns
7	DS* sampled low to AD[7:0] valid	—	0.5/MCLK +20	ns
8	CS* or DS* high to AD[7:0] invalid/three-state	0	25	ns
9	MCLK high to AS* high	1/MCLK + 12	—	ns

Figure 5-11. Motorola Synchronous Write Cycle

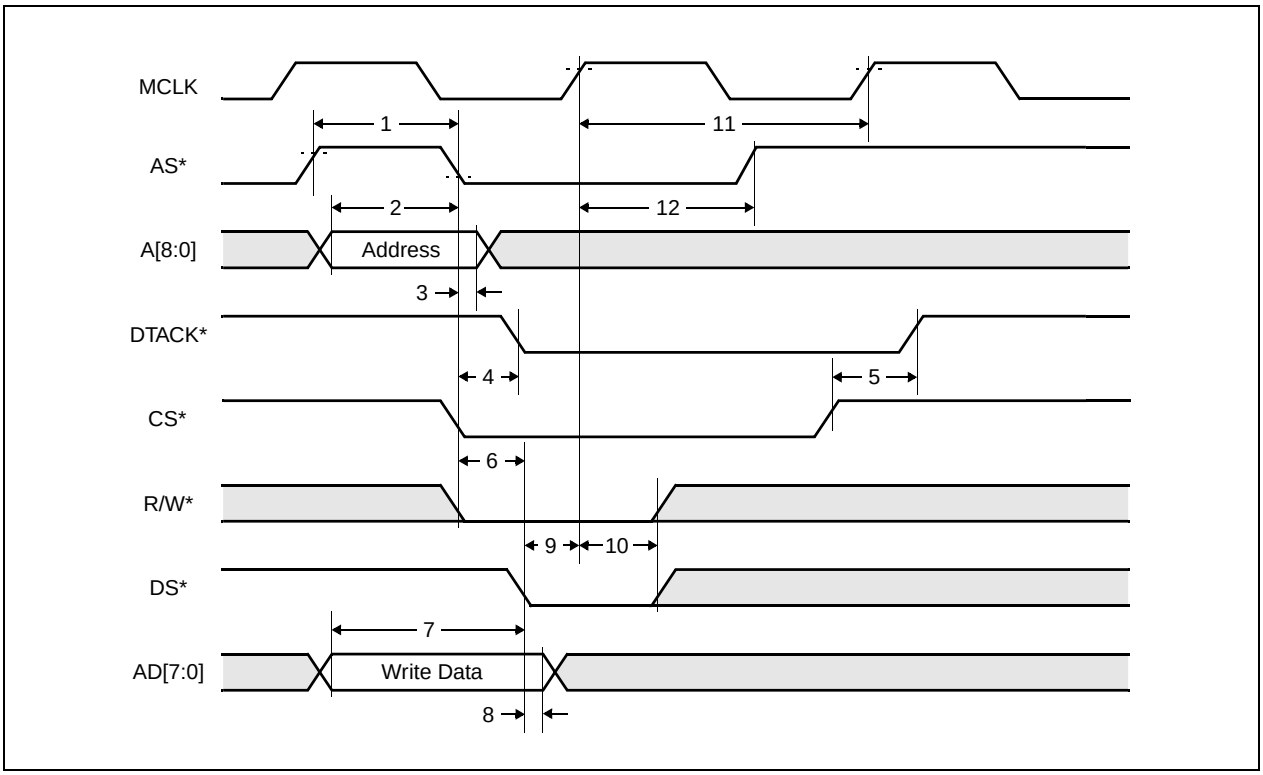


Table 5-14. Motorola Synchronous Write Cycle

Symbol	Parameter	Minimum	Maximum	Units
1	AS* high pulse width	15	—	ns
2	A[8:0] Address setup to AS* low	5	—	ns
3	A[8:0] Address hold after AS* low	10	—	ns
4	AS* and CS* low to DTACK* low	0	15	ns
5	AS* or CS* high to DTACK* high	0	10	ns
6	CS* and R/W* low to DS* low	10	—	ns
7	AD[7:0] setup to DS* low	0	—	ns
8	AD[7:0] hold after DS* low	15	—	ns
9	DS* setup to MCLK high	5	—	ns
10	DS* hold after MCLK high	10	—	ns
11	DS* sampled low to data latch (internal)	—	1 / MCLK + 15	ns
12	DS* sampled low to AS* high	1/2 MCLK + 15	—	ns

Figure 5-12. Intel Synchronous Read Cycle

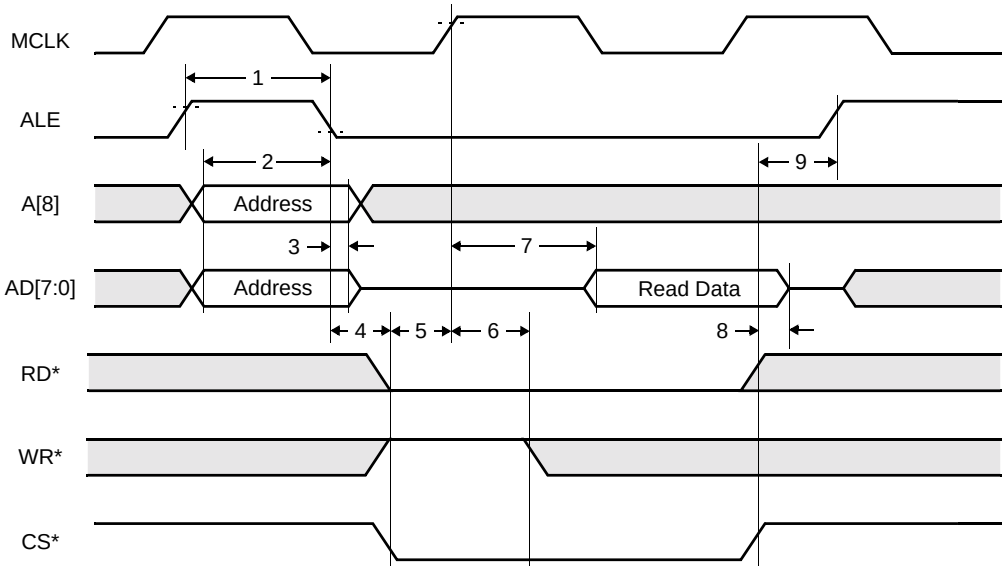


Table 5-15. Intel Synchronous Read Cycle

Symbol	Parameter	Minimum	Maximum	Units
1	ALE high pulse width	15	—	ns
2	A[8], AD[7:0] Address setup to ALE low	5	—	ns
3	A[8], AD[7:0] Address hold after ALE low	10	—	ns
4	ALE low to RD* and CS* both low	5	—	ns
5	RD*, CS*, WR* setup to MCLK high (Start RD cycle)	5	—	ns
6	RD*, CS*, WR* hold after MCLK high	10	—	ns
7	Start RD* cycle to AD[7:0] valid	—	*(1)*	ns
8	RD* or CS* high to AD[7:0] invalid/three-state	0	25	ns
9	End RD cycle to next ALE high	0	—	ns

NOTE(S):
(1) Parameter 7 equals 40 ns or 1/2 MCLK + 17 ns, whichever is greater.

Figure 5-13. Intel Synchronous Write Cycle

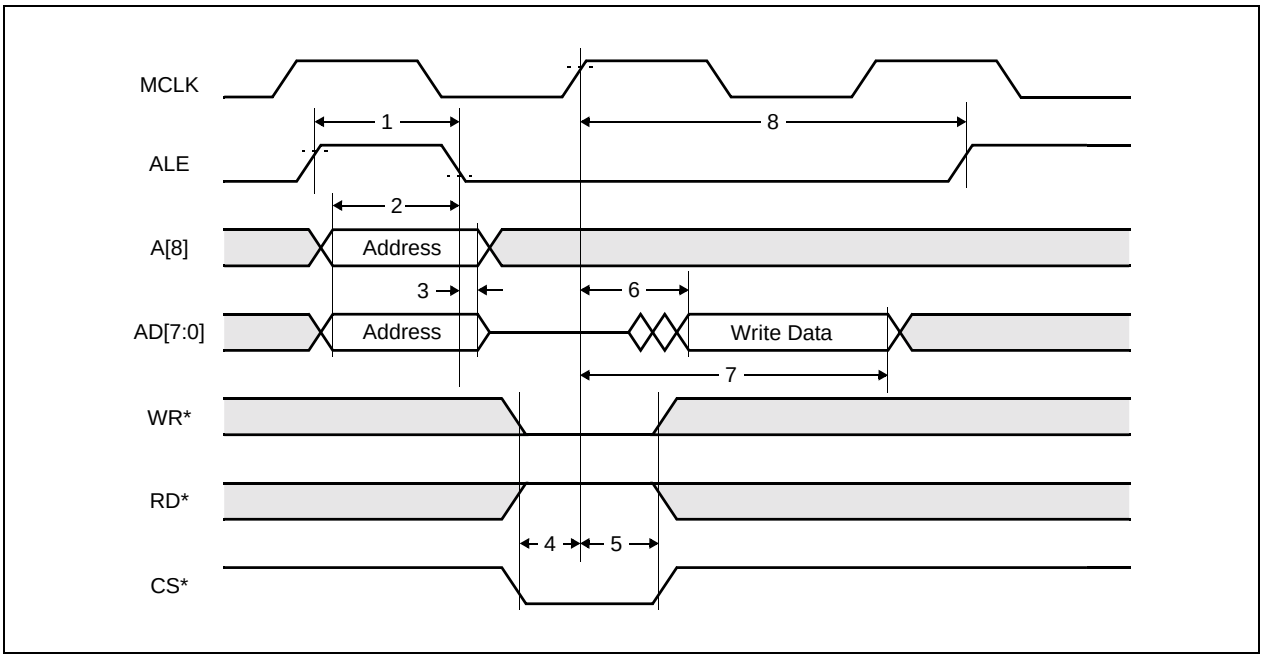
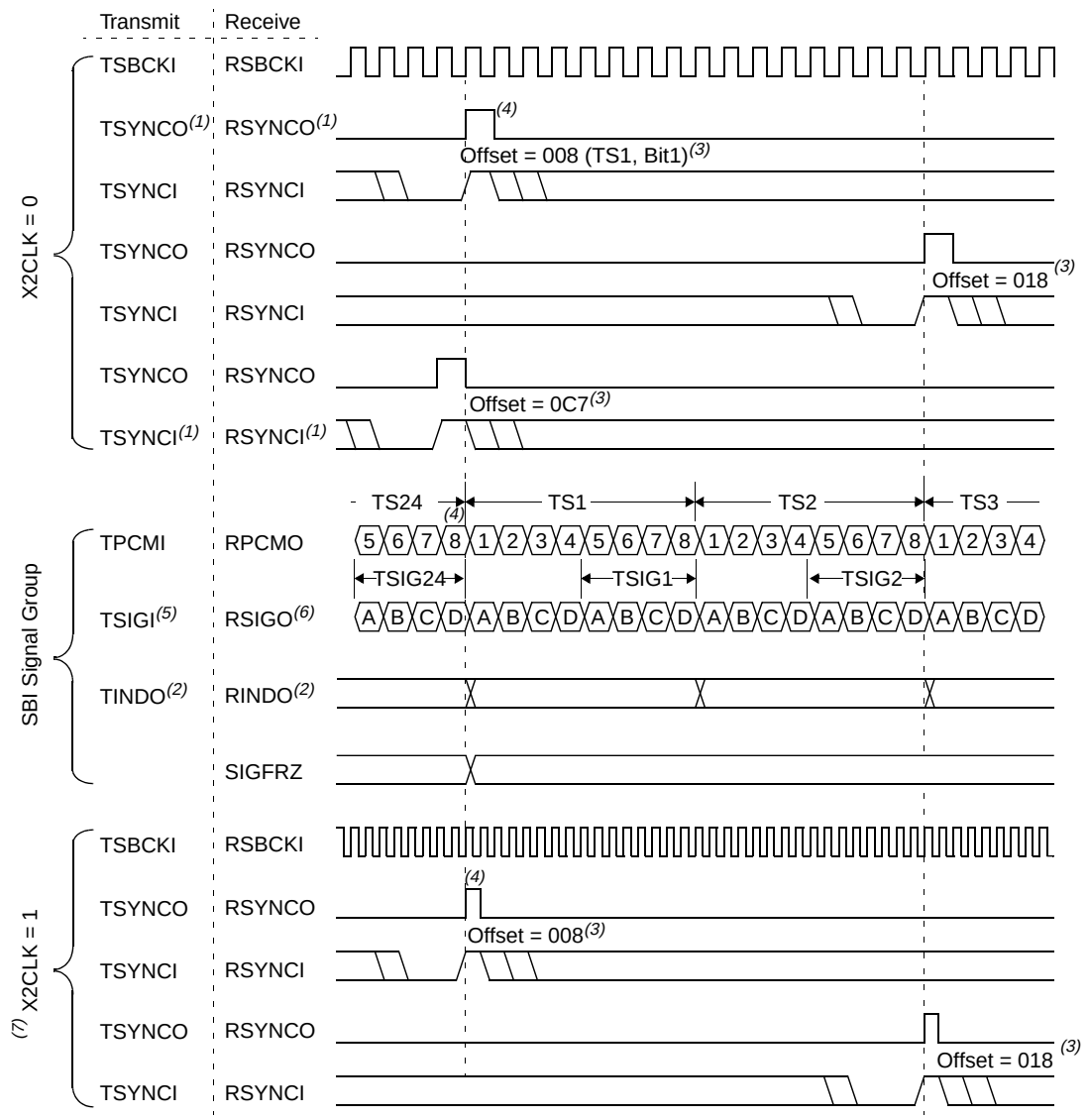


Table 5-16. Intel Synchronous Write Timing

Symbol	Parameter	Minimum	Maximum	Units
1	ALE high pulse width	15	—	ns
2	A[8], AD[7:0] Address setup to ALE low	5	—	ns
3	A[8], AD[7:0] Address hold after ALE low	10	—	ns
4	WR*,RD*,CS* setup to MCLK high (start WR cycle)	5	—	ns
5	WR*,RD*,CS* hold after MCLK high	10	—	ns
6	Start WR* cycle to AD[7:0] input data valid	—	1/MCLK–10	ns
7	AD[7:0] input data hold after Start WR cycle	1 / MCLK + 9	—	ns
8	Start WR cycle to next ALE high	1 / MCLK + 10	—	ns

5.6 System Bus Interface (SBI) Timing

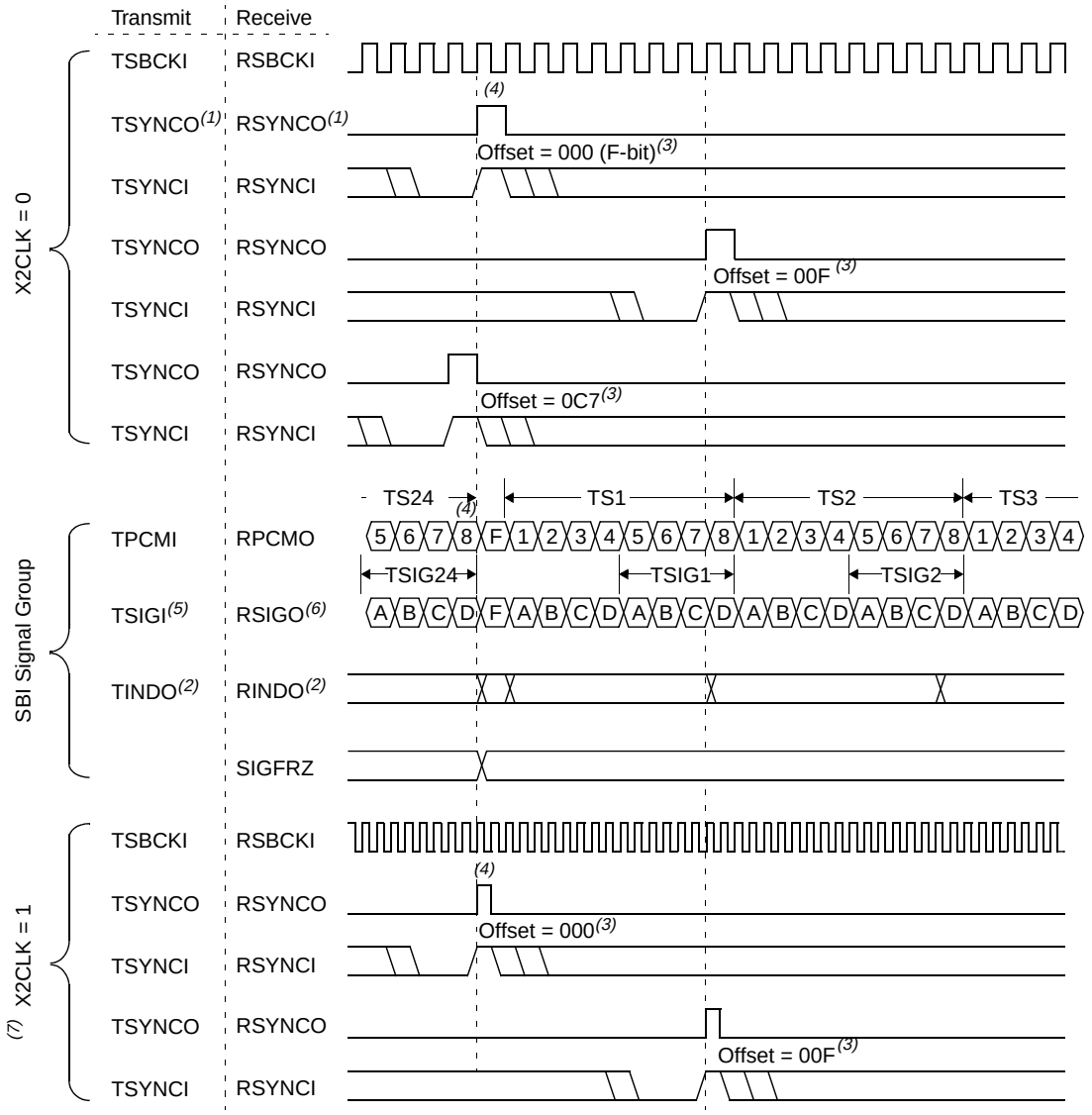
Figure 5-14. SBI Timing - 1536K Mode



NOTE(S):

1. TSYNC/RSYNC represents frame (TFSYNC/RFSYNC) and multiframe (TMSYNC/RMSYNC) offset.
2. RINDO/TINDO programmed high or low on a per-time slot basis (SBCn; addr 0E0-0FF).
3. Multiple offset values shown for illustration, refer to OFFSET controls (addr 0D2-0D3, 0D5-0D6).
4. Rising edge outputs and falling edge inputs shown. Refer to Figure 5-19 for other edge combinations.
5. Transmit ABCD signalling on TSIGI is sampled only during low nibble.
6. Received ABCD signalling on RSIGO is repeated in both high and low nibbles.
7. X2CLK control bit located in SBI_CR (addr 0D0).

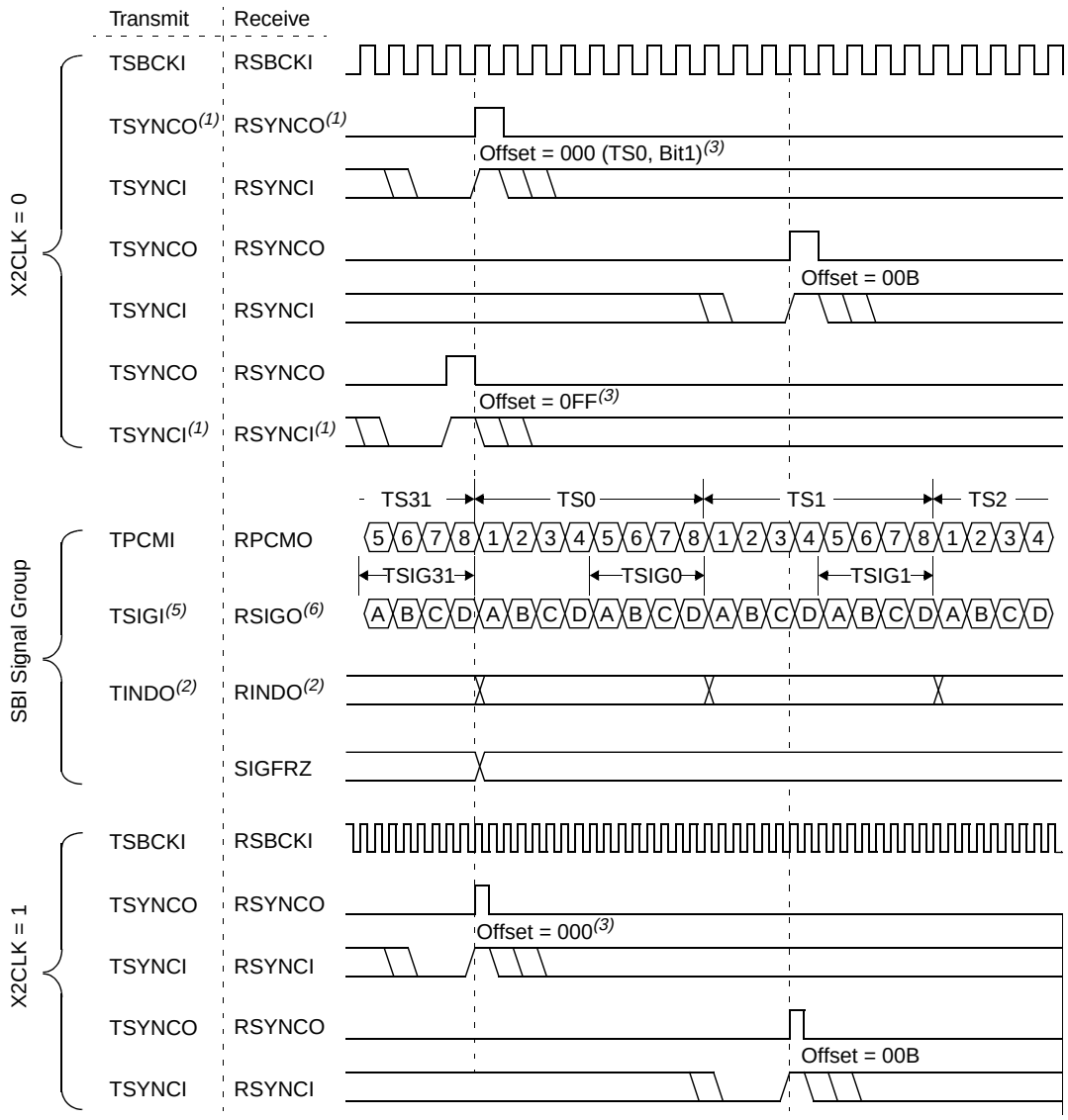
Figure 5-15. SBI Timing—1544K Mode



NOTE(S):

1. TSYNC/RSYNC represents frame (TFSYNC/RFSYNC) and multiframe (TMSYNC/RMSYNC) offset.
2. RINDO/TINDO programmed high or low on a per-time slot basis (SBCn; addr 0E0-0FF).
3. Multiple offset values shown for illustration, refer to OFFSET controls (addr 0D2-0D3, 0D5-0D6).
4. Rising edge outputs and falling edge inputs shown. Refer to Figure 5-19 for other edge combinations.
5. Transmit ABCD signalling on TSIGI is sampled only during low nibble.
6. Received ABCD signalling on RSIGO is repeated in both high and low nibbles.
7. X2CLK control bit located in SBI_CR (addr 0D0).

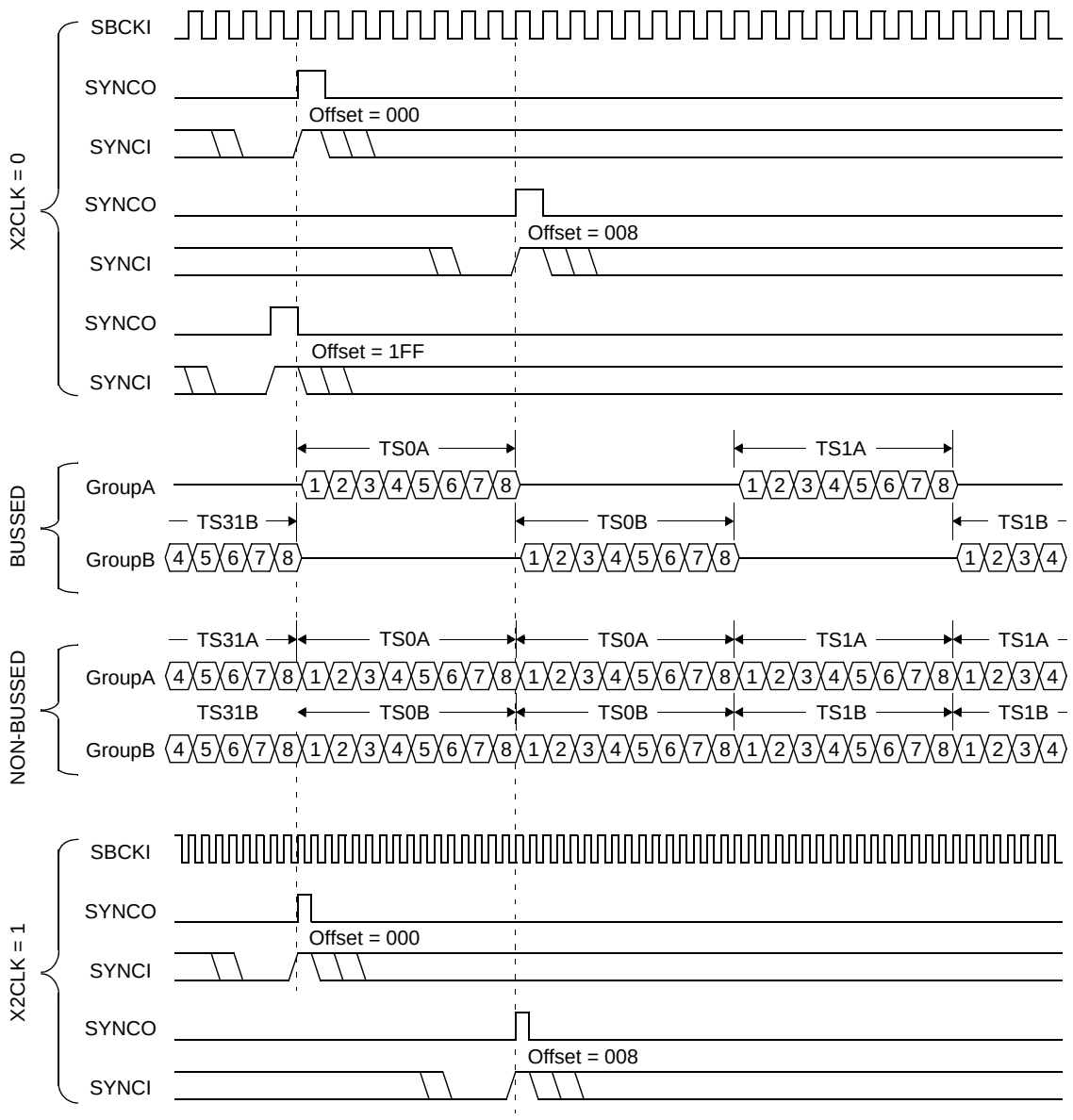
Figure 5-16. SBI Timing—2048K Mode



NOTE(S):

1. TSYNC/RSYNC represents frame (TFSYNC/RFSYNC) and multiframe (TMSYNC/RMSYNC) offset.
2. RINDO/TINDO programmed high or low on a per-time slot basis (SBCn; addr 0E0-0FF).
3. Multiple offset values shown for illustration, refer to OFFSET controls (addr 0D2-0D3, 0D5-0D6).
4. Rising edge outputs and falling edge inputs shown. Refer to Figure 5-19 for other edge combinations.
5. Transmit ABCD signalling on TSIGI is sampled only during low nibble.
6. Received ABCD signalling on RSIGO is repeated in both high and low nibbles.
7. X2CLK control bit located in SBI_CR (addr 0D0).

Figure 5-17. SBI Timing—4096K Mode



NOTE(S):

1. Rising edge outputs and falling edge inputs shown. Refer to Figure 5-19 for other edge combinations.
2. BUSSED or NON-BUSSED signal group controls located in BUS_RSB, BUS_FRZ (addr 0D1) and BUS_TSB (addr 0D4).

Figure 5-18. SBI Timing—8192K Mode

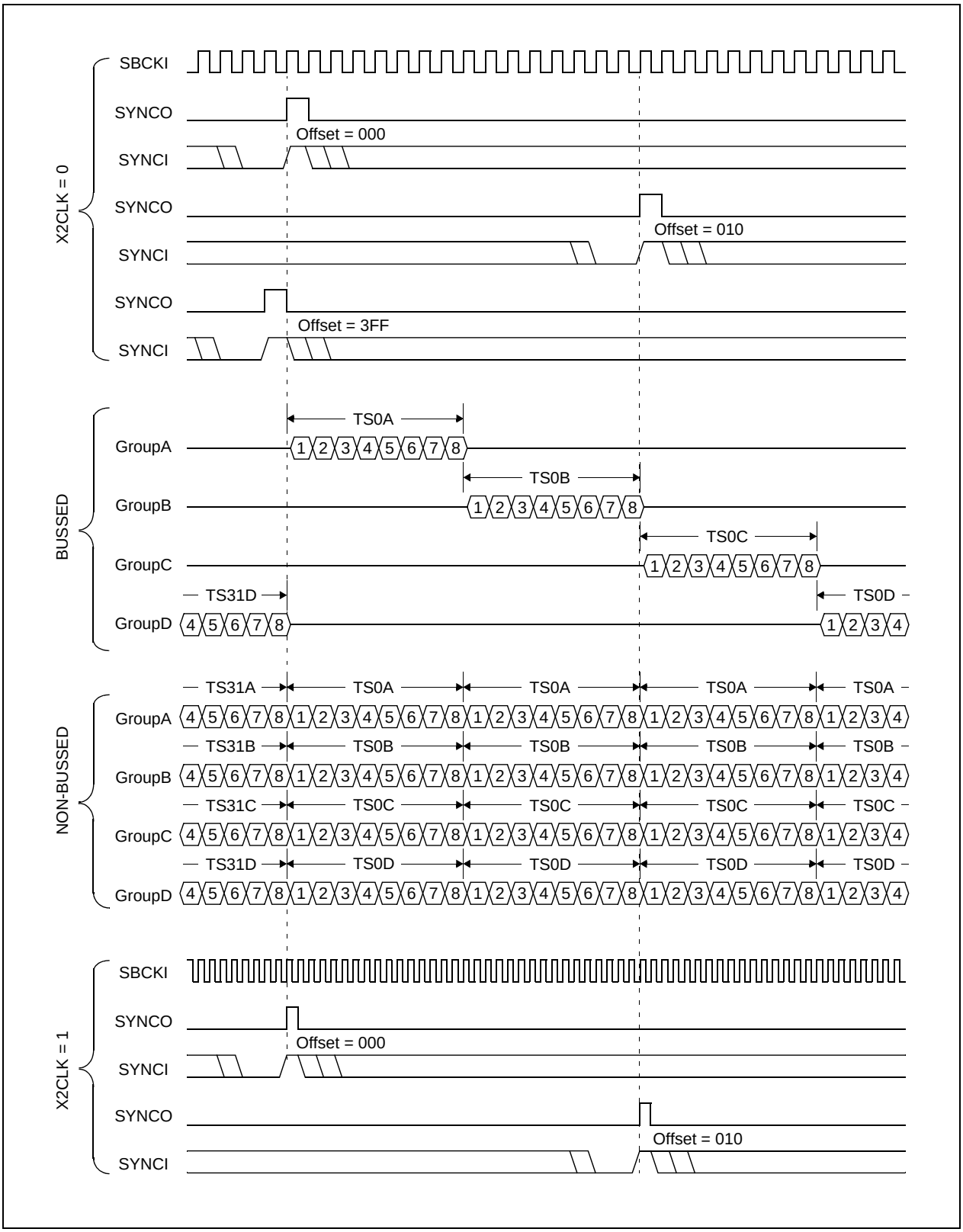
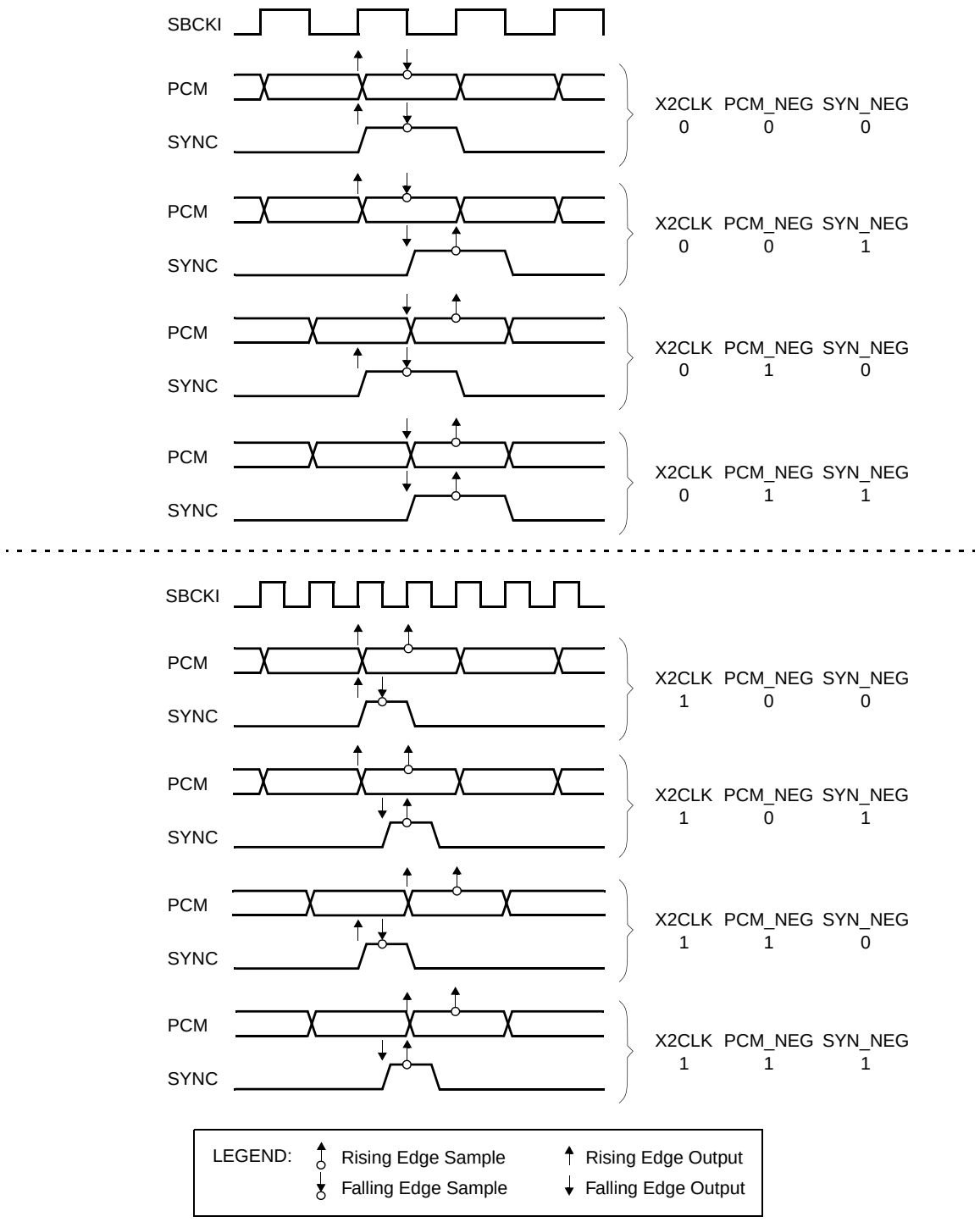


Figure 5-19. SBI Timing—Eight Clock Edge Combinations (Applicable to Any SBI Mode)



NOTE(S): PCM output/sample points are shown only for the corresponding SYNC output/sample point.

5.7 JTAG Interface Timing

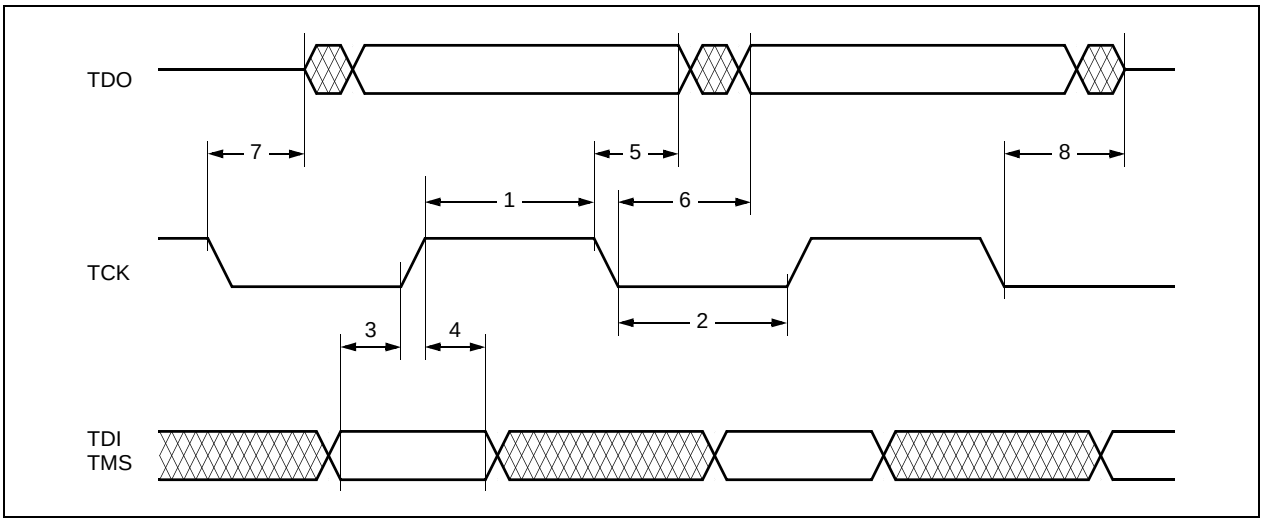
Table 5-17. Test and Diagnostic Interface Timing Requirements

Symbol	Parameter	Minimum	Maximum	Units
1	TCK pulse width high	80	—	ns
2	TCK pulse width low	80	—	ns
3	TMS, TDI setup to TCK rising edge	20	—	ns
4	TMS, TDI hold after TCK high	20	—	ns

Table 5-18. Test and Diagnostic Interface Switching Characteristics

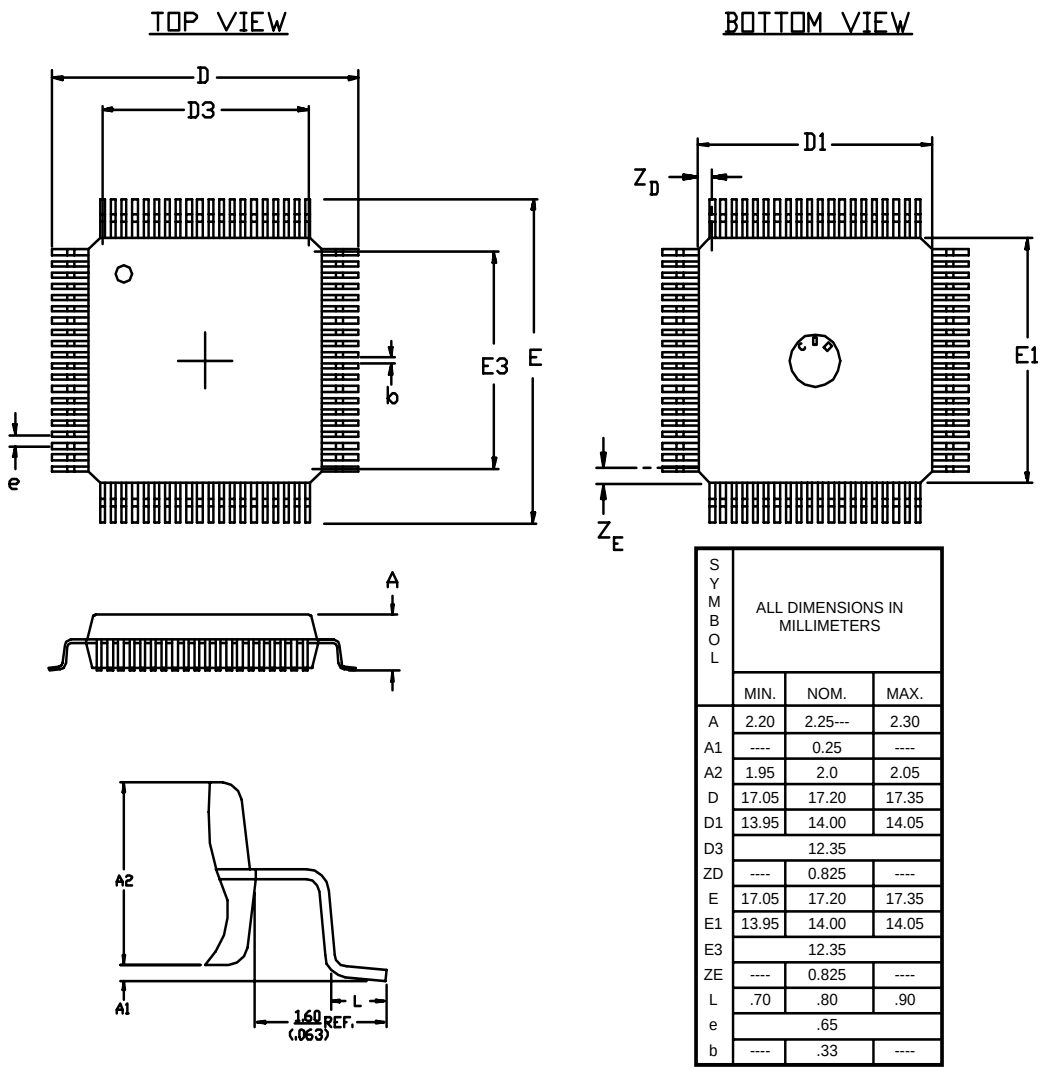
Symbol	Parameter	Minimum	Maximum	Units
5	TDO hold after TCK falling edge	0	—	ns
6	TDO delay after TCK low	—	50	ns
7	TDO enable (Low Z) after TCK falling edge	2	—	ns
8	TDO disable (High Z) after TCK low	—	25	ns

Figure 5-20. JTAG Interface Timing



5.8 Mechanical Specifications

Figure 5-21. 80-Pin Metric Quad Flat Pack (MQFP)



SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.25---	2.30
A1	----	0.25	----
A2	1.95	2.0	2.05
D	17.05	17.20	17.35
D1	13.95	14.00	14.05
D3		12.35	
ZD	----	0.825	----
E	17.05	17.20	17.35
E1	13.95	14.00	14.05
E3		12.35	
ZE	----	0.825	----
L	.70	.80	.90
e		.65	
b	----	.33	----

Appendix A

A.1 Superframe Format (SF)

The Superframe Format (SF), is also referred to as the D4 format. The requirement for associated signaling in frames 6 and 12 dictates that the frames be distinguishable. This leads to a multiframe structure consisting of 12 frames per superframe (SF). See Figure A-1 and Table A-1 and A-2.

The SF structure consists of a multiframe of 12 frames. Each frame has 24 channels, plus an F-bit, and 8 bits per channel. A channel is equivalent to one voice circuit or one 64 kbps data circuit.

This structure of frames and multiframes is defined by the F-bit pattern. The F-bit is designated alternately as an Ft bit (terminal framing bit) or an Fs bit (signalling framing bit). The Ft bit carries a pattern of alternating 0s and 1s (101010) in odd frames that defines the frame boundaries so that one channel can be distinguished from another. The Fs bit carries a pattern of (001110) in even frames, and defines the multiframe boundaries so that one frame can be distinguished from another.

Figure A-1. T1 Superframe PCM Format

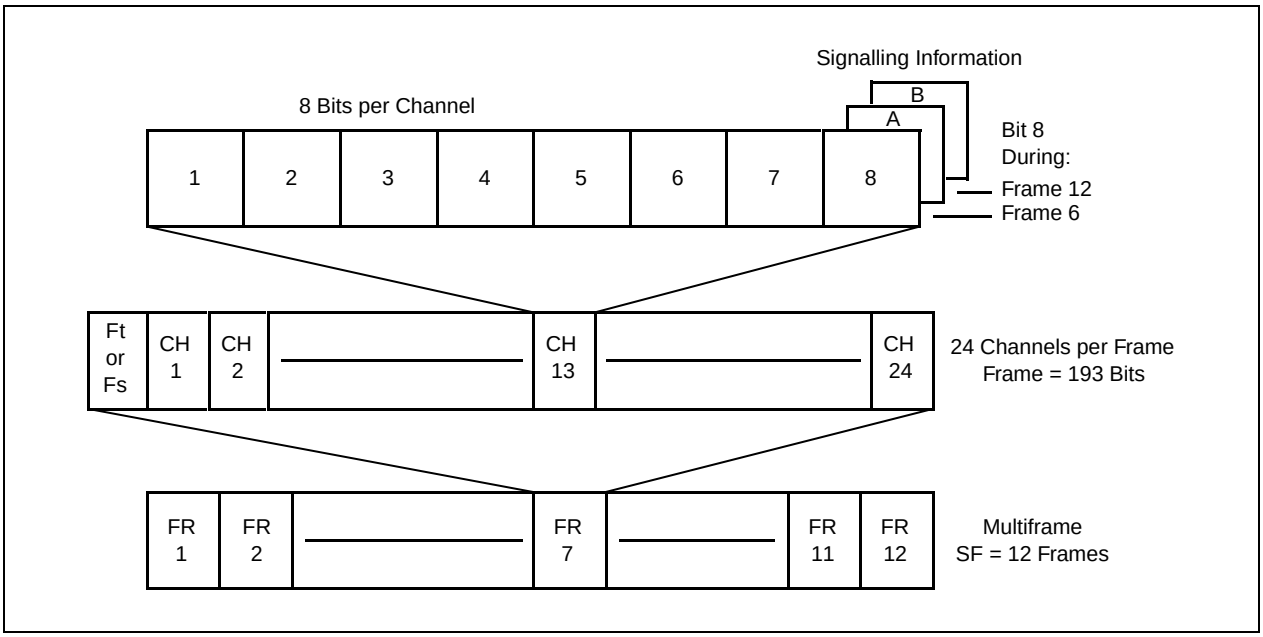


Table A-1. Superframe Format

Frame #	Bit #	F-Bits		Bit Use in Each Time Slot		Signaling Channel
		Terminal Framing Ft	Signaling Framing Fs	Traffic	Signal	
1	0	1	—	1–8	—	—
2	193	—	0	1–8	—	—
3	386	0	—	1–8	—	—
4	579	—	0	1–8	—	—
5	772	1	—	1–8	—	—
6	965	—	1	1–7	8	A
7	1158	0	—	1–8	—	—
8	1351	—	1	1–8	—	—
9	1544	1	—	1–8	—	—
10	1737	—	1	1–8	—	—
11	1930	0	—	1–8	—	—
12	2123	—	0	1–7	8	B

A.2 T1DM Format

Table A-2. T1DM Frame Format

Frame #	Bit #	F-Bits			Bit Use in Each Time Slot	
		Terminal Framing Ft	Signaling Framing Fs	Sync Byte	Info	Ctrl
1	0	1	—	—	1–7	8
1	185–192	—	—	10111YR0	—	—
2	193	—	0	—	1–7	8
2	378–385	—	—	10111YR0	—	—
3	386	0	—	—	1–7	8
3	571–578	—	—	10111YR0	—	—
4	579	—	0	—	1–7	8
4	764–771	—	—	10111YR0	—	—
5	772	1	—	—	1–7	8
5	957–964	—	—	10111YR0	—	—
6	965	—	1	—	1–7	8
6	1150–1157	—	—	10111YR0	—	—
7	1158	0	—	—	1–7	8
7	1343–1350	—	—	10111YR0	—	—
8	1351	—	1	—	1–7	8
8	1536–1543	—	—	10111YR0	—	—
9	1544	1	—	—	1–7	8
9	1729–1736	—	—	10111YR0	—	—
10	1737	—	1	—	1–7	8
10	1922–1929	—	—	10111YR0	—	—
11	1930	0	—	—	1–7	8
11	2115–2122	—	—	10111YR0	—	—
12	2123	—	0	—	1–7	8

Note:
1. Y-bit is used to indicate a Yellow Alarm (active-low).
2. R-bit is used solely by AT&T as an 8 kbps communications channel to collect performance data on long haul DDS facilities.

A.3 SLC 96 Format (SLC)

SLC framing mode allows synchronization to the SLC 96 data link pattern. This pattern, which is described in the *Bellcore TR-TSY-000008*, contains both signaling information and a framing pattern that overwrites the Fs bit of the SF framer pattern (Table A-1). See Table A-3 for SLC-96 Fs bit contents.

Table A-3. SLC-96 Fs Bit Contents

Frame #	Fs Bit	Frame #	Fs Bit	Frame #	Fs Bit
2	0	26	C2	50	0
4	0	28	C3	52	M1
6	1	30	C4	54	M2
8	1	32	C5	56	M3
10	1	34	C6	58	A1
12	0	36	C7	60	A2
14	0	38	C8	62	S1
16	0	40	C9	64	S2
18	1	42	C10	66	S3
20	1	44	C11	68	S4
22	1	46	0	70	1
24	C1	48	1	72	0

Note:
1. The SLC-96 frame format is similar to that of SF as shown in Table A-1 with the exceptions shown in this table.
2. C1 to C11 are concentrator field bits.
3. M1 to M3 are maintenance field bits.
4. A1 and A2 are alarm field bits.
5. S1 to S4 are line switch field bits.
6. The Fs bits in frames 46, 48, and 70 are spoiler bits which are used to protect against false multiframing.

A.4 Extended Superframe Format (ESF)

In Extended Superframe Format (ESF) Figure A-2, and Table A-4, the multiframe structure is extended to 24 frames. The channel structure is identical to D4 (SF) format. Robbed-bit signaling is accommodated in frame 6 (A-bit), frame 12 (B-bit), frame 18 (C-bit), and frame 24 (D-bit).

The F-bit pattern of ESF contains three functions:

1. Framing Pattern Sequence (FPS), which defines the frame and multiframe boundaries.
2. Facility Data Link (FDL), which allows data such as error performance to be passed within the T1 link.
3. Cyclic Redundancy Check (CRC), which allows error performance to be monitored and enhances the reliability of the receiver's framing algorithm.

Figure A-2. T1 Extended Superframe PCM Format

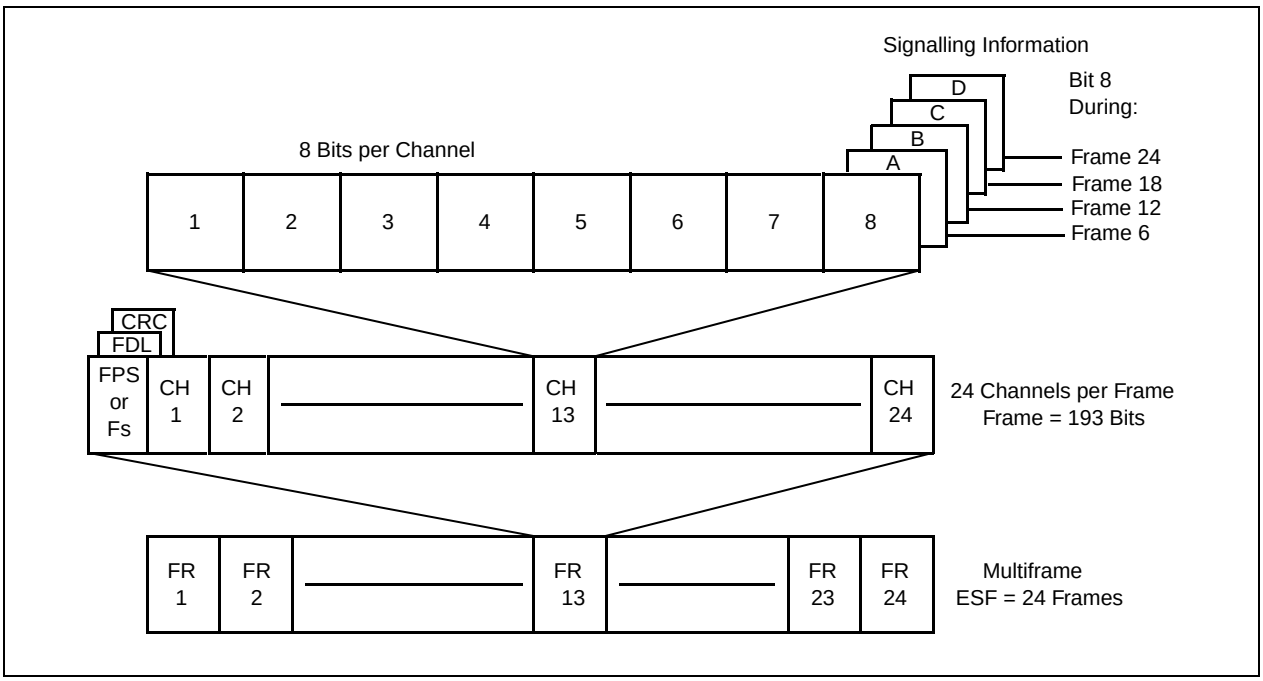


Table A-4. Extended Superframe Format

Frame #	Bit #	F-Bits			Bit Use in Each Time Slot		Signaling Channel		
		FPS	DL	CRC	Traffic	Signal	16	4	2
1	0	—	m	—	1–8	—	—	—	—
2	193	—	—	C1	1–8	—	—	—	—
3	386	—	m	—	1–8	—	—	—	—
4	579	0	—	—	1–8	—	—	—	—
5	772	—	m	—	1–8	—	—	—	—
6	965	—	—	C2	1–7	8	A	A	A
7	1158	—	m	—	1–8	—	—	—	—
8	1351	0	—	—	1–8	—	—	—	—
9	1544	—	m	—	1–8	—	—	—	—
10	1737	—	—	C3	1–8	—	—	—	—
11	1930	—	m	—	1–8	—	—	—	—
12	2123	1	—	—	1–7	8	B	B	A
13	2316	—	m	—	1–8	—	—	—	—
14	2509	—	—	C4	1–8	—	—	—	—
15	2702	—	m	—	1–8	—	—	—	—
16	2895	0	—	—	1–8	—	—	—	—
17	3088	—	m	—	1–8	—	—	—	—
18	3281	—	—	C5	1–7	8	C	A	A
19	3474	—	m	—	1–8	—	—	—	—
20	3667	1	—	—	1–8	—	—	—	—
21	3860	—	m	—	1–8	—	—	—	—
22	4053	—	—	C6	1–8	—	—	—	—
23	4246		m	—	1–8	—	—	—	—
24	4439	1	—	—	1–7	8	D	B	A

Note:
1. FPS indicates the Framing Pattern Sequence (...001011...).
2. DL indicates the 4 kbps Data Link with message bits m.
3. CRC indicates the cyclic redundancy check with bits C1 to C6.
4. Signaling options include 16-state, 4-state, and 2-state.

Table A-5 provides the performance report message structure.

Table A-5. Performance Report Message Structure

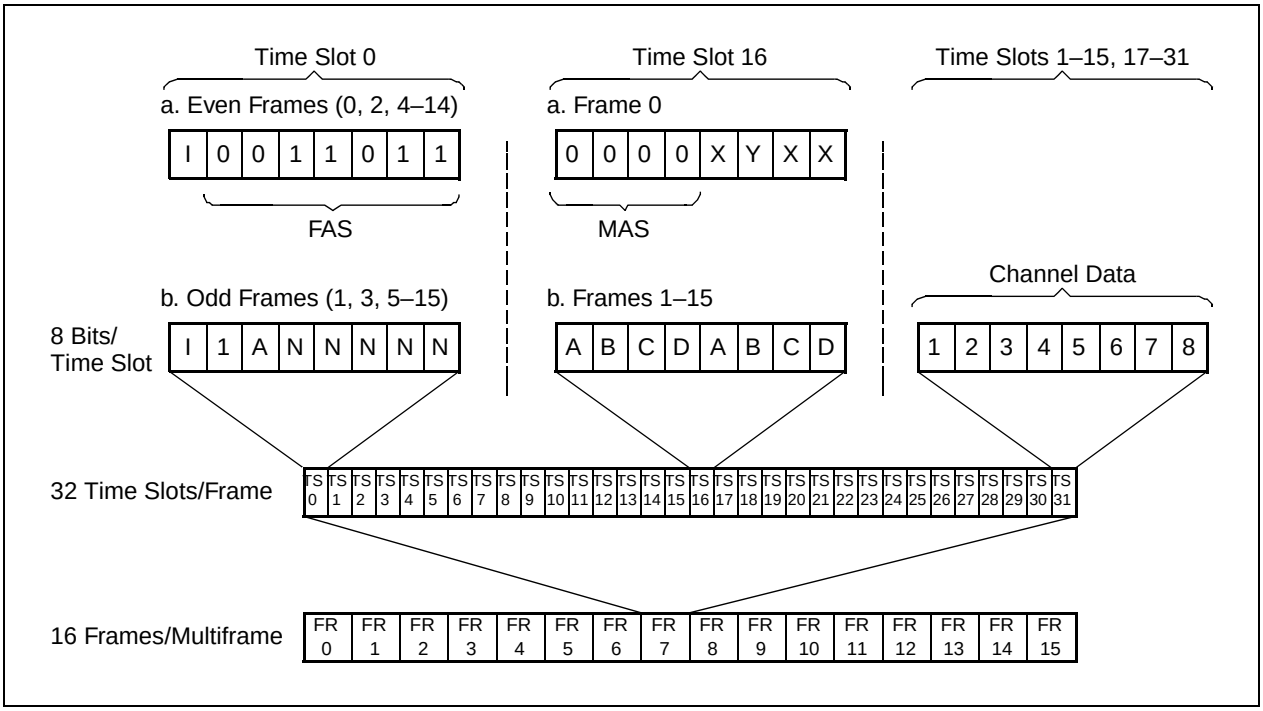
Octet No.	LSB							MSB
1	FLAG							
2	SAPI						C/R	EA
3	TEI							EA
4	CONTROL							
5	G3	LV	G4	U1	U2	G5	SL	G6
6	FE	SE	LB	G1	R	G2	Nm	NI
7	G3	LV	G4	U1	U2	G5	SL	G6
8	FE	SE	LB	G1	R	G2	Nm	NI
9	G3	LV	G4	U1	U2	G5	SL	G6
10	FE	SE	LB	G1	R	G2	Nm	NI
11	G3	LV	G4	U1	U2	G5	SL	G6
12	FE	SE	LB	G1	R	G2	Nm	NI
13	FCS (Most Significant Byte)							
14	FCS (Least Significant Byte)							

Note:
1. The 1-second report consists of octets 5–12.
2. R, U1, and U2 are reserved for future standardization and should be set to 0.

A.5 E1 Frame Format

Figure A-3 illustrates E1 format.

Figure A-3. E1 Format



Tables A-6 and A-7 define the frame format time slot 0-bit allocations for ITU-T CEPT and IRSM CEPT, respectively.

Table A-6. ITU–T CEPT Frame Format Time Slot 0-Bit Allocations

SMF	Frame #	Time Slot 0 Bits 1 to 8 of Each Frame							
		1	2	3	4	5	6	7	8
I	0	C1/Si	0	0	1	1	0	1	1
	1	0/Si	1	A	SA4	SA5	SA6	SA7	SA8
	2	C2/Si	0	0	1	1	0	1	1
	3	0/Si	1	A	SA4	SA5	SA6	SA7	SA8
	4	C3/Si	0	0	1	1	0	1	1
	5	1/Si	1	A	SA4	SA5	SA6	SA7	SA8
	6	C4/Si	0	0	1	1	0	1	1
	7	0/Si	1	A	SA4	SA5	SA6	SA7	SA8
II	8	C1/Si	0	0	1	1	0	1	1
	9	1/Si	1	A	SA4	SA5	SA6	SA7	SA8
	10	C2/Si	0	0	1	1	0	1	1
	11	1/Si	1	A	SA4	SA5	SA6	SA7	SA8
	12	C3/Si	0	0	1	1	0	1	1
	13	E/Si	1	A	SA4	SA5	SA6	SA7	SA8
	14	C4/Si	0	0	1	1	0	1	1
	15	E/Si	1	A	SA4	SA5	SA6	SA7	SA8

Note:
1. SMF indicates the sub-multiframe. This partitioning is used in the CRC-4 calculation.
2. Si bits are International Spare Bits.
3. A bit is used to indicate a remote alarm condition (active-high).
4. SA4 to SA8 are spare bits that may be recommended by ITU–T for use in specific point-to-point applications (e.g., transcoder equipment conforming to Recommendation G.761).
5. SA4 to SA8 where these are not used should be set to 1 on links crossing an international border.
6. E bit is used to indicate a CRC-4 error. The normal state is both bits set to 1, when a CRC-4 error is detected one of the E bits is set to 0.
7. C1 to C4 bits are used to carry the CRC-4 code.
8. Time slot 0 that contains the 0011011 sequence is defined as the FAS word and Time Slot 0 that does not contain the FAS is the Not-Word.

A.6 IRSM CEPT Frame Format

Table A-7. IRSM CEPT Frame Format Time Slot 0-Bit Allocations

SMF	Frame #	Time Slot 0 Bits 1 to 8 of Each Frame							
		1	2	3	4	5	6	7	8
I	0	C1/Si	0	0	1	1	0	1	1
	1	0/Si	1	A	D	E0	E1	E16	E17
	2	C2/Si	0	0	1	1	0	1	1
	3	0/Si	1	A	D	E2	E3	E18	E19
	4	C3/Si	0	0	1	1	0	1	1
	5	1/Si	1	A	D	E4	E5	E20	E21
	6	C4/Si	0	0	1	1	0	1	1
	7	0/Si	1	A	D	E6	E7	E22	E23
II	8	C1/Si	0	0	1	1	0	1	1
	9	1/Si	1	A	D	E8	E9	E24	E25
	10	C2/Si	0	0	1	1	0	1	1
	11	1/Si	1	A	D	E10	E11	E26	E27
	12	C3/Si	0	0	1	1	0	1	1
	13	E/Si	1	A	D	E12	E13	E28	E29
	14	C4/Si	0	0	1	1	0	1	1
	15	E/Si	1	A	D	E14	E15	E30	E31

Note:
1. SMF indicates the sub-multiframe. This partitioning is used in the CRC-4 calculation.
2. Si bits are International Spare Bits.
3. A bit is used to indicate a remote alarm condition (active-high).
4. Ei are per channel control bits.
5. E-bit is used to indicate a CRC-4 error. The normal state is both bits set to 1, when a CRC-4 error is detected, one of the E bits is set to 0.
6. C1 to C4 bits are used to carry the CRC-4 code.
7. Time slot 0 that contains the 0011011 sequence is defined as the FAS word and time slot 0 that does not contain the FAS is the Not-Word.
8. D-bits are a 4 kbps data link.
9. Bit 2 of the Not-Word is defined as the alternate framing bit.

Table A-8 defines the frame format time slot 16-bit allocations for ITU-T CEPT and IRSM CEPT.

Table A-8. CEPT (ITU–T and IRSM) Frame Format Time Slot 16-Bit Allocations

SMF	Frame #	Time Slot 16 Bits 1 to 8 of Each Frame							
		1	2	3	4	5	6	7	8
I	0	0	0	0	0	X0	Y	X1	X2
	1	A1	B1	C1	D1	A17	B17	C17	D17
	2	A2	B2	C2	D2	A18	B18	C18	D18
	3	A3	B3	C3	D3	A19	B19	C19	D19
	4	A4	B4	C4	D4	A20	B20	C20	D20
	5	A5	B5	C5	D5	A21	B21	C21	D21
	6	A6	B6	C6	D6	A22	B22	C22	D22
	7	A7	B7	C7	D7	A23	B23	C23	D23
II	8	A8	B8	C8	D8	A24	B24	C24	D24
	9	A9	B9	C9	D9	A25	B25	C25	D25
	10	A10	B10	C10	D10	A26	B26	C26	D26
	11	A11	B11	C11	D11	A27	B27	C27	D27
	12	A12	B12	C12	D12	A28	B28	C28	D28
	13	A13	B13	C13	D13	A29	B29	C29	D29
	14	A14	B14	C14	D14	A30	B30	C30	D30
	15	A15	B15	C15	D15	A31	B31	C31	D31

Note:
1. SMF indicates the sub-multiframe.
2. Ai–Di are the per channel signaling bits.
3. X0–X2 are the X spare bits normally set to 1.
4. Y is the Remote Multiframe Yellow Alarm Indication bit. When Y is set to a 1, this indicates that the alarm is active.
5. The Multiframe Alignment Sequence (MAS) is defined as the time slot 16 word that contains the 0000XYXX sequence.

Appendix B

B.1 Applicable Standards

Table B-1. Applicable Standards *(1 of 3)*

Standard	Title
ANSI	
T1.101-1987	Digital Hierarchy—Timing Synchronization
T1.102-1993	Digital Hierarchy—Electrical Interfaces
T1.107-1991 (Newer Draft Standard T1X1.4/93-002R3)	Digital Hierarchy—Formats Specification
T1.403-1995	Network to Customer Installation—DS1 Metallic Interface
T1.408-1990	ISDN Primary Rate—Customer Installation Metallic Interfaces
T1.231-1993	Layer 1 In-Service Digital Transmission Performance Monitoring
AT&T	
TR 41449-1986	ISDN Primary Rate Interface Specification
TR 43801(A)-1985	Digital Channel Bank—Requirements and Objectives
TR 54016-1989	Rqts. for Interfacing DTE to Services Employing Extended Superframe Format
TR 62411-1990	Accunet T1.5 Service Description and Interface Specification
Bellcore	
TR-TSY-000008 Issue 2, 1987	Digital Interface Between the SLC 96 Digital Loop Carrier System and a Local Digital Switch
TR-TSY-000009 Issue 1, 1986	Asynchronous Digital Multiplexer Requirements and Objectives
TR-NPL-000054 Issue 1, 1989	High-Capacity Digital Service (HCDS) Interface Generic Requirements
TR-NWT-000057 Issue 2, 1993	Functional Criteria for Digital Loop Carrier Systems
TA-TSY-000147 Issue 1, 1987	DS1 Rate Digital Service Monitoring Unit
TR-TSY-000170 Issue 2, 1993	Digital Cross-Connect System (DCS) Requirements and Objectives
TR-TSY-000191 Issue 1, 1986	Alarm Indication Signal (AIS) Requirements and Objectives

Table B-1. Applicable Standards *(2 of 3)*

Standard	Title
TR-TSY-000194 Issue 1, 1987	The Extended Superframe Format Interface
TA-TSY-000278 Issue 1, 1985	Digital Data System (DDS)—T1 Digital Multiplexer (T1DM) Requirements
TR-TSY-000303 Issue 2, 1992	Integrated Digital Loop Carrier (IDLC) System Generic Requirements
TR-TSY-000312 Issue 1, 1988	Functional Criteria for the DS1 Interface Connector
TR-NPL-000320 Issue 1, 1988	Fundamental Generic Requirements for Metallic Digital Signal Cross-connect Systems
TA-TSY-000435 Issue 1, 1987	DS1 Automatic Facility Protection Switching (AFPS) Rqts. and Objectives
TR-NWT-000499 Issue 5, 1993	Transport Systems Generic Requirements
TR-TSY-000510 Issue 2, 1987	LSSGR: System Interfaces, Section 10
TR-NWT-000773 Issue 1, 1991	Local Access System Requirements, Objectives and Interfaces for SMDS
TR-TSY-000776 Issue 2, 1993	Network Interface Description for ISDN Customer Access
GR-820-CORE Issue 1, 1994 (replaced TR-NWT-000820)	Generic Digital Transmission Surveillance
TA-NWT-000821 Issue 1, 1991 (replaced TR-TSY-000821)	Additional Transport and Transport-Based Surveillance Generic Rqts.
SR-TSY-000977 Issue 1, 1988	ISDN Primary Rate Access Maintenance
TR-NWT-001219 Issue 1, 1992 (Rev 1, 1993)	ISDN Primary Rate Access Testing Requirements
SR-NWT-002343 Issue 1, 1993	ISDN Primary Rate Interface Guidelines for Customer Premises Equipment
ETSI	
ETS 300 011 (4/92)	ISDN Primary Rate User-Network Interface Specification and Test Principles
ETS 300 233	Access Digital Section for ISDN Primary Rate
ITU-T	
Recommendation G.703 (1991)	Physical/Electrical Characteristics of Hierarchical Digital Interfaces
Recommendation G.704 (1991)	Synchronous Frame Structures used at Primary Hierarchical Levels
Recommendation G.706 (1991)	Frame Alignment and CRC Procedures Relating to G.704 Frame Structures
Recommendation G.732	Characteristics of Primary PCM Multiplex Equipment at 2048 kbps
Recommendation G.733	Characteristics of Primary PCM Multiplex Equipment at 1544 kbps
Recommendation G.734	Characteristics of Synchronous Digital Multiplex Equipment at 1544 kbps
Recommendation G.735	Characteristics of Primary PCM Multiplex Equipment at 2048 kbps; offering Synchronous Digital Access at 384 kbps and/or 64 kbps
Recommendation G.736	Characteristics of Synchronous Digital Multiplex Equipment at 2048 kbps
Recommendation G.737	Characteristics of External Access Equipment at 2048 kbps; offering Synchronous Digital Access at 384 kbps and/or 64 kbps
Recommendation G.738	Characteristics of Primary PCM Multiplex Equipment at 2048 kbps; offering Synchronous Digital Access at 320 kbps and/or 64 kbps
Recommendation G.739 Recommendation G.761	Characteristics of External Access Equipment at 2048 kbps; Offering Synchronous Digital Access at 320 kbps and/or 64 kbps

Table B-1. Applicable Standards *(3 of 3)*

Standard	Title
Draft Recommendation G.775	Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection
Recommendation G.796	Characteristics of 64 kbps Cross-Connect Equipment with 2048 kbps Access Ports
Recommendation G.802 (1988)	Interworking between Networks based on Different Digital Hierarchies
Recommendation G.821	Error Performance Monitoring on International Connections
Recommendation G.823 (3/93)	Control of Jitter and Wander in Digital Networks based on 2048 kbps
Recommendation G.824 (3/93)	Control of Jitter and Wander in Digital Networks based on 1544 kbps
Recommendation G.921	Digital Sections based on 2048 kbps Hierarchy
Recommendation G.962 (3/93)	Access Digital Section for ISDN Primary Rate at 2048 kbps
Recommendation G.963 (3/93)	Access Digital Section for ISDN Primary Rate at 1544 kbps
Recommendation I.411	ISDN User-Network Interfaces—References Configurations
Recommendation I.412	ISDN User-Network Interfaces—Structures and Access Capabilities
Recommendation I.421	Primary Rate User-Network Interface
Recommendation I.431	Primary Rate User-Network Interface—Layer 1 Specification
Recommendation K.10	Unbalance about Earth of Telecommunication Installations
Recommendation K.20	Resistibility of Switching Equipment to Overvoltages and Overcurrents
Recommendation M.3604	Application of Maintenance Principles to ISDN Primary Rate Access
Recommendation O.150	Digital Test Patterns for Performance Measurements
Recommendation O.151	Error Performance Measuring Equipment Operating at Primary Rate and Above
Recommendation O.152	Error Performance Measuring Equipment for Bit Rates of 64 kbit/s and NX 64 kbit/s
Recommendation O.162 (10/92)	Equipment to Perform In-Service Monitoring on 2048 kbps Signals
Recommendation Q.921	ISDN User-Network Interface - Data Link Layer Specification
IEEE Std 1149.1a-1993	IEEE Standard Test Access Port and Boundary Scan Architecture (JTAG)
Natural Microsystems Corporation, Release 1.0, March 1993	Multi-Vendor Integration Protocol (MVIP) Reference Manual
FCC Part 68.302 (d)	Environment Simulation metallic voltage surge
FCC Part 68.308	Signal Power Limitations

Appendix C

C.1 System Bus Compatibility

C.1.1 AT&T Concentration Highway Interface (CHI)

DX = RPCMO

- output on rising or falling edge of clock
- output on every CLKXR or CLKXR/2
- Tri-stated during inactive time slots

DR = TPCMI

- sampled on rising or falling edge of clock
- sampled on every CLKXR or CLKXR/2 (see X2CLK mode)

FS = TFSYNC

- sampled on rising or falling edge of clock (FE select)
- rising edge determines frame start
- 8 kHz rate

TSC* = RINDO

- Optional CHI pin is driven low during active DX time slots

CLKXR = TSBCLKI = RSBCLKI

- N x 64 kHz rates, where N=4,8,16,32,48, or 64

C.1.2 CHI Programming Options

CMS = clock mode select
0 = line rate
1 = 2X line rate

XEN = transmitter enable
0 = disable (DX tri-stated)
1 = enable (DX driven during active time slots)

FE = frame edge select
0 = falling edge
1 = rising edge

XCE = CLKXR output edge select for DX
0 = falling edge
1 = rising edge

RCE = CLKXR input edge select for DR
0 = falling edge
1 = rising edge

XBOFF = 3-bit transmit output bit offset
000-1111= CLKXR (or 2xCLKXR) delay from FS to DX bit0

RBOFF = 3-bit receive input bit offset
000-111 = CLKXR (or 2xCLKXR) delay from FS to DR bit0

XTS = 6-bit transmit output TS offset
00-3F = CLKXR (or 2xCLKXR) TS delay from FS to DX bit0

RTS = 6-bit receive input TS offset
00-3F = CLKXR (or 2xCLKXR) TS delay from FS to DR bit0

Bt8370 only supports CHI and GCI buses if N = 24, 32 or 48, although either bus is defined to operate at Nx64 from N = 4 to N = 48. Bt8370 does not support AT&T's Dual CHI (separate A/B buses) or K2 buses, nor does it support INTEL's SLD (ping/pong) 3-pin bus.

Appendix D

D.1 Notation and Acronyms

D.1.1 Arithmetic Notation

Time slot bit numbering associated with time slots in the primary rate channel are numbered 1 to 8, where bit number 1 is transmitted first and is specified as the MSB.

Configuration and Status Word Bit Numbering associated with configuration or status words are numbered 7 to 0, where bit number 7 is specified as the MSB, and bit number 0 is specified as the LSB.

D.2 Acronyms and Abbreviations

ADC	Analog to Digital Converter
AFPS	Automatic Facility Protection Switching
AGC	Automatic Gain Control
AIS	Alarm Indication Signal
ALBO	Automatic Line Build Out
ALOS	Analog Loss of Signal
AMI	Alternate Mark Inversion
ANSI	American National Standards Institute
B8ZS	Binary with 8 Zero Substitution
BER	Bit Error Rate
BERR	Bit Error Counter
BFA	Basic Frame Alignment
BOP	Bit-Oriented Protocol
BPV	Bipolar Violation
BSDL	Boundary Scan Description Language
CAS	Channel Associated Signaling
ITU–T	International Telegraph and Telephone Consultative Committee
CCS	Common Channel Signaling
CERR	CRC Errors
CGA	Carrier Group Alarm
CI	Customer Installation
CLAD	Clock Rate Adapter
CMOS	Complementary Metal Oxide Semiconductor
COFA	Change of Frame Alignment
CRC	Cyclic Redundancy Check
CSU	Channel Service Unit
DAC	Digital to Analog Converter
DCS	Digital Cross-Connect System
DDS	Digital Data System
DMI	Digital Multiplexed Interface
DPLL	Digital Phase Locked Loop
DPM	Driver Performance Monitor
DS1	Digital Signal Level 1
DSU	Data Service Unit
ESF	Extended Superframe
EXZ	Excessive Zeros
FAS	Frame Alignment Sequence (E1 Format)
FCC	Federal Communications Committee
FCS	Frame Check Sequence
FDL	Facility Data Link
FEBE	Far End Block Error
FERR	Framing Bit Error
FPS	Frame Pattern Sequence (ESF Format)

HCDS	High-Capacity Digital Service
HDB3	High-Density Bipolar of Order 3
ICOT	Intercity and Outstate Trunk
IDLC	Integrated Digital Loop Carrier
ISDN	Integrated Service Digital Network
JAT	Jitter Attenuator
JCLK	Jitter Attenuated Clock
JTAG	Joint Test Action Group
LBO	Line Build Out
LCV	Line Code Violation
LEC	Local Exchange Carrier
LIU	Line Interface Unit
LOAS	Loss of Analog Signal
LOF	Loss of Frame
LOS	Loss of Signal –DS1
LSB	Least Significant Bit
MAIS	Multiframe AIS
MART	Maximum Average Reframe Time
MAS	Multiframe Alignment Sequence (CAS Format)
MAT	Metropolitan Area Trunk
MERR	MFAS Error
MFAS	Multiframe Alignment Sequence (CRC4 format)
MOP	Message-Oriented Protocol
MOS	Message Oriented Signaling
MPU	Microprocessor Interface
MQFP	Metric Quad Flat Pack
MSB	Most Significant Bit
MVIP	Multi-Vendor Integration Protocol
MYEL	Multiframe Yellow Alarm
NCO	Numerical Controlled Oscillator
NI	Network Interface
NRZ	Non-Return to Zero
OOF	Out of Frame
PDV	Pulse Density Violation
PIC	Polyethylene-insulated Cable
PLCC	Plastic Leaded Chip Carrier
PLL	Phase Locked Loop
PM	Performance Monitoring
PQFP	Plastic Quad Flat Pack
PRBS	Pseudo-Random Bit Sequence
PRI	Primary Rate Interface
PRM	Performance Report Message
RAI	Remote Alarm Indication
RBOP	Bit-Oriented Protocol Detector
RBS	Robbed Bit Signaling
RCVR	Receiver

RDL1	Receive Data Link 1
RDL2	Receive Data Link 2
RDL3	External Receive Data Link
RFRAME	Receive Framer
RJAT	Receive Jitter Attenuator
RLIU	Receive Line Interface Unit
RMAIS	Receive Multiframe AIS
RPDV	Receive Pulse Density Violation
RPLL	Receive Phase Locked Loop
RSB	Receive System Bus
RSBI	Receive System Bus Interface
RSIG	Receive Signaling Buffer
RSLIP	Receive Slip Buffer
RXCLK	Receive Clock
RZCS	AMI/HDB3/B8ZS Line Decoder
QRSS	Quasi-Random Signal Source
SEF	Severely Errored Framing Event
SERR	CAS Error
SF	Super Frame
SLC	Subscriber Loop Carrier
TAP	Test Access Port
TBOP	Bit Oriented Protocol Formatter
TDL1	Transmit Data Link 1
TDL2	Transmit Data Link 2
TDL3	External Transmit Data Link
TDM	Time Division Multiplexed
TSB	Transmit System Bus
TSBI	Transmit System Bus Interface
TJAT	Transmit Jitter Attenuator
TLIU	Transmit Line Interface Unit
TLOS	Transmit Loss of Signal
TSB	Transmit System Bus
TSIC	Time Slot Inter-Change
TSIG	Transmit Signaling Buffer
TSLIP	Transmit Slip Buffer
TZCS	AMI/HDB3/B8ZS Line Encoder
UI	Unit Interval
UMC	Unassigned Mux Code
UNICODE	Universal Trunk Out Of Service Code
UTP	Unshielded Twisted Pair
VCO	Voltage Controlled Oscillator
VCXO	Voltage Controlled Crystal Oscillator
VGA	Variable Gain Amplifier
XMTR	Digital Transmitter
YEL	Yellow Alarm
ZCS	Zero Code Suppression

D.2.1 Revision History

Rev	
A	Initial Release
B	Technical Corrections
C	Technical Corrections
D	Technical Corrections (added changes for Bt8375 and Bt8376)

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Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения **«JONHON»**, а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов **«FORSTAR»**.

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