

NJU26060 Series Hardware Specification

■ General Description

The NJU26060 Series is a high performance 24-bit digital signal processor. The NJU26060 Series provides stereo PWM modulators, one Sampling Rate Converter(SRC), Digital Interface Transmitter(DIT) and four GPI/O ports.

The NJU26060 Series with the OTP(One Time Programmable) function provides the wide range of applications of sound technologies and fast time to market service.

■ Package



NJU26060V

■ Features

- Hardware

- 24bit Fixed-point Digital Signal Processing
- Maximum Clock Frequency : 24.576MHz (Standard), Embedded PLL Circuit
- PWM modulator : stereo 4ch Outputs
- Sampling rate converter (SRC) : $F_s=8\text{kHz} \sim 192\text{kHz}$ 48kHz
- Digital interface transmitter (DIT)
- Digital Audio Interface : 3 Input ports / 3 Output ports
- Digital Audio Format : I²S 24bit, Left-justified, Right-justified, BCK : 32/64fs
- Master / Slave Mode
 - Sampling Rate Converter: Slave mode
 - In Master Mode: MCKO(256 or 512fs), BCKO(64 or 32fs), BCK (1fs)
- Host Interface
 - I²C Bus (Fast-mode/400kbps)
- Power Supply : $V_{DD} = 3.3\text{V}$
- Input terminal: : 5V Input tolerant
- Package : SSOP44 (Pb-Free)

NJU26060 Series

DSP Block Diagram

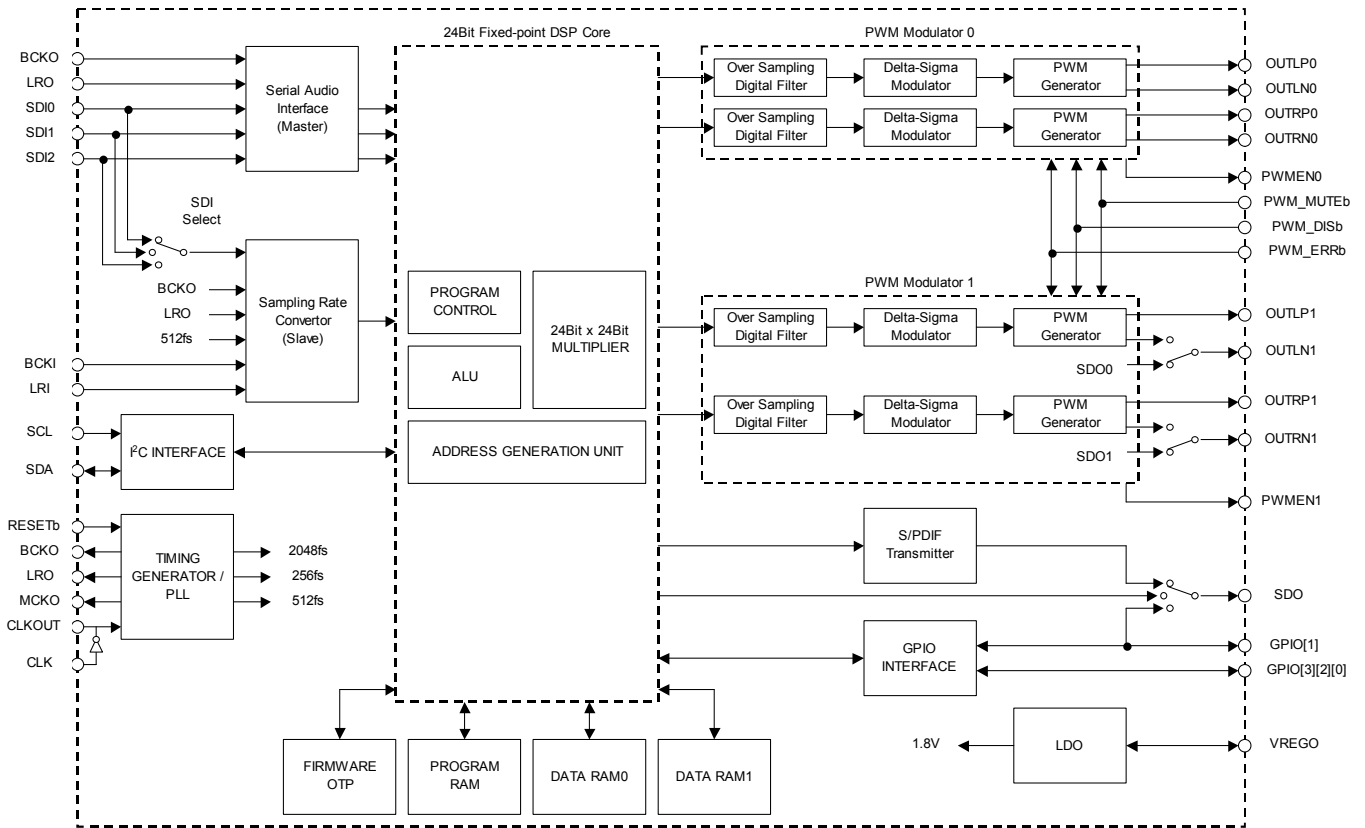


Fig.1 NJU26060 Series Block Diagram

■ Pin Configuration

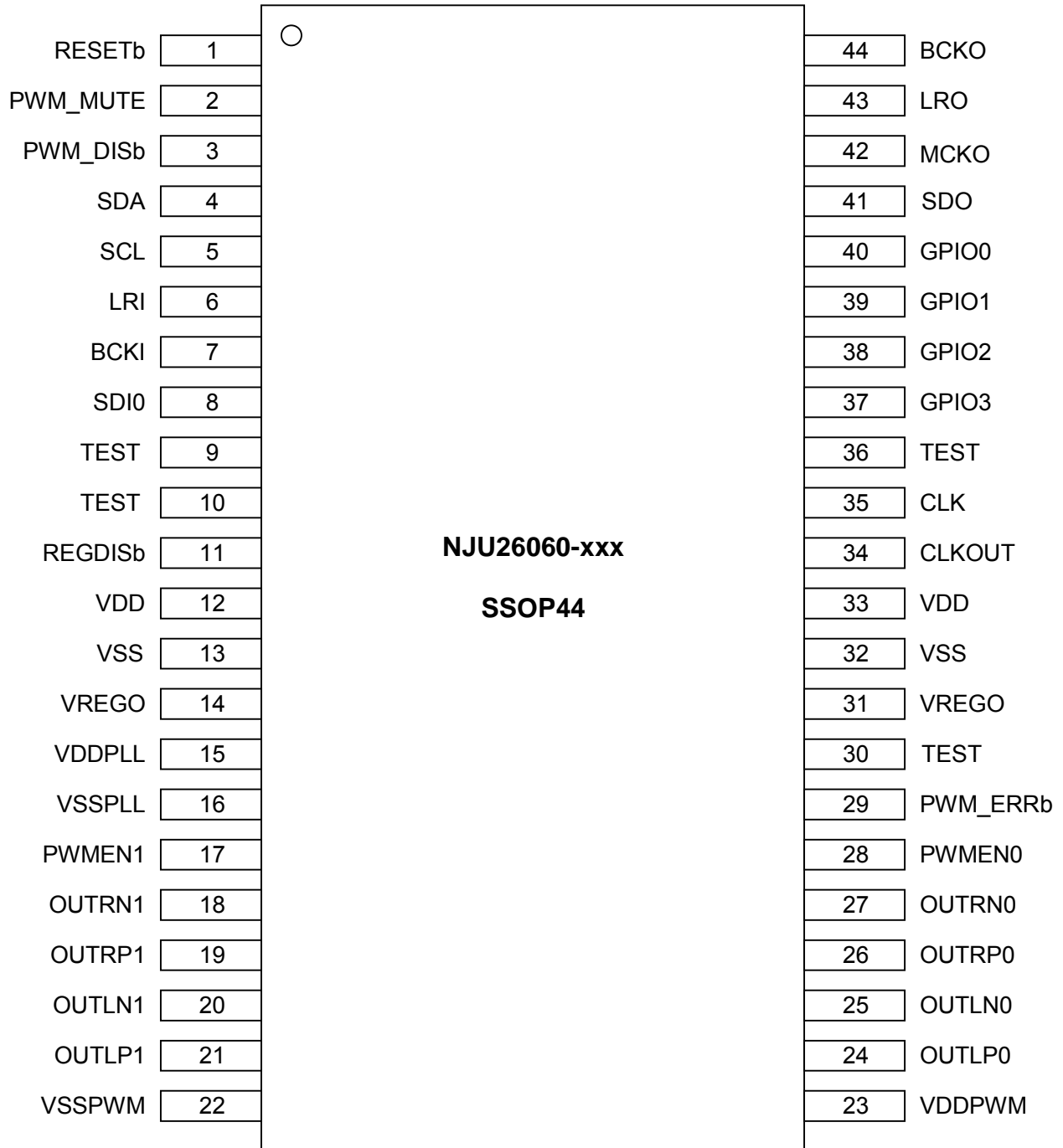


Fig.2 NJU26060 Series Pin Configuration

NJU26060 Series

■ Pin Description

Table 1. Pin Description

| Pin No. | Symbol | I/O | Description |
|---------|-----------|-----|---|
| 1 | RESETb | I | Reset (RESETb="Low" : DSP Reset) |
| 2 | PWM_MUTEb | I+ | PWM Block Mute request input |
| 3 | PWM_DISb | I+ | PWM Block Standby request input |
| 4 | SDA | OD | I ² C I/O |
| 5 | SCL | I | I ² C clock |
| 6 | LRI | I- | LR Clock Input for Fs conversion side |
| 7 | BCKI | I- | Bit Clock Input for Fs conversion side |
| 8 | SDI0 | I | Audio Data Input 0 (L/R) |
| 9 | TEST | I | For Test (connected to VSS) |
| 10 | TEST | I | For Test (connected to VSS) |
| 11 | REGDISb | I | Built-in Power Supply Enable |
| 12 | VDD | - | Power Supply +3.3V |
| 13 | VSS | - | GND |
| 14 | VREGO | PI | Built-in Power Supply Bypass |
| 15 | VDDPLL | - | PLL Power Supply +1.8V |
| 16 | VSSPLL | - | PLL Power Supply GND |
| 17 | PWMEN1 | O | PWM1 enable output (PWMEN1='1': enable) |
| 18 | OUTRN1 | OP | PWM1 R- output / Audio Data output 1 (setting Firmware) |
| 19 | OUTRP1 | OP | PWM1 R+ output |
| 20 | OUTLN1 | OP | PWM1 L- output / Audio Data output 0 (setting Firmware) |
| 21 | OUTLP1 | OP | PWM1 L+ output |
| 22 | VSSPWM | - | PWM Power Supply GND |
| 23 | VDDPWM | - | PWM Power Supply +3.3V |
| 24 | OUTLP0 | OP | PWM0 L+ output |
| 25 | OUTLN0 | OP | PWM0 L- output |
| 26 | OUTRP0 | OP | PWM0 R+ output |
| 27 | OUTRN0 | OP | PWM0 R- output |
| 28 | PWMEN0 | O | PWM0 enable output (PWMEN0='1': enable) |
| 29 | PWM_ERRb | I+ | PWM block stop request input (PWM_ERRb='0': PWM stop) |
| 30 | TEST | I | for Test (connected to VSS) |
| 31 | VREGO | PI | Built-in Power Supply Bypass |
| 32 | VSS | - | GND |
| 33 | VDD | - | Power Supply +3.3V |
| 34 | CLKOUT | O | OSC Output |
| 35 | CLK | I | OSC Clock Input |
| 36 | TEST | I- | for Test (connected to VSS) |
| 37 | GPIO3 | I/O | General Purpose IO 3 / for TEST |
| 38 | GPIO2 | I/O | General Purpose IO 2 / for TEST |
| 39 | GPIO1 | I/O | General Purpose IO 1 / for TEST |
| 40 | GPIO0 | I/O | General Purpose IO 0 / for TEST |
| 41 | SDO | O | DIT output / Audio Data Output 2 (setting Firmware) |
| 42 | MCK | O | Master Clock Output for A/D, D/A |
| 43 | LRO | O | LR clock Output |
| 44 | BCKO | O | Bit clock Output |

Note :

- I : Input
- I+ : Input (Pull-up)
- OD : Bi-directional (Open Drain) This pin requires a pull-up resistance.
- I/O : Bi-directional
- OP : PWM output(supply for VDDPWM)
- O: Output
- I -: Input (Pull-down)
- PI: Built-in Power Supply Bypass

NOTICE: Does not keep the terminal without the pull-up resistance or the pull-down resistance open.
The functions of SDIO0 to SDIO2, SDO, OUTxxx depend on the IC specifications.

■ Absolute Maximum Ratings

Table2 Absolute Maximum Ratings ($V_{SS}=V_{SSPLL}=V_{SSIO}=0V, T_a=25^{\circ}C$)

| Parameter | Symbol | Rating | Units | |
|-------------------------|--------------------|---|--------------------------------------|---|
| Supply Voltage * | V_{DD}, V_{DDPW} | -0.3 to 4.2 | V | |
| Supply Voltage Bypass * | V_{REGO} | -0.3 to 2.3 | | |
| Supply Voltage PLL * | V_{DDPLL} | -0.3 to 2.3 | | |
| Terminal Voltage * | In | $V_{x(IN)}$ | -0.3 to 5.5 ($V_{DDIO} \geq 3.0V$) | V |
| | I/O, O/D | $V_{x(I/O)}, V_{x(OD)}$ | -0.3 to 4.2 ($V_{DDIO} < 3.0V$) | |
| | Out | $V_{x(OUT)}$ | -0.3 to 4.2 | |
| | CLK | $V_{x(CLK)}$ | -0.3 to 4.2 | |
| | CLKOUT | $V_{x(CLKOUT)}$ | -0.3 to 4.2 | |
| Power Dissipation | P_D | 800 It mounts on the board of the EIAJ spec. 76.2 x 114.3 x 1.6mm, 2layer, FR-4 | mW | |
| Operating Temperature | T_{OPR} | -40 to 85 | $^{\circ}C$ | |
| Storage Temperature | T_{STR} | -40 to 125 | $^{\circ}C$ | |

- * V_{DD} : 12, 33 pin
- * V_{DDPW} : 23 pin
- * V_{REGO} : 14, 31 pin
- * V_{DDPLL} : 15 pin
- * $V_{x(IN)}$: 1~3, 5~11, 29, 30, 36 pin
- * $V_{x(OD)}$: 4 pin
- * $V_{x(I/O)}$: 37~40 pin
- * $V_{x(OUT)}$: 17~21, 24~28, 41~44 pin
- * $V_{x(CLK)}$: 35 pin
- * $V_{x(CLKOUT)}$: 34 pin

■ Equivalent Circuits

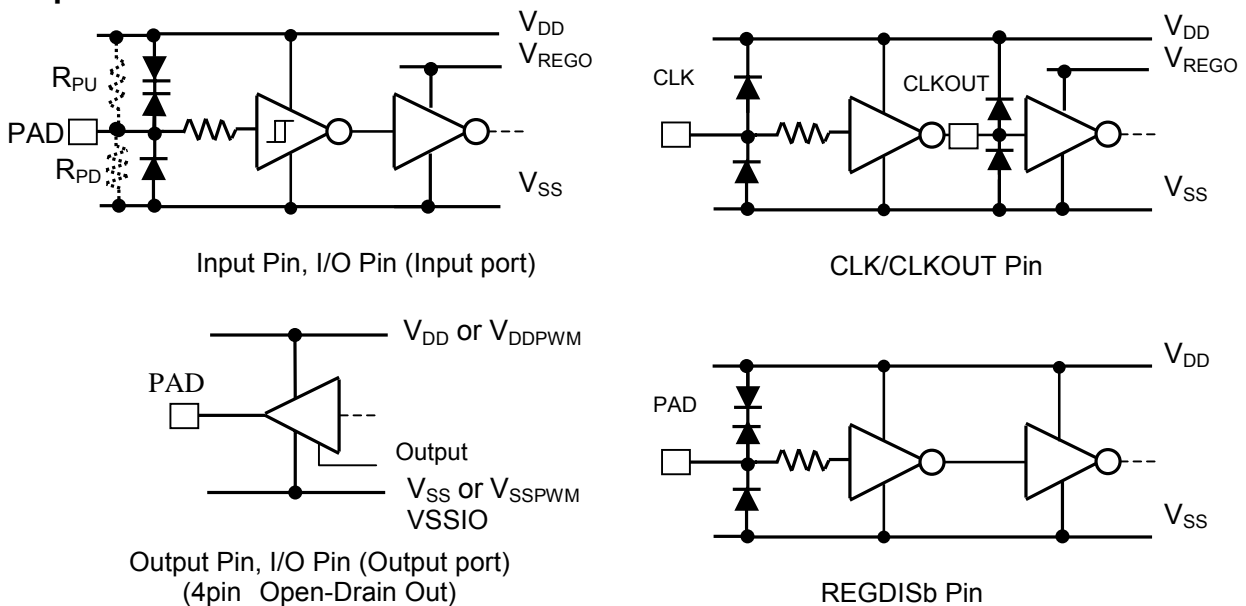


Fig.3 NJU26060 Series Equivalent Circuits

NJU26060 Series

■ Electric Characteristics

Table3 Electric Characteristics ($V_{DD}=V_{DDPWM}=3.3V$, $f_{OSC}=24.576MHz$, $T_a=25^{\circ}C$)

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Units |
|------------------------------|---------------|----------------------------------|---------------------|-------------------|---------------------|---------|
| Operating Voltage *1 | V_{DD} | V_{DD} , V_{DDPWM} Pin | 3.0 | 3.3 | 3.6 | V |
| Operating Current | I_{DD} | AT no Load, $V_{DD} + V_{DDPWM}$ | - | 35 | 50 | mA |
| High Level Input Voltage | V_{IH} | | $V_{DD} \times 0.7$ | - | $V_{DD} *2$ | V |
| Low Level Input Voltage | V_{IL} | | 0 | - | $V_{DD} \times 0.3$ | |
| High Level Output Voltage *3 | V_{OH} | $I_{OH} = -1mA$ | $V_{DD} \times 0.8$ | - | V_{DD} | |
| Low Level Output Voltage | V_{OL} | $I_{OL} = 1mA$ | 0 | - | $V_{DD} \times 0.2$ | |
| Terminal Leakage Current *4 | I_{IN} | $V_{IN} = V_{SS} \sim V_{DD}$ | -10 | - | 10 | μA |
| | $I_{IN(PU)}$ | | -120 | - | 10 | |
| | $I_{IN(PD)}$ | | -10 | - | 120 | |
| Clock Frequency | f_{OSC} | CLK Pin *5 | 20 | 22.5792 24.576 | 25 | MHz |
| Ext. System Clock Duty Cycle | Γ_{EC} | | 45 | 50 | 55 | % |

*1 Please use the V_{DD} , V_{DDpwm} within the electric characteristics. V_{DD} , V_{DDpwm} is monotonous increase. Don't drop voltage under the electric characteristics after booting V_{DD} , V_{DDpwm} to regulation voltage. When it turns off DSP and turns on DSP again, it is necessary to drop V_{DD} to GND level. Then it turns on DSP again.

*2 Input pin, Output pin and Open-Drain input/output pin are +5.0V tolerant except CLK input pin.

*3 Except 4pin (Open-Drain I/O) input pin.

*4 $I_{IN(PU)}$: 2,3,29,37,38pin, $I_{IN(PD)}$: 6~10,36,39,40 pin

*5 Please give usually the clock of 24.576MHz using for 48kHz and 22.5792MHz using for 44.1kHz.
An internal sampling frequency is 1/512 of the input clock frequency.

1. Power ,Clock and Reset

1.1 Power Supply

The NJU26060 Series has three power supplies V_{DD}/V_{SS} , V_{DDPLL}/V_{SSPLL} and V_{DDPWM}/V_{SSPWM} . V_{DD}/V_{SS} is used as an internal core supply, V_{DDPLL}/V_{SSPLL} is used as an internal PLL power supply and V_{DDPWM}/V_{SSPWM} is used as PWM output power supply.

The NJU26060 has a power supply V_{DD}/V_{SS} , V_{DDPLL}/V_{SSPLL} . To setup good power supply condition, the decoupling capacitors should be implemented at the all power supply terminals.

Please use the V_{DD}/V_{DDPWM} within the electric characteristics. V_{DD}/V_{DDPWM} is monotonous increase. Don't drop voltage under the electric characteristics after booting V_{DD}/V_{DDPWM} to regulation voltage. When it turns off DSP and turns on DSP again, it is necessary to drop V_{DD}/V_{DDPWM} to GND level. Then it turns on DSP again.

V_{DDPWM}/V_{SSPWM} is used as PWM output :OUTLP0, OUTLN0, OUTRP0, OUTLP1, OUTLN1, OUTRP1 power supply. V_{DD}/V_{SS} has a same power supply.

The NJU26060 include a built-in power supply (LDO) for internal logic. A built-in power supply generates 1.8V (-10% to +10%). VREGO (No.14,31) pin is a built-in power supply bypass pin. Connect low-ESR capacitor of 0.01uF in parallel between VSS (No.13,32) pin.

The NJU26060 include PLL for internal logic and PWM modulator. PLL power has V_{DDPWM}/V_{SSPWM} , but an include circuit unconnected straight for each other power. PLL power is supply for VREGO (No.14).

Connect the decoupling capacitor of 0.01uF in parallel between V_{DDPLL} and V_{SSPLL} . V_{SSPLL} is connected V_{SS} .

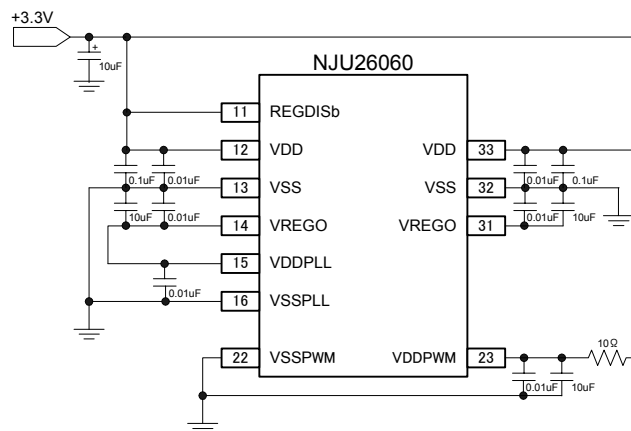


Fig.4 Simple power filter sample

A built-in power supply is used only for NJU26060 operation. Be not short-circuited of this pin. Do not take out the current, and connect other power supplies.

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1.2 Input/Output terminal

It restricts, when the input terminals, the input/output terminals and the bi-directional Open-drain terminal of NJU26060, and V_{DD} are supplied on regular voltage ($V_{DD}=3.3V$), and it becomes +5V Input tolerant.

1.3 Clock

The NJU26060 CLK pin requires the system clock that should be related to the sample frequency 512 Fs using the PWM modulator.

It is possible to be generated the system clock by connecting a crystal oscillator between CLK and CLKOUT. CLK/CLKOUT pins are not 5V tolerant, so check the voltage level of these pins.

Note: When the crystal oscillator supplies the clock, the characteristic of the NJU26060 series is secured. However, when the clock of external generation is supplied, the characteristic of the sampling rate converter and the PWM modulator might be deprived.

1.4 Reset

To initialize the NJU26060, RESETb pin should be set Low level during some period. After some period of Low level, RESETb pin should be High level. This procedure starts the initialization of the NJU26060. After the power supply and the oscillation of the NJU26060 becomes stable, RESETb pin must be kept Low-level more than t_{RESETb} period. (Fig.5)

After RESETb pin level goes to "High" (after reset release), a setup of the internal hardware of a Serial Host Interface completes NJU26060. Then, it will be in the state which can communicate.

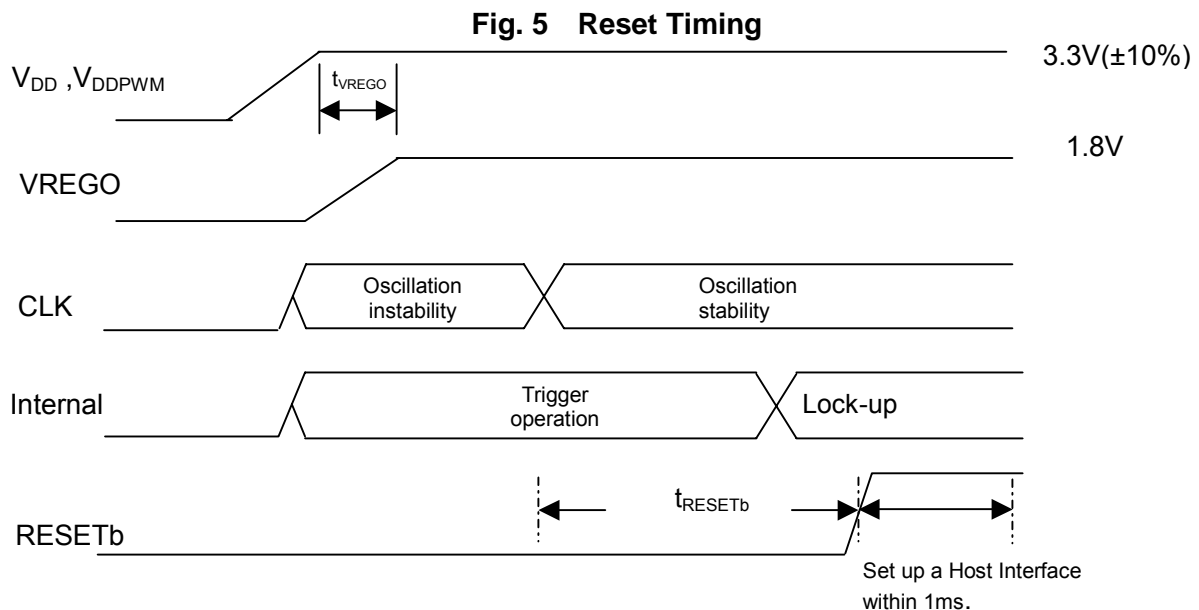


Table 4 Reset time

| Symbol | Time |
|--------------|----------------------|
| t_{VREGO} | $\geq 10\text{msec}$ |
| t_{RESETb} | $\geq 10\text{msec}$ |

NOTICE: All the output terminals are irregular from turning on the power supply to the internal reset completion. Especially, when the terminal PWMEN0/1 is used by the control signal, the redundant design is needed to protect the system.

Do not stop providing clock during operation. If stopped, the built-in PLL cannot provide a normal clock toward internal NJU26060 series doesn't work correctly.

2. Digital Audio Clock

Digital audio data needs to synchronize and transmit between digital audio systems. When the sampling rate converter is not used, the NJU26060 series is used as a master mode. Sampling rate converter is supported for slave mode only.

- In Master mode;
The clock of MCKO, BCKO, and LRO is used for digital audio data transfer as a clock of other slave devices.
- In Slave mode;
BCKI and LRI input the clock from other master devices.

2.1 Audio Clock

Three kinds of clocks are needed for digital audio data transfer.

- (1) LR clock (LRI, LRO) is needed by serial-data transmission. It is the same as the sampling frequency of a digital audio signal.
- (2) Bit clock (BCKI, BCKO) is needed by serial-data transmission. It becomes the multiple of LR clock.
- (3) Master clock (MCKO) needed by A/D, D/A converter, etc. It becomes the multiple of LR clock. It is not related to serial audio data transmission.

The NJU26060 series support serial data format that includes 32(32fs) or 64(64fs) BCK clocks.

The NJU26060 Series supplies the clock necessary for digital audio data transmission to an external device as a master device by each terminal of MCKO, BCKO, and LRO. On the other hand, the sampling rate converter that works as a slave device takes digital audio data with the clock input to BCKI and the terminal LRI, and converts the sampling frequency into the clock system composed of MCKO/BCKO/LRO. After internal reset ends as a master clock, the terminal MCKO sets the buffer output or 2 dividing frequency the output of the input clock to the terminal CLK. The stop is also possible according to the command of the firmware.

The NJU26060 Series is used by 512 times the internal operation sampling frequency (It is 24.576MHz in the sampling frequency 48kHz). In that case, NJU26060 can output 64 times, 32 times the bit clock to of the LR clock one time the sampling frequency and of each, and 512 times and 256 times the master clock as a mastering device. Table 5 shows the relation of each clock.

Table 5 Supply Clock for CLK pin Frequency and BCKO,LRO,MCKO

| Clock Signal | Multiple Frequency | Clock Frequency | |
|--------------|--------------------|-----------------|-----------|
| | | 22.5792MHz | 24.576MHz |
| LRO | 1Fs | 44.1kHz | 48kHz |
| BCKO(32Fs) | 32Fs | 1.4112MHz | 1.536MHz |
| BCKO(64Fs)* | 64Fs | 2.8224MHz | 3.072MHz |
| MCKO(256Fs)* | 256Fs | 11.2896MHz | 12.288MHz |
| MCKO(512Fs) | 512Fs | 22.5792MHz | 24.576MHz |

* default for starting up

3. Sampling Rate Converter (SRC)

The NJU26060 Series provide the stereo (two channels) Sampling Rate Converter (SRC). The internal audio sampling frequency (F_s) is 1/512 of the CLK pin.

The SRC can convert an arbitrary sampling frequency ($F_s=8\text{kHz}$ to 192kHz) into the internal sampling frequency ($F_s=\text{CLK}/512$). For example, $\text{CLK}=24.576\text{MHz}$ at $F_s=48\text{kHz}$, $\text{CLK}=22.5792\text{MHz}$ at $F_s=44.1\text{kHz}$.

3.1 Automatic Sample-frequency Detection

The NJU26060 Series provide the automatic sampling-frequency detection to provide the best converting performance. When the sample frequency changes on a large scale, this automatic detection resets the SRC.

To detect the sampling frequency change, the NJU26060 Series count the length of the LRI clock, every 2,048 LRI clock. In case of $\text{CLK}=24.576\text{MHz}$ and $\text{LRI}=48\text{kHz}$, the count of length is $24,576/48=512$. The LRI and CLK are asynchronous, so the negligible error count is about ± 1 clock. The detection block compares the previous counts f_{LRI} with the current counts $f_{\text{LRI}'}$. When the detection block finds that the count difference exceeds ± 4 , the detection block resets the SRC.

The detection function operates when the next condition occurs.

$$f_{\text{LRI}'} < 1 / \{(4+\text{CLK} / f_{\text{LRI}}) / \text{CLK}\} \quad \text{or} \quad f_{\text{LRI}'} > 1 / \{(4-\text{CLK} / f_{\text{LRI}}) / \text{CLK}\} \quad [\text{Hz}]$$

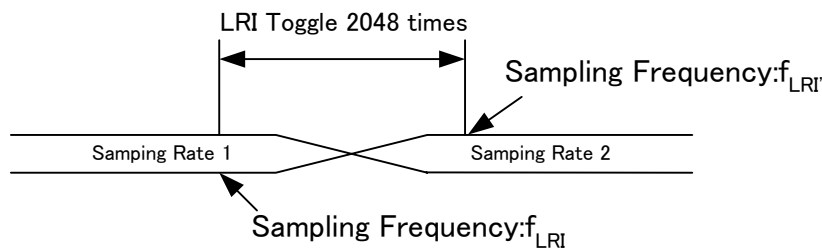


Fig.6 Relation between $f_{\text{LRI}'}$ and f_{LRI}

The automatic detection can detect the frequency change as follows:

In case of $\text{CLK}=24.576\text{MHz}$ and $f_{\text{LRI}}=8\text{kHz}$, the next two $f_{\text{LRI}'}$ frequency ranges can be detected.

$$f_{\text{LRI}'} < 7.989\text{kHz} \quad \text{or} \quad f_{\text{LRI}'} > 8,010\text{kHz}$$

$$* 2,048\text{sample}=2,048/8,000=256\text{msec}, \quad f_{\text{LRI}}=1/\{(4\pm 24.576\text{M}/8\text{k})/24.576\text{M}\}$$

In case of $\text{CLK}=24.576\text{MHz}$ and $f_{\text{LRI}}=192\text{kHz}$, the next two $f_{\text{LRI}'}$ frequency ranges can be detected.

$$f_{\text{LRI}'} < 186.18\text{kHz} \quad \text{or} \quad f_{\text{LRI}'} > 198.19\text{kHz}$$

$$* 2,048\text{sample}=2,048/192,000=10.7\text{msec}, \quad f_{\text{LRI}}=1/\{(4\pm 24.576\text{M}/192\text{k})/24.576\text{M}\}$$

The firmware can check if the SRC is reset by the automatic detection. The reset period is fixed at $2,048 \times 512(1/\text{CLK})$ seconds. This function is also effective in the reset period. During the reset this detection happens, the reset period becomes longer.

This function is active in default. When the changing speed of the LRI clock is too slow, the automatic detection could not be detected. When the input audio signal does not meet the above frequency detection requirement with bad-quality LRI and BCKI, the SRC does not convert correctly. In this case, reset the SRC by the firmware. Also reset the SRC by the firmware once when the system powers on.

The detection block cannot detect the complete stopped LRI clock. In case of the stopped LRI clock, the SRC generates the noise depending on the input signal condition. When this kind of noise happens, reset or stop the SRC function by the firmware.

3.2 Sampling Frequency Conversion Ratio and Group Delay

After the automatic detection reset or the firmware reset is done, the SRC generates an effective conversion output within 256 input samples. The NJU26060 Series does not generate digital noise after this kind of reset. The conversion ratio comes to the target specification and fixes conversion ratio within 16,384 input samples after the reset. After the automatic detection reset or the firmware reset, the LRI clock should be stable.

In case of the sampling converter ratio is fixed, the group delay is 256 sampling frequency clocks. To transfer the data to the firmware, it takes five more sampling frequency clocks. The zero data is inputted into the SRC during the group delay period, the output data of the SRC becomes zero.

3.3 Jitter-Tolerated Dose

The SRC can accept the jitter of 0.1UI. The UI is abbreviation of unit interval. The 1UI is one LRI clock time. The UI is defined by single peak.

Ex.1) $F_s=8\text{kHz}$ $0.1\text{UI} = 0.1/8,000=12.5\mu\text{sec}$

Ex.2) $F_s=192\text{kHz}$ $0.1\text{UI} = 0.1/192,000=521\text{nsec}$

The jitter-tolerated dose is shown in fig.7. The dotted line (0.1UI) is acceptable limitation to keep the performance of the SRC. The lack of data occurs above the solid line. Above the solid line, audible noise is generated.

This characteristic is measured with the sine wave jitter. Also the SRC can convert the square wave with the jitter very well as far as lower than 0.1U area.

Some kind of product generates high peak jitter instantaneously. For example, some kind of USB audio product. When the signal with more than 0.1U jitter is connected to the SRC, the SRC has possibility to generate audible noise.

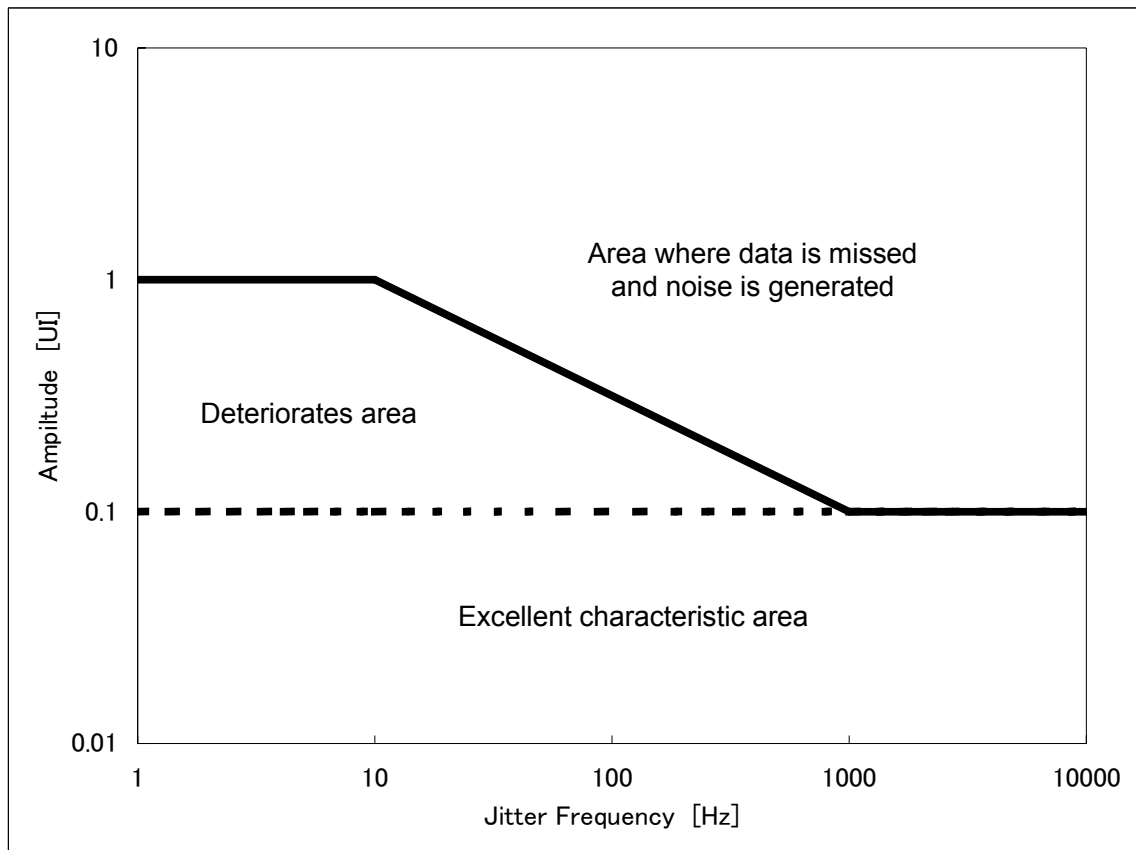


Fig.7 Jitter Tolerated dose

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3.4 Sampling Rate Converter Characteristics

This section describes Sampling Rate Converter characteristics. The characteristics are measured through the serial audio I/O interface. The characteristics depend on the PWM modulator when the output is via the PWM modulator.

Table 6 Sampling rate converter: THD+N Characteristics

| Parameter | Input Fs(kHz) | CLK pin Frequency | | Units |
|---|---------------|--|---|-------|
| | | 22.5792MHz (Inside F _{SO} =44.1kHz) | 24.576MHz (Inside F _{SO} =48.0kHz) | |
| THD+N Frequency: 22~F _{SO} /2(Hz) Input: 1kHz, 0dBFS Input bit Width:24bit | 8.0 | -114 | -120 | dB |
| | 11.025 | -122 | -122 | |
| | 12.0 | -126 | -125 | |
| | 22.05 | -130 | -130 | |
| | 24.0 | -128 | -128 | |
| | 32.0 | -124 | -124 | |
| | 44.1 | -130 | -126 | |
| | 48.0 | -119 | -130 | |
| | 64.0 | -125 | -131 | |
| | 88.2 | -133 | -132 | |
| | 96.0 | -119 | -133 | |
| | 128.0 | -131 | -134 | |
| | 176.0 | -134 | -133 | |
| | 192.0 | -132 | -135 | |

Table7 Sampling rate converter: Dynamic range Characteristics

| Parameter | Input Fs(kHz) | CLK pin Frequency | | Units |
|--|---------------|--|---|-------|
| | | 22.5792MHz (Inside F _{SO} =44.1kHz) | 24.576MHz (Inside F _{SO} =48.0kHz) | |
| Dynamic range Frequency: 22~F _{SO} /2(Hz) INPUT: 1kHz, -60dBFS Input bit Width 24bit A-Weight Filter | 8.0 | 132 | 132 | dB |
| | 11.025 | 132 | 132 | |
| | 12.0 | 132 | 132 | |
| | 22.05 | 133 | 133 | |
| | 24.0 | 133 | 133 | |
| | 32.0 | 133 | 133 | |
| | 44.1 | 133 | 133 | |
| | 48.0 | 134 | 134 | |
| | 64.0 | 135 | 134 | |
| | 88.2 | 136 | 136 | |
| | 96.0 | 136 | 136 | |
| | 128.0 | 138 | 137 | |
| | 176.0 | 139 | 138 | |
| | 192.0 | 139 | 139 | |

4. Digital Audio Interface

4.1 Digital Audio Data Format

The NJU26060 Series can use three kinds of formats hereafter as industry-standard digital audio data format.

- (1) I²S : MSB is put on the 2nd bit of LR clock change rate.(1 bit is delayed to left stuffing)
- (2) Left-justified : LR clock -- MSB is placed for changing.
- (3) Right-justified : LSB is placed just before LR clock change rate.

The main differences among three kinds of formats are in the position relation between LR clock (LRI, LRO) and an audio data (SDI, SDO).

- In every format: : a left channel is transmitted previously.
- In Right/Left-justified : LR clock ='High' shows a left channel.
- I²S : LR clock="Low" shows a left channel.
- The Bit clock BCK (BCKI, BCKO) is used as a shift clock of transmission data. The number of clocks more than the number of sum total transmission bits of a L/R channel is needed at least.
- One cycle of LR clock is one sample of a stereo audio data. The frequency of LR clock becomes equal to a sample rate (fs).

4.2 Serial Audio Data Input/output

The NJU26060 Series audio interface includes 3 data input lines: SDI0, SDI1 and SDI2 (Table 8). 3 data output lines: SDO0, SDO1 and SDO2 (Table 9). Refer to each datasheet.

Table 8 Serial Audio Input Pin Description

| Pin No. | Symbol | Description |
|---------|--------|--------------------|
| 8 | SDI0 | Audio Data Input 0 |
| 9 | SDI1 | Audio Data Input 1 |
| 10 | SDI2 | Audio Data Input 2 |

Table 9 Serial Audio Output Pin Description

| Pin No. | Symbol | Description |
|---------|--------|---------------------|
| 20 | OUTLN1 | Audio Data Output 0 |
| 18 | OUTRN1 | Audio Data Output 1 |
| 41 | SDO | Audio Data Output 2 |

The serial audio output pin switches the PWM output and the DIT output by the firmware (Table1).

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The NJU26060 Series can input and output digital audio data by the following general serial audio interfaces. The default resetting it is set to I²S 64Fs 24bit. The setting can be changed according to the firmware. The NJU26060 Series operates as a mastering device that synchronizes with the clock that consists of MCKO, BCKO, and LRO (Refer to Chapter 2) SDO set to the serial audio interface, OUTRN1, and OUTLN1 are output synchronizing with these clocks. The SDI pin that has been selected with the sampling rate converter can be operated by an independent format by the input of the data of the clock of BCKI and LRI.

The NJU26060 Series can use three kinds of formats hereafter as industry-standard digital audio data format; (1) I²S (2) Left-justified (3) Right-justified and 16 / 24bits data length. (Fig.8-1 to Fig8-6)
An audio interface input and output data format become the same data format.

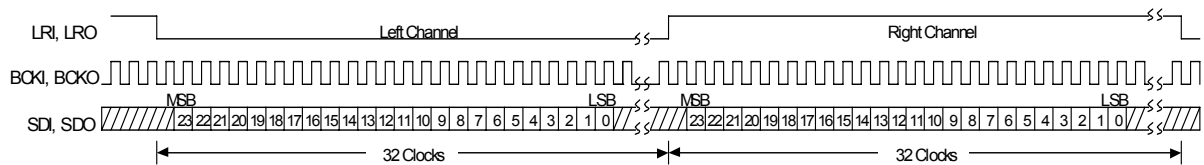


Fig8-1 I²S Data Format 64Fs, 24bit Data

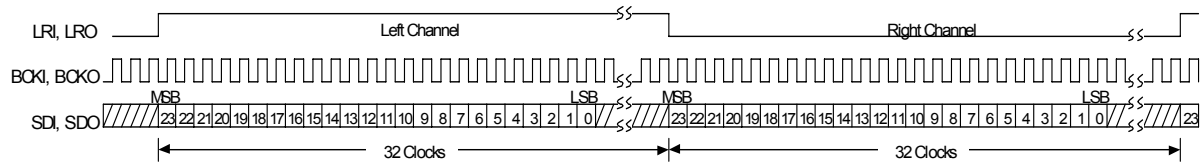


Fig.8-2 Left-Justified Data Format 64Fs, 24bit Data

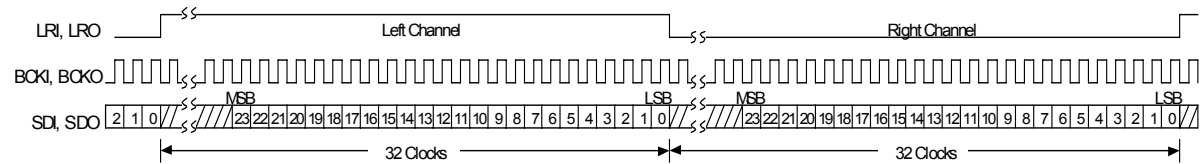


Fig.8-3 Right-Justified Data Format 64Fs, 24bit Data

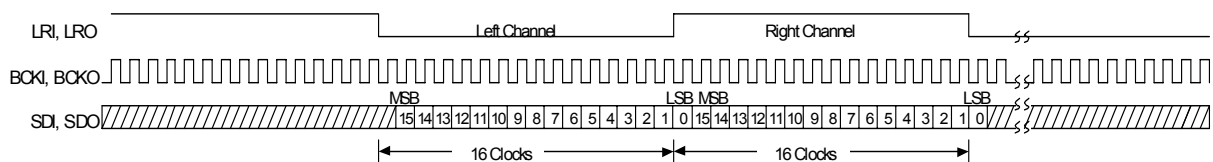


Fig.8-4 I²S Data Format 32Fs, 16bit Data

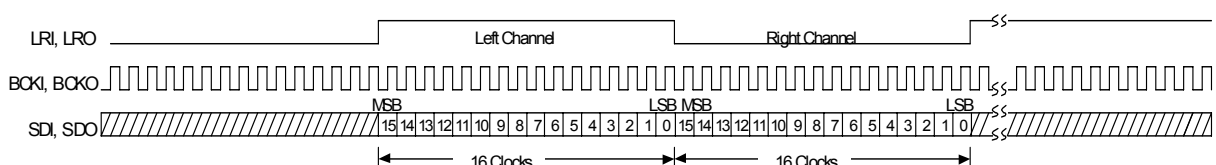


Fig.8-5 Left-Justified Data Format 32Fs, 16bit Data

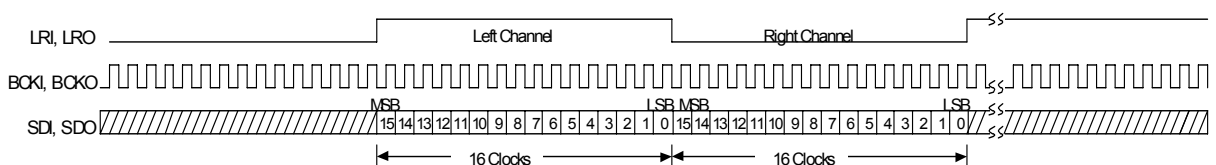


Fig.8-6 Right-Justified Data Format 32Fs, 16bit Data

4.3 Serial Audio Timing

Table 10 Serial Audio Input Timing Parameters ($V_{DD}=V_{DDPWM}=3.3V, T_a=25^\circ C$)

| Parameter | Symbol | Test Condition | Min | Typ. | Max | Units |
|--------------------|-----------|----------------|-----|------|-----|-------|
| BCK Frequency * | f_{BCK} | | - | - | 10 | MHz |
| BCK Period * | | | | | | |
| Low Pulse Width | t_{SIL} | | 35 | - | - | ns |
| High Pulse Width | t_{SIH} | | 35 | - | - | ns |
| BCK to LR Time * | t_{SLI} | | 15 | - | - | ns |
| LR to BCK Time * | t_{LSI} | | 15 | - | - | ns |
| Data Setup Time ** | t_{DS} | | 15 | - | - | ns |
| Data Hold Time ** | t_{DH} | | 15 | - | - | ns |

* It is regulations of the sampling converter interface.

** The terminal SDI selecting the sampling rate converter is regulations to BCKI. Exact to BCKO.

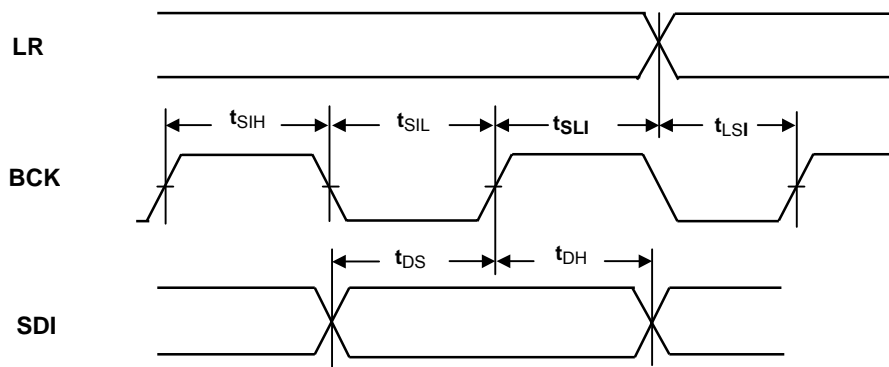


Fig. 9 Serial Audio Input Timing

Table 11 Serial Audio Output Timing Parameters ($V_{DD}=V_{DDPWM}=3.3V, T_a=25^\circ C$)

| Parameter | Symbol | Test Condition | Min | Typ. | Max | Units |
|-----------------------|-----------|----------------|-----|------|-----|-------|
| BCK to LR Time | t_{SLO} | $C_L=25pF$ | -15 | - | 15 | ns |
| Data Output Delay *** | t_{DOD} | | - | - | 15 | ns |

*** It is regulations to SDO, OUTRN1, OUTLN1 set to the serial audio output.

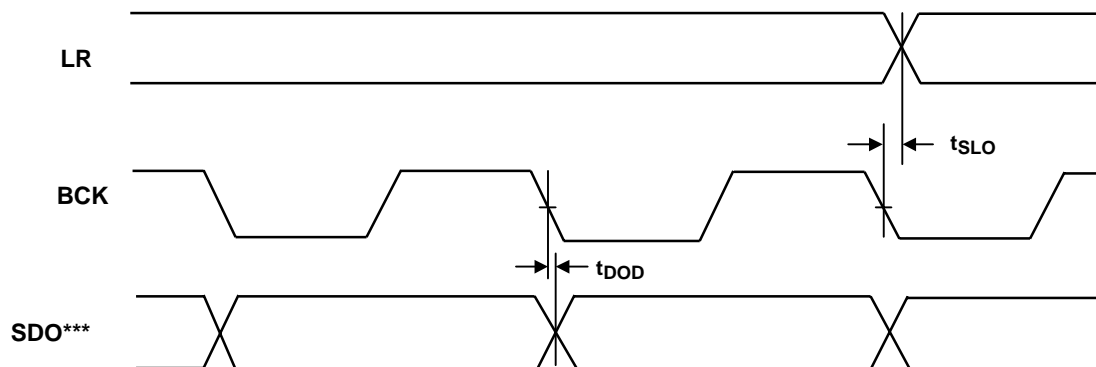


Fig.10 Serial Audio Output Timing

NJU26060 Series

5. PWM Modulator

The NJU26060 Series provide the PWM modulator with two stereo (four channels) outputs.

The PWM modulator employs eight-times over-sampling digital-filters, the fifth order $\Delta\Sigma$ modulators, and the modulation efficiency is 88%. The dynamic range is over 90dB. The PWM modulator provides the function of “noise suppression at silence period” and this function improves the S/N ratio up to 100dB.

The PWM switching frequency is eight times of the sampling frequency. For example, 384kHz at $F_s=48\text{kHz}$, 352.8kHz at $F_s=44.1\text{kHz}$. The NJU26060 Series can directly drive the speakers with the power drivers because of the high modulation efficiency.

After the reset the PWM modulator is standby mode. So the PWM modulator should be initialized by the firmware after the reset.

Table12 PWM Modulator Pin Assignment

| Pin No. | Symbol | Attribute | Description |
|---------|-----------|-----------|---|
| 23 | VDDPWM | PP | PWM Power Supply +3.3V |
| 22 | VSSPWM | GP | PWM Power Supply GND |
| 3 | PWM_DISb | I+ | PWM Block Standby request input pin (PWM_DISb = '0':Stand-BY) |
| 2 | PWM_MUTEb | I+ | PWM Block Mute request input pin (PWM_MUTEb = '0':Mute) |
| 29 | PWM_ERRb | I+ | PWM block stop request input pin (PWM_ERRb='0': PWM stop) |
| 28 | PWMEN0 | O | PWM0 enable output pin (PWMEN0='1': enable) |
| 17 | PWMEN1 | O | PWM1 enable output pin (PWMEN1='1': enable) |
| 24 | OUTLP0 | O | PWM0 L channel + output |
| 25 | OUTLN0 | O | PWM0 L channel - output |
| 26 | OUTRP0 | O | PWM0 R channel + output |
| 27 | OUTRN0 | O | PWM0 R channel - output |
| 21 | OUTLP1 | O | PWM1 L channel + output |
| 20 | OUTLN1 | O | PWM1 L channel - output |
| 19 | OUTRP1 | O | PWM1 R channel + output |
| 18 | OUTRN1 | O | PWM1 R channel - output |

Note: I+: Input (Pull-up), O: Output, PP: PWM Power Supply, PG: PWM Power Supply GND

The firmware or the external pins can select the PWM modulator functions in table13.

Table13 PWM Modulator Function

| Description (Symbol) | Setting | | Default (Reset) |
|--|---------------|-----------|-----------------|
| | Pin | Firmware | |
| PWM Recognition signal (PWMEN0, PWMEN1) | Available | Available | Invalid |
| PWM Modulator stand by (PWM_DISb) | Available * | Available | Stand-By |
| Mute Function (PWM_MUTEb) | Available * | Available | Mute |
| Request PWM Error signal (PWM_ERRb) | Available * | Available | Stop |
| Extend BPZ Output Function | Not Available | Available | Invalid |
| The terminal OUTLN1 is switched to serial audio output 0. ** | Not Available | Available | OUTLN1 |
| The OUTRN1 is connected to serial audio output 1. ** | Not Available | Available | OUTRN1 |
| Noise suppression function at silence period | Not Available | Available | Effective |
| Short plus limitation | Not Available | Available | Invalid |

* The firmware can mask the external input for the each block.

** BPZ is bipolar zero. The BPZ is a clock waveform of duty50%. It changes automatically if 'BPZ output function' is set to the PWM1 block.

5.1 PWM Effective Signal / PWM Modulator Standby

The PWMEN0/1 output shows whether the PWM output is effective or not. The PWM modulator is standby mode after the power-on or the reset and the PWMEN0/1 pin becomes GND level. The firmware can activate the PWM modulator. The PWM_DISb pin and the firmware can make the PWM modulator standby.

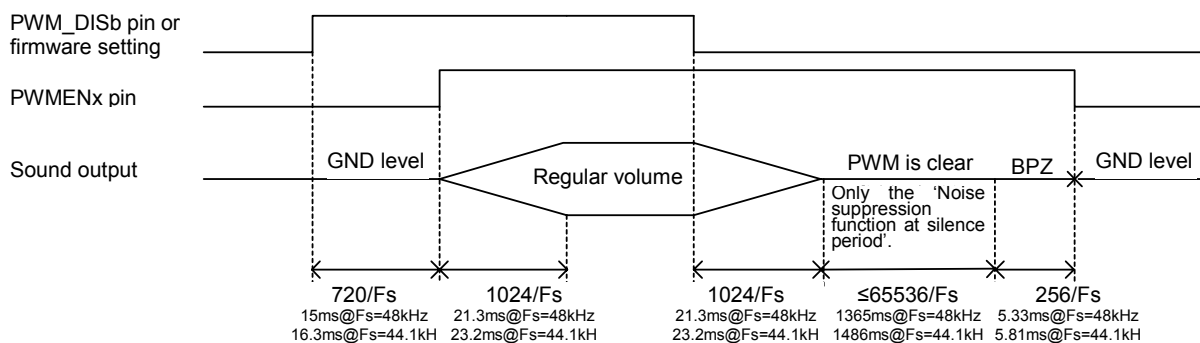


Fig.11 Relation between 'PWM Modulator Standby' and 'PWMEN, PWM output'
(Fs=48kHz: CLK=24.576MHz, Fs=44.1kHz: CLK=22.5792MHz)

After releasing the standby mode, the PWM modulator sets PWMEN0/1 pin High level and outputs the PWM signal. After activating PWM modulator, the mute is released and the signal goes up to the maximum level. This procedure takes 1,024/Fs. This mute release procedure does not provide zero-cross function.

By setting standby mode, the PWM modulator becomes the mute mode within 1,024/Fs. This mute procedure does not provide zero-cross function. If "noise suppression at silence period" mode becomes active, the clearance of the $\Delta \Sigma$ modulator is started. This procedure takes 65,536/Fs maximally. If "noise suppression at silence period" mode is not active, the clearance time is zero.

After that, BPZ signal is outputted during some periods and the PWMEN0/1 signal becomes Low. Also the PWM signal output stops at the same time as PWMEN0/1=Low. The signal level of the PWM output becomes GND level.

5.2 Mute

The NJU26060 Series can mute the PWM modulator by setting PWM_MUTEb low or the firmware. The each L/R channel is muted or unmuted respectively. The mute or un-mute is done at zero cross point. The step of the mute or the un-mute is 0.25dB/Fs.

In case of very low input frequency, the mute or un-mute is not finished within 2048/Fs. In the above case, the mute or un-mute is done with 1/Fs step. So the mute or un-mute operates under time-out condition. And the time of the mute or un-mute is not fixed under time-out condition. If this time-out condition is not good for the system, the firmware can be designed to control the time of mute or un-mute.

5.3 Stop Function for the PWM Modulator

In case that the backend IC becomes abnormal condition, the firmware or PWM_EERb=Low can stop the PWM modulator fast. But the pop noise happens.

To stop or release the PWM modulator function takes eight CLK clocks. To release the stop condition of the PWM modulator, PWM_STBYb should be High.

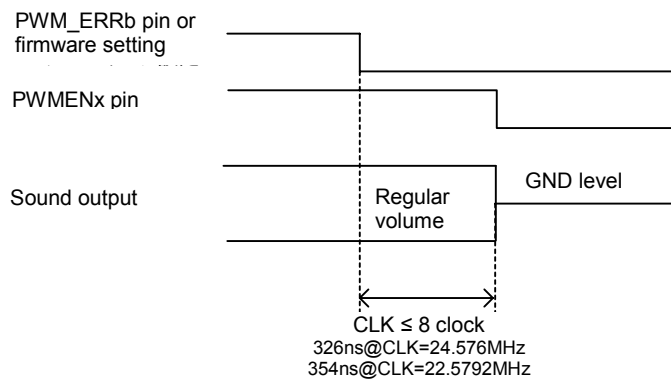


Fig.12 Relation between PWM Reset and PWMEN, PWM Output

5.4 BPZ Output Extension (BPZ : Bipolar Zero)

In case that PWMEN0/1 is GND, the PWM output is GND to prevent the power-on pop noise. The firmware can generate BPZ before and PWMEN0x=High by BPZ Output extension. The fig.13 shows the relation among PWM_DISb, PWMENx, and the sound output. The BPZ is inserted before and after PWMENx=High. The PWM modulation should be active to keep PWM modulator output.

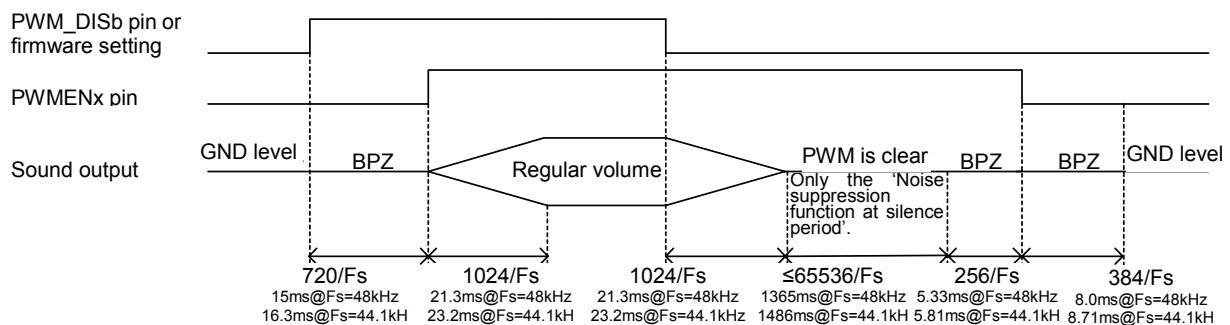


Fig.13 Relation between 'BPZ Output Extension' and 'PWMEN, PWM output'
(Fs=48kHz: CLK=24.576MHz, Fs=44.1kHz: CLK=22.5792MHz)

5.5 Switching from the PWM output to the serial audio output

In case that the BPZ output extension of PWM1 block is activated, the next two pins are assigned as follows:

OUTLN1 : Serial audio output0 that is same as PWM0 signal

OUTRN1: Serial audio output1 that is same as PWM1 signal

These pins are PWM outputs after power-on.

5.6 Noise Suppression at Silence Period

The noise suppression function of the PWM modulator can suppress an internal idle noise of the $\Delta\Sigma$ modulator in no input signal. This noise suppression function is active in default.

After the input of the PWM modulator becomes no signal, this function clear the internal PWM modulator within $65536/F_s$ and suppresses the internal noise. If the audio signal comes into the PWM modulator, the PWM modulator stops the noise suppression and generates the audio signal without any lack of audio signal.

To activate the noise suppression function, the input signal should be complete no signal. The mute function of the PWM modulator can clear all input signal and the noise suppression becomes active.

In case of the firmware mute, the input signal should be complete zero. Otherwise this function is not activated.

5.7 Short Plus Limitation

The PWM modulator generates the shortest 'Low' level pulse of 20nsec.

The PWM modulator provides the four kinds of pulse width limitation by the firmware in fig.14.

These pulse limitations do not include rising-time and falling-time of the pulse at the PWM output pin.

| Set level | The minimum "L" level width restriction value | |
|-------------|---|-------------------------------------|
| | CLK Frequency (Internal processing F_s) | |
| | 22.5792MHz ($F_s=44.1\text{kHz}$) | 24.576MHz ($F_s=48\text{kHz}$) |
| 0 (default) | 0ns(no limit) | 0ns (no limit) |
| 1 | 22.1ns | 20.3ns |
| 2 | 44.3ns | 40.7ns |
| 3 | 66.4ns | 61.0ns |

Table14 Shortest Pulse limitation

NJU26060 Series

5.8 PWM Modulator Characteristics

Table15 PWM Modulator characteristics
(CLK=24.576MHz(Fso=48kHz),LRI=48kHz,BCKI=3.072MHz, V_{DD}=V_{DDP_{WM}}=3.3V,Ta=25°C)

| Parameter | Min | Typ | Max | Unit |
|--|-----|-----|-----|------|
| THD+N (1kHz, 0dBFS) | - | -85 | -75 | dB |
| S/N ratio (1kHz, Noise decrease function as no-sound On, A-Weight) | 90 | 100 | - | dB |
| Dynamic range (1kHz, -60dBFS, A-Weight) | 85 | 90 | - | dB |
| Channel Separation (1kHz BPF) | 90 | 100 | - | dB |

The characteristics in table15 are measured with the next circuits in fig.14. This circuit includes the second low-pass filters (cut-off frequency 50kHz). The Audio Precision measures the signal with the AES17 filter (20kHz LPF). The condition of this measurement:

- 1) The conversion ratio of the SRC is 1:1 (48kHz -> 48kHz).
- 2) The outputs of the SRC go to the output pins without any DSP processing.

With this measurement condition, the power supply and the internal noise are added to the PWM output. The common mode noise is suppressed with the differential inputs. But the common mode noise is not suppressed with the single-end inputs. These characteristics have possibility to be degraded by the SRC. Because the sample rate converter is asynchronous, so some frequency degrades the characteristics.

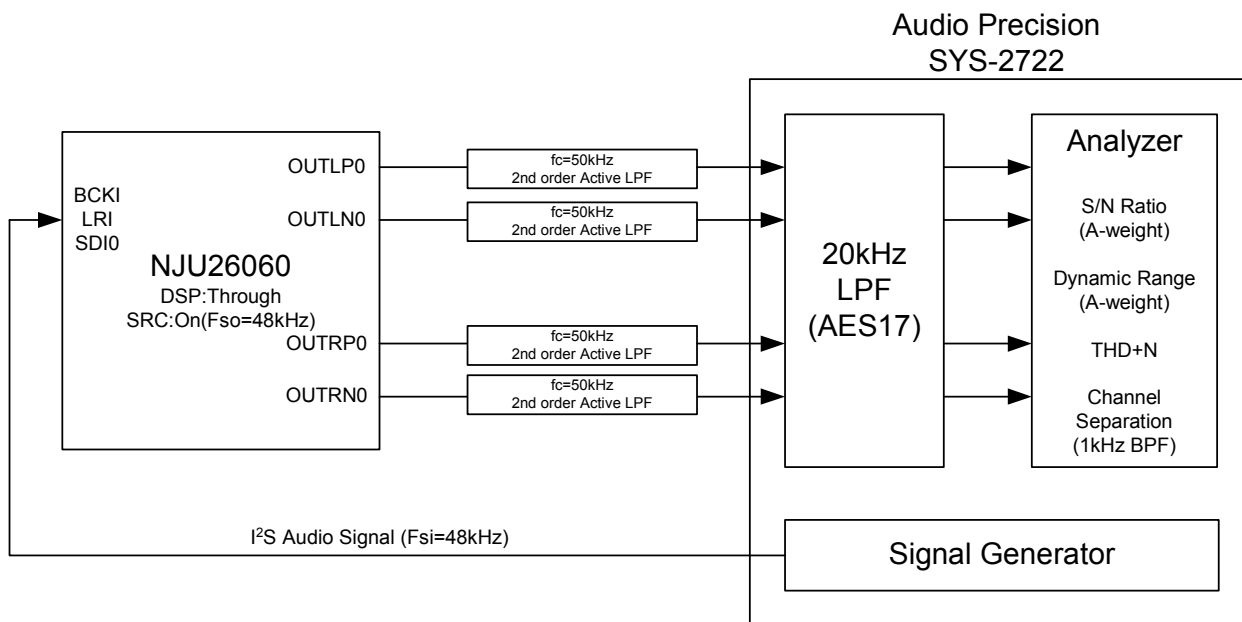


Fig.14 PWM Modulator Measuring circuit
(OUTLP1/LN1/RP1/RN1A are also the same)

6. Digital Interface Transemior (DIT)

The NJU26060 series provides Digital Interface Transemior. The DIT is compliant with AES3, IEC60958, S/PDIF and EIAJ CP1201 consumer specification. The DIT generates bi-phase signal that is CLK/512 frequency. The SDO generates bi-phase signal. The SDO is assigned as serial audio output in default. The firmware can change this output setting.

The firmware can connect the GPIO[1] input to the SDO output.
The SDO is hysteresis I/O pin with a pull-down resistor, so the input level should be adjusted.

The DIT channel status is shown in table 16. To connect a coaxial cable, the external buffer is recommended.

Table16 Channel Status Parameter

| Channel Status Parameter | | | Fixation/ Variable | Default |
|--------------------------|---------------------------|--|-----------------------|---------|
| CS0 | Consumer/ Professional | 0: Consumer mode | Fixation | 0 |
| CS1 | Data type | 0: Audio data, 1: Digital data | Variable | 0 |
| CS2 | Copyright | 0: Protection, 1: No-Protection | Variable | 0 |
| CS3 | Pre-emphasis | [CS3,CS4]=00: OFF | Variable | 0 |
| CS4 | | [CS3,CS4]=10: ON | Fixation | 0 |
| CS5 | Channel | 0: 2channel | Fixation | 0 |
| CS6~7 | Mode | 00: mode 0 | Fixation | 00 |
| CS8 | Category code | Prefer to standard book Default [CS8:CS15]=0010000 Application of Japan to digital audio broadcasting reception. | Variable | 0 |
| CS9 | | | | 0 |
| CS10 | | | | 1 |
| CS11 | | | | 0 |
| CS12 | | | | 0 |
| CS13 | | | | 0 |
| CS14 | | | | 0 |
| CS15 | | | | 0 |
| CS16 ~19 | Source number | 0000: no specification | Fixation | 0000 |
| CS20 ~23 | Channel number | 0000: no specification | Fixation | 0000 |
| CS24 | Sampling Frequency | [CS24:CS27]=0000 44.1kHz [CS24:CS27]=0100 48kHz [CS24:CS27]=1100 32kHz | Variable | 0 |
| CS25 | | | | 1 |
| CS26 | | | | 0 |
| CS27 | | | | 0 |
| CS28 | Clock Accuracy | [CS28,CS29]=00 standard mode [CS28,CS29]=10 High precision mode | Variable | 0 |
| CS29 | | | | 0 |

NJU26060 Series

7. Host Interface

The NJU26060 Series can be controlled via Serial Host Interface (SHI) using I²C bus. Data transfers are in 8 bit packets (1 byte) when using either format.

Refer to Serial Host Interface Pin Description. (Table 4)

Table.17 Serial Host Interface Pin Description

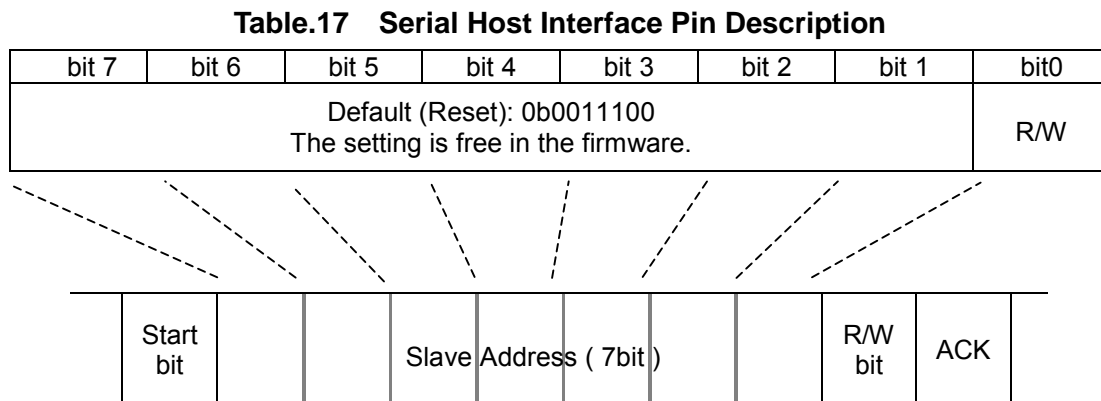
| Pin No. | Symbol | I ² C bus Format |
|---------|--------|--|
| 5 | SCL | Serial Clock |
| 4 | SDA | Serial Data Input (Open Drain Input/Output) |

Note : SDA pin (No.4) is a bi-directional open drain terminal. This pin requires a pull-up resistor.

7.1 I²C bus Interface

I²C bus interface transfers data to the SDA pin and clocks data to the SCL pin. SDA pin is a bi-directional open drain and requires a pull-up resistor.

When the NJU26060 Series is configured for I²C bus communication during the Reset initialization sequence, I²C bus interface transfers data to the SDA pin and clocks data to the SCL pin. An address can be arbitrarily set up by the seven-bit SLAVE address of the serial host interface. (Table 5)



Note : The serial host interface supports “Standard-Mode (100kbps)” and “Fast-Mode (400kbps)” I²C bus data transfer.

Table 19 I²C bus Interface Timing Parameters (V_{DD}=3.3V, f_{osc}=24.576MHz, Ta=25°C)

| Parameter | Symbol | Min | Max | Units |
|----------------------------|---------------------|-----|------|-------|
| SCL Clock Frequency | f _{SCL} | 0 | 400 | kHz |
| Start Condition Hold Time | t _{HD:STA} | 0.6 | - | μs |
| SCL "Low" Duration | t _{LOW} | 1.3 | - | μs |
| SCL "High" Duration | t _{HIGH} | 0.6 | - | μs |
| Start Condition Setup Time | t _{SU:STA} | 0.6 | - | μs |
| Data Hole Time *1 | t _{HD:DAT} | 0 | 0.9 | μs |
| Data Setup Time | t _{SU:DAT} | 250 | - | ns |
| Rising Time | t _R | - | 1000 | ns |
| Falling Time | t _F | - | 300 | ns |
| Stop Condition Setup Time | t _{SU:STO} | 0.6 | - | μs |
| Bus Release Time *2 | t _{BUF} | 1.3 | - | μs |

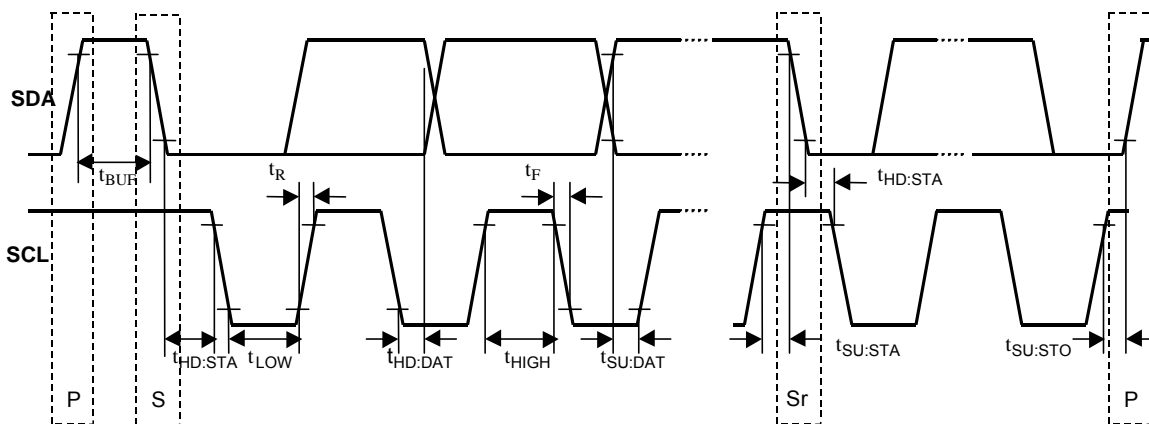


Fig. 15 I²C bus Timing

Note :

- *1 t_{HD:DAT}: Keep data 100ns hold time to avoid indefinite state by SCL falling edge.
- *2 This item shows the interface specification. The interval of a continuous command is specified separately.

8. General-purpose in/out pin

The NJU26060 Series has general-purpose in/out pin. GPIO0 pin includes with TEST mode and limits for starting up.

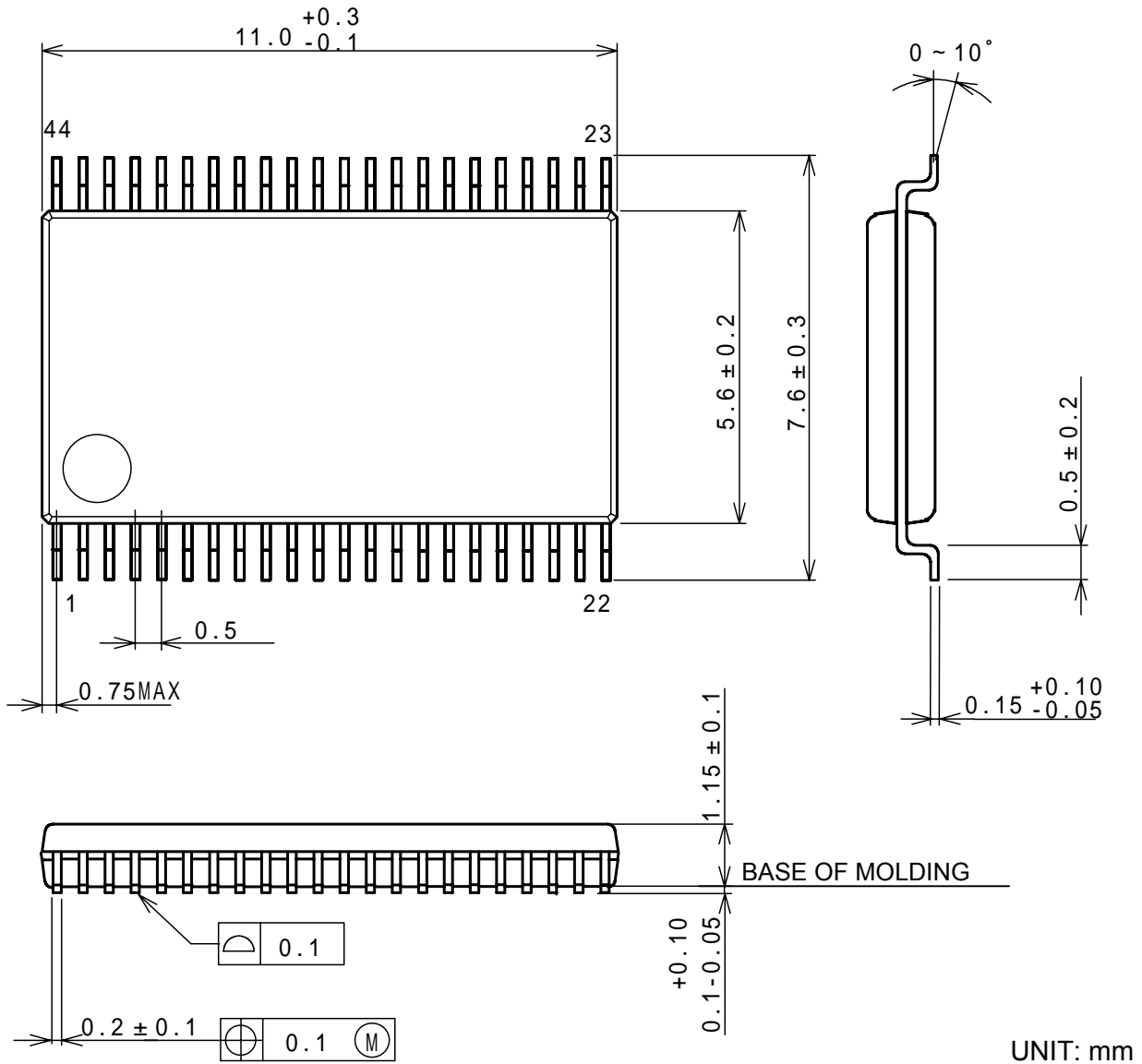
Table 20 General-purpose in/out pin and pin disposal

| Pin No. | Symbol | Description |
|---------|--------------------------|---|
| 40 | GPIO0 (Pull-down I/O) | Starts with "Low". It depends on the firmware after it starts. |
| 39 | GPIO1 (Pull-down I/O) | It depends on the firmware. |
| 38 | GPIO2 (Pull-up I/O) | It depends on the firmware. |
| 37 | GPIO3 (Pull-up I/O) | It depends on the firmware. |

NJU26060 Series

9. Package

SSOP44, Pb-Free



UNIT: mm

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