

MC74HC30A

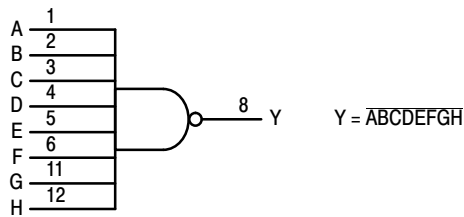
8-Input NAND Gate

High-Performance Silicon-Gate CMOS

The MC74HC30 is identical in pinout to the LS30. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- These are Pb-Free Devices



PINS 9, 10, 13 = NO CONNECTION
 PIN 14 = V_{CC}
 PIN 7 = GND

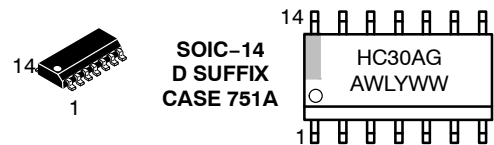
Figure 1. Logic Diagram



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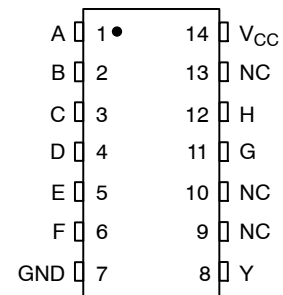
MARKING DIAGRAMS



A = Assembly Location
 WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week
 G or \blacksquare = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



NC = NO CONNECTION

FUNCTION TABLE

| Inputs A through H | Output Y |
|----------------------|----------|
| All inputs H | L |
| One or more inputs L | H |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

MC74HC30A

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|---|------------------------|-------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V_{in} | DC Input Voltage (Referenced to GND) | -1.5 to $V_{CC} + 1.5$ | V |
| V_{out} | DC Output Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| I_{in} | DC Input Current, per Pin | ± 20 | mA |
| I_{out} | DC Output Current, per Pin | ± 25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 50 | mA |
| P_D | Power Dissipation in Still Air SOIC Package TSSOP Package | 500 TBD | mW |
| T_{stg} | Storage Temperature | -65 to +150 | $^{\circ}C$ |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit | |
|-------------------|--|--|-------------|--------------------|----|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V | |
| V_{in}, V_{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V | |
| T_A | Operating Temperature, All Package Types | -55 | +125 | $^{\circ}C$ | |
| t_r, t_f | Input Rise and Fall Time (Figure 2) | $V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$ | 0 0 0 | 1000 500 400 | ns |

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

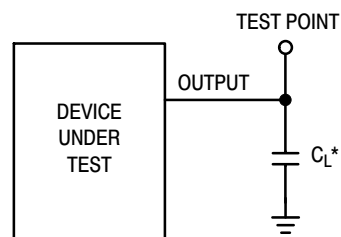
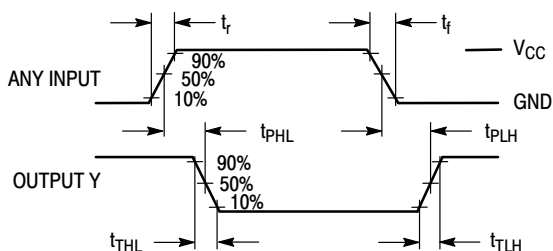
| Symbol | Parameter | Test Conditions | V_{CC} V | Guaranteed Limit | | | Unit |
|----------|--|---|--|---------------------------|--------------------|---------------------|---------------|
| | | | | - 55 to 25 $^{\circ}C$ | $\leq 85^{\circ}C$ | $\leq 125^{\circ}C$ | |
| V_{IH} | Minimum High-Level Input Voltage | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$ | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| V_{IL} | Maximum Low-Level Input Voltage | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$ | 2.0 | 0.3 | 0.3 | 0.3 | V |
| | | | 4.5 | 0.9 | 0.9 | 0.9 | |
| | | | 6.0 | 1.2 | 1.2 | 1.2 | |
| V_{OH} | Minimum High-Level Output Voltage | $V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$ | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | | $V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$ | 4.5 | 3.98 | 3.84 | |
| 6.0 | 5.48 | 5.34 | 5.20 | | | | |
| V_{OL} | Maximum Low-Level Output Voltage | $V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$ | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | | $V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$ | 4.5 | 0.26 | 0.33 | |
| 6.0 | 0.26 | 0.33 | 0.40 | | | | |
| I_{in} | Maximum Input Leakage Current | $V_{in} = V_{CC} \text{ or } GND$ | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| I_{CC} | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$ | 6.0 | 2 | 20 | 40 | μA |

MC74HC30A

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

| Symbol | Parameter | V_{CC} V | Guaranteed Limit | | | Unit |
|--------------------------|---|-------------------|------------------|-------------------------|--------------------------|------|
| | | | - 55 to 25°C | $\leq 85^\circ\text{C}$ | $\leq 125^\circ\text{C}$ | |
| t_{PLH} , t_{PHL} | Maximum Propagation Delay, Any Input to Output Y (Figures 2 and 3) | 2.0 4.5 6.0 | 175 35 30 | 220 44 37 | 265 53 45 | ns |
| t_{TLH} , t_{THL} | Maximum Output Transition Time, Any Output (Figures 2 and 3) | 2.0 4.5 6.0 | 75 15 13 | 95 19 16 | 110 22 19 | ns |
| C_{in} | Maximum Input Capacitance | - | 10 | 10 | 10 | pF |

| C_{PD} | Power Dissipation Capacitance (Per Gate) | Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$ | | pF |
|----------|--|--|--|----|
| | | 27 | | |
| | | | | |



*Includes all probe and jig capacitance

Figure 2. Switching Waveforms

Figure 3. Test Circuit

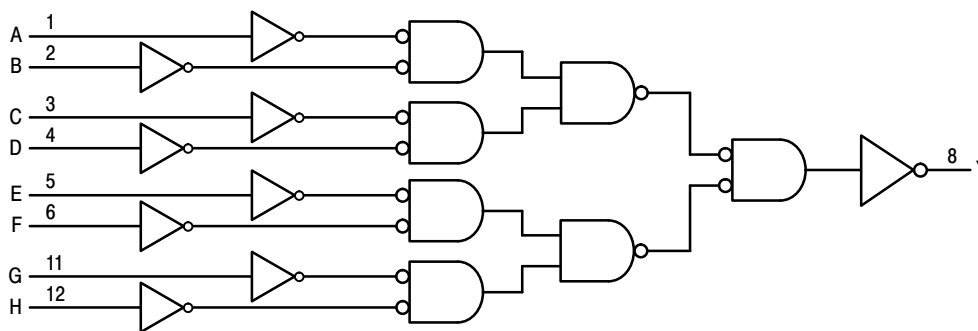


Figure 4. Expanded Logic Diagram

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|----------------------|------------------|
| MC74HC30ADG | SOIC-14 (Pb-Free) | 55 Units/Rail |
| MC74HC30ADR2G | SOIC-14 (Pb-Free) | 2500/Tape & Reel |
| MC74HC30ADTR2G | TSSOP-14* | |

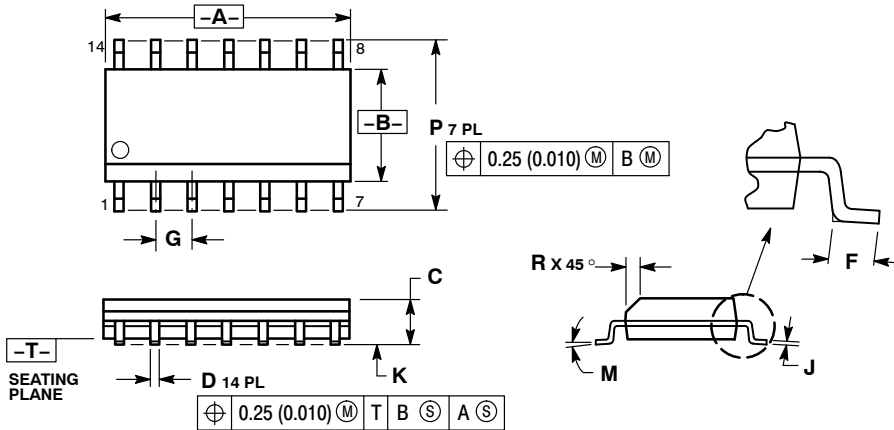
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MC74HC30A

PACKAGE DIMENSIONS

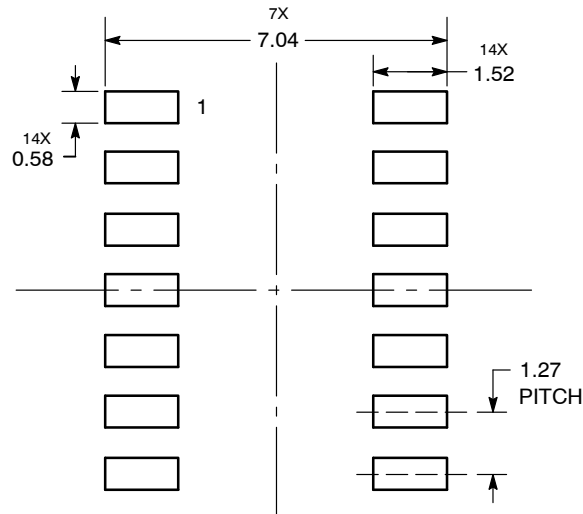
SOIC-14
CASE 751A-03
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| MILLIMETERS | | INCHES | | |
|-------------|----------|--------|-----------|-------|
| DIM | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

SOLDERING FOOTPRINT*



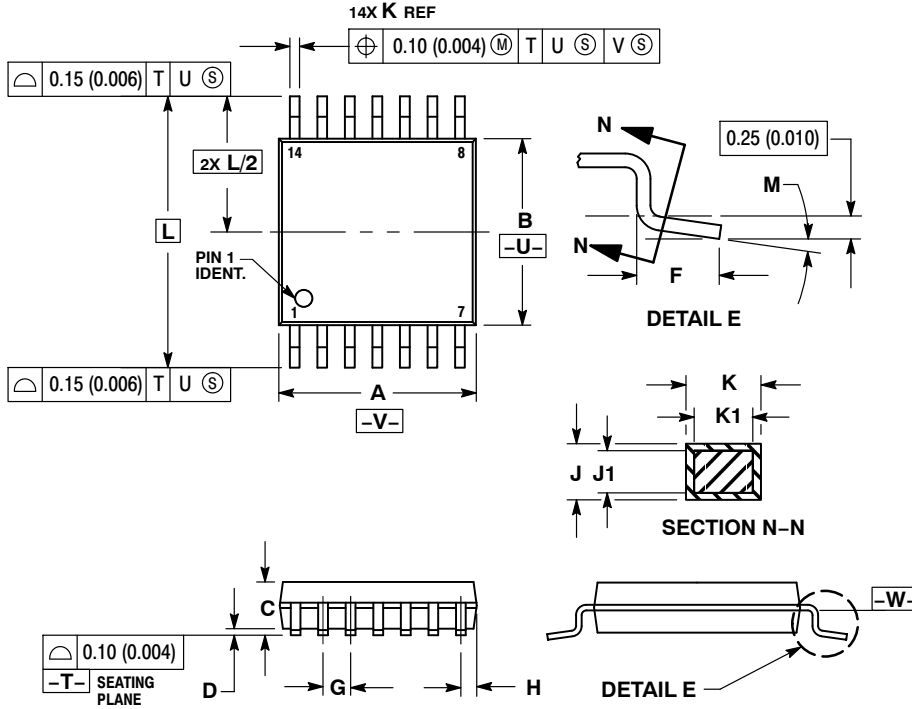
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74HC30A

PACKAGE DIMENSIONS

TSSOP-14
CASE 948G-01
ISSUE B

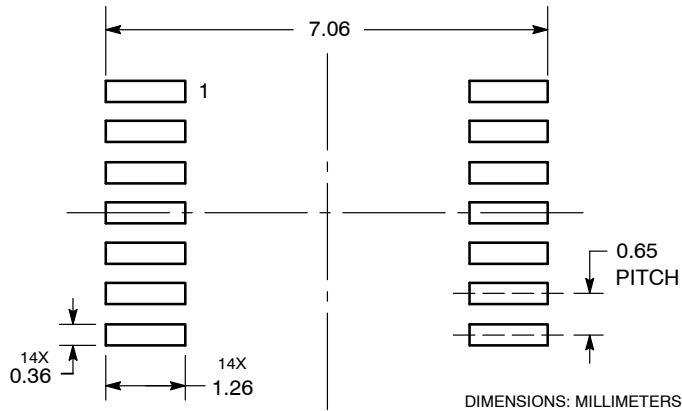


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° - 8° | | 0° - 8° | |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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