Four-Channel Universal Frequency Translator

8A34043
Datasheet

Overview

The 8A34043 Four-Channel Universal Frequency Translator is a highly integrated timing device that generates synchronous or asynchronous clocks from its reference inputs. The device can be used in any synthesizer or jitter attenuator application, including Optical Transport Network (OTN) and Synchronous Ethernet (SyncE) systems.

Typical Applications

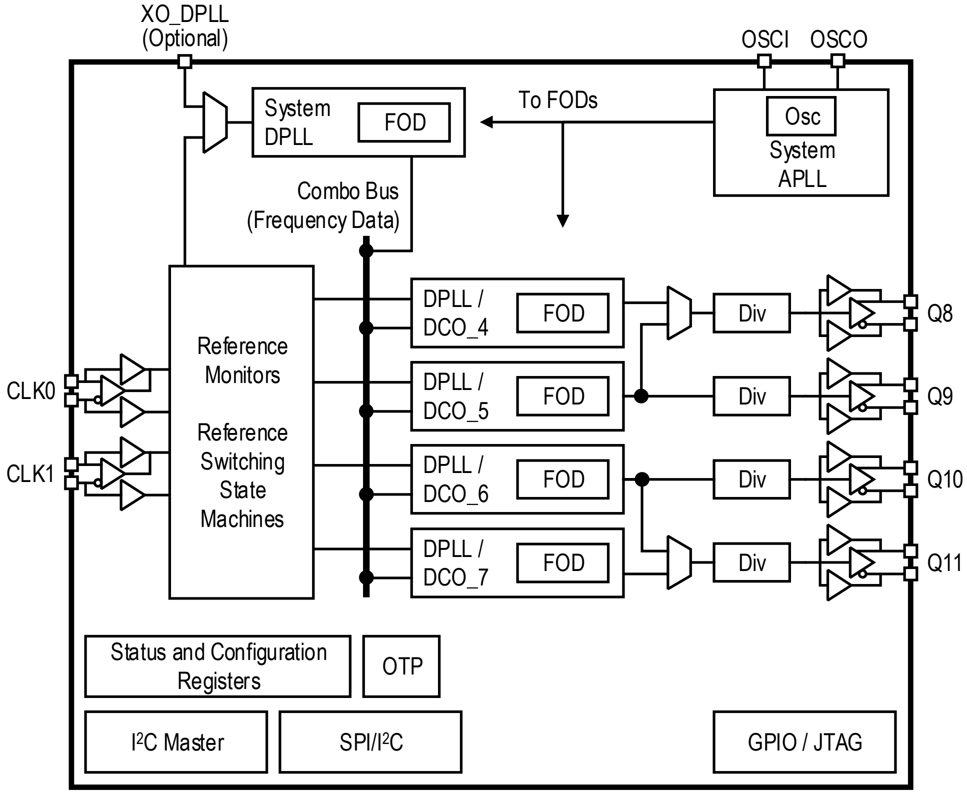
- Core and access IP switches / routers
- Synchronous Ethernet equipment
- 10Gb, 40Gb, and 100Gb Ethernet interfaces
- Wireless infrastructure for 4.5G and 5G network equipment
- OTN Muxponders and line cards

Features

- Close-in phase noise complies with Common Public Radio Interface (CPRI) frequency synchronization requirements
- Supports all ITU-T G.709 frequencies
- Meets OTN jitter and wander requirements per ITU-T G.8251
- Four independent timing channels
  - Each can act as a frequency synthesizer, jitter attenuator, Digitally Controlled Oscillator (DCO), or Digital Phase Lock Loop (DPLL)
  - DPLL Digital Loop Filters (DLFs) are programmable with cut off frequencies from 17Hz to 12kHz
  - Generates output frequencies that are independent of input frequencies via a Fractional Output Divider (FOD)
  - Each FOD supports output phase tuning with 50ps resolution
- Four differential / eight LVCMOS outputs
  - Frequencies from 0.5Hz to 1GHz (250MHz for LVCMOS)
  - Jitter below 150fs RMS (10kHz to 20MHz)
  - LVCMOS, LVDS, LVPECL, HCSL, CML, SSTL, and HSTL output modes supported
  - Differential output swing is selectable: 400mV / 650mV / 800mV / 910mV
  - Independent output voltages of 3.3V, 2.5V, or 1.8V
    - LVCMOS additionally supports 1.5V or 1.2V swings
  - The clock phase of each output is individually programmable in 1ns to 2ns steps with a total range of ±180°
- Two differential / four single-ended clock inputs
  - Support frequencies from 1kHz to 1GHz
  - Any input can be mapped to any or all of the timing channels
  - Redundant inputs frequency independent of each other
  - Any input can be designated as external frame/sync pulse of EPPS (even pulse per second), 1 PPS (Pulse per Second), 5PPS, 10 PPS, 50Hz, 100Hz, 1 kHz, 2 kHz, 4kHz, and 8kHz associated with a selectable reference clock input
  - Per-input programmable phase offset of up to ±1.638µs in 50ps steps
- Reference monitors qualify/disqualify references depending on LOS, activity, frequency monitoring, and/or LOS input pins
  - Loss of Signal (LOS) input pins (via GPIOs) can be assigned to any input clock reference
- Automatic reference selection state machines select the active reference for each DPLL based on the reference monitors, priority tables, revertive / non-revertive, and other programmable settings
- System APLL operates from fundamental-mode crystal: 25MHz to 54MHz or from a crystal oscillator
- System DPLL accepts an XO, TCXO, or OCXO operating at virtually any frequency from 1MHz to 150MHz
- DPLLs can be configured as DCOs to synthesize clocks under the control of an external algorithm
  - DCOs generate PTP based clocks with frequency resolution less than 1.11×10^{-16}
- Supports 1MHz I^2C or 50MHz SPI serial processor ports
- The device can configure itself automatically after reset via:
  - Internal Customer-programmable One-Time Programmable memory with up to 16 different configurations
  - Standard external I^2C EPROM via separate I^2C Master Port
- 1149.1 JTAG Boundary Scan
- 7 × 7 mm 48-VFQFPN package

Block Diagram

Figure 1. Block Diagram



Description

The 8A34043 Four-Channel Universal Frequency Translator is a highly integrated timing device that generates synchronous or asynchronous clocks from any of its reference inputs. The can be used in any synthesizer or jitter attenuator application, including Optical Transport Network (OTN) and Synchronous Ethernet (SyncE) systems.

The internal System APLL must be supplied with a low phase noise reference clock with frequency between 25MHz and 54MHz. The output of the System APLL is used for clock synthesis by all of the Fractional Output Dividers (FODs) in the device. The System APLL reference can come from an external crystal oscillator connected to the OSCI pin or from an internal oscillator that uses a crystal connected between the OSCI and OSCO pins.

The System DPLL generates an internal system clock that is used by the reference monitors and other digital circuitry in the device. If the reference provided to the System APLL meets the stability and accuracy requirements of the intended application then the System DPLL can free run and a System DPLL reference is not required. Alternatively, the System DPLL can be locked to an external reference that meets the stability and accuracy requirements of the intended application. The System DPLL can accept a reference from the XO_DPLL pin or via the reference selection mux.

The frequency accuracy/stability of the internal system clock determines the frequency accuracy/stability of the DPLLs in Free-Run mode and in Holdover mode; and it affects the wander generation of the DPLLs in Locked and DCO modes. When provided with a suitably stable and accurate system clock, the DPLLs meet the frequency accuracy, pull-in, hold-in, pull-out, noise generation, noise tolerance, transient response, and holdover performance requirements of ITU-T G.8262 synchronous Ethernet Equipment Clock (EEC) options 1 and 2.

The 8A34043 accepts up to two differential reference inputs and up to four single-ended reference inputs that can operate at common GNSS, Ethernet, SONET/SDH, PDH frequencies, and any input frequency from 1kHz to 1GHz (250MHz in single-ended mode). The references are continually monitored for loss of signal and for frequency offset per user programmed thresholds. All of the references are available to all the DPLLs. The active reference for each DPLL is determined by forced selection or by automatic selection based on user programmed priorities, locking allowances, reference monitors, revertive and non-revertive settings, and LOS inputs.

The 8A34043 provides four independent Digital Phase Lock Loops (DPLLs) consisting of a Phase Frequency Detector (PFD), a Low Pass Filter (LPF), and a Digitally Controlled Oscillator (DCO). The DPLL architecture allows external processors to access the control loop at several points to monitor and control the loop. A processor can directly control the DCOs, and it can implement a proprietary filter and control algorithm to replace the internal LPF.

The 8A34043 can accept a clock reference and an associated frame pulse or sync signal as a pair. DPLLs can lock to the clock reference and align the sync and clock outputs with the paired sync/frame input. The device allows any of the reference inputs to be configured as sync inputs that can be associated with any of the other reference inputs. The input sync signals can have a frequency of 1 PPS (Pulse per Second), EPPS (even pulse per second), 5PPS, 10 PPS, 50Hz, 100Hz, 1 kHz, 2 kHz, 4kHz, and 8 kHz. This feature enables any DPLL to phase align its frame sync and clock outputs with a sync input without the need to use a low bandwidth setting to lock directly to the sync input.

The DPLLs support four primary operating modes: Free-Run, Locked, Holdover, and DCO. In Free-Run mode the DPLLs synthesize clocks based on the system clock alone. In Locked mode the DPLLs filter reference clock jitter with the selected bandwidth. Also in Locked mode, the long-term output frequency accuracy is the same as the long-term frequency accuracy of the selected input reference. In Holdover mode, the DPLL uses frequency data acquired while in Locked mode to generate accurate frequencies when input references are not available. In DCO mode, the DPLL control loop is opened and the DCO can be controlled by an external algorithm such as a PTP clock recovery servo running on an external processor to synthesize PTP clocks.

The DPLLs can be configured with a range of selectable filtering bandwidths from 17Hz to 12kHz for use in jitter attenuation and rate conversion applications.

All of the channels within the 8A34043 derive their output frequencies from the same System APLL clock, and therefore the control words used to tune the DCOs are interchangeable.

The 8A34043 generates up to four differential output clocks at any frequency from 0.5Hz to 1GHz. The differential outputs can support LVPECL, LVDS, HCSL, and CML. It generates up to eight single-ended clocks with frequencies from 0.5Hz to 250MHz. LVCMOS output supports 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V. Each output stage can be independently configured.

Clocks generated by the 8A34043 have jitter below 150fs RMS (10kHz to 20MHz) and therefore are suitable for serial 100GBASE-R, 40GBASE-R, and lower rate interfaces.

All control and status registers are accessed through the I^2C / SPI slave microprocessor interface, and the SPI interface mode supports high clock rates (up to 50MHz). For configuring the DPLLs, the I^2C master interface can automatically load a configuration from an external EEPROM after reset. The 8A34043 also has an internal customer-programmable One-Time Programmable memory with up to 16 different configurations.

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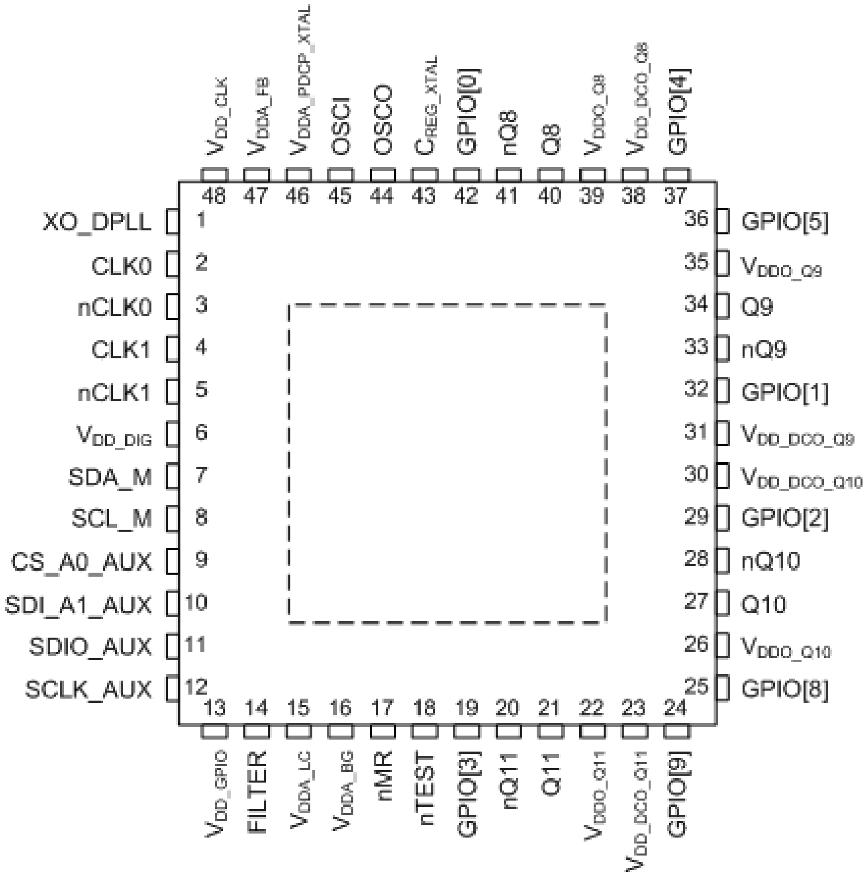
Pin Assignments

Figure 2. Pin Assignments for 7 × 7 mm 48-VFQFPN Package – Bottom View[1]



Pin Descriptions and Pin Characteristics

Table 1. Pin Descriptions[a]

Number	Name	Type		Description
1	XO_DPLL	Input		Single-ended crystal oscillator input for System Digital PLL (for more information, see Crystal Oscillator Input (XO_DPLL)).
2	CLK0	Input	Pull-down	Positive input for differential input Clock 0 or single-ended input for Clock 0 (for more information, see Input Stage).
3	nCLK0	Input	Pull-up	Negative input for differential input Clock 0 or single-ended input for Clock 8 (for more information, see Input Stage).
4	CLK1	Input	Pull-down	Positive input for differential input Clock 1 or single-ended input for Clock 1 (for more information, see Input Stage).
5	nCLK1	Input	Pull-up	Negative input for differential input Clock 1 or single-ended input for Clock 9 (for more information, see Input Stage).
6	V_{DD_DIG}	Power		Power supply for digital logic. 1.2V or 1.8V supported.

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[1] Indexed signals (e.g., GPIO[5]) are not necessarily numbered sequentially. Some indexes may be skipped. This is to maintain software compatibility with other members of the family of devices.

Table 1. Pin Descriptions[a]

Number	Name	Type		Description
7	SDA_M	I/O		I^2C Bi-directional Data for I^2C Master Operation (for more information, see I2C Master). It can be connected to SDIO_AUX if desired and the connected port is configured for I^2C operation.
8	SCL_M	Output		I^2C Clock Output for I^2C Master Operation (for more information, see I2C Master). It can be connected to SCLK_AUX if desired and the connected port is configured for I^2C operation.
9	CS_A0_AUX	Input	Pull-up	Auxiliary serial port input. Used as a chip-select input in SPI mode and optionally as an Address Bit 0 select input in I^2C mode.
10	SDI_A1_AUX	Input	Pull-up	Auxiliary serial port input. Used as Serial Data In in 4-wire SPI mode and optionally as an Address Bit 1 select input in I^2C mode. Unused in 3-wire SPI mode.
11	SDIO_AUX	I/O	Pull-up	Auxiliary serial port bi-directional data pin. Used as a bi-directional data pin in I^2C and 3-wire SPI modes. Used as Serial Data Output pin in 4-wire SPI mode. External pull-up recommended in I^2C mode.
12	SCLK_AUX	Input	Pull-up	Auxiliary serial port clock input. Used in both SPI and I^2C modes as the clock. External pull-up recommended in I^2C mode.
13	V_{DD_GPIO}	Power		Power supply for all the digital pins, including GPIO pins and serial ports pins. 3.3V, 2.5V, 1.8V, or 1.5V supported.
14	FILTER	Analog		Reference capacitor for System Analog PLL Loop Filter. Requires a 2.2nF capacitor to ground.
15	V_{DDA_LC}	Power		Analog power supply voltage for System Analog PLL's LC Resonator, 3.3V or 2.5V supported.[c]
16	V_{DDA_BG}	Power		Analog power supply voltage for System Analog PLL's bandgap regulator, 3.3V or 2.5V supported.[c]
17	nMR	Input	Pull-up	Master Reset input (for more information, see Device Initial Configuration).
18	nTEST	Input	Pull-up	Test Mode enable pin. Must be high for normal operation.
19	GPIO[3]	I/O	Pull-up[b]	General Purpose Input / Output 3 (for more information, see General Purpose Input/Outputs (GPIOs)).
20	nQ11	Output		Q11 clock negative output (for more information, see FOD Multiplexing and Output Stages).
21	Q11	Output		Q11 clock positive output (for more information, see FOD Multiplexing and Output Stages).
22	V_{DDO_Q11}	Power		Power supply for Q11/nQ11 output buffers (for more information on supported voltages, see FOD Multiplexing and Output Stages).
23	$V_{DD\_DCO\_Q11}$	Power		Power supply for FOD block supporting output clocks Q11/nQ11. Also powers the FOD control logic for FOD blocks supporting Q10/nQ10 and Q11/nQ11. 1.8V supply required.
24	GPIO[9]	I/O	Pull-up[b]	General Purpose Input / Output 9 (for more information, see General Purpose Input/Outputs (GPIOs)).
25	GPIO[8]	I/O	Pull-up[b]	General Purpose Input / Output 8 (for more information, see General Purpose Input/Outputs (GPIOs)).
26	V_{DDO_Q10}	Power		Power supply for Q10/nQ10 output buffers (for more information on supported voltages, see FOD Multiplexing and Output Stages).

Table 1. Pin Descriptions[a]

Number	Name	Type		Description
27	Q10	Output		Q10 clock positive output (for more information, see FOD Multiplexing and Output Stages).
28	nQ10	Output		Q10 clock negative output (for more information, see FOD Multiplexing and Output Stages).
29	GPIO[2]	I/O	Pull-up[b]	General Purpose Input / Output 2 (for more information, see General Purpose Input/Outputs (GPIOs).
30	$V_{DD\_DCO\_Q10}$	Power		Power supply for FOD block supporting output clocks Q10/nQ10. 1.8V supply required.
31	$V_{DD\_DCO\_Q9}$	Power		Power supply for FOD block supporting output clocks Q9/nQ9. 1.8V supply required.
32	GPIO[1]	I/O	Pull-up[b]	General Purpose Input / Output 1 (for more information, see General Purpose Input/Outputs (GPIOs)).
33	nQ9	Output		Q9 clock negative output (for more information, see FOD Multiplexing and Output Stages).
34	Q9	Output		Q9 clock positive output (for more information, see FOD Multiplexing and Output Stages).
35	V_{DDO_Q9}	Power		Power supply for Q9/nQ9 output buffers (for more information on supported voltages, see FOD Multiplexing and Output Stages).
36	GPIO[5]	I/O	Pull-up[b]	General Purpose Input / Output 5 (for more information, see General Purpose Input/Outputs (GPIOs)).
37	GPIO[4]	I/O	Pull-up[b]	General Purpose Input / Output 4 (for more information, see General Purpose Input/Outputs (GPIOs)).
38	$V_{DD\_DCO\_Q8}$	Power		Power supply for FOD block supporting output clocks Q8/nQ8. Also powers the FOD control logic for FOD blocks supporting Q8/nQ8 and Q9/nQ9. 1.8V supply required.
39	V_{DDO_Q8}	Power		Power supply for Q8/nQ8 output buffers (for more information on supported voltages, see FOD Multiplexing and Output Stages).
40	Q8	Output		Q8 clock positive output (for more information, see FOD Multiplexing and Output Stages).
41	nQ8	Output		Q8 clock negative output (for more information, see FOD Multiplexing and Output Stages).
42	GPIO[0]	I/O	Pull-up[b]	General Purpose Input / Output 0 (for more information, see General Purpose Input/Outputs (GPIOs)).
43	C_{REG_XTAL}	Power		Filter capacitor for voltage regulator for oscillator circuit associated with OSCI/OSCO pins. Requires a 10µF filter capacitor to ground.
44	OSCO	Output		Crystal Output. This pin should be connected to a crystal. If an oscillator is connected to the OSCI pin, this pin should be left unconnected.
45	OSCI	Input		Crystal Input. Accepts a reference from a clock oscillator or a fundamental mode parallel-resonant crystal (for information, see Table 36 and Table 37).
46	$V_{DDA\_PDCP\_XTAL}$	Power		Analog power supply voltage for System Analog PLL's phase detector and charge pump, as well as the oscillator circuit associated with OSCI/OSCO pins. 2.5V or 3.3V operation supported.[c]

Table 1. Pin Descriptions[a]

Number	Name	Type		Description
47	V_{DDA_FB}	Power		Analog power supply voltage for System Analog PLL's feedback divider; 1.8V required.
48	V_{DD_CLK}	Power		Power supply for input clock buffers and dividers. Supports 1.8V, 2.5V, or 3.3V as appropriate for the input clock swing (for more information, see Input Stage).
ePAD	V_{SS}	Power		Device ePAD must be connected to Ground.

[a] *Pull-up* and *Pull-down* refer to internal input resistors (for typical values, see Table 2.

[b] GPIO pins can be configured via EEPROM and/or OTP with a pull-up or pull-down. Pull-up is the default configuration.

[c] $V_{DDA\_PDCP\_XTAL}$, V_{DDA_LC}, and V_{DDA_BG} can be driven with either 2.5V or 3.3V, however all must use the same voltage level.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	OSCI, OSCO			2.5		pF
		XO_DPLL			1		
		All Other pins			2		
R_{PULLUP}	Input Pullup Resistor	nCLK[1:0]			50		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor	CLK[1:0]			50		kΩ
C_{PD}	Power Dissipation Capacitance (per output pair)	LVCMOS	V_{DDO_Qx}[a] = 3.465V		9		pF
			V_{DDO_Qx} = 2.625V		8.8		
			V_{DDO_Qx} = 1.89V		8.8		
			V_{DDO_Qx} = 1.575V		9.2		
			V_{DDO_Qx} = 1.26V		8.7		
		Differential	V_{DDO_Qx} = 3.465V		1.4		
			V_{DDO_Qx} = 2.625V		3.5		
			V_{DDO_Qx} = 1.89V		5		
R_{OUT}[b]	Output Impedance	GPIO[9:8,5:0]	V_{DD_GPIO} = 3.3V		30		Ω
			V_{DD_GPIO} = 2.5V		31		
			V_{DD_GPIO} = 1.8V		32		
			V_{DD_GPIO} = 1.5V		33		
		SCL_M, SDA_M, SDIO_AUX	V_{DD_GPIO} = 3.3V		27		
			V_{DD_GPIO} = 2.5V		30		
			V_{DD_GPIO} = 1.8V		38		
			V_{DD_GPIO} = 1.5V		47		

[a] V_{DDO_Qx} denotes: V_{DDO_Q8}, V_{DDO_Q9}, V_{DDO_Q10}, or V_{DDO_Q11}

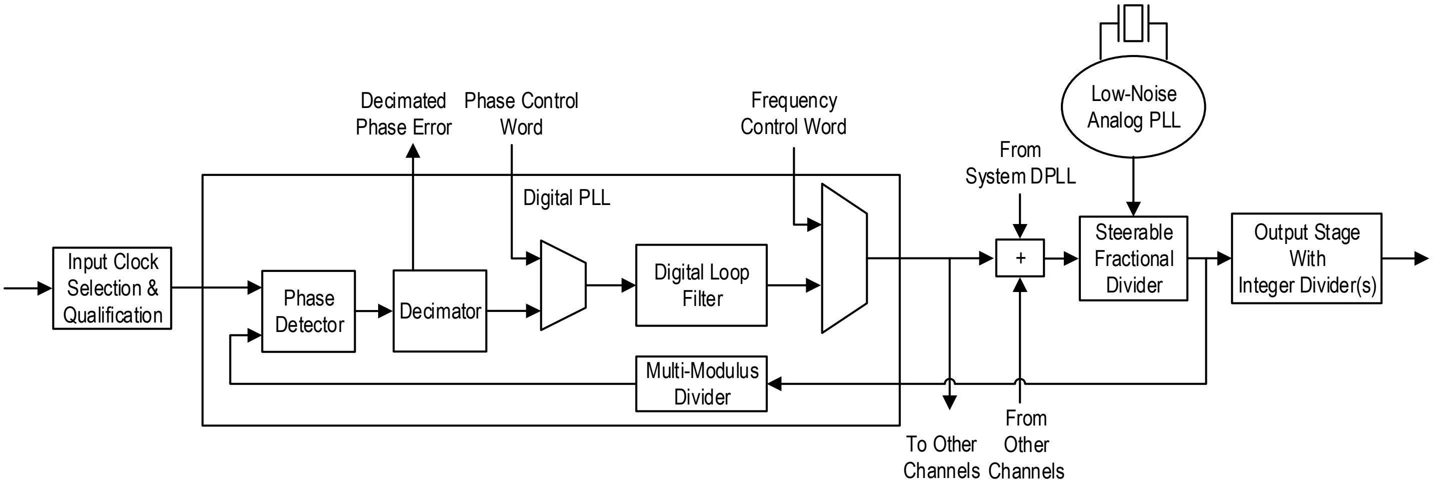
[b] Output impedance values for the Qx / nQx outputs are provided in Table 35.

Overview of the 8A3xxxx Family

The 8A3xxxx family of devices have multiple channels that can operate independently from each other, or in combination with each other (combo mode). All devices share a common channel architecture (see Figure 3) with different functional blocks within the channel being available for use in different members of the family. In addition, there are other peripheral blocks that may only be available in specific family members. The number of channels and of certain peripheral blocks (such as extra serial ports) will also vary from one device in the family to another. Across all members of the family, numbering of the functional and peripheral blocks and their associated register locations are kept consistent to enhance software compatibility and portability between members of the family.

The remaining sub-sections of this Functional Description section will describe functions within the clocking channel and peripheral functions that are available in the 8A34043 only.

Figure 3. Single PLL Channel



Functional Description

This section describes the operational modes and associated functional blocks of the 8A34043. In addition, there are several other areas of the document that describe specific functions or details that would overly burden this document. Table 3 shows related documents.

Table 3. Related Documentation

Document Title	Document Description
8A34043 Datasheet (This document)	Contains a functional overview of the device and hardware-design related details including pinouts, AC and DC specifications, and applications information related to power filtering and terminations.
8A34043-<dash code> Datasheet Addendum	Indicates pre-programmed power-up / reset configurations of this specific “dash code” part number.
8A3xxxx Family Programming Guide (v4.7)	Contains detailed register descriptions and address maps for all members of the family of devices. Please ensure to use the version indicated here for this product. The functionality described in this datasheet assumes that the device is running the update revision referred to here or a later one. For individual updates to determine differences between update revisions, see Release Note documents. Note that the device may not ship from the factory with the indicated update revision included in the device. If this is the case, the indicated revision may need to be loaded from an external EEPROM or over the serial port at each device reset.

Basic Functional Blocks of the 8A34043

Crystal Input (OSCI / OSCO)

The 8A34043 requires a 25MHz–54MHz crystal input on the OSCI/OSCO pins at all times. This input is used to drive the System APLL, which in turn is the source for all internal clocks. For more information, see Table 36 and Crystal Recommendation.

Alternatively, the crystal input can be overdriven by a crystal oscillator. For more information, see Overdriving the XTAL Interface.

Frequency Representation in 8A34043

The format for representing a frequency in the registers of the 8A34043 is:

$$f = \frac{M}{N} \text{ where M is a 48-bit integer and N is a16-bit integer}$$

M/N is a fraction that allows for the creation of non-integer frequencies

For example:

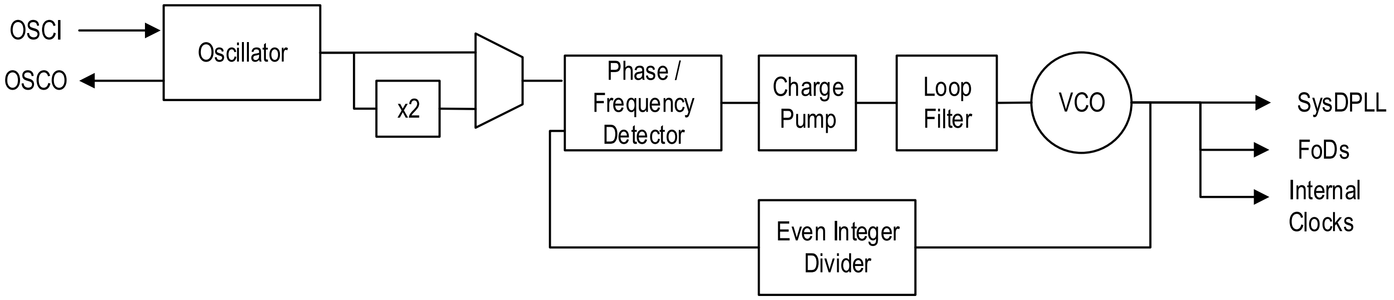
$$133.333333\text{MHz} = \frac{400}{3}\text{MHz}$$

System Analog PLL (APLL)

The System Analog Phase-Lock Loop (APLL) is shown in Figure 4. This consists of a simple analog PLL circuit that takes a reference crystal input and multiplies it up to a frequency in the 13.4GHz–13.9GHz range. That high-speed signal is then used to drive the Fractional Output Divider (FOD) circuits as described in FOD Multiplexing and Output Stages. This combination of the APLL and the FOD logic results in excellent phase noise performance and a substantial amount of flexibility in frequency and phase for the 8A34043.

One user programming option involves selecting whether the crystal reference frequency is to be used directly or run through an internal frequency doubler circuit first. An additional user programming option is to select the feedback divider value from the set of integers between 122 and 560. Between these two settings, the user should select an APLL operating frequency that is within the above-stated tuning range and also does not result in FOD divider ratios where the divide-ratio fraction is very close to 1, 0, or 1/2.

Figure 4. System Analog PLL Channel



During a device reset, the APLL is configured by loading the appropriate control register fields from the internal One-Time Programmable memory or an external serial EEPROM, whichever is enabled and has valid contents. After the reset sequence has completed, the APLL can be re-configured manually over the serial port at any time.

The System APLL is considered locked when the Loop Filter control voltage is within specified limits for the configuration selected. The 8A34043 automatically calculates these limits based on other parameters specified in the device configuration. Specific user input to set locking limits is not required. A System APLL Loss-Of-Lock alarm is generated internally. This can be read from internal status registers and/or used to drive a GPIO status signal as described in GPIO Modes.

Input Stage

The 8A34043 contains multiple input stages. An input stage can be configured as one differential or dual single-ended inputs. Some of the input stages can also be configured to support one differential plus one single-ended clock. For information on how to connect various input types to the 8A34043, see Table 4 and Applications Information.

Table 4. Input Stage Setting

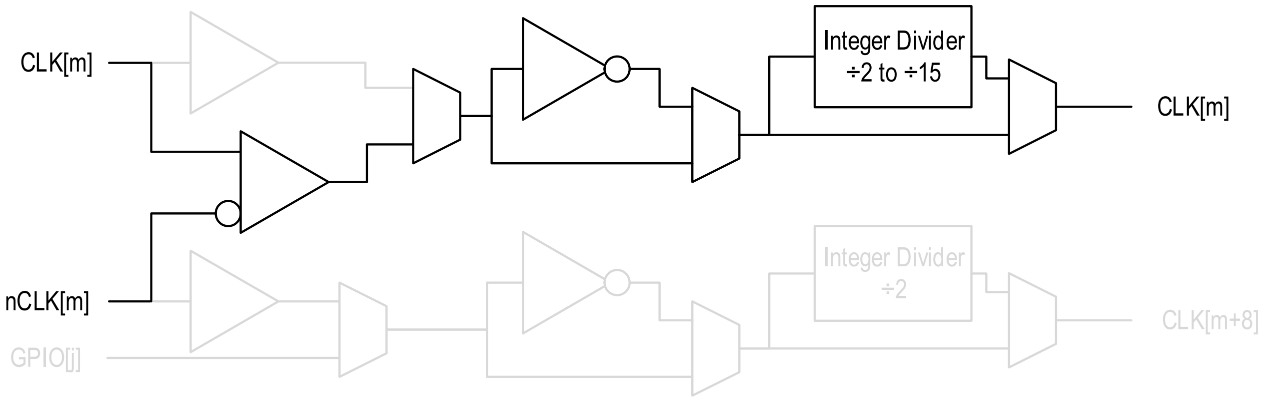
Input Protocol	Driver V_{DD} Level	Settings to Use V_{DD_CLK} Voltage 3.3V	2.5V	1.8V
PECL	3.3V	Differential + NMOS		
PECL	2.5V	Differential + PMOS		
LVDS	N/A	Differential + NMOS		
HCSL	N/A	Differential + PMOS		
CML	3.3V	Differential + NMOS		
CML	2.5V	Differential + NMOS		
CML	1.8V	Differential + NMOS		
CMOS	3.3V	Single-ended		
CMOS	2.5V			
CMOS	1.8V			

When programmed as differential only, as shown in Figure 5, the internal signal will be referred to by the index number of the input pins (e.g., CLK0 is used to refer to the differential input pair CLK0/nCLK0). It is also necessary to select the appropriate mode, PMOS or NMOS so the input buffer will work best with the incoming signal's voltage swing.

The 8A34043 supports input frequencies up to 1GHz for differential inputs. If the input reference clock frequency is higher than 150MHz, then it must be divided down to the internal frequency (less than or equal to 150MHz) used by the DPLL. An integer divider with a range between 2 to 15 is provided to divide the signal down to less than or equal to 150MHz. For input reference clock frequencies less than 150MHz, the internal divider can be bypassed.

The 8A34043 has the option to lock to the rising or falling edge of the input clock signal by selecting the inverted input path to the divider.

Figure 5. Input Stage Configured as Differential Only

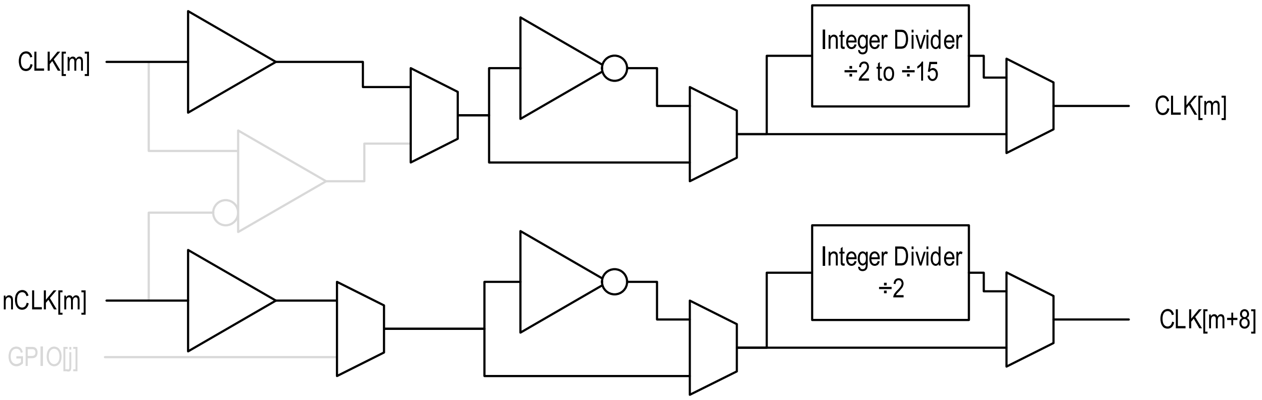


When programmed as dual single-ended as shown in Figure 6, two independent inputs are provided to the 8A34043. The input clock originating from the positive input will be referred to by using the same index number (e.g., CLK0 is used to refer to the signal originating from CLK0). The signal originating from the negative input will be referred to by using the index + 8 (e.g., CLK8 is used to refer to the signal originating from nCLK0). Note that this numbering scheme remains the same on all 8A3xxxx family members, regardless of the number of actual input pins. This is to simplify software portability between family members. PMOS versus NMOS mode does not have any effect for single-ended inputs.

The 8A34043 supports input frequencies up to 250MHz for single-ended inputs. If the input reference clock frequency is higher than 150MHz, then it needs to be divided down to the internal frequency (less or equal to 150MHz) used by the DPLL with the dividers shown in each path. For input reference clock frequencies less than 150MHz, the internal divider can be bypassed.

The 8A34043 has the option to lock to the rising or falling edge of the input clock signal for either path independently.

Figure 6. Input Stage Configured as Dual Single-Ended



When programmed as differential plus one single-ended as shown in Figure 7, two independent inputs are provided to the 8A34043. This mode can only be used with the GPIOs and input stages shown in the following table.

Table 5. Input Stages Using GPIOs as Reference Clock Inputs

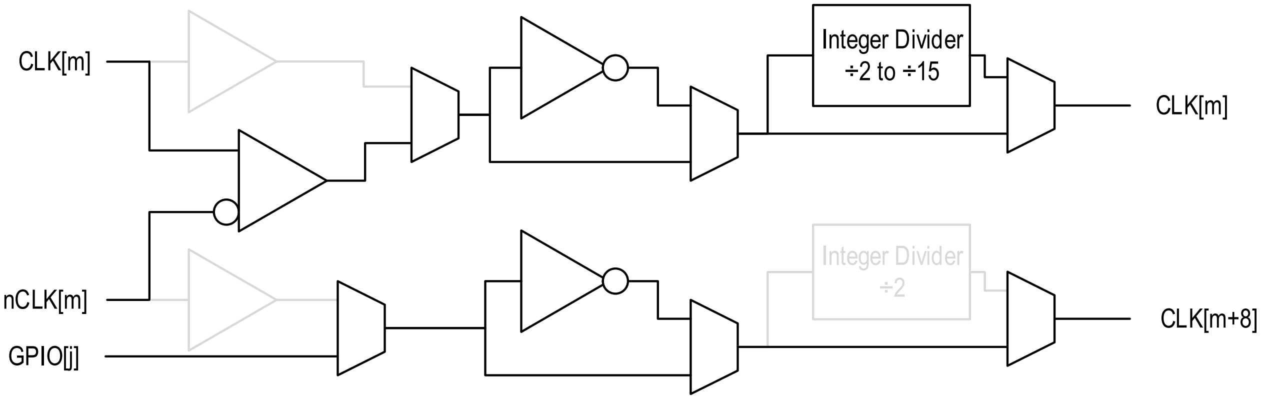
Differential Clock Input	Mapped to Internal Clock	GPIO Input	Mapped to Internal Clock
CLK0 / nCLK0	CLK[0]	GPIO[0]	CLK[8]
CLK1 / nCLK1	CLK[1]	-	CLK[9]
-	-	GPIO[3]	CLK[15]

Input stages not shown in this table can be used in the differential only mode or dual single-ended mode only. The differential input clock originating from the positive input will be referred to the same way as in differential only mode. The signal originating from the GPIO input will be referred to by using the index shown in the table. Note that this numbering scheme remains the same on all 8A3xxxx family members, regardless of the number of actual input pins. This is to simplify software portability between family members. PMOS versus NMOS mode does not have any effect for GPIO inputs.

The 8A34043 supports input frequencies up to 150MHz for GPIO inputs, so no division is necessary. If the input reference clock frequency from the differential input path is higher than 150MHz, then it needs to be divided down to the internal frequency (less or equal to 150MHz) used by the DPLL with the divider shown in its path. For input reference clock frequencies less than 150MHz, the internal divider may be bypassed.

The 8A34043 has the option to lock to the rising or falling edge of the input clock signal for either path individually.

Figure 7. Input Stage Configured as Differential Plus Single Single-Ended



In addition to the above, there are a number of other configuration bits that can be used for the input stage.

- Unused inputs can be disabled. This allows a small amount of power saving and eliminates a source of on-die noise.
- Any input can be used either as a sync or frame pulse associated with an input clock (for more information, see Frame Pulse Operation and Sync Pulse Operation).
- The frequency of each input needs to be known by the 8A34043 and so must be programmed in the registers for each active input stage.

Reference Monitoring

The quality of all input clocks is always monitored for:

- LOS (loss of signal)
- Activity
- Frequency

All input clocks are monitored all the time, including the active reference to ensure that it is still a valid reference. If any monitor detects a failure of the input clock, it will generate an internal alarm. An input clock with an alarm condition is not used for synchronization unless configured to allow it to be considered qualified in spite of the alarm.

For information on how these internal alarms can be signaled and monitored by outside resources, see Alarm Output Operation.

Loss of Signal (LOS) Monitoring

Each input clock is monitored for loss of signal (LOS). The LOS reference monitor supports normal clock operation and gapped clock operation. In normal operation, the user can specify whether the alarm condition should be tight to the expected clock period or loose. Tight monitoring will give minimum response time for loss of the input clock, but may result in false alarms due to normal clock jitter or wander. The loose threshold will take longer to detect an alarm condition but is unlikely to give false alarms. For clocks greater than 500kHz, both loose and tight specifications check for the clock edge being outside ±20nsec of the expected position to declare an alarm. For clocks less than or equal to 500kHz, loose threshold is set at ±25% of the nominal edge position and tight is set to ±1%.

In gapped clock operation, LOS is declared if the clock reference misses consecutive clock cycles. It is cleared once an active clock edge is detected. The number of consecutive clocks that are missed to declare LOS is programmable according to Table 6. A setting of 01 is equivalent to a normal clock monitor.

Table 6. Gapped Clock LOS Settings

LOS[1:0]	Number of Consecutive Clocks Missed to Declare LOS
00	Gapped Clock Monitoring Disabled (default)
01	1
10	2
11	5

There is a status register for LOS. LOS failure alarm will be set as described above. What actions are taken in the event of an alarm can be configured via registers. The LOS failure can cause a specific alarm on a GPIO and/or be used as one input to an Alert (aggregated alarm) output via GPIO if so configured.

Activity

All input reference clocks higher than 1kHz can be monitored for activity. Activity monitoring can quickly determine if a clock is within the frequency limits shown in Table 7. The method used by this monitor is not as precise as the Frequency Offset Monitor, but results are available much more quickly.

Table 7. Activity Limit

Activity_Limit[2:0]	Range for Device Update	
	v4.6 and Earlier	v4.7 and Later
000	±0.1% (default) ±1000ppm	±1000ppm
001	±1% ±10,000ppm	±260ppm
010	±2%	±130ppm
011	±4%	±83ppm
100	±8%	±65ppm
101	±10%	±52ppm
110	±15%	±18ppm
111	±20%	±12ppm

An activity failure alarm will be set if the input frequency has drifted outside the range set by the programmable range for longer than 1.25ms. What actions are taken in the event of an alarm can be configured via registers. The Activity failure can cause a specific alarm on a GPIO and/or be used as one input to an Alert (aggregated alarm) output via GPIO if so configured.

Timer

There is a timer associated with the activity qualification and disqualification of each input reference.

After an activity or LOS alarm is detected, then the timer starts. If the Activity or LOS alarm remains active for the full duration of the timer, then the reference disqualification alarm will be set to high. Register bits can be used to configure whether or not either the alarm is allowed to affect the disqualification decision or not. The disqualification timer can be selected according to Table 8.

Table 8. Disqualification Timer

CLKn_Disqualification Timer[1:0]	Description
00	2.5s (default)
01	1.25ms
10	25ms
11	50ms

After a reference is disqualified, once it returns (all alarms now clear), then a qualification timer is started. If the alarms remain cleared for the full duration selected, then the input is qualified for use again. Qualification timer settings are shown in Table 9.

Table 9. Qualification Timer

CLKn_Qualification Timer[1:0]	Description
00	4 times the Disqualification timer
01	2 times the Disqualification timer
10	8 times the Disqualification timer
11	16 times the Disqualification timer

Frequency Offset Monitoring

Each input reference is monitored for frequency offset failures. The device measures the input frequency and an alarm is raised if the input frequency exceeds the rejection range limit set as per Table 10. To avoid having the alarm toggling in case an input clock frequency is on the edge of the frequency range, a separate, narrower acceptance range must be met before the alarm will clear. The acceptance ranges are also listed in Table 10.

Table 10. Frequency Offset Limits

Frequency_Offset_Limit[2:0]	Acceptance Range	Rejection Range	Description
000	±9.2 ppm	±12 ppm	Stratum 3, Stratum 3E, G.8262 option 2
001	±13.8 ppm	±18 ppm	
010	+24.5 ppm	±32 ppm	
011	±36.6 ppm	±47.5 ppm	
100	±40 ppm	±52 ppm	SONET Minimum clock. G.813 option 2
101	±52 ppm	±67.5 ppm	
110	±64 ppm	±83 ppm	
111	±100 ppm	±130 ppm	

Advanced Input Clock Qualification

In addition to the Input Clock Selection and Qualification functions mentioned earlier, the following modes are also available.

Input Clock Qualification

For each DPLL the following conditions must be met for the input clock to be valid; otherwise, it is invalid:

- No reference monitor alarms are asserted for that input clock (unless register settings allow the alarms not to affect the decision)
- GPIO used to disqualify that input reference clock is not asserted

Clock Reference Disqualifier through GPIO

GPIO pins can be used to disqualify any input reference clock. If a GPIO is programmed to disqualify a particular input clock, then if that pin is asserted, the corresponding input reference clock will not be available for the DPLL to lock to. For example, a GPIO can be configured as an input to the 8A34043 and connected to a Loss of Signal (LOS) output coming from a PHY device that is providing a recovered clock to one of the DPLLs. If the LOS from the PHY is active, then the DPLL will disqualify that input clock and it will not be available to be locked to. If the disqualified input was the active input for the DPLL, then a switchover process will be triggered if any other valid inputs are available.

Frame Pulse Operation

In frame pulse operation, two clock signals are working together to signal alignment to a remote receiver. A higher frequency clock is providing a phase aligned reference. A second clock signal (frame signal) is running at a lower, but integer-related rate to the higher frequency clock. The active edge of the frame pulse indicates that the next rising edge of the associated higher frequency clock is to be used as an alignment edge. The 8A34043 supports either rising or falling edges on a frame pulse. The frame signal is usually implemented as a pulse rather than a square wave clock.

Any input clock and any output clock can be used as frame signal input and output respectively. This is accomplished by configuring the appropriate bits in control registers. An EPPS (even pulse per second), 1PPS, 5PPS, 10PPS, 50Hz, 100Hz, 1kHz, 2kHz, 4 kHz, or 8kHz frame input signal can be used with an associated input clock to align a frame output signal and align associated output and frame clock.

The maximum frequency for the associated input clock is 150MHz, and it can be associated with any supported frame pulse frequency for the frame signal input as long as the integer frequency relationship is maintained. The frame output frequencies are independent of the frame input frequencies; however, the output associated clock and output frame signal must have an integer relationship in order to be aligned.

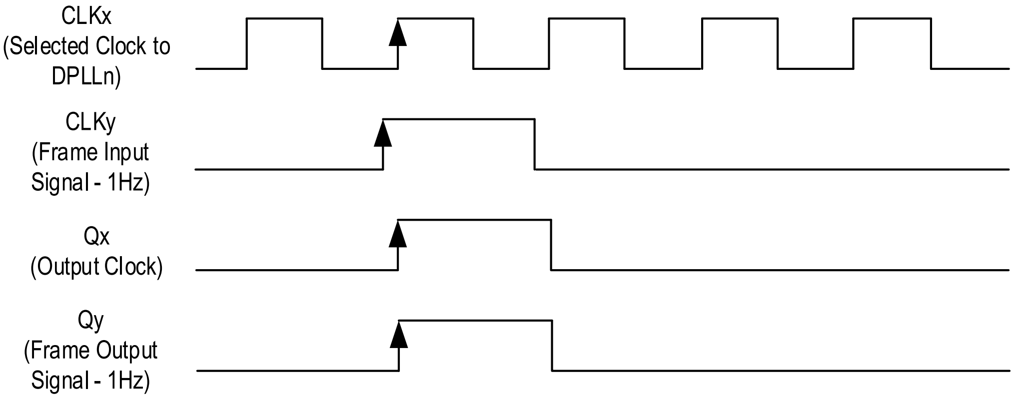
The frame pulse and clock output coming out of the same DPLL are aligned with the first rising edge of the input clock which follows the input frame pulse used by the same DPLL. The 8A34043 allows several different pulse widths to be selected (see Table 16).

When the frame input signal is enabled to synchronize the frame output signal, the output will be adjusted to align itself with the DPLLs selected input clock (associated with the input frame signal) within the input-output alignment limits indicated in AC Electrical Characteristics.

By default, the rising edge of the frame input signal identifies the rising edge of the DPLL’s selected input clock. The falling edge of the frame input signal can be used to identify the rising edge of the DPLL’s selected input clock by setting the frame pulse configuration register.

An example of the frame pulse operation is provided in Figure 8.

Figure 8. Frame Pulse Operation



In Figure 8, CLKx is the associated input clock and CLKy is the frame pulse, and they are both input to DPLLn. Qx is the output clock that is locked to CLKx, and Qy is the output frame pulse output of DPLLn.

Sync Pulse Operation

A sync pulse scenario occurs similarly to a frame pulse scenario, except that it is the rising edge of the sync signal that is used as the alignment edge rather than an edge of the associated clock.

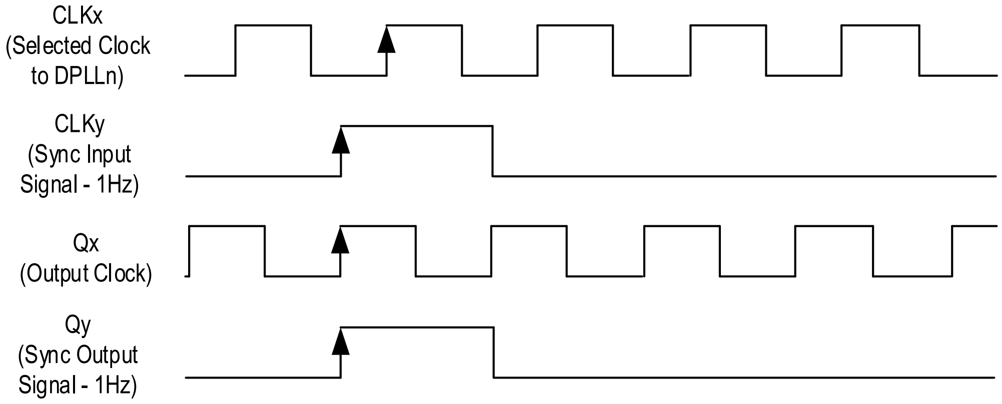
Any input clock and any output clock can be used as sync signal input and output respectively, which is done by configuring the appropriate bits in control registers. An EPPS (even pulse per second), 1PPS, 5PPS, 10PPS, 50Hz, 100Hz, 1kHz, 2kHz, 4kHz, or 8kHz sync input signal can be used with an associated input clock to align a sync output signal and output clocks.

The maximum frequency for the associated input clock is 1GHz, and it can be associated with any supported frequency for the sync signal input as long as it is an integer multiple of the sync signal frequency. The sync output frequencies should be an integer relationship of the sync input frequencies.

By default, the sync pulse and clocks output coming out of the same DPLL are aligned with the first rising edge of the sync pulse used by the same DPLL. The falling edge of the sync input signal can be used by setting the frame pulse configuration register.

An example of the sync pulse operation is provided in Figure 9.

Figure 9. Sync Pulse Operation



In Figure 9, CLKx is the associated input clock and CLKy is the sync pulse, and they are both input to DPLLn. Qx is the output clock that is locked to CLKx, and Qy is the output sync pulse output of DPLLn.

Crystal Oscillator Input (XO_DPLL)

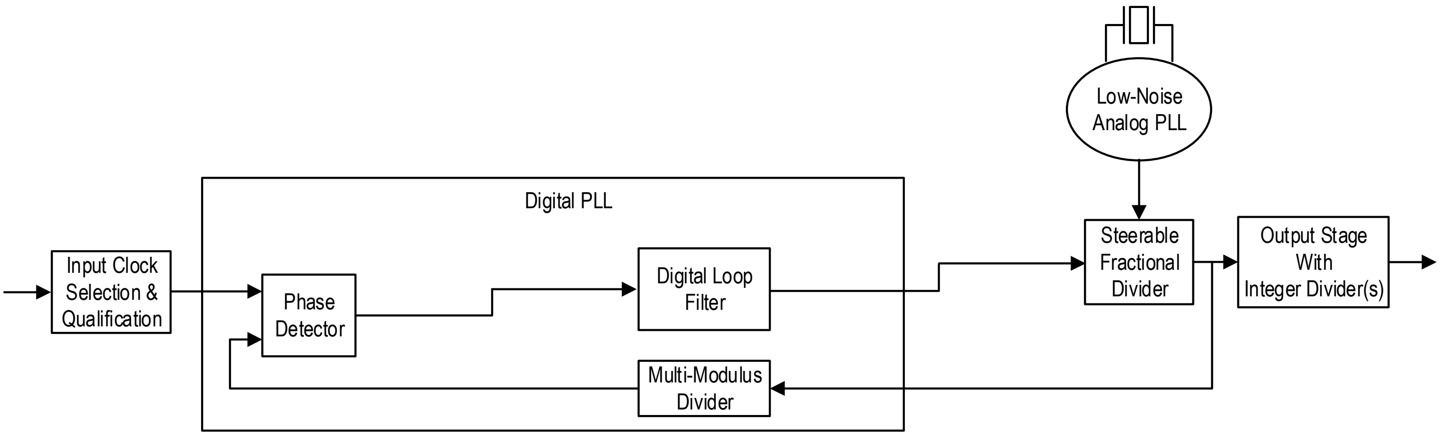
There is one additional reference clock input that is available: XO_DPLL. This is a single-ended (LVCMOS) input that is intended to be used to provide a stable frequency reference, such as an XO, TCXO or OCXO to the System DPLL. This input is not required in all cases. The crystal oscillator should be chosen accordingly to meet different applications and standard requirements (see application note, *AN-807 Recommended Crystal Oscillators for NetSynchro WAN PLL*).

Please note that there is no reference monitoring function on the XO_DPLL input. Failures of this input cannot be detected directly. Since the XO_DPLL input is usually used to drive the SysDPLL which in turn provides a reference clock to the reference monitors for all other input clocks, a simultaneous failure of all monitored input clocks could be inferred to be a failure of the XO_DPLL input in that case.

Digital Phase Locked Loop (DPLL)

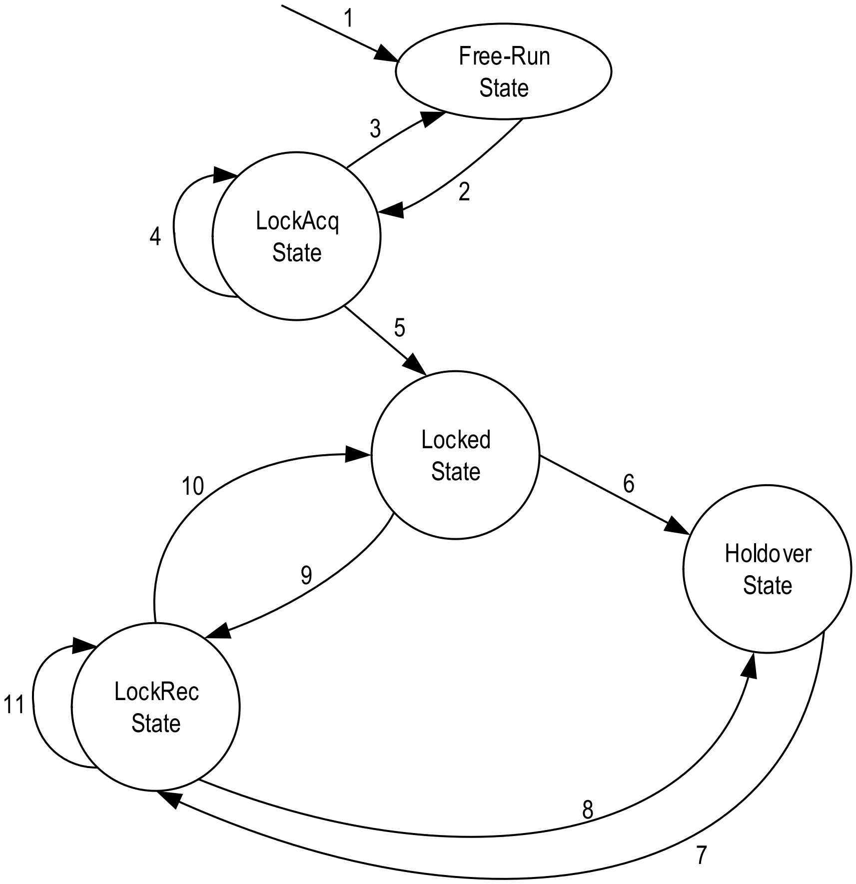
All DPLLs and the system DPLL within the 8A34043 are exactly the same. The only difference with the System DPLL channel is that it is not connected directly to any output stages. One channel of the DPLL is shown in Figure 10.

Figure 10. DPLL Channel



The DPLL operating mode operation can be set to automatic, forced locked, forced free-run, and forced holdover. The operating mode can be controlled by setting the appropriated bits in the DPLL mode register. When the DPLL is set to automatic then an internal state machine will control the states automatically. The automatic state machine is displayed in Figure 11.

Figure 11. DPLL Automatic State Machine



In Figure 11, the changes of state are based on the following:

1. Reset, the device enters Free-Run State.
2. Once an input clock is qualified and it is selected: enter the LockAcq State.
3. If the DPLL selected input clock is disqualified AND no qualified input clock is available: go back to Free-Run State.
4. DPLL switches to another qualified clock: remain in LockAcq State.
5. The DPLL locks to the selected input clock: enter Locked State.
6. The DPLL selected input clock is disqualified AND No qualified input clock is available: enter Holdover State.
7. A qualified input clock is now available: enter LockRec State.
8. If the DPLL selected input clock is disqualified AND no qualified input clock is available: go back to Holdover State.
9. The DPLL switches to another qualified clock: enter LockRec State.
10. The DPLL locks to the selected input clock: go to Locked State.
11. The DPLL switches to another qualified clock: remain in LockRec State

In items 4, 9, and 11, the DPLL switches to another qualified clock due to the selected input clock being disqualified, or the device is set to revertive mode and a qualified input clock with a higher priority becomes valid, or the device is set to Forced selection to another input clock.

Free-Run Mode

In Free-Run mode, the DPLL synthesizes clocks based on the system clock (crystal oscillator) and has no influence from a current or a previous input clock.

Combo mode can be used with Free-Run mode. In this case, the input clock of the combo master affects the combo slave's free-Run frequency. For more information, see Combo Mode.

Locked Mode

In Locked mode, the DPLL is synchronized to an input clock. The frequency and phase of the output clock track the DPLL selected input clock. The bandwidth (BW) and damping factor are programmable and are used by the DPLL when locked to an input reference. Table 11 includes some common BW settings and their associated applications.

Table 11. DPLL Bandwidth

DPLL BW (Hz)[a]	Description
17.8	
35.6	
71.2	
94.4	
142	
285	G.8251 (OTN)
333	
571	
11.4 k	
12.1 k	Jitter attenuators and Clock generators

[a] Values shown are the nominal loop bandwidths that will be provided by the DPLL. Data entry via registers uses a different format and will result in the nearest value in this table that is less than the requested value in the registers.

Holdover Mode

If all the input clocks for a particular DPLL become invalid, then the DPLL will enter holdover state.

In holdover mode, the DPLL uses stored frequency data acquired in Locked mode to control its output clocks. There are several programmable modes for the frequency offset acquisition method; it can use the frequency offset just before it entered holdover state (simple holdover), or a previously stored post-filtered frequency offset (advanced holdover).

For the advanced holdover mode, the holdover value can be post filtered and is stored in two registers at a programmable rate while the DPLL is in locked state. When the DPLL enters the advanced holdover mode, the oldest register value is restored into the integrator inside the DPLL. The rate at which the holdover registers are updated is programmable between 0s and 63s in steps of 1s.

Note: To establish an accurate holdover value for the advanced holdover mode, a stable estimate of the average input reference frequency is necessary before entering holdover. Therefore, the DPLL must have been in the locked state for a period that is based on the holdover settings (e.g., the lower the bandwidth setting for the holdover filter, the longer it takes to acquire the accurate holdover value).

The DPLL can also be forced into the holdover mode. If the forced holdover mode is used, then the DPLL will stay in holdover even if there are valid references available for the DPLL to lock to.

Manual Holdover Mode

In Manual Holdover mode, the DPLL state machine is forced into the Holdover state but the frequency offset is set by the DPLL manual holdover value register bits under user control.

DPLL Input Clock Qualification and Selection

Any Digital PLL (DPLL) can use any of the inputs as its reference. Several options exist to control how the DPLL selects which input to use at any moment in time. Whether a particular input is qualified for use at any time is based on the reference monitors. The DPLL_REF_MODE registers allow the DPLL to be set in any of the modes shown in Table 12. There is an independent reference selection process for each DPLL.

Table 12. DPLL Reference Mode

DPLL_ref_mode[3:0]	Description
0000	Automatic input clock selection
0001	Manual input clock selection
0010	GPIO
0011	Slave
0100	GPIO_Slave
0101–1111	Reserved

Automatic Input Clock Selection

If automatic input clock selection is used then the input clock selection is determined by the input clock being valid, the priority of each input clock, and the input clock configuration.

Each input can be enabled or disabled by setting register bits. If the input is enabled and reference monitors declare that input valid, then that input is qualified to be used by the DPLL. Within all the qualified inputs, the one with the highest priority is selected by the DPLL. The input clock priority is set by setting the appropriate bits in the DPLL_REF_PRIORITY registers. If a user wanted to designate several inputs as having the same priority, then an additional table allows several outputs to be placed in a group of equal priority.

Manual Input Clock Selection via Register or GPIO

If manual input clock selection is chosen then the DPLL will lock to the input clock indicated by register bits or by selected GPIO pins. The results of input reference monitoring do not affect the clock selection in manual selection mode. If the DPLL is locked to an input clock that becomes invalid, then the DPLL will go into holdover mode even in the case where there are other input clocks that are valid.

Slave or GPIO Slave Selection

This mode of clock selection is used when the 8A34043 is acting as an inactive, redundant clock source to another timing device. The other device is the master and this device is the slave. When Slave mode is selected via registers, a specific input (from the master timing device) is also indicated. That input and only that input is used in this mode. GPIO Slave mode involves the same configuration settings as if the part were a master, but a GPIO input is used to tell this device that it is now the slave and to switch to and monitor the designated input only.

DPLL Switchover Management

Revertive and Non-Revertive Switching

All DPLLs support revertive and non-revertive switching, with the default being non-revertive. During the reference selection process, a DPLL selects the valid reference with the highest priority then the DPLL locks to that input clock. In the case of non-revertive switching, the DPLL only switches to another, higher priority reference if the current reference becomes invalid. Non-revertive switching minimizes the amount of reference switches and therefore is the recommended mode.

If revertive switching is enabled and a higher priority clock becomes valid, then the DPLL will switch to that higher priority input clock unless that clock is designated as part of the same group (i.e., should be considered of equal priority).

Hitless Reference Switching

All DPLLs support Hitless Reference Switching (HS). HS is intended to minimize the phase change on the output clock when switching between input sources that may have different phases. When a DPLL switches input with HS enabled, it will first go into an internal holdover state (but not assert a holdover alarm either internally or externally), then the phase offset of the newly selected input clock with respect to the previous clock will be measured. The device then automatically compensates for the measured phase offset resulting in minimal disruption to the phase of the DPLL output clock.

The HS operation for a particular DPLL is triggered if either of the following conditions occurs:

- DPLL is locked to an input clock and switches to a different input clock
- DPLL exits from Holdover mode
- There are several additional cases where hitless reference switching can be used in synchronization applications with physical and/or packet clocks. For more information relevant to the particular application, please contact IDT.

For the two conditions, the maximum phase transient on the DPLL output clock with HS on is indicated in Table 38. Hitless reference switching can be enabled or disabled through register settings.

For 1PPS input clocks, if they have up to 100µs of phase difference between them, then the maximum phase transient on the DPLL output 1PPS clock with HS on is indicated in Table 38. If they have between 100µs and 0.5s of phase difference between them, then the maximum phase transient on the DPLL output 1PPS clock will be larger.

Phase Slope Limiting

Phase Slope Limiting (PSL) can be enabled and independently programmed for each of the DPLLs. PSL is particularly useful in the initial locking to an input or during switchover between clock inputs. If PSL is enabled then the rate of change of phase of the output clock is limited by the DPLL. The PSL settings for the device are very flexible, allowing any slope from 1ns/s to 65.536µs/s with a granularity of 1ns/s, including the values needed to meet Telecom standards as displayed in Table 13.

Table 13. Some Key DPLL Phase-Slope Limits Supported

DPLL PSL	Description
Unlimited	Limited by DPLL loop bandwidth setting
61 µs/s	Telcordia GR-1244 ST3
7.5 µs/s	G.8262 EEC option 1, G.813 SEC option 1
885 ns/s	Telcordia GR-1244 ST2, ST3E, and ST3 (objective)

DPLL Frequency Offset Limit Setting

Each DPLL has an independent setting to limit its maximum frequency range. This setting is used in conjunction with the advanced reference monitoring to provide pull-in / hold-in limit enforcement as required in many telecom standards. It will also limit the frequency deviation during locking, during holdover, and while performing switchovers. This limit must be set wide enough to cover the expected frequency range of the input when locking.

DPLL Fast Lock Operation

Each DPLL also supports a Fast Lock function. There are four options the user can choose from to perform the fast lock:

- Frequency Snap
- Phase Snap
- Open-loop phase pull-in (mutually exclusive with Phase Snap)
- Wide Acquisition Bandwidth

Any of the options can be independently enabled or disabled, and selected to be applied when the DPLL is in either the LOCKACQ state or the LOCKREC state. Although the options are mutually exclusive, the order of precedence is as listed (with frequency snap being the highest).

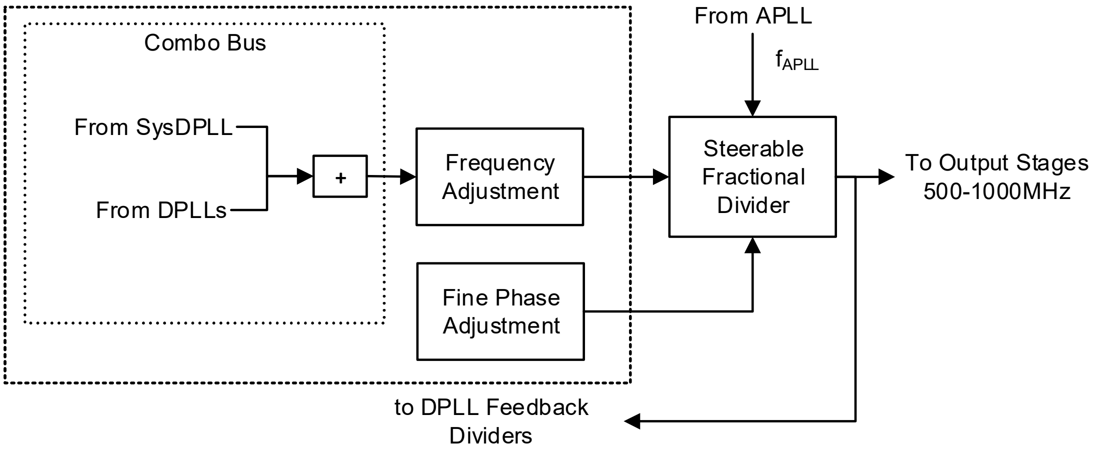
The frequency and phase snap options are recommended for locking to mid-kHz-range input clocks or lower. For frequency snap, the 8A34043 will measure the input clock from the current DPLL operating frequency, determine an approximate frequency offset, and digitally write that directly to the steerable FOD block, causing the output frequency to snap directly to the correct output frequency. The frequency snap can be optionally limited using a Frequency Slope Limit (FSL). For the phase snap and the open loop phase pull-in options, the measurement is used to determine the phase offset. With phase snap, the phase is snapped to the correct value; with open loop pull-in, the DPLL's PFD and LPF are temporarily isolated to allow for an unfiltered phase pull-in to the correct value. The combination of these methods will achieve lock very quickly, but there may be severe disruptions on the output clock while locking occurs; mainly due to the frequency/phase snaps.

The wide acquisition bandwidth option uses the DPLL in a normal operating mode, but with temporary relaxation of items like DPLL loop bandwidth, phase slope limits (PSL), or damping factor until lock is achieved. At that point, the normal DPLL limits are resumed. The user can control what limits are to be applied. In addition, for LOCKACQ state only, the DPLL's bandwidth may be temporarily opened to its maximum for a short duration of time (in ms), with the temporary phase slope limit still being applied. This pre-acquisition option is applied before the wide acquisition bandwidth option. These methods are recommended for higher frequency signals since it results in fewer perturbations on the output clock. It also allows the user to trade-off the level of changes on the clock during the locking process versus the speed of locking.

Steerable Fractional Output Divider (FOD)

The 8A34043 has multiple Steerable Fractional Divider blocks as shown in Figure 12. Each block receives a high-frequency, low-jitter clock from the System Analog PLL (APLL). It then divides that by a fixed-point (non-integer) divide ratio to produce a low-jitter output clock that is passed to the output stage(s) for further division and/or adjustment and also to the DPLL feedback dividers. The FOD output will be in the frequency range of 500MHz to 1GHz, and is independent of the output frequencies from any other FOD and from the System APLL.

Figure 12. Steerable Fractional Divider Block



The output frequency is determined by dividing the APLL frequency (f_{APLL}) by the Fractional Divider. Since f_{APLL} is between 13.4GHz and 13.9GHz and the FOD output (f_{FOD}) is between 500MHz and 1GHz, there is a limited range of valid FOD divide ratios (from 13.4 to 27.8). The Fractional Divider involves two unsigned integer values, representing the integer (INT) and fraction (FRAC) portion of the divide ratio. The fraction portion is an integer representing the 43-bit numerator of a fraction, where the denominator of that fraction is fixed at 2^{43}. IDT's Timing Commander Software can be used to determine if a particular output frequency can be represented accurately, and if not, the magnitude of the inaccuracy. If additional information is required, please contact IDT directly.

The equation for the FOD output frequency is as follows.

$$f_{FOD} = \frac{f_{APLL}}{\left(INT + \frac{FRAC}{2^{43}}\right)}$$

Note: Fractions that approach 0, 1, or 1/2 can result in increased phase noise on the output signal due to integer-boundary spurs. It is recommended that APLL frequency and FOD divider settings be coordinated to avoid such fractions.

Fine adjustments in the phase of the FOD output may also be made. A phase adjustment is performed by increasing or decreasing the frequency of operation of the FOD for a period of time. This results in the clock edges of the FOD output clock being advanced (increased FOD output frequency will move edges to the left as seen on an oscilloscope relative to some fixed reference point) or delayed (decreased FOD output frequency moves edges to the right) by some amount. The user writes a signed integer value to the fine adjust register of the FOD over the serial port. This value represents the number of picoseconds the clock edges are to be advanced (negative value) or delayed (positive value). The user can also specify a rate of phase change as Fast, Medium, or Slow. A Fast setting will apply a larger frequency change for a shorter period of time, whereas a Slow setting will apply a smaller frequency change for a longer period. Medium will choose an intermediate frequency and duration. This setting is used to accommodate devices on the output clocks that may not be able to track a fast phase change. Any number of phase changes may be applied, so the range of phase change is effectively infinite.

Note that this method of fine phase adjustment should only be used when the FOD is operating in an open-loop manner. If the FOD is being used as part of a closed-loop control, where the output phase is observed and used to track a reference input, the feedback loop may act to remove the phase adjustment. If the FOD is part of a closed-loop operation, then it is recommended that phase or frequency adjustment be performed via the Digital Phase Locked Loop (DPLL) logic.

FOD Multiplexing and Output Stages

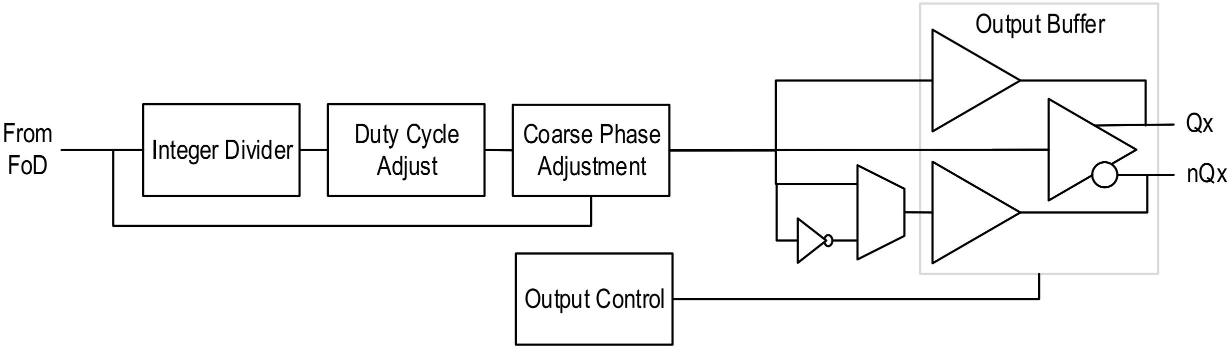
The 8A34043 has multiple output stages that are associated with the FODs and output pins as shown in the following table.

Table 14. FOD to Output Stage to Output Pin Mappings

Output Stage	Single / Dual	Output Pins	FODs that can Drive this Stage
4	Single	Q8 / nQ8	FOD_4, FOD_5
5	Single	Q9 / nQ9	FOD_5
6	Single	Q10 / nQ10	FOD_6
7	Single	Q11 / nQ11	FOD_6, FOD_7

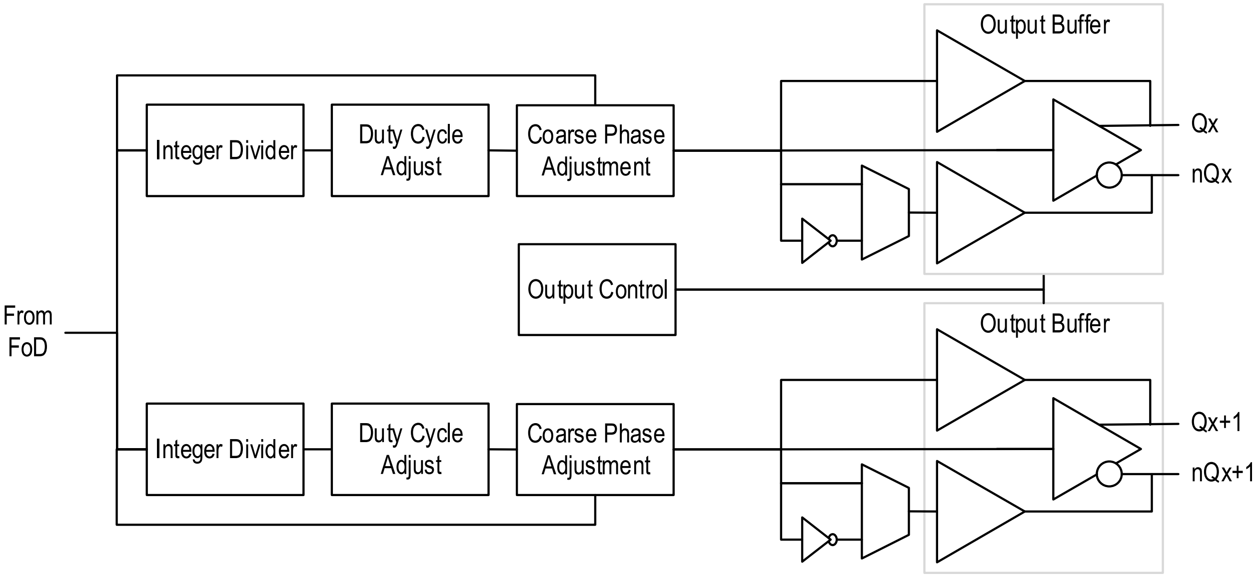
The single output stages are shown in Figure 13 and the dual output stages are shown in Figure 14.

Figure 13. Single Output Stage



Other than having two copies of each functional block fed from the same FOD, both single and dual output stages behave the same. Similarly, the two paths within the dual output stages behave the same as each other. Descriptions of each functional block are provided in the following sub-sections.

Figure 14. Dual Output Stage



Integer Output Divider

The integer output divider takes a clock signal from the FOD stage ranging from 500MHz to 1GHz and divides it by a 32-bit integer value. This results in output frequencies that range from 1GHz down to less than 0.5Hz, depending on the frequency coming from the FOD. For information on which FOD can be used with which output stage / output pins, see the previous table.

Output Duty Cycle Adjustment

The 8A34043 also has a number of options for generating pulses with different duty cycles. While these are intended primarily for frame pulses or sync pulses, duty cycle adjustment options remain accessible in all modes of operation.

As described in the previous section, each output is a divided down clock from the FOD. By default, this resulting clock will be a 50/50 duty cycle clock. If a pulse, such as a frame or sync pulse, is to be derived from the resulting clock, then the high pulse width can be programmed by a 32-bit integer value, representing the number of FOD clock cycles in the high period. This value must be less than the integer output divider value. Several examples are shown in Table 16.

Table 16. Output Duty Cycle Examples

FOD_n Frequency	Integer Output Divider Register Value	Output Frequency	Output Duty Cycle High Register Value[a]	Resulting Pulse width
500MHz	2	250MHz	0	2ns (50% / 50%)[b]
	500,000,000	1Hz (1PPS)	500	1μs[c]
655.36MHz	80	8.192MHz	0	61.035ns (50% / 50%)
	81920	8kHz	80	122ns (1UI[d])

[a] Pulses are always created by this logic as high-going pulses. If a low-going pulse is desired, the nQx output pin can be used with the inverter option selected.

[b] For precision of duty cycle achieved, see Table 38.

[c] This represents the high period of a pulse.

[d] The UI method of specifying a pulse width is often used for generation of a frame pulse. A frame pulse is always associated with another regular clock, so UI = Unit Interval of the clock output associated with the frame pulse. In this example, the associated clock is the 8.192MHz clock.

Output Coarse Phase Adjustment

The 8A34043 supports two methods for adjustment of the phase of an output clock. Fine phase adjustment can be performed in the Digital Phase Locked Loop (DPLL) block, so it can only be adjusted per-channel. In addition, coarse phase adjustment can be performed in the Output Stage and so can be performed on a per-output basis. Coarse adjust will move an output edge in units of the period of the FOD clock (T_{FOD}). Subject to the following rules, an infinite adjustment range is possible and the clock edge can be either advanced or delayed. Note that if an output phase adjustment is needed for a signal that does not meet these rules, fine phase adjustment should be used.

Rules for application of coarse phase adjust include the following:

- Coarse phase adjust lengthens or shortens the high and/or low pulses of the output clock in units of T_{FOD}.
- The coarse phase adjust will not shorten the output clock period to anything less than $2 \times T_{FOD}$ high + $2 \times T_{FOD}$ low.
  - This means coarse adjust cannot be used if the integer divider ratio is 1, 2, 3, or 4.
- Coarse phase adjust can lengthen or shorten (subject to the above rule) the output clock period by up to $2^{32} \times T_{FOD}$ high + $2^{32} \times T_{FOD}$low.
  - Such a large change in a single clock period may have serious effects on devices receiving the output clock, so the user is cautioned to consider that before applying a large adjust at one time. Multiple smaller adjustments can be performed by the user over a period of time to avoid this.

- Logic within the 8A34043 will take the positive (lengthen the period) or negative (shorten the period) adjustment value provided by the user and apply it in a single clock period to the limits listed in the preceding rules.
    - For clock signals that are using 50% / 50% duty cycle, adjustments will be applied approximately equally to the high and low portions of the clock.
    - For clock signals using other duty cycle selections, adjustments will only be applied to the low portion of the clock.
- The user can apply as many of these updates as desired, so the range of adjustment is unlimited.

Output Buffer

The output buffer structure will generate either one differential or two single-ended output signals as programmed by the user. A single output stage will have one output buffer structure and a dual stage one will have two output buffers. Each output buffer has a separate V_{DDO_Qx} pin that will affect its output voltage swing as indicated below and in Table 32.

Output Buffer in Differential Mode

When used as a differential output buffer, the user can control the output voltage swing (V_{OVS}) and common mode voltage (V_{CMR}) of the buffer. Which V_{OVS} and V_{SWING} settings may be used with a particular V_{DDO_Qx} voltage are described in Table 17. Note that V_{DDO_Qx} options of 1.5V or 1.2V cannot be used in differential mode. The nominal voltage swing options are 410mV, 600mV, 750mV, and 900mV. The nominal voltage crossing points options are 0.9V, 1.1V, 1.3V, 1.5V, 1.7V, 1.9V, 2.1V, and 2.3V. For actual values under different conditions, see Table 32.

Table 17. Configurable Output Mode Options

V_{DDO_Qx}	SWING Setting	V_{OVS} Options Supported[a]	V_{CMR} Options Supported
3.3V	00	410mV	0.9V, 1.1V, 1.3V, 1.5V, 1.7V, 1.9V, 2.1V, 2.3V
	01	600mV	0.9V, 1.1V, 1.3V, 1.5V, 1.7V, 1.9V, 2.1V, 2.3V
	10	750mV	0.9V, 1.1V, 1.3V, 1.5V, 1.7V, 1.9V, 2.1V
	11	900mV	0.9V, 1.1V, 1.3V, 1.5V, 1.7V, 1.9V
2.5V	00	410mV	0.9V, 1.1V, 1.3V, 1.5V, 1.7V
	01	600mV	0.9V, 1.1V, 1.3V, 1.5V
	10	750mV	0.9V, 1.1V, 1.3V, 1.5V
	11	900mV	0.9V, 1.1V, 1.3V
1.8V	00	410mV	0.9V, 1.1V, 1.3V
	01	600mV	0.9V, 1.1V
	10	750mV	0.9V
	11	900mV	0.9V

[a] Voltage swing values are approximate values. For actual swing values, see Table 32, Table 33, and Table 34.

The user can use this programmability to drive LVDS, 2.5V LVPECL, and 3.3V LVPECL receivers without AC-coupling. Most other desired receivers can be addressed with this programmable output, but many will require AC-coupling or additional terminations. For termination recommendations for some common receiver types, see the appropriate section of the Applications Information or contact IDT using the contact information on the last page of this document.

Output Buffer in Single-Ended Mode

When used as a single-ended output buffer, two copies of the same output clock are created with LVCMOS output levels. Each clock will have the same frequency, phase, voltage, and current characteristics. The only exception to this is that the user can program the clock from the nQx output pad to be inverted in phase relative to the one coming from the Qx output pin. The non-inverted setting may result in greater noise on these outputs and increased coupling to other output clocks in the device, so it should be used with caution.

In this mode of operation, the output buffer supports 1.8V, 2.5V, or 3.3V V_{DDO_Qx} voltages. An output swing of 1.2V or 1.5V is supported from the V_{DDO_Qx} voltage of 1.8V. For each output voltage, there are four impedance options that can be selected from. For actual voltage and impedance values under different conditions, see Table 35.

General Purpose Input/Outputs (GPIOs)

The GPIO signals are intended to provide a user with a flexible method to manage the control and status of the part via pins without providing dedicated pins for each possible function that may be wasted in a lot of applications. The GPIOs are fully configurable so that any GPIO can perform any function on any target logic block.

GPIO Modes

Each GPIO pin can be individually configured to operate in one of the following modes. Note that these modes are effective only once the 8A34043 has completed its reset sequence. During the reset sequence one or more of these pins can have different functions as outlined in Use of GPIO Pins at Reset:

- General Purpose Input – In this mode of operation, the GPIO pin will act as an input whose logic level will be monitored and reflected in an internal register that may be read over the serial port. This is the default mode if no other option is programmed in OTP or EEPROM.
- General Purpose Output – In this mode of operation, the GPIO pin will act as an output that is driven to the logic level specified in an internal register. That register can be written over the serial port.
- Alarm output – In this mode of operation, the GPIO pin will act as a single-purpose alarm or Alert (aggregated alarm) output. For information on when an alarm output will be asserted or released and alarm sources, see Alarm Output Operation. Note that each GPIO can be independently configured. If multiple GPIOs are configured the same way, they will all have the same output values.
    - Loss-of-Signal status – In this mode of operation, the GPIO pin will act as an active-high Loss-of-Signal output. There is an option to invert this output polarity via register programming. When the GPIO output is asserted, that indicates the selected input reference monitor is indicating an alarm condition. The related reference monitor and the associated GPIO pin are configured via registers. Configuration of the reference monitor will determine what constitutes an alarm. For more information on reference monitor configuration, see Reference Monitoring. Note that the GPIO output reflects the actual state of the alarm signal from the selected reference monitor. This is not a latched or “sticky” signal. This is different than the other alarm sources below.
    - Loss-of-Lock status – In this mode of operation, the GPIO pin will act as a Loss-of-Lock output. The related PLL channel and associated GPIO pin are configured via registers. For more information on alarm conditions, see Digital Phase Locked Loop (DPLL) and System Analog PLL (APLL).

      The GPIO can be programmed to show the active Loss-of-Lock status, in which case a high state on the pin will indicate that the associated DPLL or APLL is not currently locked. Alternatively, the GPIO can be programmed to flag any changes in the lock status in a “sticky” bit mode. In this mode of operation, a high state will indicate that the lock status of the associated DPLL or APLL has changed. Either the PLL has entered or left the locked state. The GPIO can be programmed to invert this polarity so that a low state indicates a status change. In either case, since this is a “sticky” status, it must be cleared by register access to the “stick” clear register to remove the alarm signal.
    - Holdover status – In this mode of operation, the GPIO pin will act as a Holdover status. The related PLL channel and associated GPIO pin are configured via registers. For more information on alarm conditions, see Digital Phase Locked Loop (DPLL).

      The GPIO can be programmed to show the active Holdover status, in which case a high state on the pin will indicate that the associated DPLL is currently in holdover state. Alternatively, the GPIO can be programmed to flag any changes in the holdover status in a “sticky” bit mode. In this mode of operation, a high state will indicate that the holdover status of the associated DPLL has changed. Either the PLL has entered or left the holdover state. The GPIO can be programmed to invert this polarity so that a low state indicates a status change. In either case, since this is a “sticky” status, it must be cleared by register access to the “stick” clear register to remove the alarm signal.

  - Alert (aggregated alarm) status – In this mode of operation, the GPIO will act as the logical OR of all alarm indicators that are enabled to drive this output. Only “sticky” bits are available to drive the GPIO in this mode. This output will be asserted if any of the “sticky” bits are asserted and enabled to cause the Alert (aggregated alarm). To clear this output, all contributing “sticky” bits must be individually cleared. This output will be active-high to indicate one or more alarms are asserted. There is an option to invert this output polarity via register programming.
- Output Disable control – In this mode of operation, the GPIO pin will act as a control input. When the GPIO input is high, the selected output clock(s) will be disabled, then placed in high-impedance state. When the GPIO pin is low, the selected output clock(s) will be enabled and drive their outputs as configured. For information on output frequency and output levels, see System Analog PLL (APLL) and FOD Multiplexing and Output Stages. Selection of which output(s) are controlled by which GPIO(s) is configured via registers over the serial port or by OTP or EEPROM at reset. Each GPIO can be configured to control any or all outputs (or none). So all combinations can be set up from a single GPIO controlling all outputs, to all outputs responding to individual GPIO signals and any grouping in between.
- Single-ended Input Clock – In this mode of operation a single-ended input clock can be applied to certain GPIOs that map to specific input stages (see Input Stage for details, including which GPIOs map to which input references). This can be used if extra single-ended inputs are needed due to all input reference clock pins being taken-up by differential input references. This mode cannot be used if an input stage already has two single-ended input references from the CLKx/nCLKx input pins.
- Manual Clock Selection control – In this mode of operation, the GPIO pin acts as an input that will manually select between one of two inputs for a specific DPLL channel. The specific input references and the PLL channel must be preconfigured via registers. Assertion of the GPIO will select the higher priority input and de-assertion will select the lower priority input. For information on how to configure the input references for a PLL channel, see DPLL Input Clock Qualification and Selection.
- DCO Increment – In this mode of operation, the GPIO pin will act as an increment command input pin for a specific channel configured as a DCO. The rising edge of the GPIO pin will cause an increment function on the indicated DCO. The amount of the increment and the related DCO to increment must be previously configured via registers. For more information, see Increment / Decrement Registers and Pins.
- DCO Decrement – In this mode of operation, the GPIO pin will act as a decrement command input pin for a specific channel configured as a DCO. The rising edge of the GPIO pin will cause a decrement function on the indicated DCO. The amount of the decrement and the related DCO to decrement must be previously configured via registers. For more information, see Increment / Decrement Registers and Pins.
- Clock Disqualification Input – In this mode of operation, the GPIO pin will act as an active-high disqualification input for a preconfigured input and DPLL. This is intended to be connected to the LOS output of a PHY or other device. For more information, see DPLL Input Clock Qualification and Selection.

GPIO Pin Configuration

GPIO pins are all powered off a separate voltage supply that supports 1.5V, 1.8V, 2.5V, or 3.3V operation. An internal register bit must be set to indicate which voltage level is being used on the GPIO pins. This setting is a global one for all GPIOs.

In addition, each GPIO can be enabled or disabled under register control. If enabled and configured in an operating mode that makes it an output, the user can choose if the GPIO output will function as an open-drain output or a CMOS output. The open-drain output drives low but is pulled high by a pull-up resistor. There is a very weak pull-up internal to the 8A34043, but an external pull-up is strongly recommended. In CMOS mode, the output voltage will be driven actively both high and low as needed. Register control can also enable a pull-up (default) or pull-down.

Alarm Output Operation

There are many internal status and alarm conditions within the 8A34043 that can be monitored over the serial port by polling registers. Several of these can be directed to GPIO pins as indicated in General Purpose Input/Outputs (GPIOs). In addition, one of the GPIOs can be designated as an Alert (aggregated alarm) output signal called an Alert output.

The 8A34043 provides both a "live" and a "sticky" status for each potential alarm condition. A "live" bit shows the status of that alarm signal at the moment it is read over the serial port. A "sticky" bit will assert when an alarm condition changes state and will remain asserted until the user clears it by writing to the appropriate clear bit over the serial port. When a GPIO is configured to show the status of a specific alarm, it will show the "live" or sticky status of that alarm, depending on the specific alarm, where a high output on the GPIO indicates the alarm is present. For more information, see GPIO Modes. The GPIO can be programmed to invert the alarm if desired.

The Alert (aggregated alarm) output logic only uses the "sticky" status bit for alarms. This ensures when a software routine reads the 8A34043 there will be an indication of what caused the alarm in the first place. Note that there can be multiple sticky bits asserted. Table 18 shows the alarm conditions possible within the 8A34043. Note that the reference monitor, the DPLL, and the System DPLL blocks can generate the indicated alarms.

Table 18. Alarm Indications

Logic Bloc	Specific Alarm	Conditions for Live Alarm[a] to Assert	Conditions for Live Alarm[a] to Negate[b]
Reference Monitoring	Frequency Offset Limit Exceeded	See Frequency Offset Monitoring	See Frequency Offset Monitoring
	Loss-of-Signal	See Loss of Signal (LOS) Monitoring	See Loss of Signal (LOS) Monitoring
	Activity Alarm	See Activity Monitor	See Activity Monitor
Digital Phase Locked Loop (DPLL)[c][d]	Holdover	DPLL has entered / is in the Holdover state	DPLL no longer in Holdover state
	Locked	DPLL has entered / is in the Locked state and System APLL is in the Locked state	DPLL and/or System APLL no longer in the Locked state

[a] "Sticky" alarm bits are set whenever the associated live alarm changes state. So there will be a new "sticky" alarm on both assertion and negation of the appropriate live alarm indication.

[b] Only the "live" status will negate by itself. The "sticky" needs to be explicitly cleared by the user.

[c] For the Digital PLL, "sticky" alarms are raised when the state machine transitions into specific states and "live" status indicates that the Digital PLL is currently in a specific state. The user can read the current state of the Digital PLL state machine from status registers over the serial port.

[d] This includes the System DPLL, as well as all Digital PLLs.

For each alarm type in each logic block that can generate them, there is a "live" status, a "sticky" status, a "sticky" clear control and a series of control bits that indicate what effects the alarm will have. When the "live" status changes state, the "sticky" status will assert. If so configured via registers, that alarm may generate an external signal via GPIO. That signal may be an individual alarm output or an Alert (aggregated alarm). Once external software responds, it is expected to read the sticky status bits to determine the source(s) of the alarm and any other status information it may need to take appropriate action. The "sticky" clear control can be used to clear any or all of the bits that contributed to the alarm output being asserted.

In addition to the above controls and status, each potential alarming logic block has its own controls and status. Each of the reference monitors has a "sticky" status bit, a "sticky" clear bit and various control bits. Each of the DPLLs and the SysDPLL have a "sticky" status bit, a "sticky" clear bit, control bits and a PLL state status field. These functions behave as described in the previous paragraph. Note that both the individual alarm "sticky" status and the logic block "sticky" status must be cleared to fully remove the source of the alarm output. Individual "sticky" alarms should be cleared first so that all individual alarms associated with a logic block won't cause a re-assertion of the block "sticky" alarm.

Note: Clearing of all sticky bits via the registers may not result in the Alarm output pin negating for up to 200µsec and so that GPIO should not be used as a direct input to a CPU's interrupt input or multiple interrupts may be generated within that CPU for a single alarm event.

There are also several configuration bits that act on the alarm output logic as a whole. There is a global alarm enable control that will enable or disable all alarm sources. This can be used during alarm service routines to prevent new alarms while that handler is executing in external software. The user can also designate a GPIO as an Alert (aggregated alarm) output and determine which individual alarms will be able to drive it. The GPIO can be programmed to invert the Alert (aggregated alarm) if desired.

Temperature Sensor

The 8A34043 includes a temperature sensor. The accuracy of the sensor is ±2°C. The temperature can be read in degrees Celsius from registers. The reading is updated once every 10 seconds.

Device Initial Configuration

During its reset sequence, the 8A34043 will load its initial configuration, enable internal regulators, establish and enable internal clocks, perform initial calibration of the Analog PLL, and lock it to the reference on the OSCI/OSCO pins. Depending on the initial configuration, it may also bring up Digital PLLs, lock to input references including any OCXO/TCXOs, and generate output clocks.

The following four mechanisms can be used to establish the initial configuration during the reset sequence:

- State of certain GPIO pins (see Table 19) at the rising edge of the nMR signal
- Configuration previously stored in One-Time Programmable memory
- Configuration stored in an external I^2C EEPROM
- Default values for internal registers

Each of these is discussed individually in the following sections and then integrated into the reset sequence.

Use of GPIO Pins at Reset

All of the device GPIO pins are sampled at the rising edge of the nMR (master reset) signal and some of them may be used in setting the initial configuration. Table 19 shows which pins are used to control what aspects of the initial configuration. All of these register settings can be overwritten later via serial port accesses. Note also that several GPIOs can be used as a JTAG port when in Test mode. For information, see JTAG Interface. If these GPIOs are being used as a JTAG interface, it is recommended that they not be used for any of the reset functions outlined below.

Table 19. GPIO Pin Usage at Start-Up

GPIO Number	Function	Internal Pull-up or Pull-down
9	0 = Auxiliary serial port uses SPI protocol 1 = Auxiliary serial port uses I^2C protocol	Pull-up
8	Must be high during reset active period	Pull-up
4 pins user selectable[a]	Identifies which stored configuration in OTP to use for initial configuration (has no effect with “-000” unprogrammed devices). See details just below this table.	Pull-up
1 pin user selectable[a]	Disables EEPROM accesses during start-up sequence. By default, no GPIO is used for this purpose, so the device will attempt to find an external EEPROM to check for additional start-up information by default. See details just below this table.	Pull-up
1 pin user selectable[a]	Provides pin control for I^2C slave serial port (for serial port selected by GPIO[9] as I^2C) default base address bit A2. Has no effect on serial port selected as SPI. By default no GPIO is used for this purpose, so the default I^2C slave port base address will have a 0 for bit A2. See details just below this table.	Pull-up

[a] Selection of this mode for a GPIO is performed using the Device Information block in the OTP memory, which is programmed by IDT at the factory for dash codes that are non-zero. “-000” dash code devices are considered unprogrammed and so will have the default behavior indicated above.

Any of the available GPIOs can be used as the following:

- I^{2}C base address bit A2 – This is for the serial port when selected as I^{2}C during the start-up sequence using GPIO[9]. If no GPIOs are configured in this mode, bit A2 of the slave serial port base address will be zero. The value of the I^{2}C base address and the serial port configuration can be overwritten by SCSR configuration data or serial port accesses later in the start-up sequence. If more than one GPIO is programmed with this functionality, only the one with the highest index will be used (e.g., if both GPIO[5] and GPIO[7] are programmed to do this, only GPIO[7] would be used).
- EEPROM Access Disable control – A high input value on a GPIO programmed with this function prevents a device from attempting to read device update information or SCSR configuration data from an external I^{2}C EEPROM. This will speed up device reset time but prevent access to updated information that may be stored in EEPROM. If no GPIOs are configured in this mode then the device will attempt to locate an external EEPROM at the appropriate point in the start-up sequence. If multiple GPIOs are configured to perform this function then any one of them being active will disable EEPROM accesses, so it is recommended that no more than one GPIO be programmed for this function.
- Default Configuration Select control – If no GPIOs are selected then GPIO[3:0] will be assumed and the value on those pins at the rising edge of the nMR signal will be used to select which of the SCSR configurations in OTP memory is to be used. Note that since a GPIO is pulled-up by default, unless these pins are pulled or driven low during the reset period, this will select SCSR Configuration 15. If one or more GPIOs are selected for this function, then the value on those pins at the rising edge of nMR will be used to select the SCSR configuration to be loaded. The Device Information block of the OTP can be configured to select any of up to four GPIO pins to be used for this purpose if the default GPIOs are not convenient. The GPIOs chosen do not have to be sequential, but whichever ones are chosen, the one with the lowest index number will be the LSB and so on in order of the index until the GPIO with the highest index is the MSB. No GPIO that appears elsewhere in this table should be used for this purpose.
  For example, if GPIO[8], GPIO[6], GPIO[5] and GPIO[2] are used, GPIO[8] is the MSB, GPIO[6] is next most significant, GPIO[5] is next and GPIO[2] is the LSB.

  If less than four GPIO pins are selected, then the selected GPIOs will be used as the least-significant bits of a 4-bit selection value, with the upper bits set to zero. If more than four GPIOs are programmed for this function, then the GPIOs will form a larger bit-length word for selection of internal configuration.

Default Values for Registers

All registers are defined so that the default state (without any configuration data from OTP or EEPROM being loaded) will cause the device to power-up with none of the outputs enabled and all GPIO signals in General-Purpose Input mode. Users can then program any desired configuration data over the serial port once the reset sequence has completed.

One-Time Programmable (OTP) Memory

The 8A34043 contains a 32kbytes One-Time Programmable (OTP) memory block that is customer programmable. The term “one-time programmable” refers to individual blocks within the memory structure. Different blocks can be programmed at different times, but each block can only be programmed once. The data structure within the OTP is designed to facilitate multiple updates and multiple configurations being stored, up to the limit of the physical memory space.

Access to OTP memory is via serial port through registers that communicate with an internal OTP controller state machine. The state machine protocol is handled via IDT’s Timing Commander GUI software, which is the recommended access mechanism. For customers that wish to program OTP via another method, such as in their own production processes, should contact IDT for details on this state machine interface. Note that OTP programming is considered an “offline” function and should not be performed while the device is in an operational system.

After reset of the 8A34043, all internal registers are reset to their default values, then OTP contents are loaded into the device’s internal registers. A Device Information block programmed by IDT at Final Test will always be loaded. This provides information that is specific to the device, including product ID codes and revision information. In addition there are zero or more device configurations stored in the OTP by customer programming or by IDT at the factory if a special dash-code part number is requested. Certain GPIO pins are sampled at the rising edge of the external nMR input signal. The state of those pins at that time will be used by the 8A34043 to determine which of up to 16 configurations stored in the OTP to load into the device registers. For information on how to select a configuration, see Use of GPIO Pins at Reset.

Storage of configuration data in OTP does not require having a value stored for every register in the device. Register default values are defined to ensure that most functions will be disabled or otherwise made as neutral as possible. This allows only features that are being used in any particular configuration (and their associated trigger registers as defined in the *8A3xxxx Family Programming Guide*) to need to be stored in OTP for that configuration. The intent of this is to minimize the size a configuration takes in OTP to allow more configurations to be stored there. For this reason, the exact number of configurations storeable in OTP cannot be predetermined. There will be a minimum of two configurations and a maximum of 16 configuration capacity in the OTP.

Part numbers with -000 as the dash code number are considered “unprogrammed” parts, but will come with at least a Device Information block pre-programmed with IDT-proprietary information, including parameters needed to successfully boot the device to the point where it can read its configuration data. One Device Update block may also be programmed if determined to be appropriate by IDT.

Custom user configurations indicated with non-zero dash code part numbers will in addition have one or more SCSR Configuration sections pre-programmed as indicated in the datasheet addendum for that particular dash code part number.

Note that a programmed configuration, Device Information block, or Device Update block may be invalidated via the OTP programming interface, and if sufficient OTP space remains, a new one added to replace it. Note that this does not erase or remove the original data and the space it consumes. It just marks it to be ignored by the device. This allows for a limited ability to update a device in the field either from a device functional update or configuration data perspective. This is a purely software-driven process handled over the serial port. Please contact IDT for support if this type of in-field upgrade / change is desired. Note that the ability to perform this type of in-field update is highly dependent on the size of the change versus the remaining space in OTP, so it will not be possible in all cases.

Configuration Data in OTP

Users can program multiple configurations into the internal One-Time Programmable memory. IDT’s Timing Commander GUI Software can perform this function. Please contact IDT for sample code if this needs to be performed in another way by the end user. By using the GPIO pins at start-up as outlined in Use of GPIO Pins at Reset, one of those configurations can be chosen for use as the initial values in the device registers after reset. Register values can be changed at any time over the serial port, but any such changes are not stored in OTP and will be lost on reset or power-down.

The OTP is organized so that only configuration data that changes from the register default values needs to be stored. This saves OTP space and allows the potential for more configurations to be stored in the OTP.

If the indicated configuration in OTP has a checksum error, it will not be loaded and registers will be left at their default values.

Use of External I^{2}C EEPROM

The 8A34043 can search for additional configuration or device updates in an external I^{2}C EEPROM. As described in the Use of GPIO Pins at Reset, a GPIO can be configured to select whether or not this search will be performed during the reset sequence.

The remainder of this description assumes the EEPROM search is enabled.

The 8A34043 will use its I^{2}C Master Port to attempt to access an external I^{2}C EEPROM at base address 1010000 (binary) at an I^{2}C frequency of 1MHz. If there is no response, this will be repeated at base address 1010001 (binary) at 1MHz. This will repeat up to address 1010111 (binary) at 1MHz. If there still are no responses, the search will be repeated at 400kHz and then again at 100kHz. If no response is received after this entire sequence, the device will assume there is no EEPROM available. Any errors in the process will be reported in status registers.

Device Updates in External I^{2}C EEPROM

As indicated in Reset Sequence, if enabled, the 8A34043 will search for Device Update information in an external I^{2}C EEPROM. It will first identify all valid EEPROMs attached to the I^{2}C master port as described above. Each valid EEPROM will be checked for a valid Device Update Block header with valid checksum at address offset 0x0000 within the EEPROM. The first such valid block will be used as described in Reset Sequence.

Configuration Data in External I^2C EEPROM

As a final option for device configuration, the initial configuration can be read from an external I^2C EEPROM. IDT's Timing Commander GUI Software can generate the necessary EEPROM load information as an Intel HEX file for this purpose. The 8A34043 will search each EEPROM identified during the above search sequence for a valid configuration data block (valid header and checksum). The first valid block found will be loaded into internal registers after checksum validation. The search will terminate after the first valid block is found and loaded. This means that only a single valid configuration block can be stored via the EEPROM method.

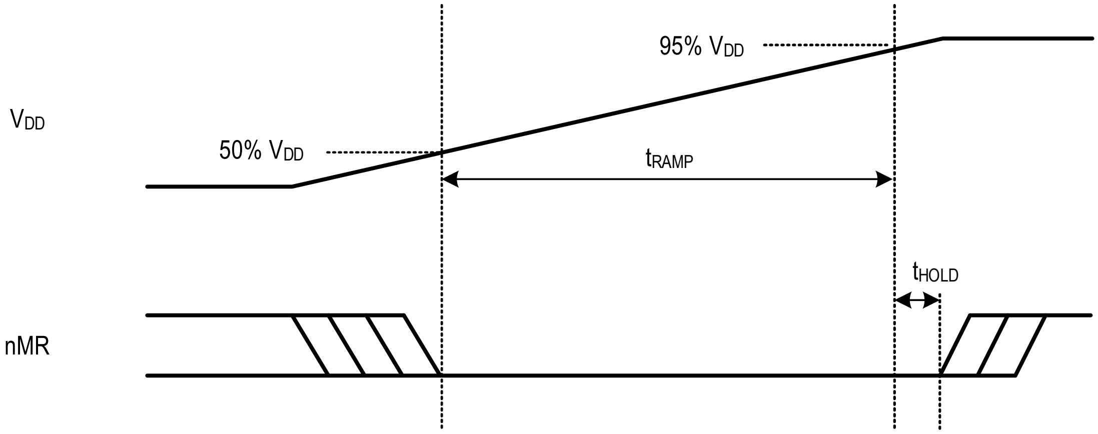
When the device searches for an EEPROM configuration, it will check for a valid block at address offsets 0x0000 and 0xF000 within an EEPROM. If using this configuration method, see the warning in Step 5 – Search for Configuration in External EEPROM.

Reset Sequence

Figure 15 shows the relationship between the master reset signal (nMR) and the supply voltages for the 8A34043. There are no power sequencing requirements between the power rails, so V_{DD} in the diagram represents any of the supply voltages. To ensure there is no anomalous behavior from the device as it powers up, it is recommended that the nMR signal be asserted (low) before any voltage supply reaches the minimum voltage shown in the figure. nMR should remain asserted until a short hold time (t_{HOLD} ~10nsec) after all supply voltages reach the operating window of 95% of nominal voltage. nMR must be asserted or the device will not function correctly after power-up.

One additional consideration is that once minimum voltage is reached on all voltage supplies, internal regulators and voltage references will need the amount of start-up time specified in Table 38, "Regulators Ready." If the time t_{RAMP} shown in Figure 15 is less than the voltage regulators' start-up time indicated in Table 38, then release of nMR should be delayed.

Figure 15. Power-Up Reset Sequencing



In cases where the device is not powering up and just being reset, a low pulse on nMR of 20ns will be sufficient to reset the device.

The following reset sequence will start from the rising (negating) edge of the nMR (master reset) signal when nTEST is de-asserted (high).

Step 0 – Reset Sequence Starting Condition

Once power rails reach nominal values and the nMR signal has been asserted, the 8A34043 will be in the following state:

- All Qx / nQx outputs will be in a high-impedance state.
- All GPIO pins will be set to General-Purpose Inputs, so none will be driving the output.
- The serial port protocols are not set at this point in the reset sequence, so the ports will not respond.
- Device Information block loaded from internal OTP to configure what GPIOs will be used for what start-up functions in Step 1.
- The System APLL will be configured and calibrated based on frequency information in the Device Information block then locked to the reference clock on the OSCI input.

Step 1 – Negation of nMR (Rising Edge)

At the rising edge of the nMR signal, the state on the GPIO pins at that time is latched. After a short hold time, the GPIOs can release their reset levels and assume their normal operation modes. The latched values will be used in later stages of the reset sequence.

Step 2 – Internally Set Default Conditions

An internal image of the device registers will be created in internal RAM with all registers set to their default values. This will not result in any changes to the GPIO or output clock signals from their Step 0 condition.

Based on the serial port protocol selection made via the GPIO pin in Step 1, serial port configuration will be completed as indicated by the GPIO input pin. If SPI mode is selected by the GPIO, the register default values will configure it to use 4-wire SPI mode.

Step 3 – Scan for Device Updates in EEPROM

If enabled to do so, the 8A34043 will check for device functional update information in any available EEPROMs (for information on how EEPROMs are searched for, see Use of External I^2C EEPROM). If such information is found, it will be loaded, the device functionality updated, and then the part will reinitialize to Step 0.

Step 4 – Read Configuration from OTP

Using the GPIO values latched in Step 1, the device will search the internal OTP memory for the indicated configuration number. If no such configuration is found or the configuration has an invalid checksum, the device will skip to Step 5. Any errors in this process will be reported. If loading from OTP was successful, which configuration number was loaded will be reported.

If the requested configuration is found and is valid, the device will load the registers indicated in the configuration data with the stored data values in the internal register image. Any register not included in the configuration data set will remain at its default value in the register image.

Note: Many register modules have explicitly defined trigger registers that when written will cause the other register settings in that module to take effect. Users must ensure that the configuration in OTP will cause a write to all applicable trigger registers, even if that register's contents would be all zero. Multi-byte register fields also require all bytes of the field to be written to ensuring triggering. For indications of which trigger registers are associated with which other registers, see the *8A3xxxx Family Programming Guide*.

The contents of several of the registers will be used to guide the remainder of the reset sequence:

- If the APLL feedback divider value was programmed in this step, perform APLL calibration in parallel with remaining reset activities.
- Re-configure the serial ports to use I^2C or SPI protocols as indicated. For information, see I2C Slave Operation or SPI Operation.

Step 5 – Search for Configuration in External EEPROM

The 8A34043 will check for configuration information in any available EEPROM (for information on how EEPROMs are searched for, see Use of External I^2C EEPROM).

If a valid configuration data block is found, it will be read, its checksum validated and if that passes, loaded into the internal register image similarly to OTP configuration data described in Step 4. If the data found is not of the correct format or the data block fails a checksum comparison, it will be ignored. The search will continue through the EEPROM and on to the next EEPROM address until the complete range has been searched or a valid configuration block has been found and applied to the internal register image. Then the sequence will proceed to Step 6.

Note: Since OTP and EEPROM configuration data rarely consists of a full register image, reading of configuration data from OTP and then from a configuration block stored in EEPROM may result in internal registers being loaded with conflicting settings drawn partially from each of the configuration data sets being loaded. It is strongly recommended that a configuration block placed in EEPROM only be used when no valid configuration is being pointed to in OTP by GPIO signals (or there is no valid configuration in OTP at all). If multiple configurations are to be used then the user must ensure all registers are set to the desired values by the final configuration block to be loaded.

Step 6 - Load OTP Hotfix and Execute

If the 8A34043 OTP memory contains a hotfix, that information will be loaded into RAM and executed at this point.

Step 7 – Complete Configuration

The 8A34043 will complete the reset and initial configuration process at this point and begin normal operations. Completion steps include the following:

1. If configuration information was loaded in Step 4 or Step 5, recalibrate the System APLL and lock it to the reference clock on the OSCI input.
2. Perform a temperature sensor cycle to establish an initial value in internal registers.
3. Enable serial port operation as configured.
4. Apply configuration settings from the internal register image to the actual registers and enable output clocks and GPIOs as configured.
5. Begin operation on input reference monitors and PLL state machine alarms/status.
6. Enable alarm operation as configured.

Note that there are several scenarios in which the reset sequence will reach this point without retrieving any configuration data and with all registers in the default state. This may be intentional for users who wish to configure only via the serial port or the result of a problem in the loading of a configuration. Users can read appropriate status bits to determine what failures, if any, occurred during the reset sequence.

Clock Gating and Logic Power-Down Control

The 8A34043 can disable the clocks to many logic blocks inside the device. It also can turn off internal power regulators, disabling individual power domains within the part. Because of the potentially complex interactions of the logic blocks within the device, logic within the part will handle the decision-making of what will be powered-off, versus clock-gated, versus fully operational at any time. By default, the device will configure itself with functions in the lowest power-consuming state consistent with powering up the part and reading a user configuration. User configurations, whether stored in internal OTP, external EEPROM, or manually adjusted over the serial port, should make use of register bits to only turn on functions that are needed. Also if a function is no longer needed, register bits should be used to indicate it is no longer required. Internal logic will reduce its power-consumption state in reaction to these indicators to the greatest extent possible.

For more information on how to calculate power consumption for a particular configuration, consult IDT's Timing Commander software for more precise results for a particular configuration.

Serial Port Functions

The 8A34043 supports two serial ports. One is a dedicated I^2C Master port used for loading configuration data at reset and the other is a configurable slave I^2C or SPI port that can be used at any time after the reset sequence is complete to monitor and/or configure the device.

The operation of the I^2C Master Port is described in I2C Master. The SCL_M and SDA_M pins are used for this port and can be connected to the same I^2C bus as the slave port if it is configured in I^2C mode.

For information on the operation of the master I^2C and slave I^2C or SPI ports, see the appropriate section below.

A slave serial port can be reconfigured at any time by accessing the appropriate registers within a single burst write. This includes configuration options with each protocol or switching between protocols (I^2C to SPI or vice versa). However, it is recommended that the full operating mode configuration, including page sizes for registers for a serial port be set in the initial configuration data read from OTP or external EEPROM (for information, see Device Initial Configuration).

Note on Signal Naming in the Remainder of the Serial Port Sections

The pin names indicated in the Pin Description table are meant to indicate the function of that signal when used in SPI mode and also the function when in I^{2}C mode. In the remainder of the Serial Port Functions descriptions, the SPI descriptions will refer to the signals by their function in the selected mode, as shown in Table 20.

Table 20. Serial Port Pin to Function Mapping

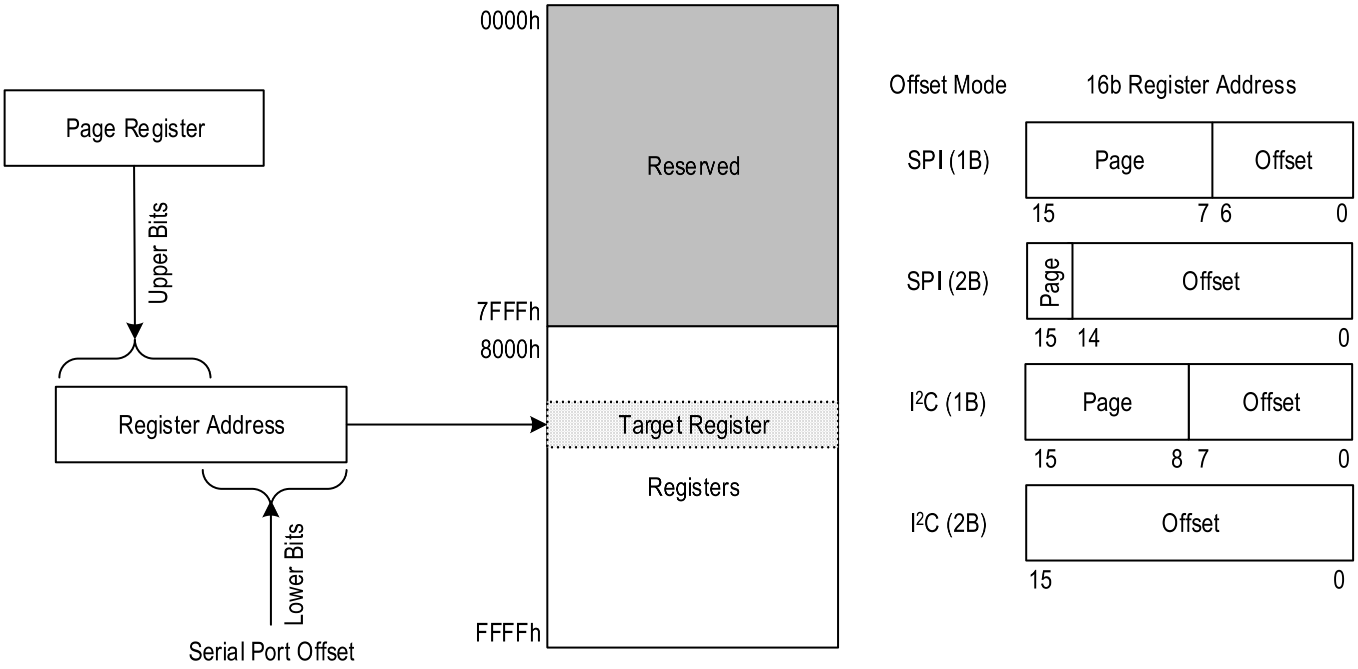
SPI Mode Signal Name	Function	I^{2}C Mode Signal Name	Function	Package Pin Name
SCLK	SPI Clock Input	SCLK	I^{2}C Clock Input	SCLK_AUX
CS	SPI Chip Select (active low)	A0	I^{2}C Slave Address Bit 0	CS_A0_AUX
SDI	SPI Data Input (unused in 3-wire mode)	A1	I^{2}C Slave Address Bit 1	SDI_A1_AUX
SDIO	SPI Data Out (4-wire mode) SPI Data In/Out (3-wire mode)	SDA	I^{2}C Data In/Out	SDIO_AUX

Addressing Registers within the 8A34043

The address space that is externally accessible within the 8A34043 is 64KB in size, and thus, needs 16 bits of address offset information to be provided during slave serial port accesses. Of that 64KB, only the upper 32KB contains user accessible registers.

The user may choose to operate the serial port providing the full offset address within each burst, or to operate in a paged mode where part of the address offset is provided in each transaction and another part comes from an internal page register in each serial port. Figure 16 shows how page register and offset bytes from each serial transaction interact to address a register within the 8A34043.

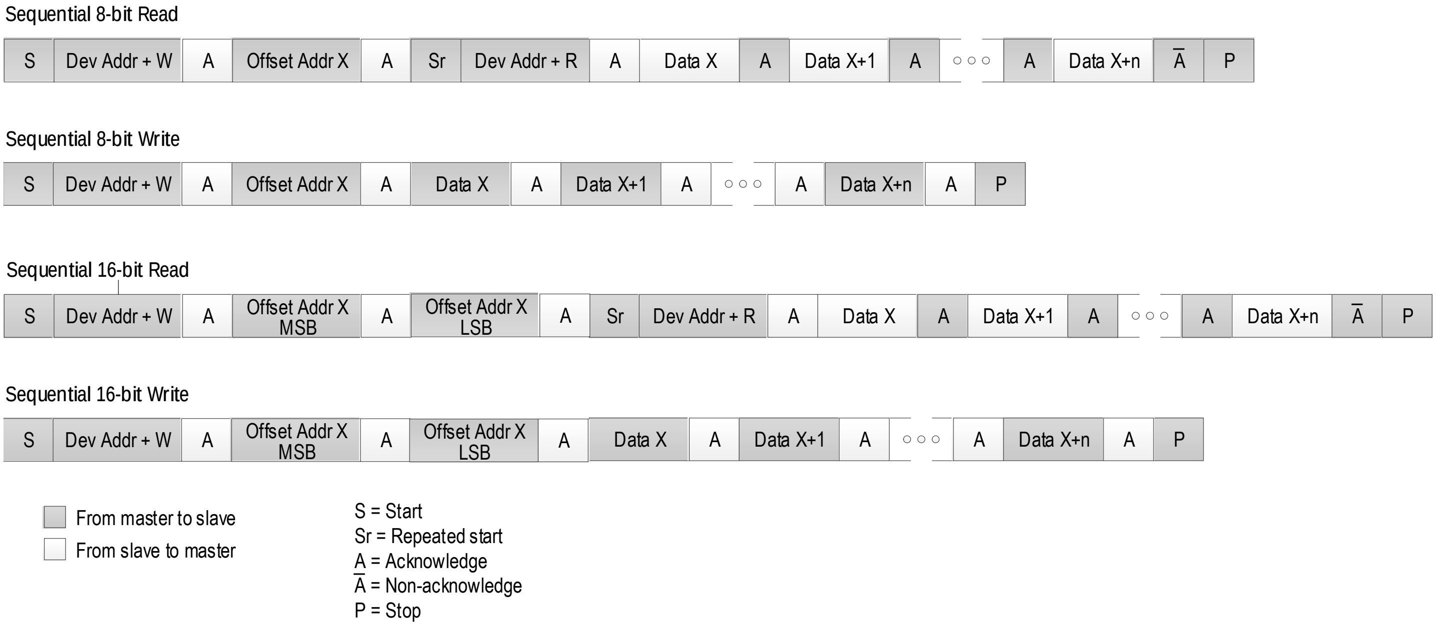
Figure 16. Register Addressing Modes via Serial Port



I^{2}C Slave Operation

The I^{2}C slave protocol of the 8A34043 complies with the I^{2}C specification, version UM10204 Rev.6 – 4 April 2014. Figure 17 shows the sequence of states on the I^{2}C SDA signal for the supported modes of operation.

Figure 17. I^{2}C Slave Sequencing



The Dev Addr shown in the figure represents the base address of the 8A34043. This 7-bit value can be set in an internal register that can have a user-defined value loaded at reset from internal OTP memory or an external EEPROM. The default value if those methods are not used is 1011000b. Note that the levels on the A0 and A1 signals can be used to control Bit 0 and Bit 1, respectively, of this address. There is also an option to designate the reset state of a GPIO pin to set the default value of the A2 bit of the I^{2}C slave port base address (for information, see Use of GPIO Pins at Reset). In I^{2}C operation these inputs are expected to remain static. They have different functions when the part is in SPI mode. The resulting base address is the I^{2}C bus address that this device will respond to.

When I^{2}C operation is selected for a slave serial port, the selection of 1-byte (1B) or 2-byte (2B) offset addressing must also be configured. These offsets are used in conjunction with the page register for each serial port to access registers internal to the device. Because the I^{2}C protocol already includes a read/write bit with the Dev Addr, all bits of the 1B or 2B offset field can be used to address internal registers.

- In 1B mode, the lower 8 bits of the register offset address come from the Offset Addr byte and the upper 8 bits come from the page register. The page register can be accessed at any time using an offset byte value of 0xFC. This 4-byte register must be written in a single-burst write transaction.
- In 2B mode, the full 16-bit register address can be obtained from the Offset Addr bytes, so the page register only needs to be set up once after reset via a 4-byte burst access at offset 0xFFFC.

Note: I^{2}C burst mode operation is required to ensure data integrity of multi-byte registers. When accessing a multi-byte register, all data bytes must be written or read in a single I^{2}C burst access. Bursts can be of greater length if desired, but must not extend beyond the end of the register page (Offset Addr 0xFF in 1B mode, no limit in 2B mode). An internal address pointer is incremented automatically as each data byte is written or read.

Figure 18 and Table 21 show the detailed timing on the interface. 100kHz, 400kHz, and 1MHz operation are supported.

I^{2}C 1-byte (1B) Addressing Examples

8A34043 I^{2}C 7-bit I^{2}C address is 0x5B with LSB = R/W

Example write “0x50” to register 0xCBE4:

```
B6* FC 00 CB 10 20      #Set Page Register, *I2C Address is left-shifted one bit.
B6 E4 50                #Write data 5B to CB E4
```

Example read from register 0xC024:

```
B6* FC 00 C0 10 20      #Set Page Register, *I2C Address is left-shifted one bit.
B6 24*                  #Set I2C pointer to 0xC024, *I2C instruction should use “No Stop”
B7 <read back data>     #Send address with Read bit set.
```

I^{2}C 2-byte (2B) Addressing

8A34043 I^{2}C 7-bit I^{2}C address is 0x5B with LSB = R/W

Example write “50” to register 0xCBE4:

```
B6* FF FD 00 10 20      #Set Page Register, *I2C Address is left-shifted one bit.
B6 CB E4 50             #Write data to CB E4
```

Example read from register 0xC024:

```
B6* FF FD 00 10 20      #Set Page Register (*I2C Address is left-shifted one bit.)
B6 C0 24*               #Set I2C pointer to 0xC024, *I2C instruction should use “No Stop”
B7 <read back data>     #Send address with Read bit set.
```

Figure 18. I^{2}C Slave Timing Diagram

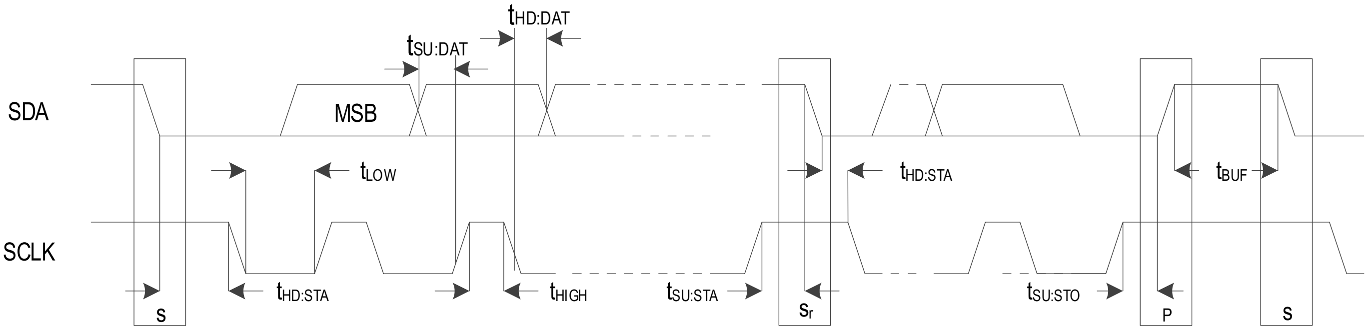


Table 21. I^{2}C Slave Timing

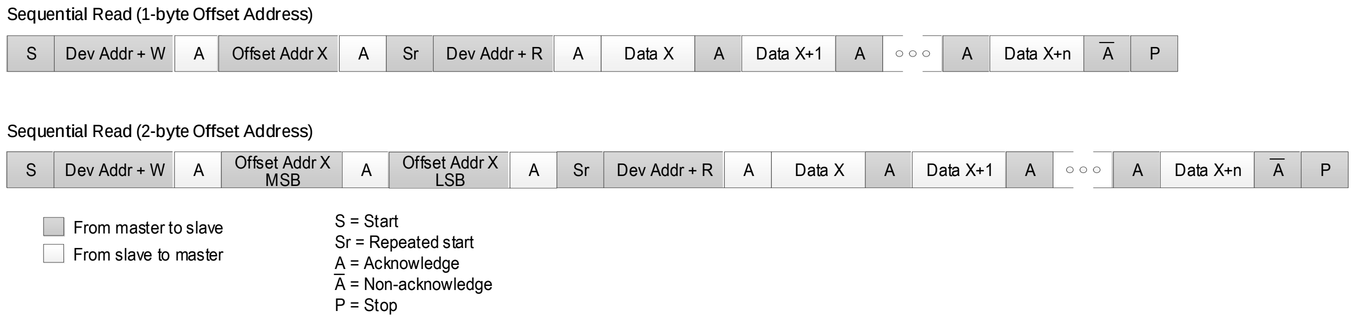
Parameter	Description	Minimum	Typical	Maximum	Units
f_{SCLK}	SCLK Operating Frequency			1	MHz
t_{LOW}	SCLK Pulse Width Low		130		ns
t_{HIGH}	SCLK Pulse Width High		9		ns
$t_{SU:STA}$	Start or Repeat Start Setup Time to SCLK		6		ns
$t_{HD:STA}$	Start or Repeat Start Hold Time from SCLK		18		ns
$t_{SU:DAT}$	Data Setup Time to SCLK rising edge		5		ns
$t_{HD:DAT}$	Data Hold Time from SCLK rising edge		0		ns
$t_{SU:STO}$	Stop Setup Time to SCLK		12		ns
t_{BUF}	Minimum Time from Stop to Next Start		0.5		ns

I^{2}C Master

The 8A34043 can load its register configuration from an external I^{2}C EEPROM during its reset sequence. For information on what accesses occur under what conditions, see Reset Sequence.

As needed during the reset sequence, the 8A34043 will arbitrate for the I^{2}C bus and attempt to access an external I^{2}C EEPROM using the access sequence shown in Figure 19. The I^{2}C master protocol of the 8A34043 complies with the I^{2}C specification, version UM10204 Rev.6 – 4 April 2014. As displayed in the figure, the I^{2}C master port can be configured to support I^{2}C EEPROMs with either 1-byte or 2-byte offset addressing. The I^{2}C master logic will negotiate with any EEPROMs found to use the highest speed of 1MHz, 400kHz, or 100kHz.

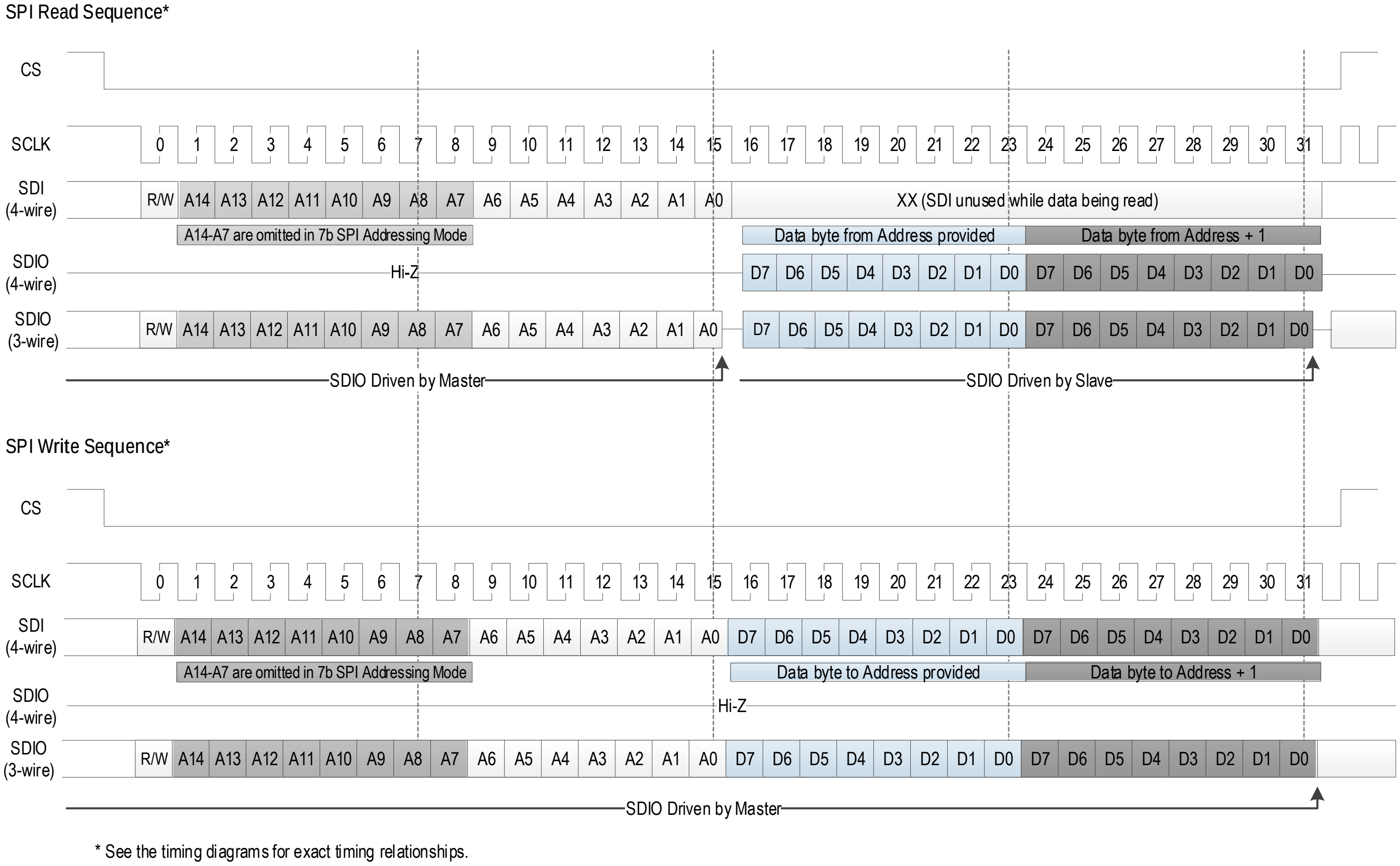
Figure 19. I^{2}C Master Sequencing



SPI Operation

The 8A34043 supports SPI operation as a selectable protocol on the serial port. The port can be configured for either 3-wire or 4-wire operation. In 4-wire mode, there are separate data in (to the 8A34043) and data out signals (SDI and SDIO respectively). In 3-wire mode, the SDIO signal is used as a single, bidirectional data signal. Figure 20 shows the sequencing of address and data on the serial port in both 3-wire and 4-wire SPI mode. 4-wire SPI mode is the default. The R/W bit is high for Read Cycles and low for Write Cycles.

Figure 20. SPI Sequencing



* See the timing diagrams for exact timing relationships.

A serial port can be configured for the following settings. These settings can come from register defaults, or from an internal OTP or external EEPROM configuration loaded at reset:

- 1-byte (1B) or 2-byte (2B) offset addressing (see Figure 16)
  - In 1B operation, the 16-bit register address is formed by using the 7 bits of address supplied in the SPI access and taking the upper 9 bits from the page register. The page register is accessed using an Offset Address of 0x7C with a 4-byte burst access.
  - In 2B operation, the 16-bit register address is formed by using the 15 bits of address supplied in the SPI access and taking the upper 1-bit from the page register. Note that this bit will always be 1 for register accesses, so the page register only needs to be set once in 2B operation. The page register can be accessed using a 3-byte burst access Offset Address of 0x7FFD. It should be accessed in a single burst write transaction to set it.
- Data sampling on falling or rising edge of SCLK
- Output (read) data positioning relative to active SCLK edge
- 4-wire (SCLK, CS, SDIO, SDI) or 3-wire (SCLK, CS, SDIO) operation
- In 3-wire mode, SDIO is a bi-directional data pin.
- Output signal protocol compatibility / drive strength and termination voltage

Note: SPI burst mode operation is required to ensure data integrity of multi-byte registers. When accessing a multi-byte register, all data bytes must be written or read in a single SPI burst access. Bursts can be of greater length if desired, but must not extend beyond the end of the register page. An internal address pointer is incremented automatically as each data byte is written or read.

SPI 1-byte (1B) Addressing Example

Example write to “50” to register 0xCBE4

```
7C 80 CB 10 20          #Set Page register
64* 50                  #*MSB is 0 for write transactions
```

Example read from 0xC024:

```
7C 00 C0 10 20          #Set Page register
A4* 00                  #*MSB is set, so this is a read command
```

SPI 2-byte (2B) Addressing Example

Example write to “50” to register 0xCBE4

```
7F FD 80 10 20          #Set Page register
4B E4* 50               #*MSB is 0 for write transactions
```

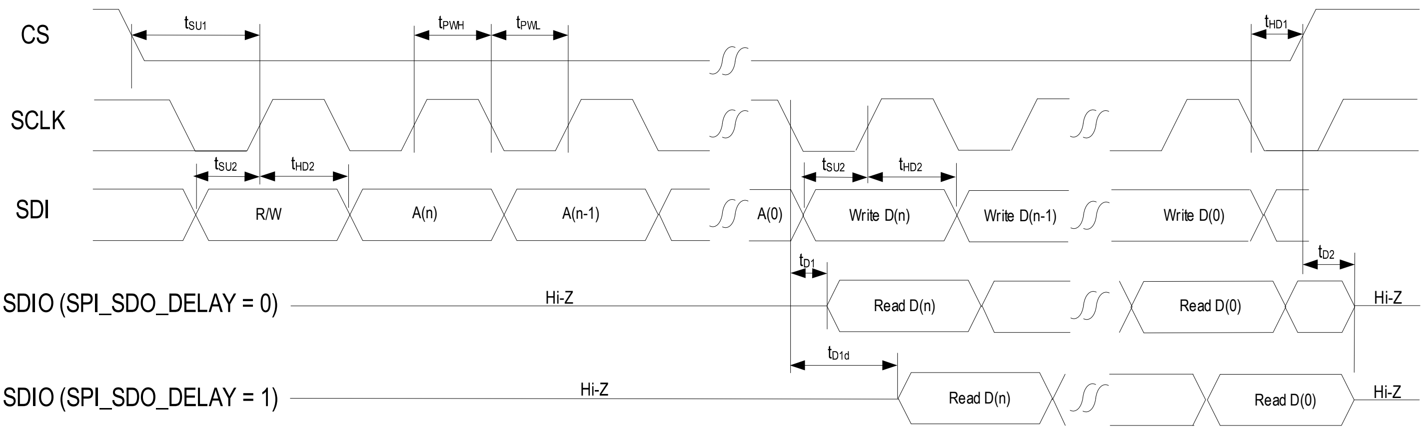
Example read from 0xC024:

```
7F FD 80 10 20          #Set Page register
C0* 24 00               #*MSB is set, so this is a read command
```

SPI timing is shown in Figure 21 and Table 22.

Figure 21. SPI Timing Diagram

SPI_CLOCK_SELECTION = 0



SPI_CLOCK_SELECTION = 1

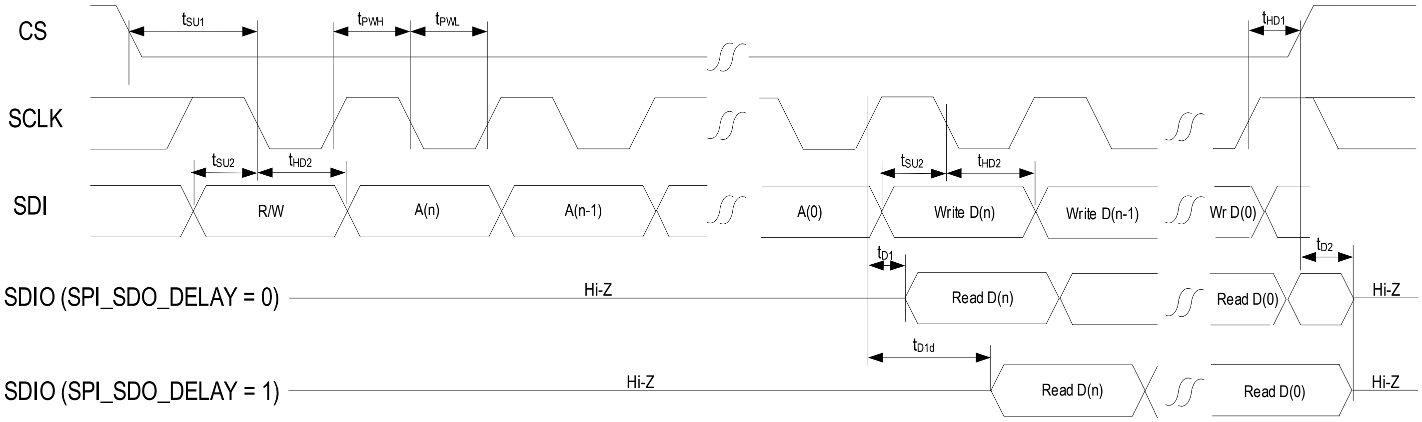


Table 22. SPI Timing

Parameter	Description		Minimum	Typical	Maximum	Units
f_{MAX}	Maximum operating frequency for serial port				50	MHz
t_{PWH}	SCLK Pulse Width High			5		ns
t_{PWL}	SCLK Pulse Width Low			6		ns
t_{SU1}	CS Setup Time to SCLK rising or falling edge			3		ns
t_{HD1}	CS Hold Time from SCLK rising or falling edge			1		ns
t_{SU2}	SDIO Setup Time to SCLK rising or falling edge			4		ns
t_{HD2}	SDIO Hold Time from SCLK rising or falling edge			1		ns
t_{D1}[a]	Read Data Valid Time from SCLK rising or falling edge with no data delay added	V_{CCCS} = 3.3V		6		ns
		V_{CCCS} = 2.5V		6		ns
		V_{CCCS} = 1.8V		6		ns

Table 22. SPI Timing (Cont.)

Parameter	Description		Minimum	Typical	Maximum	Units
t_{D1d}[a]	Read Data Valid Time from SCLK rising or falling edge including half period of SCLK delay added to data timing[b]	V_{CCCS} = 3.3V		6 + half SCLK period		ns
		V_{CCCS} = 2.5V		6 + half SCLK period		ns
		V_{CCCS} = 1.8V		6 + half SCLK period		ns
t_{D2}	SDIO Read Data Hi-Z Time from CS High[c]			10		ns

[a] Measurement performed approximately 1cm away from device pad. Observing at a greater distance on a heavily loaded trace may show slower edge rates and longer delays. This is highly dependent on PCB loading.

[b] Adding the extra half period of delay is a register programming option to emulate read data being clocked out on the opposite edge of the SCLK to the write data.

[c] This is the time until the 8A34043 releases the signal. Rise time to any specific voltage is dependent on pull-up resistor strength and PCB trace loading.

JTAG Interface

The 8A34043 provides a JTAG interface that can be used in non-operational situations with the device when nTEST control pin is held low. The JTAG interface is compliant with IEEE-1149.1 (2001) and supports the IDCODE, BYPASS, EXTEST, SAMPLE, PRELOAD, HIGHZ, and CLAMP instructions.

For information on the value the IDCODE instruction will return for the 8A34043, see the “Product Identification” table located at the end of this document.

JTAG port signals share five pins with GPIO functions as outlined in Table 23. Assertion of the nTEST input (active low) will place those pins in JTAG mode and the device in non-operational mode. The nMR signal should be asserted when nTEST is negated to ensure the device resumes operational mode in a clean state.

Table 23. JTAG Signal Mapping

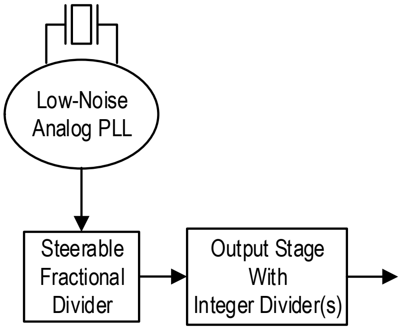
Function with nTEST Active (Low)	Function when nTEST Inactive (High)
TCK	GPIO[0]
TMS	GPIO[1]
TDI	GPIO[2]
TDO	GPIO[3]
TRSTn	GPIO[4]

Basic Operating Modes (Synthesizer / Clock Generator / Jitter Attenuator)

Free-Running Synthesizer Operation

Any DPLL channel can be used in a free-running synthesizer configuration independently of any of the other channels in the part. When configured as a free-running synthesizer, the blocks shown in Figure 22 are used. An external crystal is used as a reference by the System Analog PLL (APLL) which generates a high-frequency, low phase-noise signal. For information on APLL configuration, see System Analog PLL (APLL).

Figure 22. Free-Running Synthesizer Operation

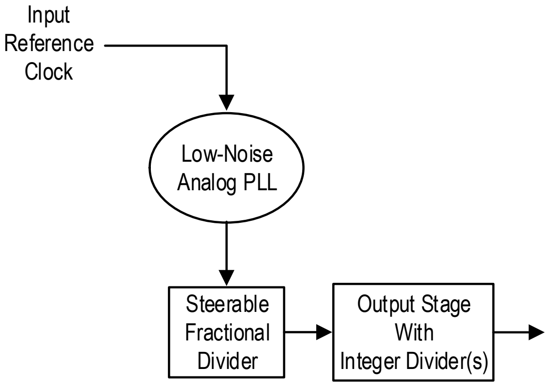


The high-frequency output signal from the APLL is divided-down by the Fractional Divider block to a frequency from 500MHz to 1GHz (for information, see System Analog PLL (APLL)). The output frequency is unrelated to the APLL frequency since fractional division is used. Note that in synthesizer mode, the Fractional Divider block is not steerable, so it is just performing the divide function. That signal is in turn fed to the output stage, where it is further divided by the integer divider(s) and provided to the output in the selected output format. For more information, see FOD Multiplexing and Output Stages.

Clock Generator Operation

Any DPLL channel can be used in a clock generator configuration. When configured as a clock generator as shown in Figure 23, the external crystal input (OSCI) is over-driven (for more information, see Overdriving the XTAL Interface) by an external clock signal which is used as a reference by the System Analog PLL (APLL). The APLL generates a high-frequency, low phase-noise signal from this reference. Note that because the APLL is shared by all channels, this mode is not truly independent for all channels. Each channel can generate unrelated output frequencies via the Fractional Divider. Otherwise, this mode of operation functions the same as the free-running synthesizer operation in the previous section.

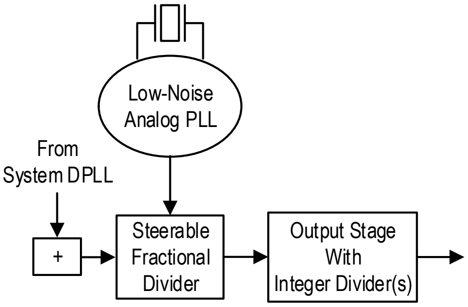
Figure 23. Clock Generator Operation



Synthesizer Disciplined with Oscillator Operation

If an external oscillator, such as an XO, TCXO or OCXO is used, any channel may have its output frequency disciplined by the oscillator for stability and/or close-in phase noise improvement reasons. When configured as shown in Figure 24, the Fractional Divider is behaving as indicated in the description, but in this case the System Digital PLL (SDPLL) is locked to the oscillator and providing a steering signal to the Fractional Divider. Note that the oscillator may be connected to the dedicated oscillator input pin (XO_DPLL) or to any of the input reference clocks (CLKx / nCLKx). Please refer to the Digital Phase Locked Loop (DPLL) section for details.

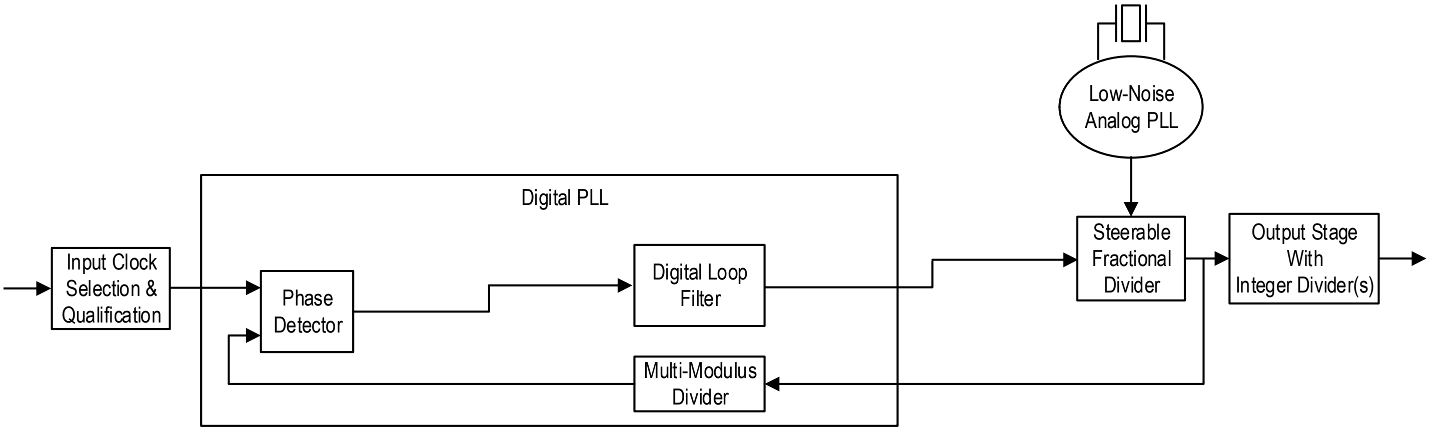
Figure 24. Synthesizer Disciplined with Oscillator Operation



Jitter Attenuator Operation

Any DPLL channel can be operated as a Jitter Attenuator independently from any other channel as shown in Figure 25.

Figure 25. Jitter Attenuator Operation



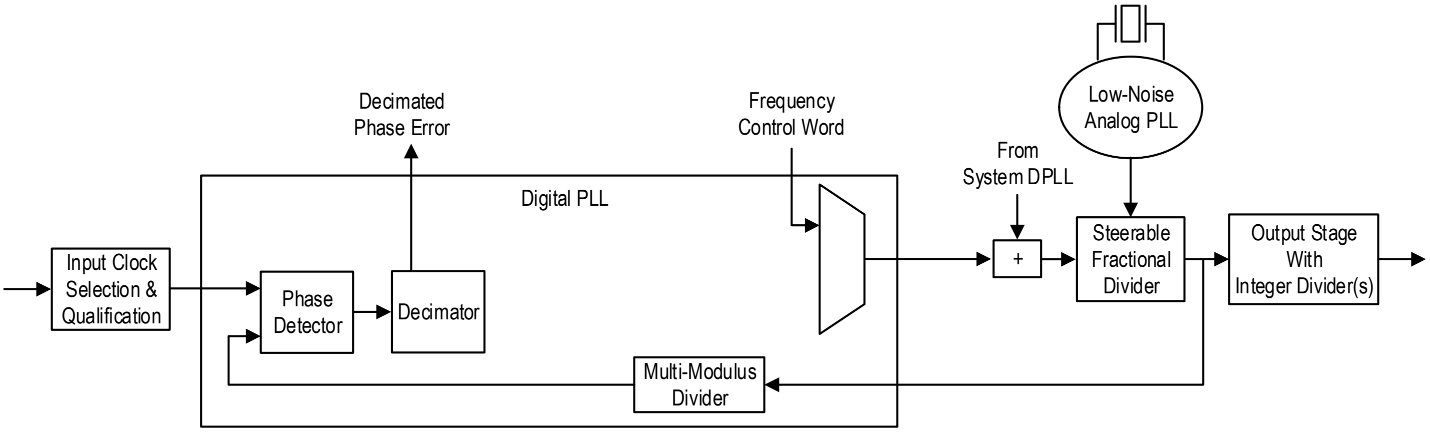
The high-frequency output signal from the APLL is divided-down by the FOD block to a frequency from 500MHz to 1GHz. The output frequency is unrelated to the APLL frequency since fractional division is used (for information, see System Analog PLL (APLL)). That signal is in turn fed to the output stage, where it is further divided by the integer divider(s) and provided to the output in the selected output format. For more information, see FOD Multiplexing and Output Stages.

The DPLL is locked to the input clock, and therefore there is a digital control signal from the Digital PLL (DPLL) block being used to steer the FOD. This signal will adjust the frequency of the FOD to track the input reference signal the DPLL is locked to. So the steerable FOD is acting as a Digitally Controlled Oscillator (DCO) in this mode. The DPLL logic supports several options on how the phase of the output reacts to changes in which input reference is selected, as well as supporting holdover operation if all relevant inputs are lost. For information on how the input reference clock is selected, see DPLL Input Clock Qualification and Selection; for information on DPLL options and operation, see Digital Phase Locked Loop (DPLL).

Jitter Attenuator Operation with External Digital Loop Filter

For some applications, it may be preferable to use an external digital loop filter implemented in software to control a DPLL channel. This function is supported as shown in Figure 26.

Figure 26. Jitter Attenuator Operation with External Digital Loop Filter



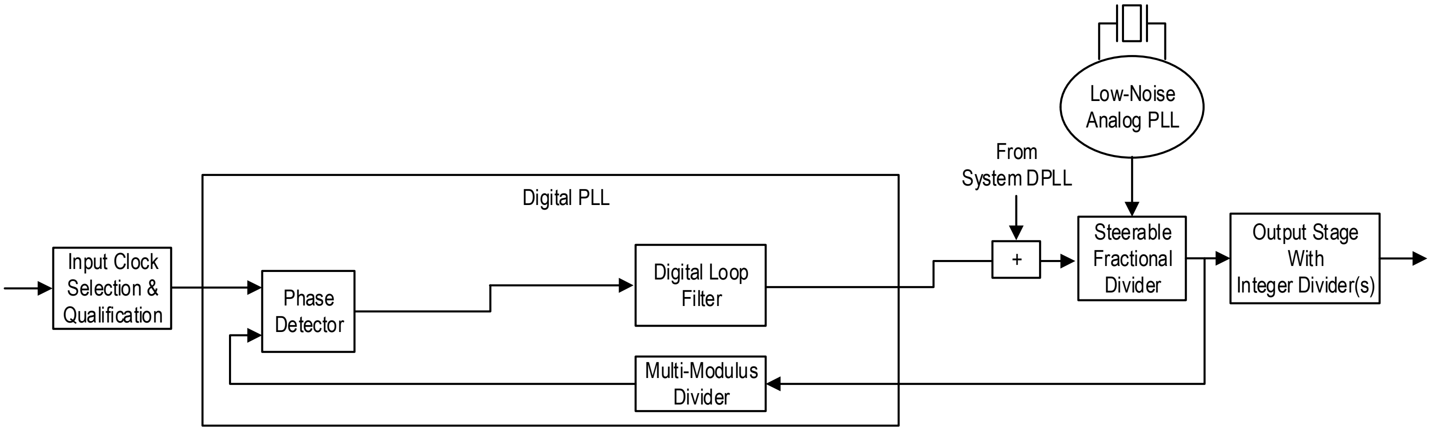
In this case, the phase error measured by the DPLL's phase detector is digitized and decimated to a user selected update rate and provided via registers for use by an external digital filter (for information, see Digital Phase Locked Loop (DPLL)). That data is read from the 8A34043 and provided to the digital filter algorithm. That algorithm then generates a Frequency Control Word (FCW) and writes that back into 8A34043's registers. The FCW will provide direct control of the steerable FOD.

Handling of input reference switchover and holdover operation is under control of the external filter algorithm in this case. Necessary control and status signals to handle these cases in external logic can be provided by proper configuration of the GPIO pins, as described in the General Purpose Input/Outputs (GPIOs).

Jitter Attenuator Disciplined with Oscillator Operation

Similarly to the Synthesizer mode being disciplined by an external oscillator, a jitter attenuator may also be similarly disciplined as shown in Figure 27. This provides stability for the DPLL channel when in holdover. Also, when the jitter attenuator is locked, the oscillator may be used to enhance close-in phase noise performance.

Figure 27. Jitter Attenuator Disciplined with Oscillator Operation



Digitally-Controlled Oscillator Operation via External Control

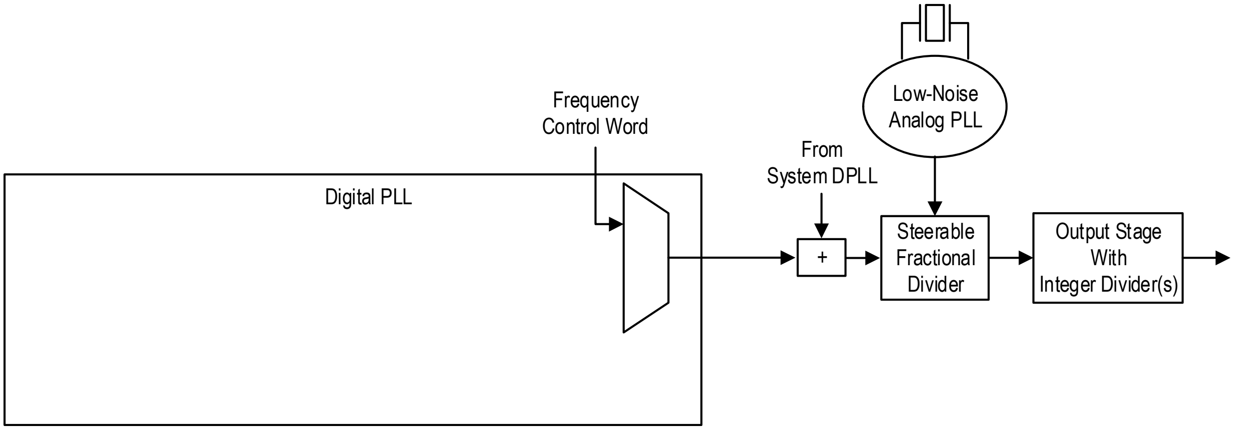
Any DPLL channel can be operated as an externally-controlled DCO independently from any other channel. There are several different control methods that can be used depending on the application needs. Each is described individually in the following sub-sections. Phase and/or frequency updates will be calculated using external methods and written into the 8A34043 over the serial port.

Write-Frequency Mode

For a DPLL channel in this mode a Frequency Control Word (FCW) is used to adjust the frequency output of the DCO (by steering the FOD) and the phase detector and loop filter are essentially bypassed. All the filtering is done by an external device and the frequency offset written into the Write Frequency Configuration register is passed on directly to the output clocks, as displayed in Figure 28. When applied, the FCW will not cause any missing pulses or glitches in the output clock, although a large frequency jump may cause issues with devices receiving this clock. The output will remain at this frequency until a new FCW is written.

If supported by the device, Combo Mode can be used to add additional offsets to the write frequency offset.

Figure 28. External DCO Control via Frequency Control Word



The FCW is a 42-bit 2's-complement value. The FCW has a granularity of 1.11×10^{-10}ppm and a full range of +244.20ppm to -244.08ppm of the nominal DCO frequency. A positive value will increase the output frequency and a negative one will decrease the output frequency. The formula for calculation of the FCW from the fractional frequency offset (FFO) is:

$$\mathrm{FCW} = \left(1 - \frac{1}{\left(1 + \frac{\mathrm{FFO}}{10^6}\right)}\right) \times 2^{53}$$

Where,
FFO = Fractional Frequency Offset, in ppm
FCW = Frequency Control Word (Positive or Negative Integer)

The value resulting from the above calculation must be converted to a 42-bit 2's complement value and then sign-extended to 48 bits to be written into the register.

Write frequency mode can be used to make phase changes on the output. For fine resolution, phase changes are done by controlling the DCO's frequency. Coarse phase adjustments should be done by snap-alignment method by using the Phase Offset registers (for information, see Output Coarse Phase Adjustment). Using the Phase Offset registers is referred to as the snap-alignment method since the output will snap directly to that new phase rather than moving smoothly to it over time. The snap-alignment method provides fast coarse phase alignments, and therefore, it should be used to bring the phase close to the desired value and then use the DCO in write frequency mode to fine tune it. Since write frequency mode is changing the frequency, the phase will move smoothly over time without any jumps.

Increment / Decrement Registers and Pins

The DCO frequency update can also be done by applying a preset frequency offset value to be added or to be subtracted from a cumulative FCW value. The cumulative FCW value functions as described in the previous section.

Once the individual frequency offset values are configured for all applicable DCOs, then a single 16-bit register can be written over the serial port and cause an increment or decrement frequency offset to be applied to one or more DCOs with a single register access. Subsequent accesses to this register can apply additional frequency offsets to any or all DCOs.

Alternatively, one or more GPIO pins can be configured to perform the increment or decrement frequency offset function on a specific DCO. For information on how to configure the GPIOs, see General Purpose Input/Outputs (GPIOs).

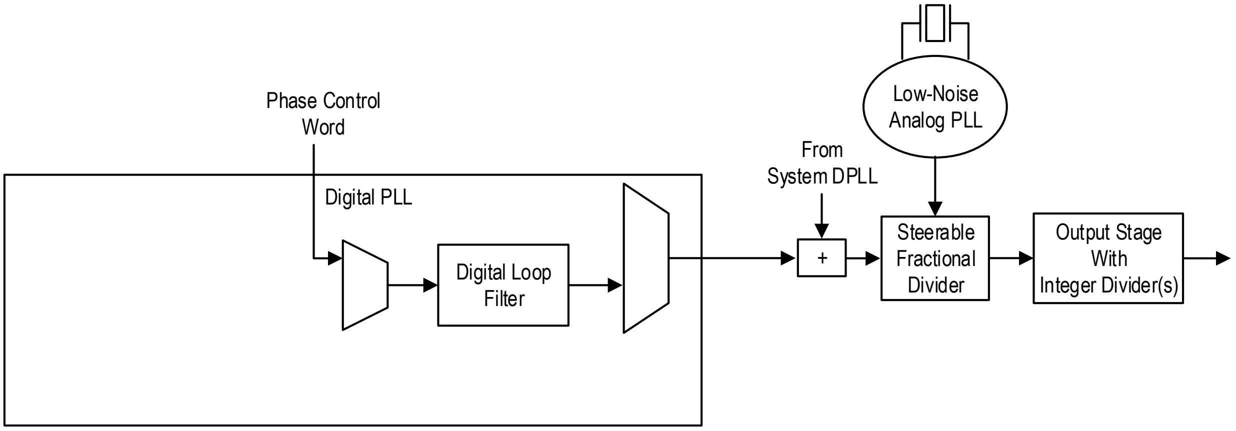
Write-Phase Mode

In this mode of operation for a DPLL channel, the Phase Control Word (PCW) is written by the external control logic over the serial port to directly control the DCO phase with hardware controlled bandwidth and phase slope limiting (see Figure 29). In this mode, the DPLL loop bandwidth and the phase slope limiting are programmable and will affect the output phase as it is adjusted.

The PCW applied to the Digital Loop Filter is equivalent to applying a phase error measured by the on-chip Phase / Frequency Detector to the Digital Loop Filter when the DPLL is operating in closed loop. The update rate needs to be at least 60 times the loop filter bandwidth. As an example, for 0.1Hz per G.8273.2, the update should be greater than 6Hz; but for 17Hz the update should be greater than 1000Hz.The rate of adjustment of phase on the DCO output is controlled by Digital Loop Filter settings. For information on configuring related DPLL parameters such as loop bandwidth and phase slope limiting, see Digital Phase Locked Loop (DPLL). This method allows for a better control of the output clock since all parameters are controlled in hardware. This change will not cause any missing pulses or glitches in the output clock. Also, because the output frequency is changed only at a rate determined by the loop filter, this should not cause any issues, if properly configured, with devices receiving this clock.

Note that the PCW must be reduced over time or the DPLL will continue to adjust the DCO frequency to remove the “phase error”. This can be adjusted by external software.

Figure 29. External DCO Control via Phase Control Word



To assist in the above, there is an optional timer associated with the PCW. This allows a phase control word to be applied for a limited period of time after which it will be automatically reset to zero or placed into holdover by the 8A34043, and therefore, it will avoid the DCO continuing to apply the phase adjustment indefinitely until it reaches its tuning range limits. The timer value is a 16-bit integer that has a granularity of 1 millisecond and a full range of up to 65.535 seconds.

The PCW is a 32-bit 2’s-complement value. The resolution of the PCW is 50ps and the range is ±107.3741824 ms. Writing a positive value will result in the output frequency getting faster. This will shorten the clock periods, moving the clock edges to the left as seen on an oscilloscope. A negative value will slow the output frequency.

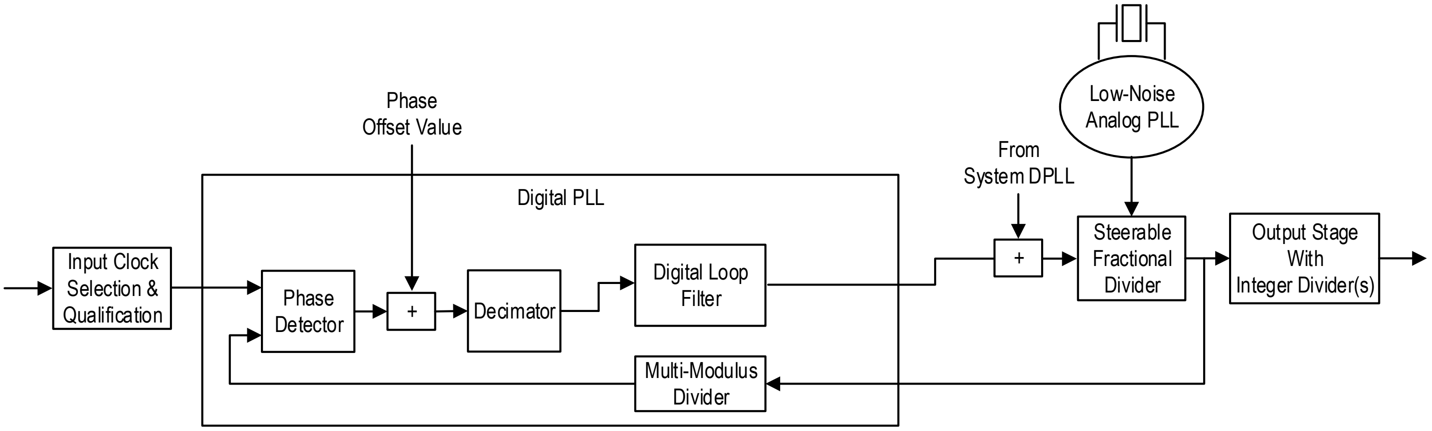
Adjusting Phase while in Closed Loop Operation

There may be usage scenarios that require adding a phase offset from an external software-controlled process to an output clock that is locked to an input clock. That function can also be supported as shown in Figure 30. In this mode, the amount of phase offset needed consists of two components. The first is dependent on which input the DPLL is locked to. So a phase offset register is provided for each input to allow individual offsets to be specified per-input.

The second part of the phase offset configuration is for each DPLL. There is a register for each DPLL that allows for another offset value to be specified that is independent of which input is active. The actual Phase Offset Value applied will be calculated by the 8A34043 using the per-input phase offset value for the currently active input summed with the phase offset value for the DPLL channel. During input reference switching, this value will be automatically recalculated at any switchover and applied as shown. Note that if an input is used on multiple DPLL channels, it may not be possible to maintain unique values per-input-per-DPLL. The calculated offset value is then summed with the measured phase error for that channel (phase difference between input reference and feedback value) to drive the DPLL to the desired phase.

The Phase Offset Value applied to the Digital Loop Filter is equivalent to applying a phase error measured by the on-chip Phase / Frequency Detector to the Digital Loop Filter when the DPLL is operating in closed loop.

Figure 30. Phase Control in Closed Loop Operation

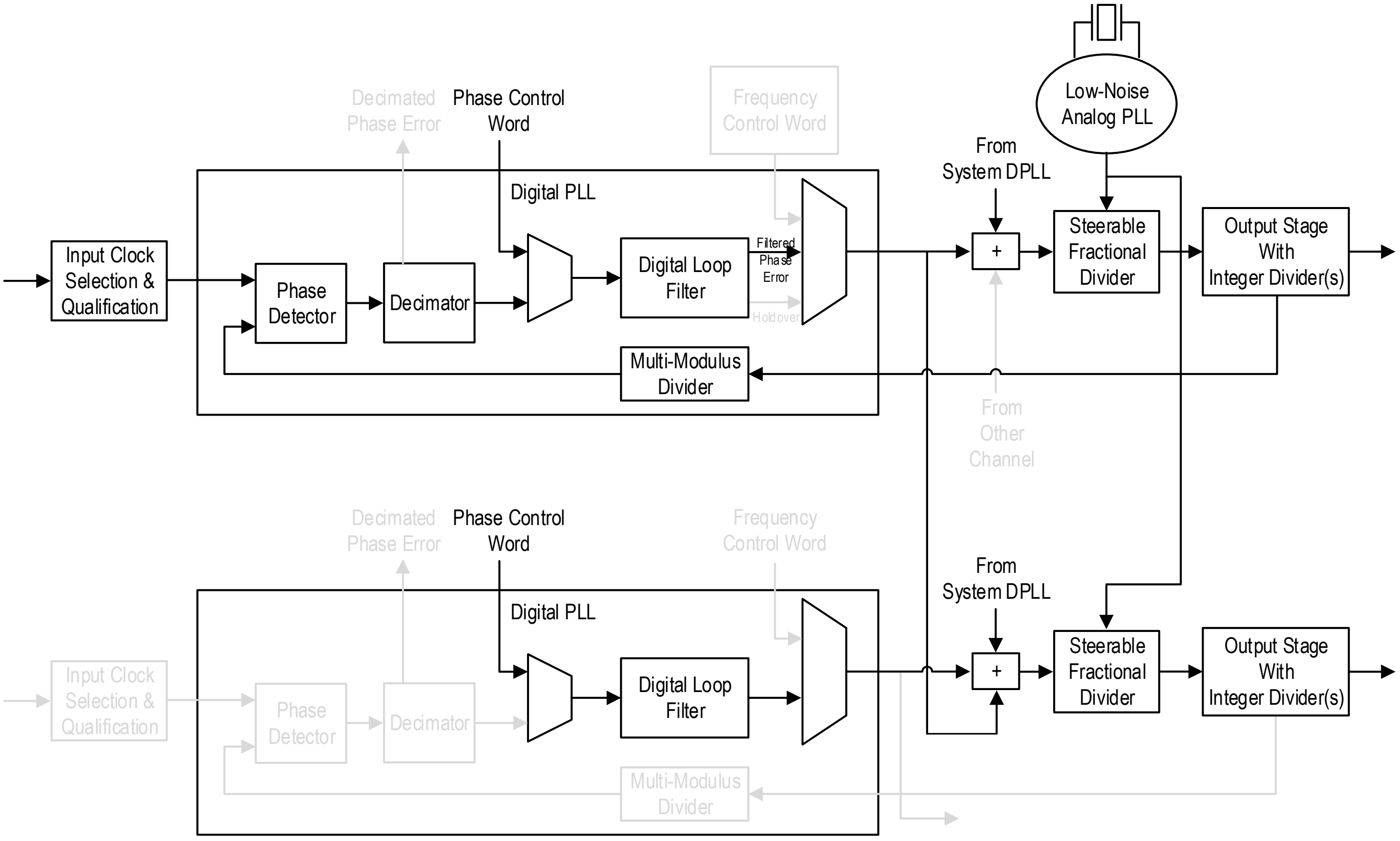


Combo Mode

The combo mode is shown in Figure 31. In this mode, up to three channels are used, one of which is usually a DPLL channel. Each (receiving) DPLL channel can source up to two other DPLLs including the System DPLL. In this mode, one DPLL is locked to an input reference clock, such as a Synchronous Ethernet clock, and can generate output clocks of different frequencies that track the Synchronous Ethernet input reference clock. The second channel is used as a DCO and it will be controlled externally, as an example by an IEEE 1588 clock recovery servo algorithm running in an external processor, or just track the first channel directly. This will not cause any missing pulses or glitches in the output clocks from either channel since all frequency changes are limited by at least one loop filter.

The physical layer clock and its output clock will act as the local oscillator for the DCO, and therefore the DCO can rely on a very stable clock. This is done all inside the device, no need to route the clocks externally. It is also important to be able to control phase transients in the SyncE clock. This can be done by either using an internal filter that will filter the SyncE transients, or by suppressing the SyncE based on SSM clock quality level.

Figure 31. Combo Mode



In this example, the IEEE 1588 timestamps are used to calculate the phase offset between the IEEE 1588 master's 1PPS pulse and the IEEE 1588 slave's 1PPS pulse and then align the two pulses by moving the slave's 1PPS pulse in phase. The slave must be able to move the 1PPS pulse by ±0.5s, and the 8A34043 provides this capability.

AC and DC Specifications

Abbreviations Used in this Section

Many signals will be concatenated in the specification tables that follow. Table 24 shows a list of abbreviations used and will be referred to in footnotes for the various other tables.

Table 24. Abbreviated Signal Names and the Detailed Signal Names Referenced by Them

Abbreviation	Signals Referenced by this Abbreviation
V_{DD_CLKx}	V_{DD_CLK}
Input CLK	CLK[1:0], nCLK[1:0]
Output Q	Q[11:8], nQ[11:8]
Status Outputs	GPIO[9,8,5:0], SDIO_AUX, SDA_M, SCL_M
GPIO	GPIO[9,8,5:0]
V_{DDx}	$V_{DDA\_PDCP\_XTAL}$, V_{DD_CLK}, V_{DDA_FB}, V_{DDA_BG}, V_{DDA_LC}, V_{DD_DIG}, V_{DD_GPIO}, $V_{DD\_DCO\_Q8}$, $V_{DD\_DCO\_Q9}$, $V_{DD\_DCO\_Q11}$ $V_{DD\_DCO\_Q11}$, V_{DDO_Q8}, V_{DDO_Q9}, V_{DDO_Q10}, V_{DDO_Q11}
V_{DDO_Qx}	V_{DDO_Q8}, V_{DDO_Q9}, V_{DDO_Q10}, V_{DDO_Q11}
$V_{DD\_DCO\_Qx}$	$V_{DD\_DCO\_Q8}$, $V_{DD\_DCO\_Q9}$, $V_{DD\_DCO\_Q11}$ $V_{DD\_DCO\_Q11}$

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8A34043 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 25. Absolute Maximum Ratings

Symbol	Parameter	Test Condition	Minimum	Maximum	Units
V_{DDx}[a]	Any voltage supply		-0.5	3.63	V
V_{IN}	Voltage on any input	OSCI[b], OSCO, FILTER, C_{REG_XTAL}	0	2.75	V
		All other inputs	-0.5	3.63	V
I_{IN}	Differential Input Current	Input CLK[a]		±50	mA
I_O	Output Current - Continuous	Output Q[a]		30	mA
		Status Outputs[a]		25	mA
	Output Current - Surge	Output Q		60	mA
		Status Outputs		50	mA
T_{JMAX}	Maximum Junction Temperature			150	°C
T_S	Storage temperature		-65	150	°C
-	ESD - Human Body Model			2000	V
-	ESD - Charged Device Model			1500	V

[a] For information on the signals referenced by this abbreviation, see Table 24.

[b] This limit only applies to the OSCI input when being over-driven by an external signal. No limit is implied when this is connected directly to a crystal.

Recommended Operating Conditions

Table 26. Recommended Operating Conditions[a][b]

Symbol	Parameter	Minimum	Typical	Maximum	Units
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C

[a] It is the user’s responsibility to ensure that device junction temperature remains below the maximum allowed.

[b] All conditions in this table must be met to guarantee device functionality.

Supply Voltage Characteristics

Table 27. Power Supply DC Characteristics[a][b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD_CLK}	Supply Voltage for Input Clock Buffers and Dividers		1.71	[c]	3.465	V
I_{DD_CLKx}[d]	Supply Current for V_{DD_CLKx}	$V_{DD\_CLKx} = 3.465V$, PMOS mode		3	4	mA
		$V_{DD\_CLKx} = 3.465V$, NMOS mode		6	7	
		$V_{DD\_CLKx} = 3.465V$, CMOS mode		1.5	4	
		$V_{DD\_CLKx} = 2.625V$, PMOS mode		2.6	3	
		$V_{DD\_CLKx} = 2.625V$, NMOS mode		6	7	
		$V_{DD\_CLKx} = 2.625V$, CMOS mode		1	2	
		$V_{DD\_CLKx} = 1.89V$, PMOS mode		2.5	3	
		$V_{DD\_CLKx} = 1.89V$, NMOS mode		5	7	
		$V_{DD\_CLKx} = 1.89V$, CMOS mode		1	2	
$V_{DDA\_PDCP\_XTAL}$	Analog Supply Voltage for oscillator and for SysAPLL Phase Detector and Charge Pump		2.375	[e]	3.465	V
$I_{DDA\_PDCP\_XTAL}$	Supply Current for $V_{DDA\_PDCP\_XTAL}$	$V_{DDA\_PDCP\_XTAL} = 3.3V$		48	55	mA
		$V_{DDA\_PDCP\_XTAL} = 2.5V$		33	40	mA
V_{DDA_FB}	Analog Supply Voltage for SysAPLL Feedback Divider		1.71	1.8	1.89	V
I_{DDA_FB}	Supply Current for V_{DDA_FB}	$V_{DDA\_FB} = 1.89V$		22	37	mA
V_{DDA_BG}	Analog Supply Voltage for SysAPLL Bandgap reference		2.375	[e]	3.465	V
I_{DDA_BG}	Supply Current for V_{DDA_BG}	$V_{DDA\_BG} = 3.465V$		19	26	mA
		$V_{DDA\_BG} = 2.625V$		16	22	mA
V_{DDA_LC}	Analog Supply Voltage for SysAPLL LC Resonator		2.375	[e]	3.465	V
I_{DDA_LC}	Supply Current for V_{DDA_LC}	$V_{DDA\_LC} = 3.465V$		97	121	mA
		$V_{DDA\_LC} = 2.625V$		65	71	mA
V_{DD_GPIO}	Supply Voltage for GPIO and other status / control pins		1.425	[f]	3.465	V

Table 27. Power Supply DC Characteristics[a][b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{DD_GPIO}	Supply Current for V_{DD_GPIO}	V_{DD_GPIO} = 3.465V		9	15	mA
		V_{DD_GPIO} = 2.625V		7	12	mA
		V_{DD_GPIO} = 1.89V		4	9	mA
		V_{DD_GPIO} = 1.575V		1	6	mA
V_{DD_DIG}	Digital Supply Voltage		1.14	[g]	1.89	V
I_{DD_DIG}	Supply Current for V_{DD_DIG}	V_{DD_DIG} = 1.89V		190	380	mA
		V_{DD_DIG} = 1.26V		180	295	mA
$V_{DD\_DCO\_Q8}$	Supply Voltage for: ▪ FOD_4 ▪ FOD_4 control logic ▪ FOD_5 control logic		1.71	1.8	1.89	V
$I_{DD\_DCO\_Q8}$	Supply Current for $V_{DD\_DCO\_Q8}$[h]	$V_{DD\_DCO\_Q8}$ = 1.89V Base current (FODs Off) $I_{DD(BASE)}$		21	39	mA
		Adder for FOD at 500MHz $I_{DD(DCOPERFOD)}$		30		mA
		Adder for each FOD control (if enabled) at 500MHz $I_{DD(CTLPERFOD)}$		10		mA
		Adder per 1MHz over 500MHz on FOD $I_{DD(DCOPERMHZ)}$		0.012		mA/MHz
		Adder per 1MHz over 500MHz on FOD control that is enabled $I_{DD(CTLPERMHZ)}$		0.018		mA/MHz
$V_{DD\_DCO\_Q9}$	Supply Voltage for FOD_5		1.71	1.8	1.89	V
$I_{DD\_DCO\_Q9}$	Supply Current for $V_{DD\_DCO\_Q9}$[i]	$V_{DD\_DCO\_Q9}$ = 1.89V Base current (FODs Off) $I_{DD(BASE)}$		12	22	mA
		Adder for FOD at 500MHz $I_{DD(DCOPERFOD)}$		30		mA
		Adder per 1MHz over 500MHz on FOD $I_{DD(DCOPERMHZ)}$		0.012		mA/MHz
$V_{DD\_DCO\_Q10}$	Supply Voltage for FOD_6		1.71	1.8	1.89	V

Table 27. Power Supply DC Characteristics[a][b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{DD\_DCO\_Q10}$	Supply Current for $V_{DD\_DCO\_Q10}$[j]	$V_{DD\_DCO\_Q10}$ = 1.89V Base current (FODs Off) $I_{DD(BASE)}$		12	22	mA
		Adder for FOD at 500MHz $I_{DD(DCOPERFOD)}$		30		mA
		Adder per 1MHz over 500MHz on FOD $I_{DD(DCOPERMHZ)}$		0.012		mA/MHz
$V_{DD\_DCO\_Q11}$	Supply Voltage for: ▪ FOD_6 control logic ▪ FOD_7 ▪ FOD_7 control logic		1.71	1.8	1.89	V
$I_{DD\_DCO\_Q11}$	Supply Current for $V_{DD\_DCO\_Q11}$[k]	$V_{DD\_DCO\_Q11}$ = 1.89V Base current (FODs Off) $I_{DD(BASE)}$		44	66	mA
		Adder for FOD at 500MHz $I_{DD(DCOPERFOD)}$		30		mA
		Adder for each FOD control (if enabled) at 500MHz $I_{DD(CTLPERFOD)}$		10		mA
		Adder per 1MHz over 500MHz on FOD $I_{DD(DCOPERMHZ)}$		0.012		mA/MHz
		Adder per 1MHz over 500MHz on FOD control that is enabled $I_{DD(CTLPERMHZ)}$		0.012		mA/MHz
V_{DDO_Qx}[l]	Output Clock Q Supply Voltage[m]		1.14		3.465	V

[a] V_{SS} = 0V, T_A = -40°C to 85°C

[b] Current consumption figures represent a worst-case consumption with all functions associated with the particular voltage supply being all enabled and running at full capacity. This information is provided to allow for design of appropriate power supply circuits that will support all possible register-based configurations for the device. Please refer to the section Power Consumption to determine actual consumption for the exact configuration of the device.

[c] Supports 1.8V±5%, 2.5V±5% or 3.3V±5% operation, not a continuous range.

[d] I_{DD_CLKx} denotes the current consumed by the appropriate V_{DD_CLKx} supply voltage

[e] Supports 2.5V±5% or 3.3V±5% operation, not a continuous range.

[f] Supports 1.5V, 1.8V, 2.5v or 3.3V operation.

[g] Supports 1.2V±5% or 1.8V±5% operation, not a continuous range.

[h] The $I_{DD\_DCO\_Q8}$ current consumed is highly dependent on the frequency it is running at. So a calculation needs to be performed as shown below. First the current being consumed by FOD_4 is calculated, $I_{DD(DCOPERFOD)}$ is added for FOD_4 if enabled where f_{FOD} is the frequency the FOD is operating at in MHz. Then add the control logic current for whichever of FOD_4 and/or FOD_5 are operating and their respective operating frequencies. Note that only the base current is needed if both FODs are disabled.

$$I_{DD(DCOQ8)} = I_{DD(BASE)} + I_{DD(DCOPERFOD)} + (f_{FOD} - 500) \times I_{DD(DCOPERMHZ)} +$$

$$NumCTRL \times I_{DD(CTLPERFOD)} + \sum_{operatingCTRL} (f_{FOD} - 500) \times I_{DD(CTLPERMHZ)}$$

[i] The $I_{DD\_DCO\_Q9}$ current consumed is highly dependent on the frequency it is running at. So a calculation needs to be performed as shown below. First the current being consumed by FOD_5 is calculated, $I_{DD(DCOPERFOD)}$ is added if FOD_5 is enabled and where f_{FOD} is the frequency the FOD is operating at in MHz. Note that only the base current is needed if the FOD is disabled.

$$I_{DD(DCOQ9)} = I_{DD(BASE)} + I_{DD(DCOPERFOD)} + (f_{FOD} - 500) \times I_{DD(DCOPERMHZ)}$$

[j] The $I_{DD\_DCO\_Q10}$ current consumed is highly dependent on the frequency it is running at. So a calculation needs to be performed as shown below. First the current being consumed by FOD_6 is calculated, $I_{DD(DCOPERFOD)}$ is added if FOD_6 is enabled and where f_{FOD} is the frequency the FOD is operating at in MHz. Note that only the base current is needed if the FOD is disabled.

$$I_{DD(DCOQ10)} = I_{DD(BASE)} + I_{DD(DCOPERFOD)} + (f_{FOD} - 500) \times I_{DD(DCOPERMHZ)}$$

[k] The $I_{DD\_DCO\_Q11}$ current consumed is highly dependent on the frequency it is running at. So a calculation needs to be performed as shown below. First the current being consumed by FOD_2 and FOD_7 is calculated, $I_{DD(DCOPERFOD)}$ is added for each of FOD_2 and/or FOD_7 that are enabled and where f_{FOD} is the frequency the FOD is operating at in MHz. Then add the control logic current for whichever of FOD_2, FOD_6 and/or FOD_7FOD_6 are operating and their respective operating frequencies. Note that only the base current is needed if all FODs are disabled.

$$I_{DD(DCOQ11)} = I_{DD(BASE)} + NumFOD \times I_{DD(DCOPERFOD)} + \sum_{operatingFOD} (f_{FOD} - 500) \times I_{DD(DCOPERMHZ)} +$$

$$NumCTRL \times I_{DD(CTLPERFOD)} + \sum_{operatingCTRL} (f_{FOD} - 500) \times I_{DD(CTLPERMHZ)}$$

[l] Please refer to Table 24 for details on the signals referenced by this abbreviation.

[m] Currents for the outputs are shown in Table 28 or Table 29 as appropriate for the mode the individual output is operating in.

Table 28. Output Supply Current (Output Configured as Differential)[a][b][c]

Symbol	Parameter	Test Condition	SWING[d] = 00		SWING = 01		SWING = 10		SWING = 11		Units
			Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{DDO_Qx}[e]	Qx / nQx Supply Current[f]	V_{DDO_Qx}[g] = 3.465V	15	22	17	24	19	26	20	26	mA
		V_{DDO_Qx} = 2.625V	14	20	16	21	18	22	19	23	mA
		V_{DDO_Qx} = 1.89V	14	19	15	20	16	21	16	21	mA

[a] Output current consumption is not affected by any of the core device power supply voltage levels.

[b] Internal dynamic switching current at maximum f_{OUT} is included.

[c] V_{DDO_Qx} = 3.3V±5% or 2.5V±5% or 1.8V±5%, V_{SS} = 0V, T_A = -40°C to 85°C.

[d] Refers to the output voltage (swing) setting programed into device registers for each output.

[e] I_{DDO_Qx} denotes the current consumed by each V_{DDO_Qx} supply.

[f] Measured with outputs unloaded.

[g] For information on the signals referenced by this abbreviation, see Table 24.

Table 29. Output Supply Current (Output Configured as LVCMOS)[a][b][c]

Symbol	Parameter	Test Condition	TERM[d] = 00		TERM = 01		TERM = 10		TERM = 11		Units
			Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{DDO_Qx}[e]	Qx, nQx Supply Current[f] Qx and nQx Both Enabled	V_{DDO_Qx}[g] = 3.465V	24	32	25	35	25	37	25	39	mA
		V_{DDO_Qx} = 2.625V	18	25	19	27	19	29	20	30	
		V_{DDO_Qx} = 1.89V	12	20	14	21	15	22	15	23	
		V_{DDO_Qx} = 1.575V	9	17	11	18	11	19	12	20	
		V_{DDO_Qx} = 1.26V	6	13	6	13	6	14	6	14	
	Qx, nQx Supply Current[h] Qx enabled and nQx Tri-stated	V_{DDO_Qx} = 3.465V	14	23	14	24	14	25	14	26	mA
		V_{DDO_Qx} = 2.625V	11	19	11	20	11	20	11	21	
		V_{DDO_Qx} = 1.89V	9	16	10	17	10	17	10	18	
		V_{DDO_Qx} = 1.575V	8	15	8	16	9	16	9	16	
		V_{DDO_Qx} = 1.26V	5	12	5	12	5	12	5	12	

[a] Output current consumption is not affected by any of the core device power supply voltage levels.

[b] Internal dynamic switching current at maximum f_{OUT} is included.

[c] V_{SS} = 0V, T_A = -40°C to 85°C

[d] Refers to the LVCMOS output drive strength (termination) setting programed into device registers for each output.

[e] I_{DDO_Qx} denotes the current consumed by each V_{DDO_Qx} supply.

[f] Measured with outputs unloaded.

[g] For information on the signals referenced by this abbreviation, see Table 24.

[h] Measured with outputs unloaded.

DC Electrical Characteristics

Table 30. LVCMOS/LVTTL DC Characteristics[a][b][c][d][e]

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	nMR, nTEST, GPIO[9,8,5:0], SCLK_AUX, SDIO_AUX, SDI_A1_AUX, CS_A0_AUX, SDA_M	V_{DD_GPIO} = 3.3V±5%	2		V_{DD_GPIO} + 0.3	V
			V_{DD_GPIO} = 2.5V±5%	1.7		V_{DD_GPIO} + 0.3	V
			V_{DD_GPIO} = 1.8V±5%	0.65 × V_{DD_GPIO}		V_{DD_GPIO} + 0.3	V
			V_{DD_GPIO} = 1.5V±5%	0.65 × V_{DD_GPIO}		V_{DD_GPIO} + 0.3	V
V_{IH}	Input High Voltage	XO_DPLL	V_{DD_DIG} = 1.8V±5%	1.17		3.465V	V
			V_{DD_DIG} = 1.2V±5%	1.17		3.465V	V
V_{IH}	Input High Voltage	CLK[1:0], nCLK[1:0][e]	V_{DD_CLK} = 3.3V±5%	2		V_{DD_CLK} + 0.3	V
			V_{DD_CLK} = 2.5V±5%	1.7		V_{DD_CLK} + 0.3	V
			V_{DD_CLK} = 1.8V±5%	0.65 × V_{DD_CLK}		V_{DD_CLK} + 0.3	V
V_{IL}	Input Low Voltage	nMR, nTEST, GPIO[9,8,5:0], SCLK_AUX, SDIO_AUX, SDI_A1_AUX, CS_A0_AUX, SDA_M	V_{DD_GPIO} = 3.3V±5%	-0.3		0.8	V
			V_{DD_GPIO} = 2.5V±5%	-0.3		0.7	
			V_{DD_GPIO} = 1.8V±5%	-0.3		0.35 × V_{DD_GPIO}	
			V_{DD_GPIO} = 1.5V±5%	-0.3		0.35 × V_{DD_GPIO}	
V_{IL}	Input Low Voltage	XO_DPLL	V_{DD_DIG} = 1.8V±5%	-0.3		0.35 × V_{DD_DIG}	V
			V_{DD_DIG} = 1.2V±5%	-0.3		0.35 × V_{DD_DIG}	
V_{IL}	Input Low Voltage	CLK[1:0], nCLK[1:0][e]	V_{DD_CLK} = 3.3V±5%	-0.3		0.8	V
			V_{DD_CLK} = 2.5V±5%	-0.3		0.7	
			V_{DD_CLK} = 1.8V±5%	-0.3		0.35 × V_{DD_CLK}	
I_{IH}	Input High Current	nMR, nTEST, GPIO[9,8,5:0], SDA_M, SCLK_AUX, SDIO_AUX, SDI_A1_AUX, CS_A0_AUX	V_{IN} = V_{DD_GPIO} = V_{DD_GPIO} (max)			5	μA
I_{IH}	Input High Current	XO_DPLL	V_{IN} = 3.465V, V_{DD_DIG} = V_{DD_DIG} (max)			150	μA
I_{IH}	Input High Current	CLK[1:0]	V_{IN} = V_{DD_CLK} = V_{DD_CLK} (max)			150	μA
		nCLK[1:0]				5	
I_{IL}	Input Low Current	nMR, nTEST, GPIO[9,8,5:0], SDA_M, SCLK_AUX, SDIO_AUX, SDI_A1_AUX, CS_A0_AUX	V_{IN} = 0V, V_{DD_GPIO} = V_{DD_GPIO} (max)	-150			μA

Table 30. LVCMOS/LVTTL DC Characteristics[a][b][c][d][e] (Cont.)

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Units
I_{IL}	Input Low Current	XO_DPLL	V_{IN} = 0V, V_{DD_DIG} = V_{DD_DIG} (max)	-5			µA
I_{IL}	Input Low Current	CLK[1:0]	V_{IN} = 0V, V_{DD_CLK} = V_{DD_CLK} (max)	-5			µA
		nCLK[1:0]		-150			
V_{OH}	Output High Voltage	GPIO[9,8,5:0], SDA_M, SCL_M, SCLK_AUX, SDIO_AUX	V_{DD_GPIO} = 3.3V±5%, I_{OH} = -100µA	V_{DD_GPIO} - 0.2			V
			V_{DD_GPIO} = 3.3V±5%, I_{OH} = -12mA	2.6			
			V_{DD_GPIO} = 2.5V±5%, I_{OH} = -100µA	V_{DD_GPIO} - 0.2			
			V_{DD_GPIO} = 2.5V±5%, I_{OH} = -8mA	1.8			
			V_{DD_GPIO} = 1.8V±5%, I_{OH} = -100µA	V_{DD_GPIO} - 0.2			
			V_{DD_GPIO} = 1.8V±5%, I_{OH} = -2mA	V_{DD_GPIO} - 0.45			
			V_{DD_GPIO} = 1.5V±5%, I_{OH} = -100µA	1.2			
			V_{DD_GPIO} = 1.5V±5%, I_{OH} = -2mA	0.75 × V_{DD_GPIO}			
V_{OL}	Output Low Voltage	GPIO[9,8,5:0], SDA_M, SCL_M, SCLK_AUX, SDIO_AUX	V_{DD_GPIO} = 3.3V±5%, I_{OL} = 100µA			0.2	V
			V_{DD_GPIO} = 3.3V±5%, I_{OL} = 12mA			0.5	
			V_{DD_GPIO} = 2.5V±5%, I_{OL} = 100µA			0.2	
			V_{DD_GPIO} = 2.5V±5%, I_{OL} = 8mA			0.5	
			V_{DD_GPIO} = 1.8V±5%, I_{OL} = 100µA			0.2	
			V_{DD_GPIO} = 1.8V±5%, I_{OL} = 2mA			0.45	
			V_{DD_GPIO} = 1.5V±5%, I_{OL} = 100µA			0.2	
			V_{DD_GPIO} = 1.5V±5%, I_{OL} = 2mA			0.25 × V_{DD_GPIO}	

[a] V_{IL} should not be less than -0.3V.

[b] 3.3V characteristics in accordance with JESD8C-01,
2.5V characteristics in accordance with JESD8-5A.01,
1.8V characteristics in accordance with JESD8-7A,
1.5V characteristics in accordance with JESD8-11A.01,
1.2V characteristics in accordance with JESD8-12A.01

[c] V_{SS} = 0V, T_A = -40°C to 85°C.

[d] When Output Q are configured as LVCMOS, their output characteristics are specified in Table 35.

[e] Input pair used as two single-ended clocks rather than as a differential clock.

Table 31. Differential Input DC Characteristics[a]

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK[1:0]	$V_{IN} = V_{DD\_CLK} = V_{DD\_CLK}$ (max)			150	µA
		nCLK[1:0]				5	
I_{IL}	Input Low Current	CLK[1:0]	V_{IN} = 0V, $V_{DD\_CLK} = V_{DD\_CLK}$ (max)	-5			µA
		nCLK[1:0]		-150			
V_{PP}	Peak-to-Peak Voltage[b][c]		Any input protocol	0.15		1.3	V
V_{CMR}	Common Mode Input Voltage[b][d]	CLK[1:0], nCLK[1:0]	Input protocol = HCSL, HSTL, SSTL	0.1		V_{DD_CLK} - 1.2	V
			Input protocol = LVDS, LVPECL, CML	0.7		V_{DD_CLK}	

[a] V_{SS} = 0V, T_A = -40°C to 85°C.

[b] V_{IL} should not be less than -0.3V.

[c] V_{PP} is the single-ended amplitude of the output signal. The differential specs is 2*V_{PP}.

[d] Common mode voltage is defined as the cross-point.

Table 32. Differential Output DC Characteristics (V_{DDO_Qx} = 3.3V+5%, V_{SS} = 0V, T_A = -40°C to 85°C)[a][b][c][d]

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Units
V_{OVS}[e]	Output Voltage Swing	Output Q[a]	SWING = 00[f]	336	402	462	mV
			SWING = 01	478	605	698	
			SWING = 10	658	791	910	
			SWING = 11	739	870	997	
V_{CMR}[g]	Output Common Mode Voltage	Output Q[a]	CENTER = 000[h]	0.86	0.95	1.07	V
			CENTER = 001	0.98	1.14	1.28	
			CENTER = 010	1.13	1.33	1.51	
			CENTER = 011	1.30	1.53	1.73	
			CENTER = 100	1.46	1.73	1.95	
			CENTER = 101	1.63	1.93	2.17	
			CENTER = 110	1.80	2.12	2.39	
			CENTER = 111	1.96	2.30	2.59	

[a] For information on the signals referenced by this abbreviation, see Table 24.

[b] Terminated with 100Ω across Qx and nQx.

[c] If LVDS operation is desired, the user should select SWING = 00 and CENTER = 001 or 010.

[d] If LVPECL operation is desired, the user should select SWING = 10 and CENTER = 101 or 110 for 3.3V LVPECL, and SWING = 10 and CENTER = 001 or 010 for 2.5V LVPECL operation.

[e] V_{OVS} is the single-ended amplitude of the output signal. The differential specs is 2*V_{OVS}.

[f] Refers to the differential voltage swing setting programed into device registers for each output.

[g] Not all V_{CMR} selections can be supported with particular V_{DDO_Qx} and V_{OVS} settings. For information on which combinations are supported, see Table 17.

[h] Refers to the differential voltage crossing point (center voltage) setting programed into device registers for each output.

Table 33. Differential Output DC Characteristics (V_{DDO_Qx} = 2.5V+5%, V_{SS} = 0V, T_A = -40°C to 85°C)[a][b][c][d]

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Units
V_{OVS}[e]	Output Voltage Swing	Output Q[a]	SWING = 00[f]	295	393	448	mV
			SWING = 01	457	591	677	
			SWING = 10	587	761	881	
			SWING = 11	733	835	943	
V_{CMR}[g]	Output Common Mode Voltage	Output Q[a]	CENTER = 000[h]	0.85	0.93	1.03	V
			CENTER = 001	0.94	1.10	1.23	
			CENTER = 010	1.09	1.28	1.44	
			CENTER = 011	1.24	1.46	1.65	
			CENTER = 100	1.39	1.65	1.86	
			CENTER = 101	Not Supported			
			CENTER = 110				
			CENTER = 111				

[a] For information on the signals referenced by this abbreviation, see Table 24.

[b] Terminated with 100Ω across Qx and nQx.

[c] If LVDS operation is desired, the user should select SWING = 00 and CENTER = 001 or 010.

[d] If LVPECL operation is desired, the user should select SWING = 10 and CENTER = 001 or 010 for 2.5V LVPECL operation. For V_{DDO} = 2.5V, 3.3V LVPECL levels cannot be generated.

[e] V_{OVS} is the single-ended amplitude of the output signal. The differential specs is $2*V_{OVS}$.

[f] Refers to the differential voltage swing setting programed into device registers for each output.

[g] Not all V_{CMR} selections can be supported with particular V_{DDO_Qx} and V_{OVS} settings. For information on which combinations are supported, see Table 17.

[h] Refers to the differential voltage crossing point (center voltage) setting programed into device registers for each output.

Table 34. Differential Output DC Characteristics (V_{DDO_Qx} = 1.8V+5%, V_{SS} = 0V, T_A = -40°C to 85°C)[a][b][c]

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Units
V_{OVS}[d]	Output Voltage Swing	Output Q[a]	SWING = 00[e]	299	411	485	mV
			SWING = 01	470	586	700	
			SWING = 10	582	713	852	
			SWING = 11	612	750	899	
V_{CMR}[f]	Output Common Mode Voltage	Output Q[a]	CENTER = 000[g]	0.84	0.91	0.99	V
			CENTER = 001	0.91	1.05	1.18	
			CENTER = 010	1.05	1.21	1.36	
			CENTER = 011	Not Supported			
			CENTER = 100				
			CENTER = 101				
			CENTER = 110				
			CENTER = 111				

[a] For information on the signals referenced by this abbreviation, see Table 24.

[b] Terminated with 100Ω across Qx and nQx.

[c] If LVDS operation is desired, the user should select SWING = 00 and CENTER = 010.

[d] V_{OVS} is the single-ended amplitude of the output signal. The differential specs is 2*V_{OVS}.

[e] Refers to the differential voltage swing setting programed into device registers for each output.

[f] Not all V_{CMR} selections can be supported with particular V_{DDO_Qx} and V_{OVS} settings. For information on which combinations are supported, see Table 17.

[g] Refers to the differential voltage crossing point (center voltage) setting programed into device registers for each output.

Table 35. LVCMOS Clock Output DC Characteristics[a][b]

Symbol	Parameter	Test Condition	TERM[c] = 00			TERM = 01			TERM = 10			TERM = 11			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output High Voltage	V_{DDO_Qx} = 3.3V±5%	$0.74 \times V_{DDO\_Qx}$			$0.75 \times V_{DDO\_Qx}$			$0.75 \times V_{DDO\_Qx}$			$0.75 \times V_{DDO\_Qx}$			V
		V_{DDO_Qx} = 2.5V±5%	$0.70 \times V_{DDO\_Qx}$			$0.75 \times V_{DDO\_Qx}$			$0.75 \times V_{DDO\_Qx}$			$0.75 \times V_{DDO\_Qx}$			
		V_{DDO_Qx} = 1.8V±5%	$0.65 \times V_{DDO\_Qx}$			$0.71 \times V_{DDO\_Qx}$			$0.75 \times V_{DDO\_Qx}$			$0.75 \times V_{DDO\_Qx}$			
		V_{DDO_Qx} = 1.5V±5%	$0.61 \times V_{DDO\_Qx}$			$0.66 \times V_{DDO\_Qx}$			$0.70 \times V_{DDO\_Qx}$			$0.72 \times V_{DDO\_Qx}$			
		V_{DDO_Qx} = 1.2V±5%	$0.56 \times V_{DDO\_Qx}$			$0.59 \times V_{DDO\_Qx}$			$0.63 \times V_{DDO\_Qx}$			$0.66 \times V_{DDO\_Qx}$			
V_{OL}	Output Low Voltage	V_{DDO_Qx} = 3.3V±5%			$0.29 \times V_{DDO\_Qx}$			$0.25 \times V_{DDO\_Qx}$			$0.25 \times V_{DDO\_Qx}$			$0.25 \times V_{DDO\_Qx}$	V
		V_{DDO_Qx} = 2.5V±5%			$0.32 \times V_{DDO\_Qx}$			$0.27 \times V_{DDO\_Qx}$			$0.25 \times V_{DDO\_Qx}$			$0.25 \times V_{DDO\_Qx}$	
		V_{DDO_Qx} = 1.8V±5%			$0.39 \times V_{DDO\_Qx}$			$0.33 \times V_{DDO\_Qx}$			$0.30 \times V_{DDO\_Qx}$			$0.26 \times V_{DDO\_Qx}$	
		V_{DDO_Qx} = 1.5V±5%			$0.44 \times V_{DDO\_Qx}$			$0.38 \times V_{DDO\_Qx}$			$0.35 \times V_{DDO\_Qx}$			$0.31 \times V_{DDO\_Qx}$	
		V_{DDO_Qx} = 1.2V±5%			$0.50 \times V_{DDO\_Qx}$			$0.46 \times V_{DDO\_Qx}$			$0.42 \times V_{DDO\_Qx}$			$0.38 \times V_{DDO\_Qx}$	
Z_{OUT}	Output Impedance	V_{DDO_Qx} = 3.3V±5%		35			25			21			18		Ω
		V_{DDO_Qx} = 2.5V±5%		31			23			20			17		
		V_{DDO_Qx} = 1.8V±5%		42			31			25			21		
		V_{DDO_Qx} = 1.5V±5%		71			47			35			29		
		V_{DDO_Qx} = 1.2V±5%		101			86			66			49		

[a] V_{SS} = 0V, T_A = -40°C to 85°C.

[b] V_{DDO_Qx} is used to refer to the appropriate V_{DDO_Qx} power supply voltage for each output. For more information, see Table 24 and the "Pin Description" table.

[c] This refers to the register settings for the LVCMOS output drive strength within the device.

Table 36. Input Frequency Characteristics[a]

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	OSCI, OSCO	Using a Crystal[b]	25		54	MHz
			Over-driving Crystal Input Doubler Logic Enabled[c]	25		62.5	
			Over-driving Crystal Input Doubler Logic Disabled	50		125	
		Input CLK[d][e]	Differential Mode	0.001		1000	
			Single-ended Mode	0.001		250	
		GPIO	Used as Clock Input			150	
f_{IN}	Input Frequency	XO_DPLL		1		150[f]	MHz
f_{SCLK}	Serial Port Clock SCLK_AUX (slave mode)	I^2C Operation		100		1200	kHz
		SPI Operation		0.1		50	MHz

[a] V_{SS} = 0V, T_A = -40°C to 85°C

[b] For crystal characteristics, see Table 37.

[c] Refer to Overdriving the XTAL Interface.

[d] For information on the signals referenced by this abbreviation, see Table 24.

[e] For proper device operation, the input frequency must be divided down to 150MHz or less (DPLL Phase Detector maximum frequency = 150MHz).

[f] If the System DPLL needs to be driven with a higher frequency, one of the CLKx / nCLKx inputs can be routed via register settings to the System DPLL instead of using XO_DPLL.

Table 37. Crystal Characteristics[a]

Parameter	Test Condition	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		25		54	MHz
Equivalent Series Resistance (ESR)	C_L= 18pF, crystal frequency $\leq$ 40MHz			50	Ω
	C_L= 18pF, crystal frequency > 40MHz			25	
	C_L= 12pF			50	
Load Capacitance (C_L)			12		pF

[a] V_{SS} = 0V, T_A = -40°C to 85°C

AC Electrical Characteristics

Table 38. AC Characteristics[a][b]

Symbol	Parameter		Test Condition		Minimum	Typical	Maximum	Units
f_{VCO}	Analog PLL VCO Operating Frequency		V_{DDA_X}[c] = 3.3V±5%		13.4		13.8	GHz
			V_{DDA_X}[c] = 2.5V±5%		13.5		13.9	
f_{FOD}	Fractional Output Divider Operating Frequency		Measured with output divider set to /1		500		1000	MHz
f_{OUT}	Output Frequency	Differential Output			0.0000005		1000	MHz
		LVCMOS Output			0.0000005		250	
Δf_{OUT}	Output Frequency Accuracy[d]					0		ppb
	Initial Frequency Offset[e]		Switchover or Entering Holdover State			1		ppb
	Output Phase Change in Fully Hitless Switching[f]		Input references with phase difference < 100μs			350		ps
			Input references with phase difference ≥ 100μs			1000		
t_{SK}	Output to Output Skew[g][h]		Any two differential outputs[i]			80	160	ps
			Any two outputs configured as LVCMOS in-phase[j]	V_{DDO_Qx} = 3.3V±5%, 2.5V±5%, 1.8V±5% or 1.5V±5%		100	300	
				V_{DDO_Qx} = 1.2V ±5%		160	360	

Table 38. AC Characteristics[a][b] (Cont.)

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
$t_{SK(B)}$	Output to Output Skew within a Bank[g][h]	Differential Outputs	1st Bank: Q8, Q11		25	65	ps
			2nd Bank: Q9, Q10		25	50	
		Outputs Configured as LVCMOS in-phase V_{DDO_Qx} = 3.3V±5%, 2.5V±5% or 1.8V±5%	1st Bank: Q8, Q11		30	110	
			2nd Bank: Q9, Q10		30	110	
		Outputs Configured as LVCMOS in-phase V_{DDO_Qx} = 1.5V ±5% or 1.2V ±5%	1st Bank: Q8, Q11		50	200	
			2nd Bank: Q9, Q10		50	200	
		Q to nQ of same output pair, cfg. as LVCMOS, in-phase[j]	V_{DDO_Qx} = 3.3V ±5% or 2.5V ±5%		10	60	
			V_{DDO_Qx} = 1.8V ±5% or 1.5V ±5% or 1.2V ±5%		15	100	
Δt_{SK}	Temperature Variation[k] Output-Output					4	ps/°C
t_{ALIGN}	Input - Output Alignment Variation[l]	Delay variation as shown in Figure 32 for any CLK/CLKn input pair to any Q/Qn output pair in differential mode when using internal loopback.		-500		500	ps
Δt_{ALIGN}	Temperature Variation[k] Input-Output					4	ps/°C

Table 38. AC Characteristics[a][b] (Cont.)

Symbol	Parameter		Test Condition		Minimum	Typical	Maximum	Units
t_R / t_F	Output Rise and Fall Times 20% to 80%	Differential Output[m][n]	V_{DDO_Qx}[o] = 3.3V±5%, 2.5V±5% or 1.8V±5%	SWING[p] = 00	100		450	ps
				SWING = 01				
				SWING = 10				
				SWING = 11				
		LVCMOS Output[q]	V_{DDO_Qx} = 3.3V±5%	TERM[r] = 00	100	254	380	ps
				TERM = 01	100	262	400	
				TERM = 10	110	275	460	
				TERM = 11	115	268	510	
			V_{DDO_Qx} = 2.5V±5%	TERM = 00	115	285	405	ps
				TERM = 01	120	293	470	
				TERM = 10	120	315	525	
				TERM = 11	140	347	565	
			V_{DDO_Qx} = 1.8V±5%	TERM = 00	205	417	590	ps
				TERM = 01	205	458	715	
				TERM = 10	230	459	800	
				TERM = 11	235	482	880	
			V_{DDO_Qx} = 1.5V±5%[s]	TERM = 00	415	558	730	ps
				TERM = 01	545	747	985	
				TERM = 10	615	890	1145	
				TERM = 11	690	1011	1305	
			V_{DDO_Qx} = 1.2V±5%[s]	TERM = 00	800	986	1250	ps
				TERM = 01	1180	1416	1835	
				TERM = 10	1415	1715	2195	
				TERM = 11	1650	1980	2520	

Table 38. AC Characteristics[a][b] (Cont.)

Symbol	Parameter		Test Condition		Minimum	Typical	Maximum	Units
odc	Output Duty Cycle	Differential Output	PULSE = 50%	f_{OUT} < 500MHz	47	50	53	%
				500MHz ≤ f_{OUT} < 800MHz	45	50	55	%
				f_{OUT} ≥ 800MHz	40	50	60	%
		LVCMOS	PULSE = 50%	V_{DDO_Qx} = 3.3V or 2.5V	47	50	53	%
				V_{DDO_Qx} = 1.8V or 1.5V	45	50	55	
				V_{DDO_Qx} = 1.2V	42	50	58	
		Any Output Type Operating as a Frame or Sync Pulse	PULSE = Sync Pulse, 100ns		100			ns
			PULSE = Sync Pulse, 1µs		1			µs
			PULSE = Sync Pulse, 10µs		10			µs
			PULSE = Sync Pulse, 100µs		200			µs
			PULSE = Sync Pulse, 1ms		2			ms
			PULSE = Sync Pulse, 10ms		10			ms
			PULSE = Sync Pulse, 100ms		100			ms
			PULSE = Frame Pulse, 0.2UI		0.2			UI
			PULSE = Frame Pulse, 1UI		1			UI
			PULSE = Frame Pulse, 2UI		2			UI
tjit(Φ)	Phase Jitter, RMS (Random)[t]		10kHz to 20MHz 49.152MHz Crystal, Synthesizer Mode	122.88MHz		133	168	fs
				156.25MHz		156	229	
				245.76MHz		115	140	
				312.5MHz		146	186	
				322.265625MHz		155	210	
				983.04MHz		109	179	
			10kHz to 20MHz 49.152MHz Crystal, DPLL Mode	122.88MHz		138	184	fs
				156.25MHz		153	208	
				245.76MHz		126	182	
				312.5MHz		147	194	
				322.265625MHz		160	216	
				983.04MHz		104	167	
$t_{startup}$	Start-up Time[u]	Regulators Ready[v]				3		µs
		Internal OTP Start-up	Synthesizer mode			7	10	ms
			DPLL mode, with a loop bandwidth setting of 300Hz[w]			1.5		s

[a] V_{SS} = 0V, T_A = -40°C to 85°C.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[c] V_{DDA_X} refers to V_{DDA_PDCP}, V_{DDA_XTAL}, V_{DDA_LC}, and V_{DDA_BG}.

[d] Long-term frequency error with respect to the DPLL input reference. The typical value shown assumes the DPLL has been phase-locked to a stable input reference for at least 306 minutes (based on a 0.1mHz advanced holdover filter setting) before going into an advanced holdover state on disqualification of the input reference.

[e] This parameter will vary with the quality of the reference to the system DPLL. The typical value shown assumes an ideal reference used for the system DPLL.

[f] This parameter will vary with the quality of the TDC and system DPLL references. The typical value shown assumes an ideal reference is used as input to the TDC and system DPLL.

[g] Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage

[h] This parameter is defined in accordance with JEDEC Standard 65.

[i] Measured at the differential cross points.

[j] Measured at V_{DDO_Qx} / 2.

[k] This parameter is measured across the full operating temperature range and the difference between the slowest and fastest numbers is the variation.

[l] Measured from the differential cross point of the input to the differential cross point of the associated output after device is locked and input is stable. Measured using integer-related input and output frequencies.

[m] Rise and fall times on differential outputs are independent of the power supply voltage on the output.

[n] Measured with outputs terminated with 50Ω to GND.

[o] For information on the signals referenced by this abbreviation, see Table 24.

[p] Refers to the differential voltage swing setting programed into device registers for each output.

[q] Measured with outputs terminated with 50Ω to V_{DDO_Qx} / 2.

[r] Refers to the LVCMOS output drive strength (termination) setting programed into device registers for each output.

[s] This parameter has been characterized with F_{OUT} = 50MHz.

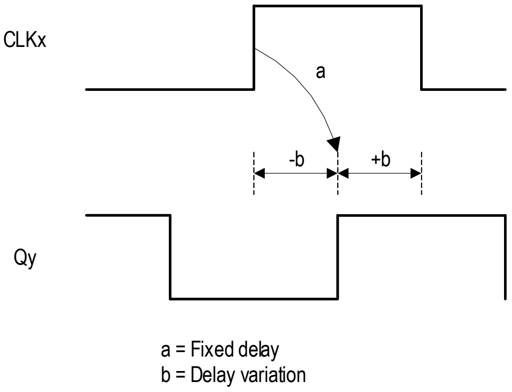
[t] Characterized using a Rohde and Schwarz SMA100A overdriving the XTAL Interface.

[u] Measured from the rising edge of nMR after all power supplies have reached > 80% of nominal voltage to the first stable clock edge on the output. A stable clock is defined as one generated from a locked analog or digital PLL (as appropriate for the configuration listed) with no further perturbations in frequency expected.

[v] At power-up, the nMR signal must be asserted for at least this period of time.

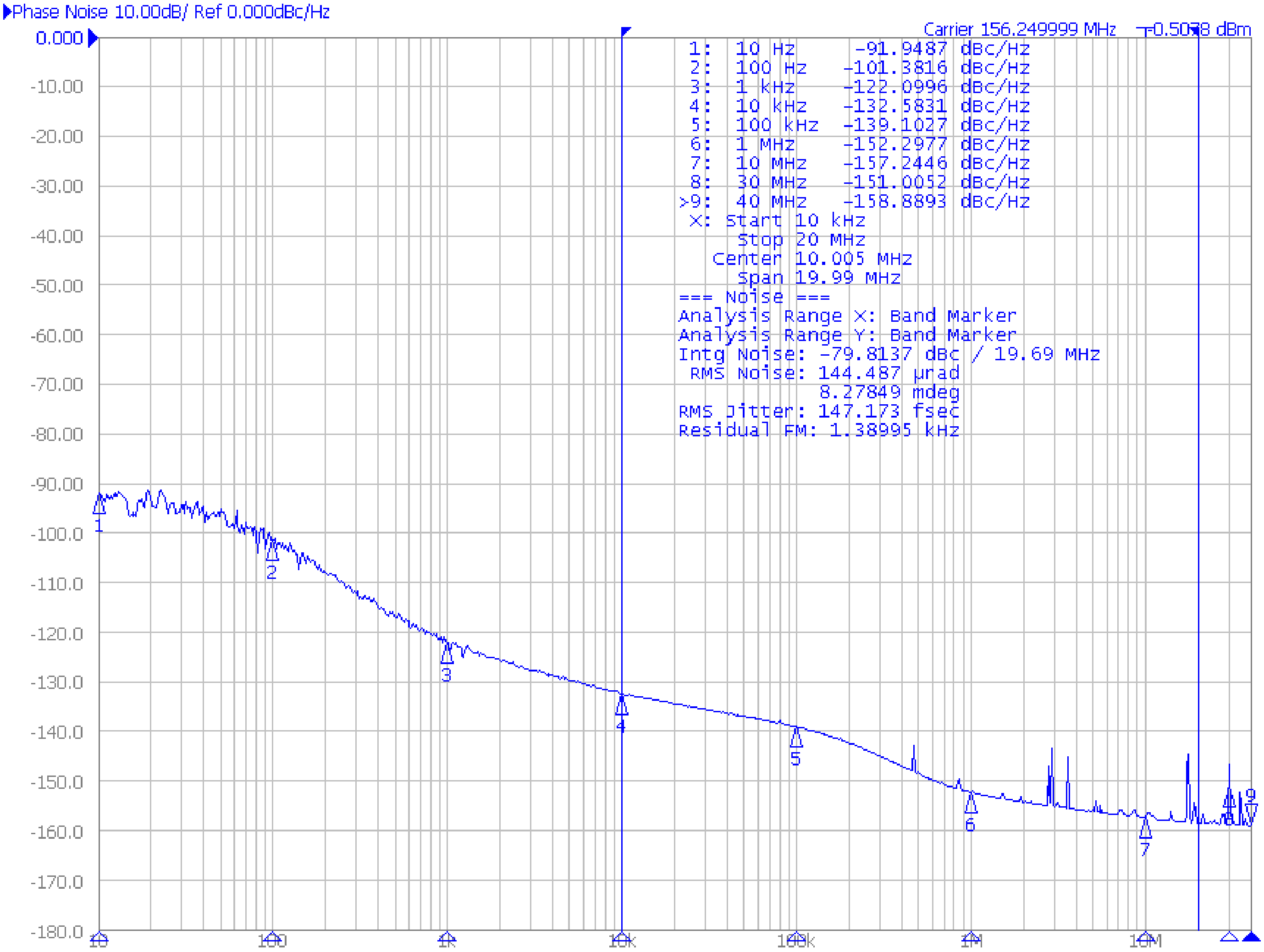
[w] Start-up time will depend on the actual configuration used. For more information on estimating start-up time, please contact IDT technical support.

Figure 32. Input-Output Delay



Clock Phase Noise Characteristics

Figure 33. 156.25MHz Output Phase Noise



```
 1:  10 Hz     -91.9487 dBc/Hz
 2:  100 Hz   -101.3816 dBc/Hz
 3:  1 kHz    -122.0996 dBc/Hz
 4:  10 kHz   -132.5831 dBc/Hz
 5:  100 kHz  -139.1027 dBc/Hz
 6:  1 MHz    -152.2977 dBc/Hz
 7:  10 MHz   -157.2446 dBc/Hz
 8:  30 MHz   -151.0052 dBc/Hz
>9:  40 MHz   -158.8893 dBc/Hz
 X: Start 10 kHz
     Stop 20 MHz
   Center 10.005 MHz
     Span 19.99 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -79.8137 dBc / 19.69 MHz
 RMS Noise: 144.487 µrad
              8.27849 mdeg
RMS Jitter: 147.173 fsec
Residual FM: 1.38995 kHz
```

Applications Information

Recommendations for Unused Input and Output Pins

Inputs

CLKx / nCLKx Input

For applications that do not require the use of the reference clock input, both CLK and nCLK should be left floating. If the CLK/nCLK input is connected but not used by the device, it is recommended that CLK and nCLK not be driven with active signals.

LVCMOS Control Pins

LVCMOS control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs

LVCMOS Outputs

Any LVCMOS output can be left floating if unused. There should be no trace attached. The mode of the output buffer should be set to tri-stated to avoid any noise being generated.

Differential Outputs

All unused differential outputs can be left floating. IDT recommends that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Power Connections

The power connections of the 8A34043 can be grouped as shown if all members of the groups are using the same voltage level:

- V_{DD_DIG},V_{DD_GPIO}, V_{DD_CLK}
- $V_{DDA\_PDCP\_XTAL}$
- V_{DDA_FB}
- V_{DDA_BG}, V_{DDA_LC} (not ideal to combine, so if board space allows keep separated)
- $V_{DD\_DCO\_Qn}$ (should keep separated except where FOD blocks are all running at the same frequency)
  - If all outputs Qn/nQn and functions associated with any particular $V_{DD\_DCO\_Qn}$ pin are not used, the power pin can be left floating
- V_{DDO_Qn} (can share supplies if output frequencies are the same, otherwise keep separated to avoid spur coupling)
  - If all outputs Qn/nQn associated with any particular V_{DDO_Qn} pin are not used, the power pin can be left floating

Clock Input Interface

The 8A34043 accepts both single-ended and differential inputs. For information on input terminations, see *Quick Guide - Output Terminations (AN-953)* located on the 8A34043 product page.

If you have additional questions on input types not covered in the application discussion, or if you require information about register programming sequences for changing the differential inputs to accept LVCMOS inputs levels, see *Termination - AC Coupling Clock Receivers (AN-844)* or contact IDT technical support.

Overdriving the XTAL Interface

The OSCI input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The OSCO pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. For limits on the frequency that can be used, see Table 36.

Figure 34 shows an example of the interface diagram for a high-speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver.

Figure 34. LVCMOS Driver to XTAL Input Interface

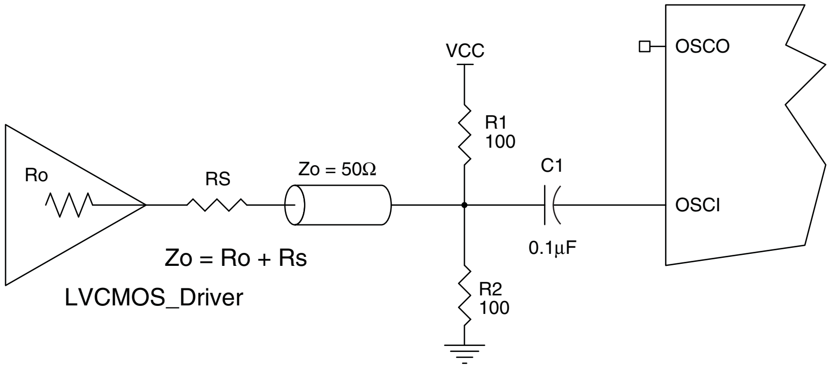
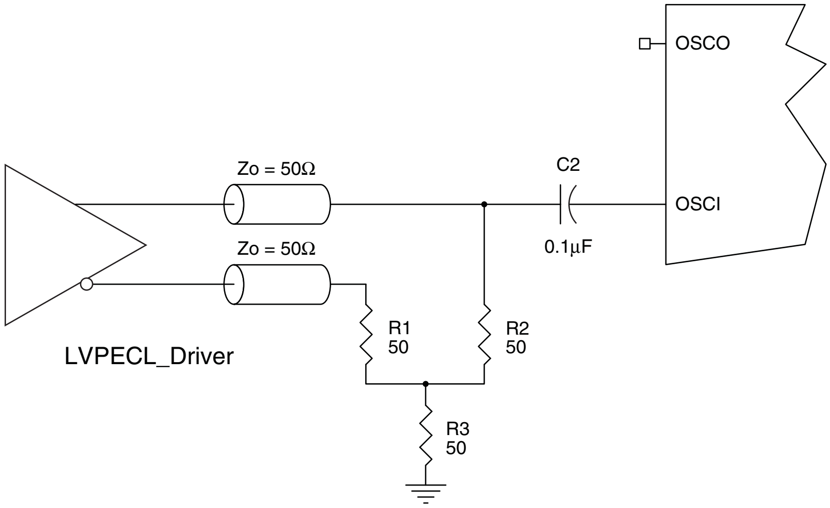


Figure 35 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components may not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

Figure 35. LVPECL Driver to XTAL Input Interface



Wiring the Differential Input to Accept Single-Ended Levels

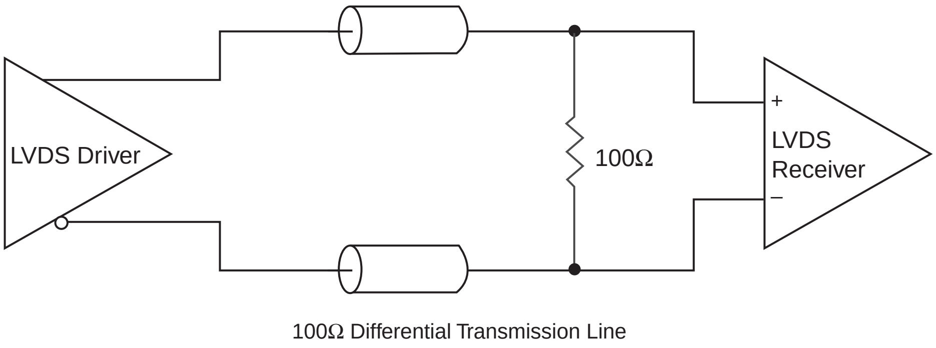
For information, see the *Differential Input to Accept Single-ended Levels Application Note (AN-836)*.

Differential Output Termination

For all types of differential protocols, the same termination scheme is recommended (see Figure 36). This scheme is the same as normally used for an LVDS output type: the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface-mounted and must be placed as close to the receiver as possible.

For alternate termination schemes, see “LVDS Termination” in *Quick Guide - Output Terminations (AN-953)* located on the 8A34043 product page, or contact IDT for support.

Figure 36. Standard LVDS Termination



Crystal Recommendation

For the latest vendor / frequency recommendations, please contact IDT.

External I^2C Serial EEPROM Recommendation

An external I^2C EEPROM can be used to store configuration data or to contain device update data. IDT has validated and recommends the use of the Microchip 24FC1025 or OnSemi CAT24M01 1Mbit EEPROM. Note: The EEPROM must have a 1Mbit capacity.

Schematic and Layout Information

The 8A34043 requires external load capacitors to ensure the crystal will resonate at the proper frequency. For recommended values for external tuning capacitors, see Table 39.

Table 39. 8A34043 Recommended Tuning Capacitors for Crystal Input

Crystal Nominal C_L Value	Recommended Tuning Capacitor Value
10pF	4.7pF
12pF	10pF
18pF	22pF

Power Considerations

For power and current consumption calculations, refer to IDT’s Timing Commander tool.

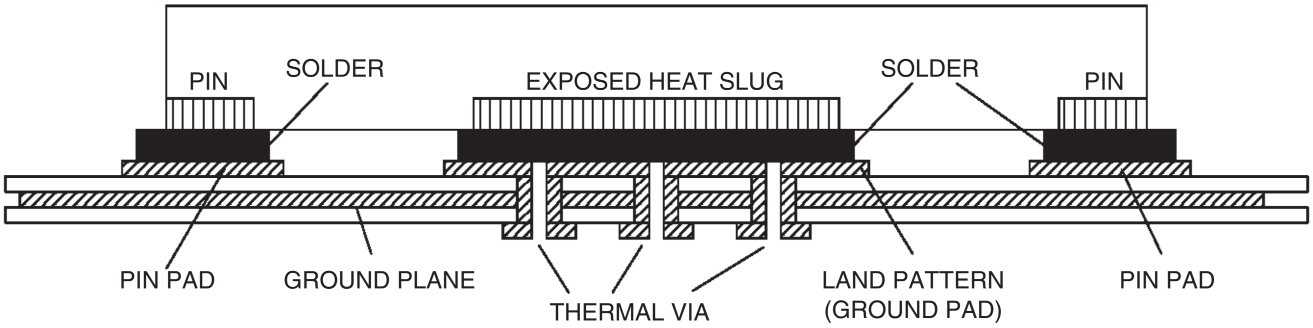
VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 37. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed.

Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

Figure 37. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (Drawing not to Scale)



Thermal Characteristics

Table 40. Thermal Characteristics for 72-VFQFPN Package

Symbol	Parameter		Value	Units
θ_{JA}	Theta J_A. Junction to Ambient Air Thermal Coefficient[a][b]	0 m/s air flow	14.75	°C/W
		1 m/s air flow	11.79	°C/W
		2 m/s air flow	10.59	°C/W
θ_{JB}	Theta J_B. Junction to Board Thermal Coefficient[a]		0.66	°C/W
θ_{JC}	Theta J_C. Junction to Device Case Thermal Coefficient[a]		14.5	°C/W
-	Moisture Sensitivity Rating (Per J-STD-020)		3	

[a] Multi-Layer PCB with 2 ground and 2 voltage planes.

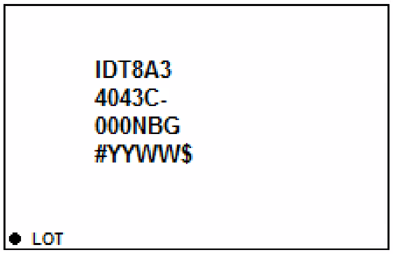
[b] Assumes ePAD is connected to a ground plane using a grid of 7x7 thermal vias.

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/48-vfqfpn-package-outline-drawing-70-x-70-x-075mm-body-epad-565-x-565-mm-050-mm-pitch-nbg48p1

Marking Diagram



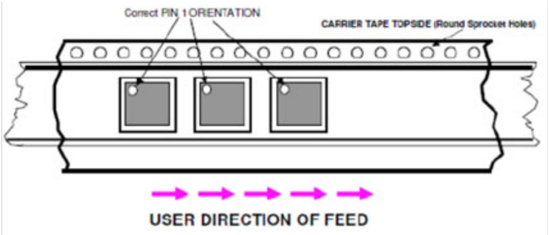
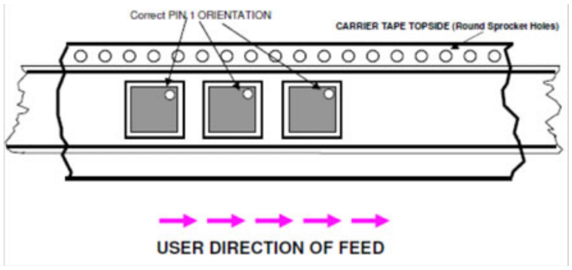
- Lines 1 to 3 denote the part number.
  - “000” denotes dash code.
  - “NBG” denotes the package code.
- Line 4:
  - “YYWW” is the last digits of the year and week that the part was assembled
  - “$” denotes mark code.
- Line 4 denotes sequential lot number.

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
8A34043C-dddNBG[a]	7 × 7 × 0.75 mm 48-VFQFPN with 5.65mm ePAD	3	Tray	-40° to +85°C
8A34043C-dddNBG8	7 × 7 × 0.75 mm 48-VFQFPN with 5.65mm ePAD	3	Tape and Reel, Pin 1 Orientation: EIA-481-C	-40° to +85°C
8A34043C-dddNBG#	7 × 7 × 0.75 mm 48-VFQFPN with 5.65mm ePAD	3	Tape and Reel, Pin 1 Orientation: EIA-481-D	-40° to +85°C

[a] Replace “ddd” with the desired pre-programmed configuration code provided by IDT in response to a custom configuration request or use “000” for unprogrammed parts.

Table 41. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
NBG8	Quadrant 1 (EIA-481-C)	
NBG#	Quadrant 2 (EIA-481-D)	

Product Identification

Table 42: Product Identification

Part Number	JTAG ID	Product ID
8A34043	0x064D	0x4043

Glossary

Term	Definition
1PPS	One Pulse Per Second.
eCLK	Embedded clock.
eCSR	Embedded CSR access.
eDATA	Embedded DATA channel.
ePP2S	Embedded PP2S.
ePPS	Embedded PPS. This describes a means to embed 1PPS on a clock using PWM.
EPPS	Even PPS.
ESEC	Even Second pulse. PP2S and ESEC are used interchangeably or sometimes combined as PP2S/ESEC.
eSYNC	Embedded SYNC pulse.
PP2S	Pulse Per 2 Second. This represents a 0.5Hz pulse.
PPS	Pulse Per Second.
REF-SYNC	Combination of high-speed clock (i.e., > 1MHz) and low-speed frame/sync pulse (i.e., < 8kHz).
SCSR	Standard Control / Status Register

Revision History

Revision Date	Description of Change
February 8, 2019	▪ Revision C device (which has Device Update v4.7 embedded) has the following functional differences: • Reset sequence sped-up, altering the way external EEPROMs are searched. Changes made to Reset Sequence and Use of External I^2C EEPROM sections • Changed Activity Monitor limits (this is with Device Update v4.7 regardless of hardware revision) in Table 7 ▪ Corrected the clock and GPIO mapping in Table 5 ▪ Clarified the following areas of the datasheet: Steerable Fractional Output Divider (FOD), JTAG Interface, and External I2C Serial EEPROM Recommendation ▪ Changed the Marking Diagram and Ordering Information to show C revision
November 19, 2018	Initial release.

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support

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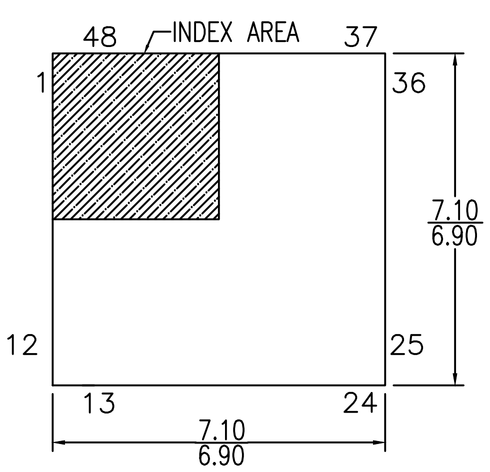
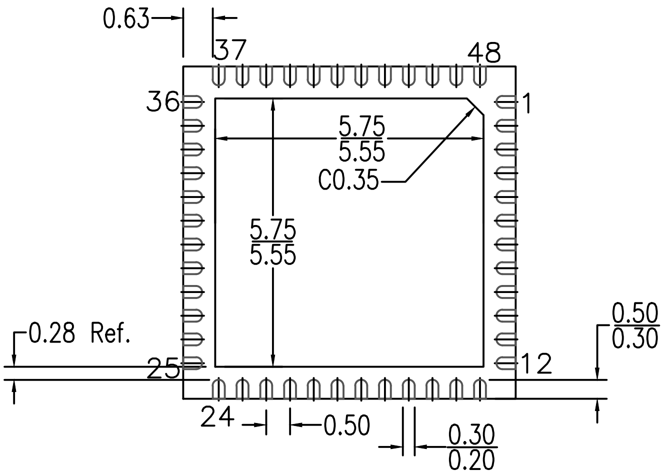
48-VFQFPN, Package Outline Drawing

7.0 x 7.0 x 0.75 mm Body, Epad 5.65 x 5.65 mm, 0.5mm Pitch
NBG48P1, PSC-4228-01, Rev 02, Page 1

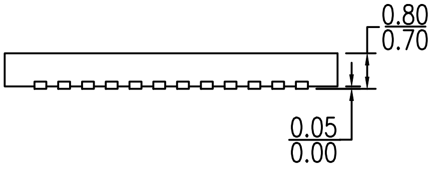
TOP VIEW



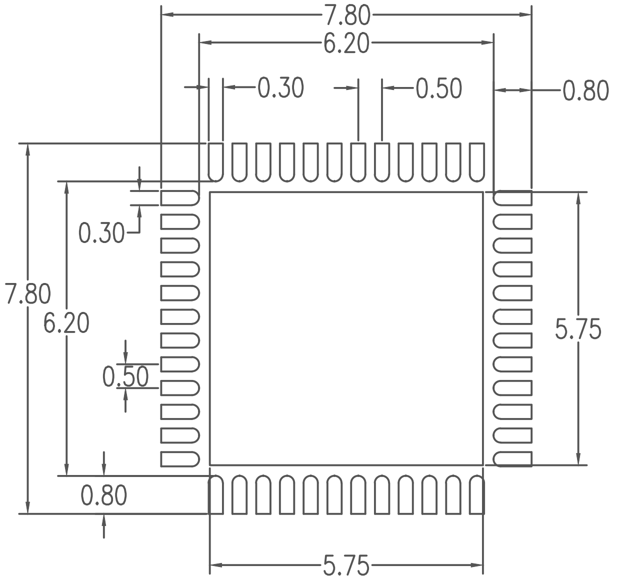
BOTTOM VIEW



SIDE VIEW



NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.



RECOMMENDED LAND PATTERN RECOMMENDATION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Sept 10, 2018	Rev 02	Correct VFQFP-N to VFQFPN, Remove Black Package Code
Sept 27, 2017	Rev 01	New Format

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Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А