

TAT7457

CATV 75 Ω pHEMT Adjustable Gain RF Amplifier



Applications

- Single-ended and Push-pull Optical Receivers
- Low-noise Drop Amplifiers
- Distribution Amplifiers
- Multi-Dwelling Units
- Single-ended Gain Block

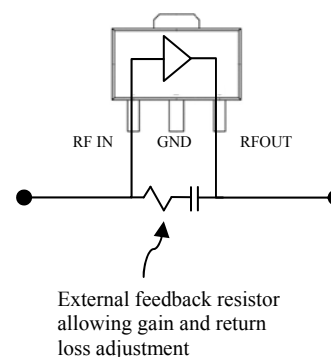


SOT-89 package

Product Features

- Gain, return loss and bias externally adjustable
- On-chip active bias for consistent bias current and repeatable performance
- DC – 2000 MHz bandwidth
- Low noise: typical NF < 2 dB to 1000MHz
- Flexible 5 V to 8 V biasing
- $I_{DD}(5V) = 120$ mA typical in application circuit
- 19 dB typical gain in application circuit
- +40 dBm typical OIP3
- +xx dBm typical P1dB
- Low distortion: CSO -66 dBc, CTB -78 dBc (10 dBmV/ch at input, 80 ch NTSC flat)
- pHEMT device technology
- SOT-89 package

Functional Block Diagram



General Description

The TAT7457 is a low cost RF amplifier designed for applications from DC to 2000 MHz. The balance of low noise and distortion provides an ideal solution for a wide range of broadband amplifiers used in cable television applications such as optical receivers and low noise front ends.

The TAT7457 has features allowing a great deal of design-in flexibility. Gain and return loss are adjustable with an external feedback resistor. An internal bias circuit mitigates the effect of temperature and process variation and an external resistor may be used to adjust the bias current to optimize distortion or noise performance. There are no on-chip capacitors limiting the low freq response which extends down to DC.

The TAT7457 is fabricated using 6-inch GaAs pHEMT technology to optimize performance and cost. It provides excellent gain and return loss consistency inherent to the pHEMT process.

Pin Configuration

| Pin # | Symbol |
|-------|------------|
| 1 | RF IN |
| 2 | GND |
| 3 | RF OUT |
| 4 | GND PADDLE |

Ordering Information

| Part No. | Description |
|------------|---|
| TAT7457 | 75 Ω High linearity pHEMT amplifier (lead-free/RoHS compliant SOT-89 Pkg) |
| TAT7457-EB | Amplifier evaluation board |

Standard T/R size = 1000 pieces on a 7" reel.

Specifications

Absolute Maximum Ratings

| Parameter | Rating |
|---|----------------|
| Storage Temperature | -65 to +150 °C |
| Device Voltage | +TBD V |
| Thermal Resistance (jnc. to case) θ_{jc} | TBD °C/W |

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

| Parameter | Min | Typ | Max | Units |
|---|-----|-----|-----|-------|
| V_{cc} | 5 | | 8 | V |
| I_{cc} | | 120 | | mA |
| T_J (for >10 ⁶ hours MTTF) | | | TBD | °C |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25°C case temp, +5V Vsupply, DC to 1200 MHz, 1 k Ω feedback resistor

| Parameter | Conditions | Min | Typical | Max | Units |
|-----------------------------|-------------|-----|---------|------|-------|
| Operational Frequency Range | | DC | | 1200 | MHz |
| Gain | | | 19 | | dB |
| Gain Flatness | | | +/- 0.7 | | dB |
| Noise Figure at 1 GHz | | | 2.0 | | dB |
| Input Return Loss | | | 18 | | dB |
| Output Return Loss | | | 18 | | dB |
| Output P1dB | | | +xx | | dBm |
| Output IP3 | See Note 1. | | +40 | | dBm |
| Output IP2 | See Note 1. | | +61 | | dBm |
| CSO | See Note 2. | | -66 | | dBc |
| CTB | See Note 2. | | -78 | | dBc |
| Idd | | | 120 | | mA |

Notes:

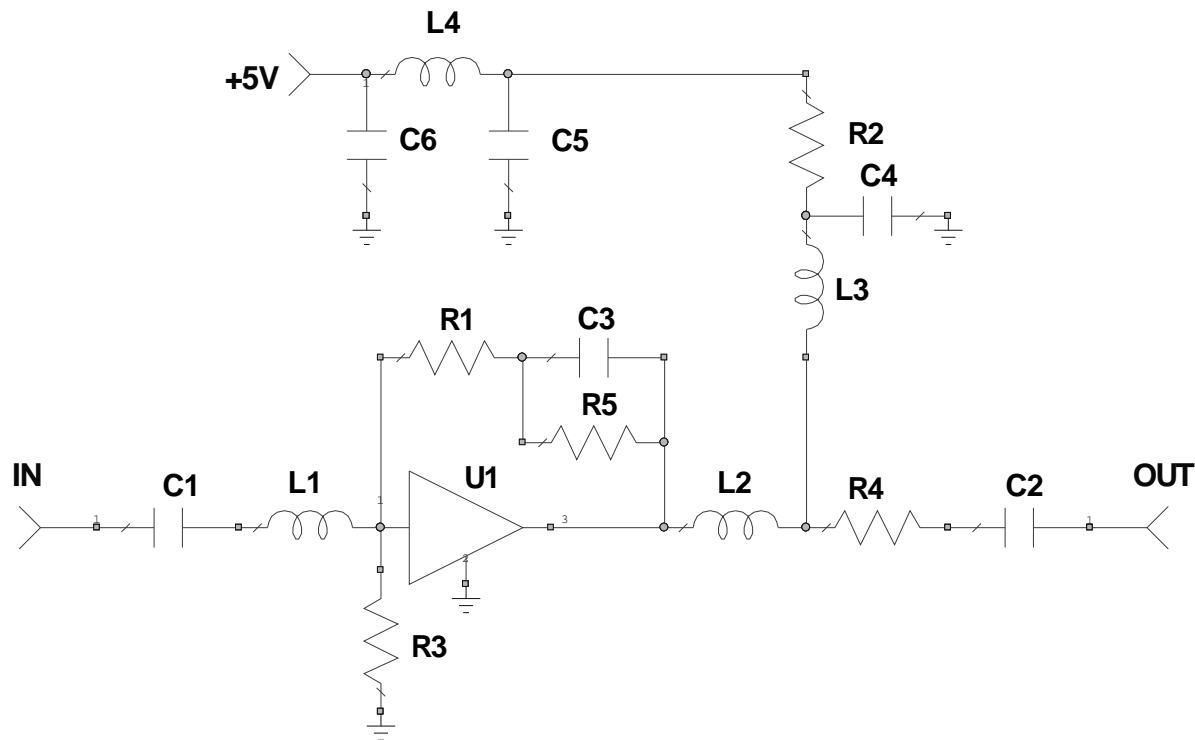
1. At -17 dBm/toner at input.
2. 10 dBmV/ch at input, 80 ch flat NTSC
3. Electrical specifications are measured at specified test conditions.
4. Specifications are not guaranteed over all recommended operating conditions.

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Reference Design DC-1200 MHz



Notes:

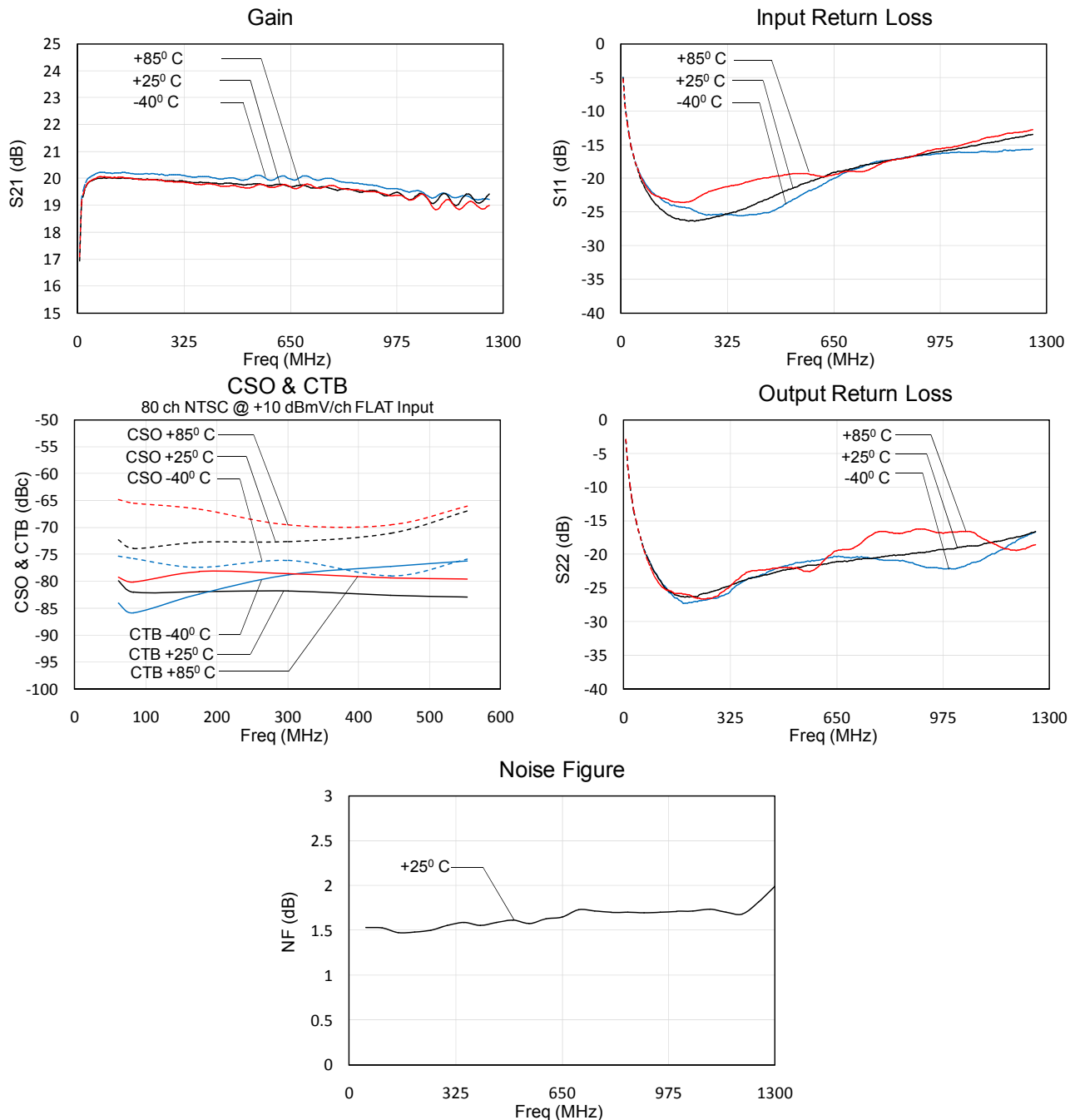
1. See PC Board Layout, page 6 for more information

Bill of Material

| Ref Des | Value | Description | Manufacturer | Part Number |
|---------|---------------|--|--------------|-------------|
| U1 | | Amplifier, SOT-89 | TriQuint | TAT7457 |
| R1 | 1 k Ω | Thick Film Res., 0402, 1% | various | |
| R2 | 0 Ω | Thick Film Res., 1206 | various | |
| R3 | N/L | | | |
| R4 | 0 Ω | Thick Film Res., 0402 | various | |
| R5 | 75 k Ω | Thick Film Res., 0402, 1% | various | |
| C1, C2 | 0.01 uF | Ceramic Cap, 0603, X7R, 16V, 10% | various | |
| C3, C4 | 0.01 uF | Ceramic Cap, 0402, X7R, 16V, 10% | various | |
| C5, C6 | 0.1 uF | Ceramic Cap, 0603, X7R, 16V, 10% | various | |
| L1, L2 | 4.7 nH | Ceramic Wire-Wound Ind, 0402, 5% | various | |
| L3 | 880 nH | Ferrite Ind., Vertical Wire-Wound, 1206, 10% | various | |
| L4 | 910 nH | Ferrite Ind., Vertical Wire-Wound, 1008, 10% | various | |

Application Board Typical Performance

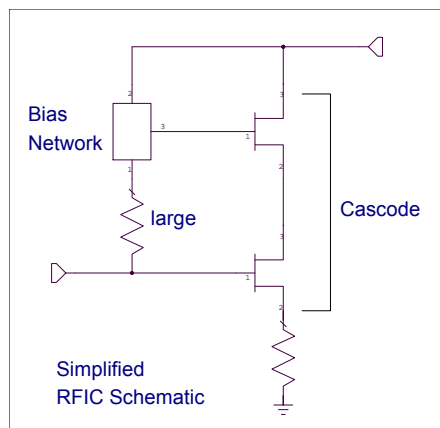
Case temperature noted on graphs. $V_{supply} = 5V$.



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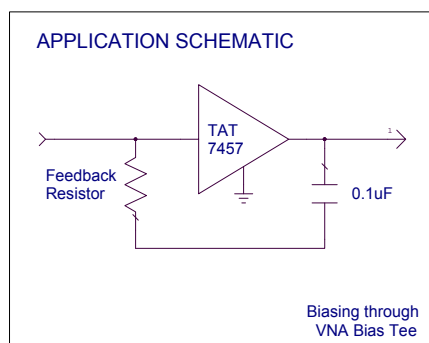
Detailed Device Description



The TAT7457 was designed to be a low cost general purpose amplifier suitable for a wide range of applications.

The TAT7457 is a high gain cascode amplifier with no internal shunt feedback.

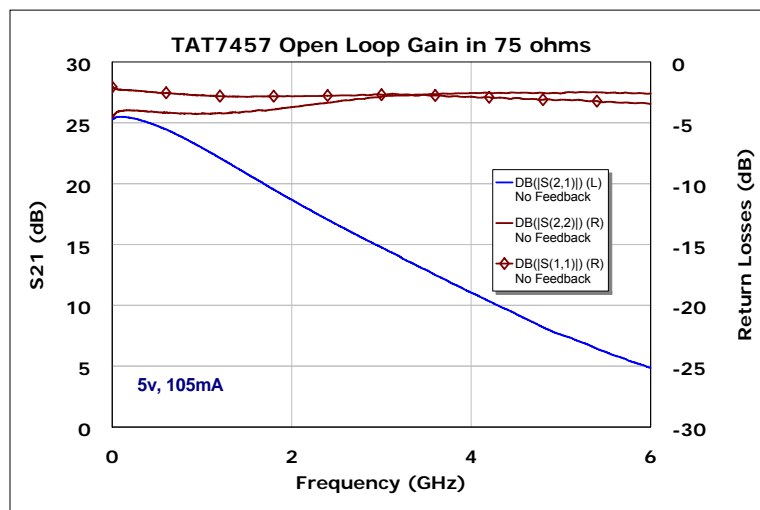
An on-chip biasing network sets the operating conditions for the FETs. This network stabilizes bias current against changes in temperature as well as against the normal process variations expected from wafer to wafer. Stabilized bias current will lead to more consistent RF performance.



Customers may set the gain and return loss of their amplifier by selecting an appropriate external feedback resistor.

Reducing the value of the feedback resistor will reduce the gain and lower the input and output impedances.

Low noise TIA designers may set the value of feedback to a high value (>1k ohm) for best performance.



There are no on-chip capacitors that limit the low frequency response, enabling the TAT7457 frequency response to extend to DC. The open loop gain (no external feedback) and high frequency gain performance is shown in the plot to the left.

Biasing Options for Improved Performance

Distortion and noise performance may be optimized with simple changes to the application circuit.

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Noise performance may be improved by adding a large resistor R3 of approximately 20 k Ω to ground. This resistor will reduce the bias current and improve noise.

Best distortion occurs on a 6v supply; however for improved distortion on a 5v supply, bias current may be increased by adding a large pull up resistor R5 of approximately 75 k Ω in parallel with the feedback capacitor.

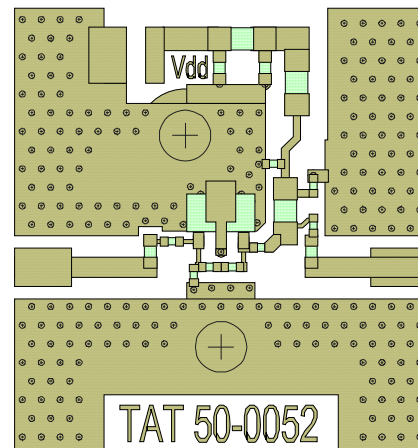
Applications Information

PC Board Layout

Core is .062" FR-4, $\epsilon_r = 4.7$. Metal layers are 1-oz copper.

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

For further technical information, Refer to <http://www.triquint.com/TAT7457>



Mechanical Information

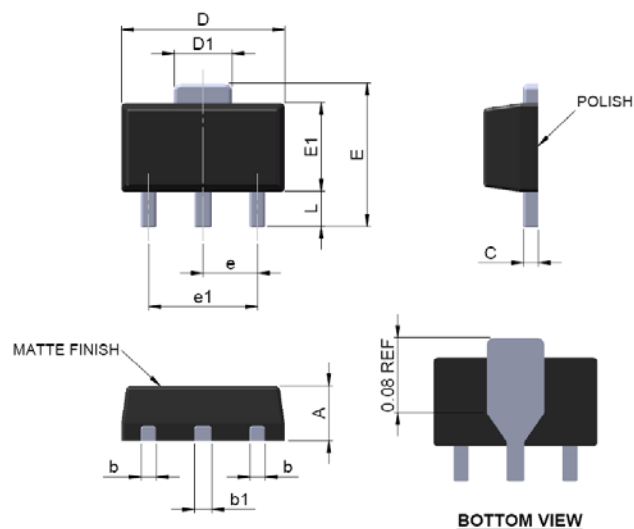
Package Information and Dimensions

This package is lead-free/RoHS-compliant. The plating material on the leads is 100 % Matte Tin. It is compatible with both lead-free (maximum 260 $^{\circ}$ C reflow temperature) and lead (maximum 245 $^{\circ}$ C reflow temperature) soldering processes.

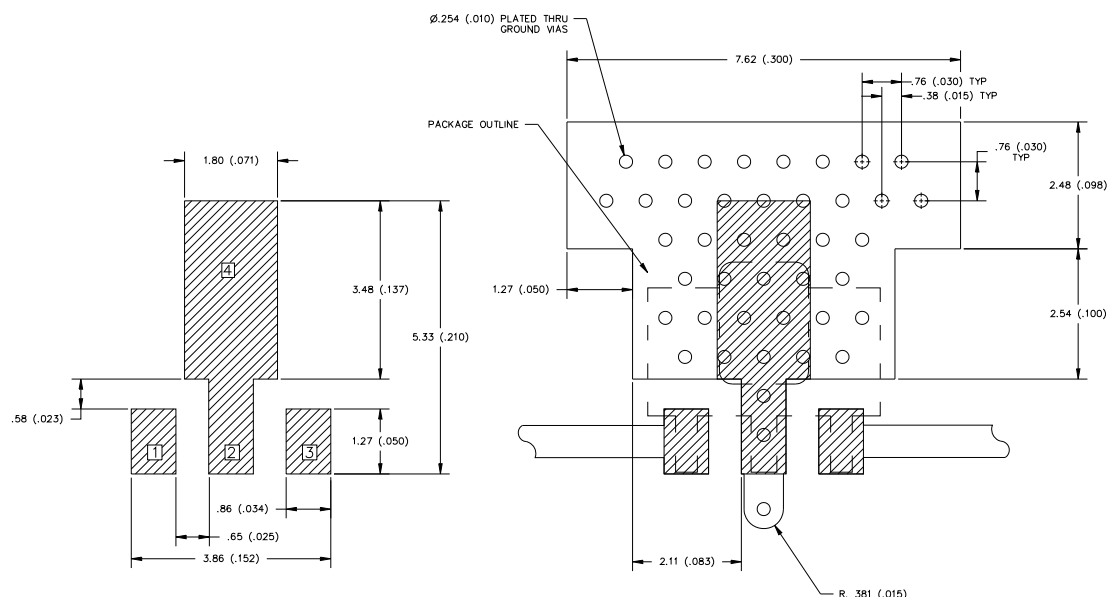
The TAT7457 will be marked with a "TAT7457" designator and an alphanumeric lot code.

| SYMBOL | MIN | NOM | MAX |
|------------------------|------|------|------|
| A - Thickness | 1.40 | 1.50 | 1.60 |
| C - Lead thickness | 0.35 | | 0.43 |
| D - Body width | 4.40 | | 4.60 |
| E1 - Body length | 2.30 | | 2.60 |
| E - Total length | 3.64 | | 4.25 |
| e - Lead spacing | 1.40 | 1.50 | 1.60 |
| e1 - Dual lead spacing | 2.90 | 3.00 | 3.10 |
| b - Outer lead width | 0.35 | | 0.48 |
| b1 - Center lead width | 0.40 | | 0.56 |
| L - Lead length | 0.74 | | 1.20 |
| d1 - Tab lead width | 1.40 | | 1.80 |
| Above body | 0.35 | | 0.64 |

DIMENSIONS ARE IN MM



Mounting Configuration



Notes:

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35 mm (#80/.0135") diameter drill and have a final, plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. RF trace width depends upon the PC board material and construction.
4. All dimensions are in millimeters (inches). Angles are in degrees.

Product Compliance Information

ESD Information



Caution! ESD-Sensitive Device

ESD Rating: Class TBD
Value: Passes \geq TBD V min.
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class TBD
Value: Passes \geq TBD V min.
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

Level x at +260 °C convection reflow
The part is rated Moisture Sensitivity Level x at TBD°C per
JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260 °C.

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

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Contact Information

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