

# RMLV0808BGSB - 4S2

8Mb Advanced LPSRAM (1024k word × 8bit)

R10DS0232EJ0201  
Rev.2.01  
2020.02.20

## Description

The RMLV0808BGSB is a family of 8-Mbit static RAMs organized 1,048,576-word × 8-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMLV0808BGSB has realized higher density, higher performance and low power consumption. The RMLV0808BGSB offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 44pin TSOP (II).

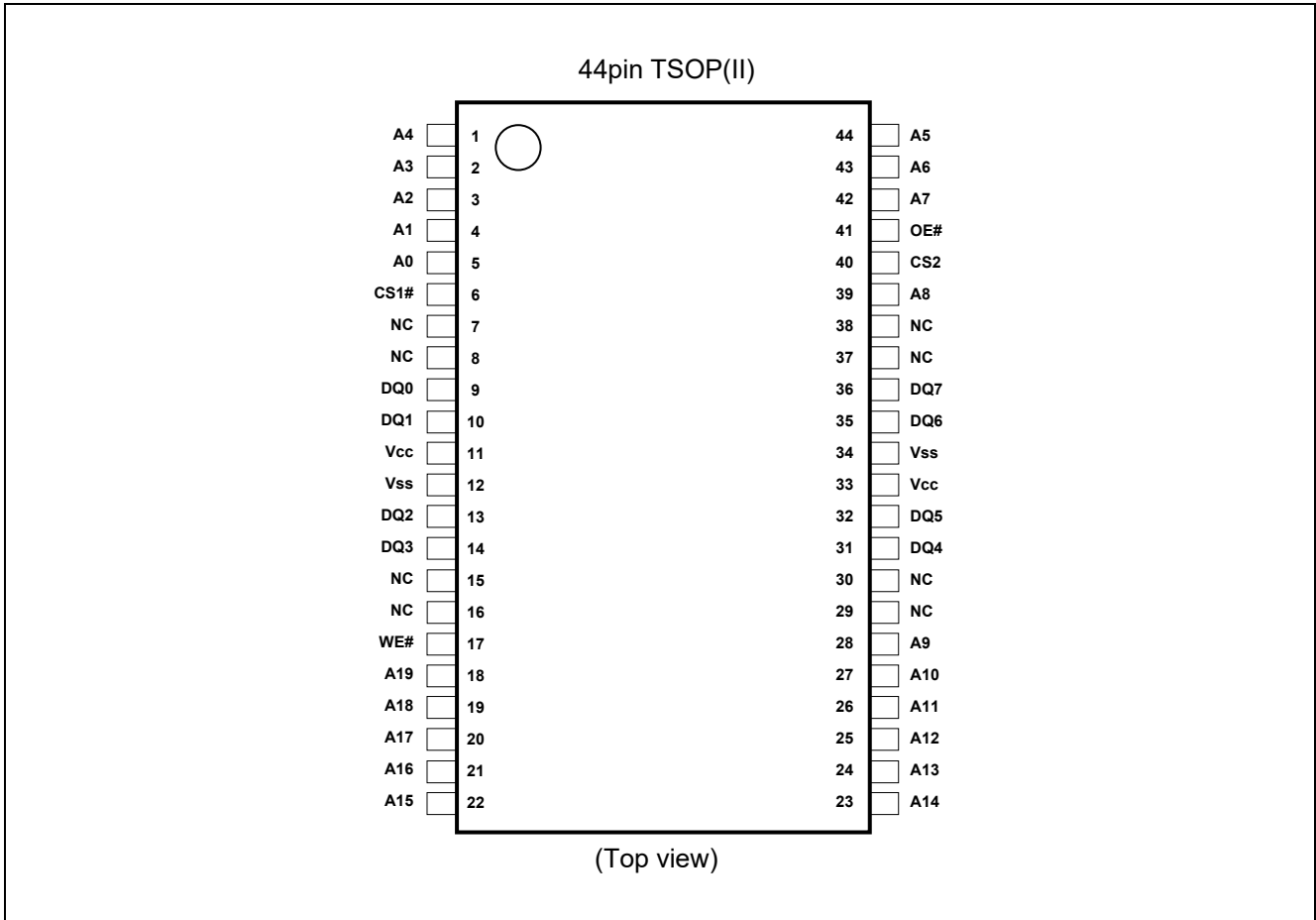
## Features

- Single 3V supply: 2.4V to 3.6V
- Access time:
  - Power supply voltage from 2.7V to 3.6V: 45ns (max.)
  - Power supply voltage from 2.4V to 2.7V: 55ns (max.)
- Current consumption:
  - Standby: 0.45μA (typ.)
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible
  - All inputs and outputs
- Battery backup operation

## Part Name Information

| Part Name        | Power supply | Access time | Temperature Range | Package                                |
|------------------|--------------|-------------|-------------------|--|
| RMLV0808BGSB-4S2 | 2.7V to 3.6V | 45 ns       | -40 ~ +85°C       | 11.76mm×18.41mm 44pin plastic TSOP(II) |
|                  | 2.4V to 2.7V | 55 ns       |                   |  |

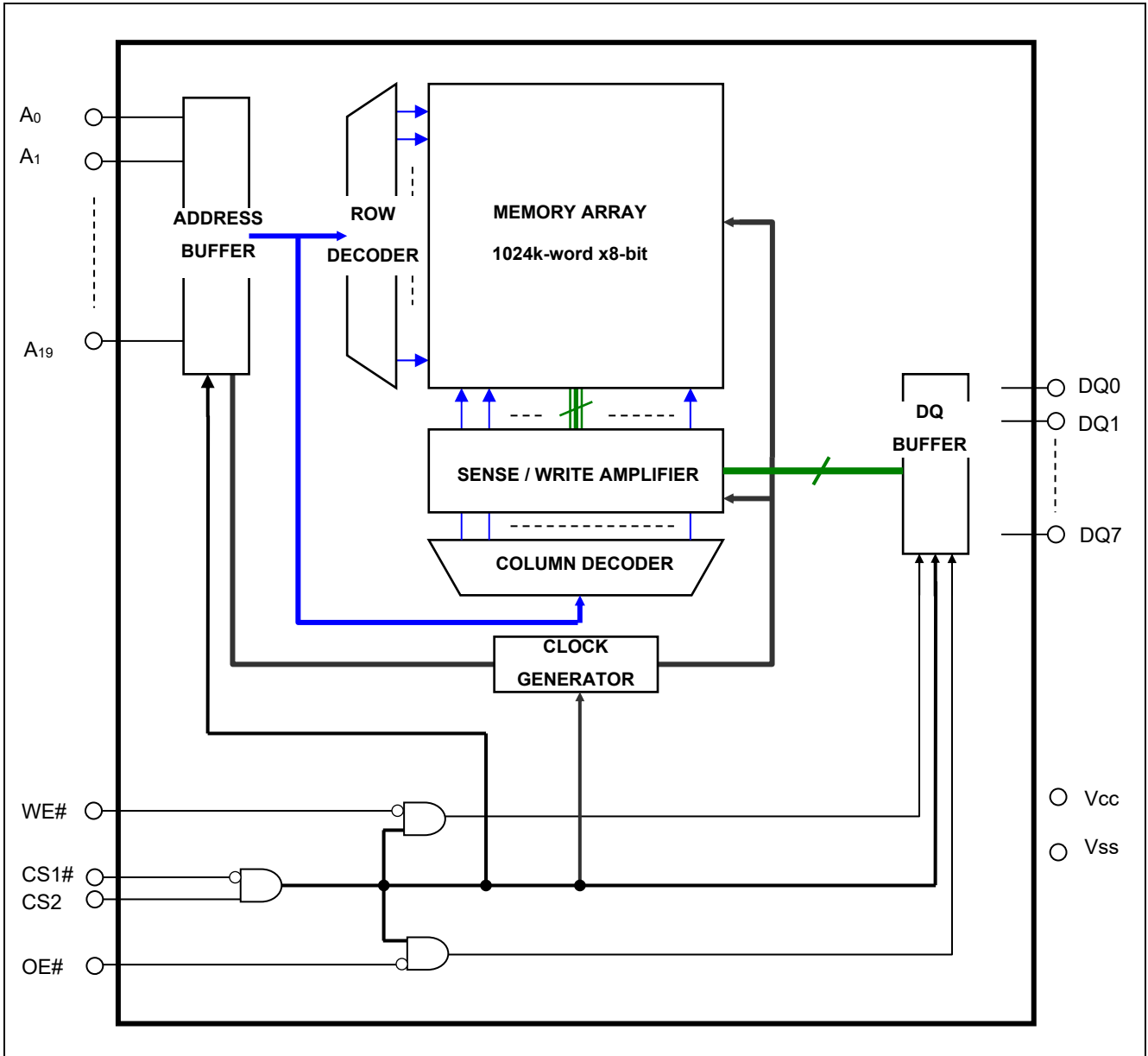
## Pin Arrangement



## Pin Description

| Pin name        | Function          |
|-----------------|-------------------|
| V <sub>CC</sub> | Power supply      |
| V <sub>SS</sub> | Ground            |
| A0 to A19       | Address input     |
| DQ0 to DQ7      | Data input/output |
| CS1#            | Chip select 1     |
| CS2             | Chip select 2     |
| OE#             | Output enable     |
| WE#             | Write enable      |
| NC              | No connection     |

### Block Diagram



### Operation Table

| CS1# | CS2 | WE# | OE# | DQ0~7  | Operation      |
|------|-----|-----|-----|--------|----------------|
| H    | X   | X   | X   | High-Z | Stand-by       |
| X    | L   | X   | X   | High-Z | Stand-by       |
| L    | H   | L   | X   | Din    | Write          |
| L    | H   | H   | L   | Dout   | Read           |
| L    | H   | H   | H   | High-Z | Output disable |

Note 1. H: V<sub>IH</sub> L: V<sub>IL</sub> X: V<sub>IH</sub> or V<sub>IL</sub>

## Absolute Maximum Ratings

| Parameter   | Symbol            | Value  | unit |
|---|-------------------|--|------|
| Power supply voltage relative to V <sub>SS</sub>        | V <sub>CC</sub>   | -0.5 to +4.6   | V    |
| Terminal voltage on any pin relative to V <sub>SS</sub> | V <sub>T</sub>    | -0.5 <sup>2</sup> to V <sub>CC</sub> +0.3 <sup>3</sup> | V    |
| Power dissipation                                       | P <sub>T</sub>    | 0.7  | W    |
| Operation temperature                                   | T <sub>opr</sub>  | -40 to +85   | °C   |
| Storage temperature range                               | T <sub>stg</sub>  | -65 to +150  | °C   |
| Storage temperature range under bias                    | T <sub>bias</sub> | -40 to +85   | °C   |

Note 2. -3.0V for pulse ≤ 30ns (full width at half maximum)

3. Maximum voltage is +4.6V.

## DC Operating Conditions

| Parameter                 | Symbol          | Min. | Typ. | Max.                 | Unit | Test conditions               | Note |
|---------------------------|-----------------|------|------|----------------------|------|-------------------------------|------|
| Supply voltage            | V <sub>CC</sub> | 2.4  | 3.0  | 3.6                  | V    |                               |      |
|                           | V <sub>SS</sub> | 0    | 0    | 0                    | V    |                               |      |
| Input high voltage        | V <sub>IH</sub> | 2.0  | —    | V <sub>CC</sub> +0.2 | V    | V <sub>CC</sub> =2.4V to 2.7V |      |
|                           |                 | 2.2  | —    | V <sub>CC</sub> +0.2 | V    | V <sub>CC</sub> =2.7V to 3.6V |      |
| Input low voltage         | V <sub>IL</sub> | -0.2 | —    | 0.4                  | V    | V <sub>CC</sub> =2.4V to 2.7V | 4    |
|                           |                 | -0.2 | —    | 0.6                  | V    | V <sub>CC</sub> =2.7V to 3.6V | 4    |
| Ambient temperature range | T <sub>a</sub>  | -40  | —    | +85                  | °C   |                               |      |

Note 4. -3.0V for pulse ≤ 30ns (full width at half maximum)

## DC Characteristics

| Parameter                 | Symbol           | Min. | Typ.               | Max. | Unit | Test conditions   |
|---------------------------|------------------|------|--------------------|------|------|---|
| Input leakage current     | I <sub>LI</sub>  | —    | —                  | 1    | μA   | V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>  |
| Output leakage current    | I <sub>LO</sub>  | —    | —                  | 1    | μA   | CS1# = V <sub>IH</sub> or CS2 = V <sub>IL</sub> or OE# = V <sub>IH</sub> or WE# = V <sub>IL</sub> , V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>   |
| Average operating current | I <sub>CC1</sub> | —    | 20 <sup>*5</sup>   | 25   | mA   | Cycle = 55ns, duty = 100%, I <sub>I/O</sub> = 0mA, CS1# = V <sub>IL</sub> , CS2 = V <sub>IH</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub>               |
|                           |                  | —    | 25 <sup>*5</sup>   | 30   | mA   | Cycle = 45ns, duty = 100%, I <sub>I/O</sub> = 0mA, CS1# = V <sub>IL</sub> , CS2 = V <sub>IH</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub>               |
|                           | I <sub>CC2</sub> | —    | 1.5 <sup>*5</sup>  | 3    | mA   | Cycle = 1μs, duty = 100%, I <sub>I/O</sub> = 0mA, CS1# ≤ 0.2V, CS2 ≥ V <sub>CC</sub> -0.2V, V <sub>IH</sub> ≥ V <sub>CC</sub> -0.2V, V <sub>IL</sub> ≤ 0.2V |
| Standby current           | I <sub>SB</sub>  | —    | —                  | 0.3  | mA   | CS2 = V <sub>IL</sub> , Others = V <sub>SS</sub> to V <sub>CC</sub>   |
| Standby current           | I <sub>SB1</sub> | —    | 0.45 <sup>*5</sup> | 2    | μA   | ~+25°C  |
|                           |                  | —    | 0.6 <sup>*6</sup>  | 4    | μA   | ~+40°C  |
|                           |                  | —    | —                  | 7    | μA   | ~+70°C  |
|                           |                  | —    | —                  | 10   | μA   | ~+85°C  |
| Output high voltage       | V <sub>OH</sub>  | 2.4  | —                  | —    | V    | I <sub>OH</sub> = -1mA<br>V <sub>CC</sub> ≥ 2.7V  |
|                           | V <sub>OH2</sub> | 2.0  | —                  | —    | V    | I <sub>OH</sub> = -0.1mA  |
| Output low voltage        | V <sub>OL</sub>  | —    | —                  | 0.4  | V    | I <sub>OL</sub> = 2mA<br>V <sub>CC</sub> ≥ 2.7V   |
|                           | V <sub>OL2</sub> | —    | —                  | 0.4  | V    | I <sub>OL</sub> = 0.1mA   |

Note 5. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub>=25°C), and not 100% tested.

Note 6. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub>=40°C), and not 100% tested.

## Capacitance

(Ta =25°C, f =1MHz)

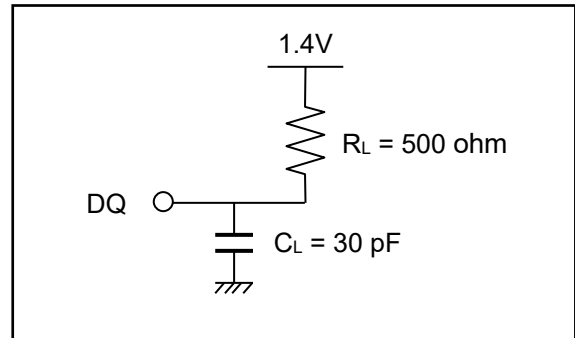
| Parameter                  | Symbol           | Min. | Typ. | Max. | Unit | Test conditions      | Note |
|----------------------------|------------------|------|------|------|------|----------------------|------|
| Input capacitance          | C <sub>in</sub>  | —    | —    | 8    | pF   | V <sub>in</sub> =0V  | 7    |
| Input / output capacitance | C <sub>I/O</sub> | —    | —    | 10   | pF   | V <sub>I/O</sub> =0V | 7    |

Note 7. This parameter is sampled and not 100% tested.

## AC Characteristics

Test Conditions (V<sub>cc</sub> = 2.4V ~ 3.6V, Ta = -40 ~ +85°C)

- Input pulse levels:
  - V<sub>IL</sub> = 0.4V, V<sub>IH</sub> = 2.4V (V<sub>cc</sub>=2.7V to 3.6V)
  - V<sub>IL</sub> = 0.4V, V<sub>IH</sub> = 2.2V (V<sub>cc</sub>=2.4V to 2.7V)
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



## Read Cycle

| Parameter                          | Symbol            | V <sub>cc</sub> =2.7V to 3.6V |      | V <sub>cc</sub> =2.4V to 2.7V |      | Unit | Note   |
|------------------------------------|-------------------|-------------------------------|------|-------------------------------|------|------|--------|
|                                    |                   | Min.                          | Max. | Min.                          | Max. |      |        |
| Read cycle time                    | t <sub>RC</sub>   | 45                            | —    | 55                            | —    | ns   |        |
| Address access time                | t <sub>AA</sub>   | —                             | 45   | —                             | 55   | ns   |        |
| Chip select access time            | t <sub>ACS1</sub> | —                             | 45   | —                             | 55   | ns   |        |
|                                    | t <sub>ACS2</sub> | —                             | 45   | —                             | 55   | ns   |        |
| Output enable to output valid      | t <sub>OE</sub>   | —                             | 22   | —                             | 30   | ns   |        |
| Output hold from address change    | t <sub>OH</sub>   | 10                            | —    | 10                            | —    | ns   |        |
| Chip select to output in low-Z     | t <sub>CLZ1</sub> | 10                            | —    | 10                            | —    | ns   | 8,9    |
|                                    | t <sub>CLZ2</sub> | 10                            | —    | 10                            | —    | ns   | 8,9    |
| Output enable to output in low-Z   | t <sub>OLZ</sub>  | 5                             | —    | 5                             | —    | ns   | 8,9    |
| Chip deselect to output in high-Z  | t <sub>CHZ1</sub> | 0                             | 18   | 0                             | 20   | ns   | 8,9,10 |
|                                    | t <sub>CHZ2</sub> | 0                             | 18   | 0                             | 20   | ns   | 8,9,10 |
| Output disable to output in high-Z | t <sub>OHZ</sub>  | 0                             | 18   | 0                             | 20   | ns   | 8,9,10 |

Note 8. This parameter is sampled and not 100% tested.

- At any given temperature and voltage condition, t<sub>CHZ1</sub> max is less than t<sub>CLZ1</sub> min, t<sub>CHZ2</sub> max is less than t<sub>CLZ2</sub> min, and t<sub>OHZ</sub> max is less than t<sub>OLZ</sub> min, for any device.
- t<sub>CHZ1</sub>, t<sub>CHZ2</sub> and t<sub>OHZ</sub> are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

## Write Cycle

| Parameter                          | Symbol           | Vcc=2.7V to 3.6V |      | Vcc=2.4V to 2.7V |      | Unit | Note  |
|------------------------------------|------------------|------------------|------|------------------|------|------|-------|
|                                    |                  | Min.             | Max. | Min.             | Max. |      |       |
| Write cycle time                   | t <sub>WC</sub>  | 45               | —    | 55               | —    | ns   |       |
| Address valid to write end         | t <sub>AW</sub>  | 35               | —    | 50               | —    | ns   |       |
| Chip select to write end           | t <sub>CW</sub>  | 35               | —    | 50               | —    | ns   |       |
| Write pulse width                  | t <sub>WP</sub>  | 35               | —    | 40               | —    | ns   | 11    |
| Address setup time to write start  | t <sub>AS</sub>  | 0                | —    | 0                | —    | ns   |       |
| Write recovery time from write end | t <sub>WR</sub>  | 0                | —    | 0                | —    | ns   |       |
| Data to write time overlap         | t <sub>DW</sub>  | 25               | —    | 25               | —    | ns   |       |
| Data hold from write end           | t <sub>DH</sub>  | 0                | —    | 0                | —    | ns   |       |
| Output enable from write end       | t <sub>OW</sub>  | 5                | —    | 5                | —    | ns   | 12    |
| Output disable to output in high-Z | t <sub>OHZ</sub> | 0                | 18   | 0                | 20   | ns   | 12,13 |
| Write to output in high-Z          | t <sub>WHZ</sub> | 0                | 18   | 0                | 20   | ns   | 12,13 |

Note 11. t<sub>WP</sub> is the interval between write start and write end.

A write starts when all of (CS1#), (WE#) and (CS2) become active.

A write is performed during the overlap of a low CS1#, a low WE# and a high CS2.

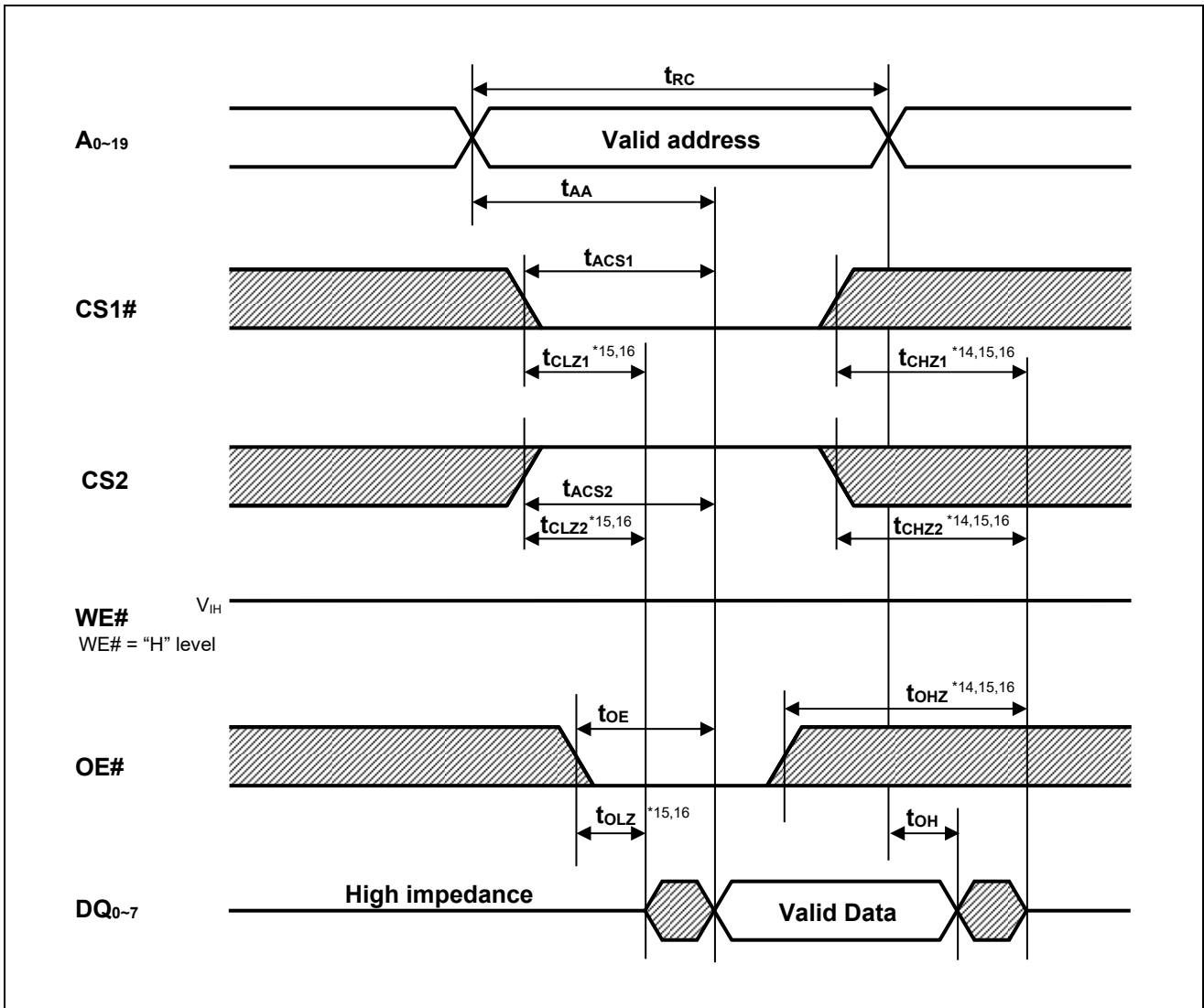
A write ends when any of (CS1#), (WE#) or (CS2) becomes inactive.

12. This parameter is sampled and not 100% tested.

13. t<sub>OHZ</sub> and t<sub>WHZ</sub> are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

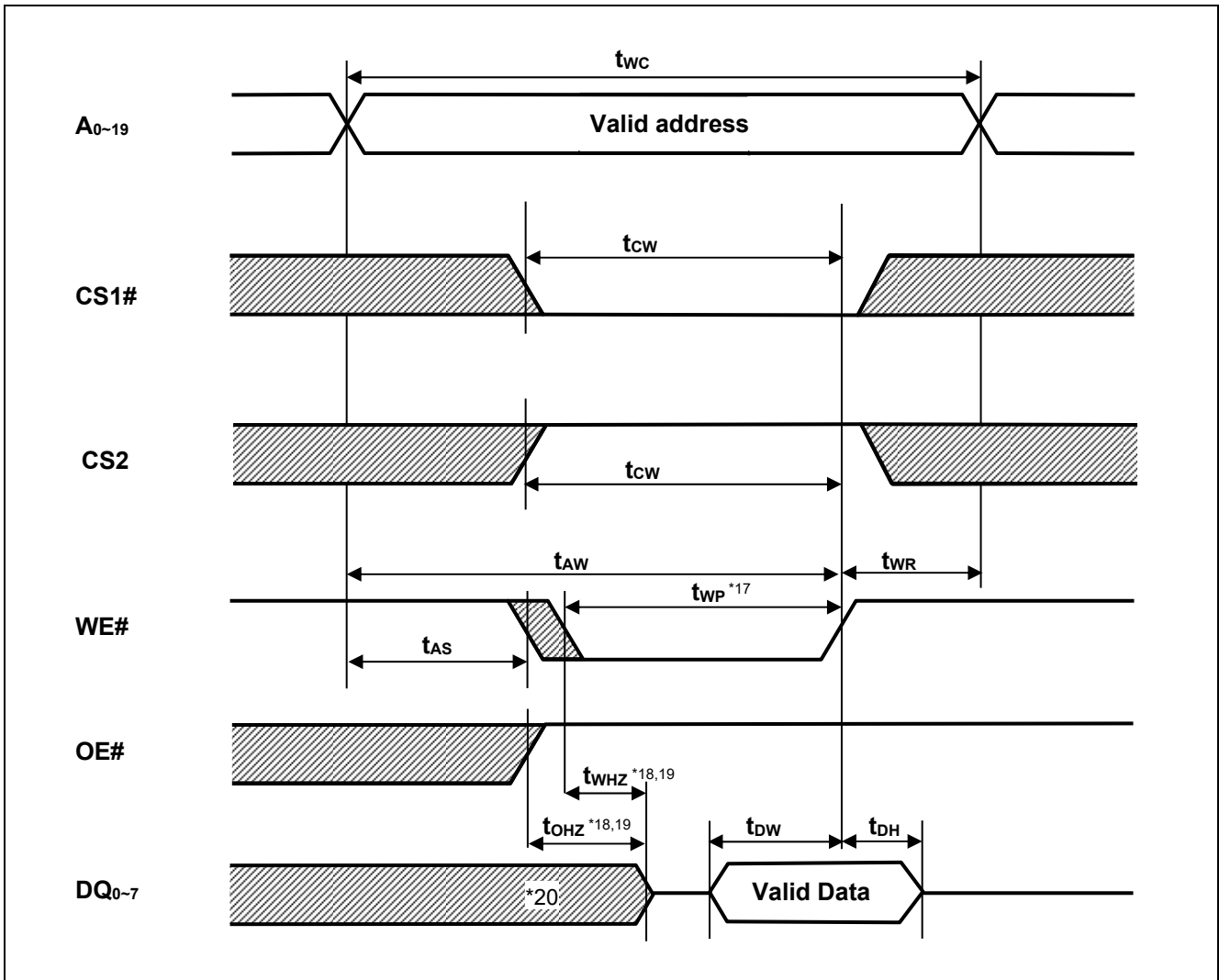
## Timing Waveforms

### Read Cycle



- Note 14.  $t_{CHZ1}$ ,  $t_{CHZ2}$  and  $t_{OHZ}$  are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.
15. This parameter is sampled and not 100% tested
16. At any given temperature and voltage condition,  $t_{CHZ1}$  max is less than  $t_{CLZ1}$  min,  $t_{CHZ2}$  max is less than  $t_{CLZ2}$  min, and  $t_{OHZ}$  max is less than  $t_{OLZ}$  min, for any device.

Write Cycle (1) (WE# CLOCK, OE#="H" while writing)



Note 17.  $t_{WP}$  is the interval between write start and write end.

A write starts when all of (CS1#), (WE#) and (CS2) become active.

A write is performed during the overlap of a low CS1#, a low WE# and a high CS2.

A write ends when any of (CS1#), (WE#) or (CS2) becomes inactive.

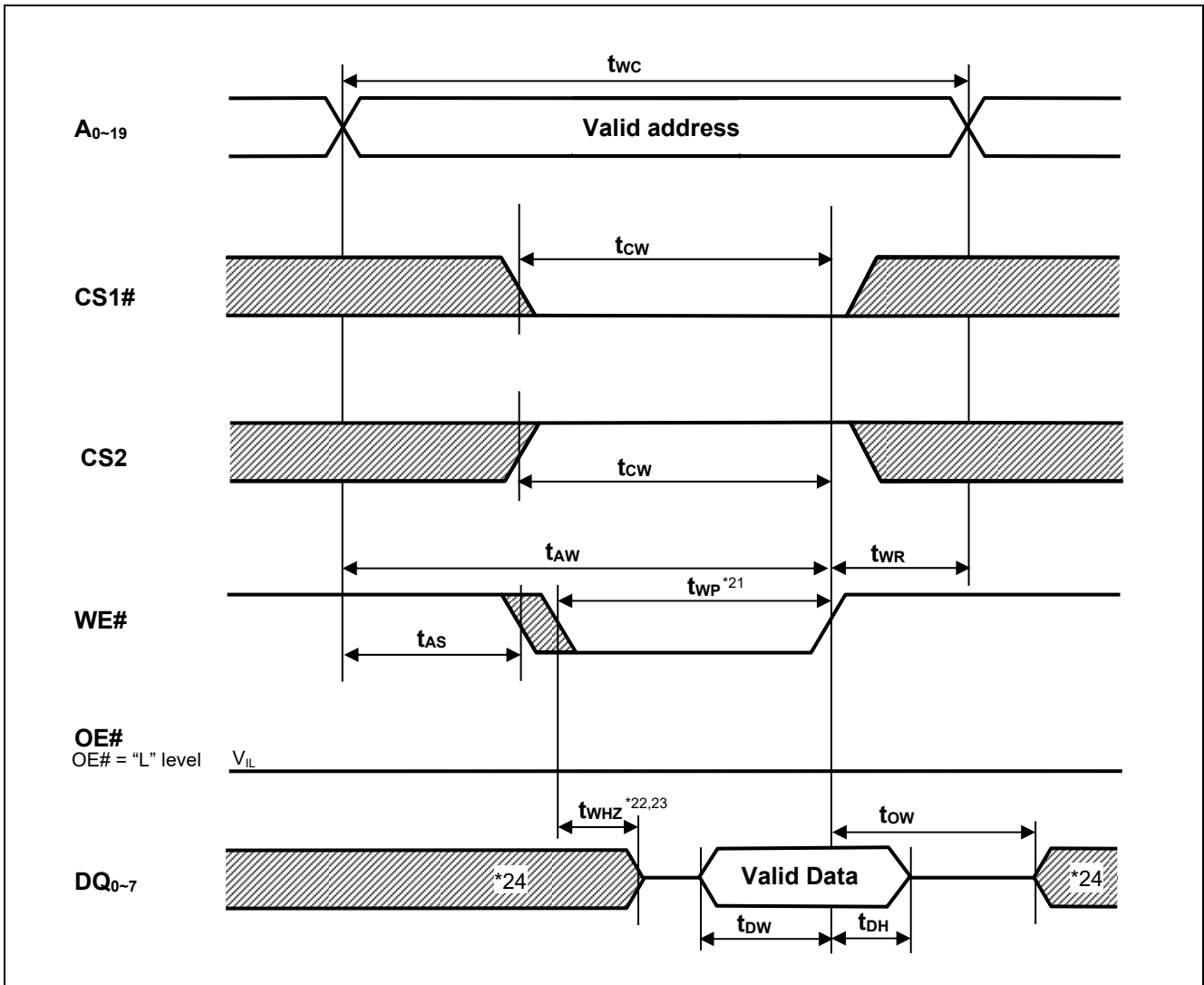
18.  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

19. This parameter is sampled and not 100% tested

20. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

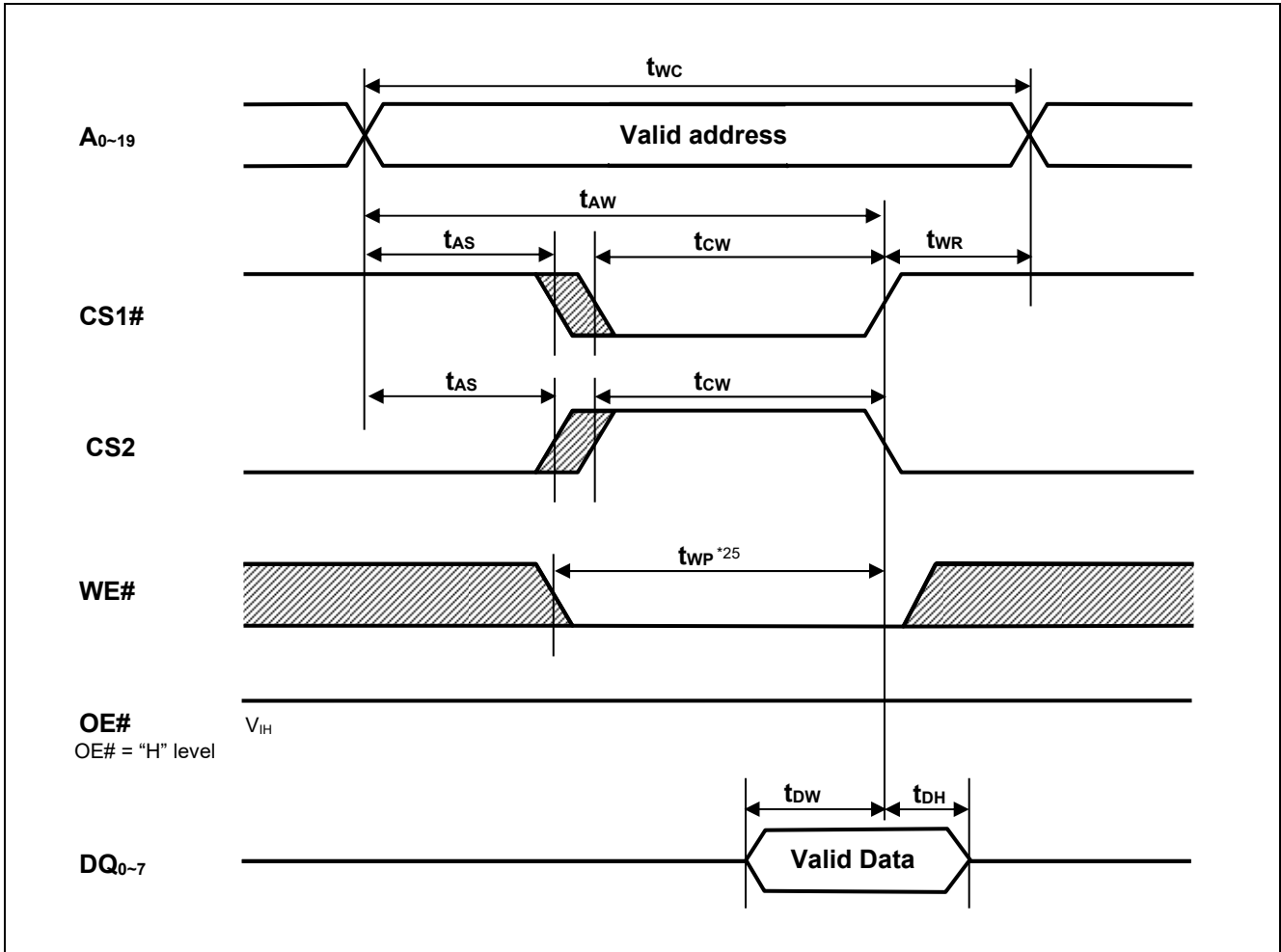


Write Cycle (2) (WE# CLOCK, OE# Low Fixed)



- Note 21.  $t_{WP}$  is the interval between write start and write end.  
 A write starts when all of (CS1#), (WE#) and (CS2) become active.  
 A write is performed during the overlap of a low CS1#, a low WE# and a high CS2.  
 A write ends when any of (CS1#), (WE#) or (CS2) becomes inactive.
22.  $t_{WHZ}$  is defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.
23. This parameter is sampled and not 100% tested.
24. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (3) (CS1#, CS2 CLOCK)



Note 25.  $t_{WP}$  is the interval between write start and write end.  
 A write starts when all of (CS1#), (WE#) and (CS2) become active.  
 A write is performed during the overlap of a low CS1#, a low WE# and a high CS2.  
 A write ends when any of (CS1#), (WE#) or (CS2) becomes inactive.

Low V<sub>CC</sub> Data Retention Characteristics

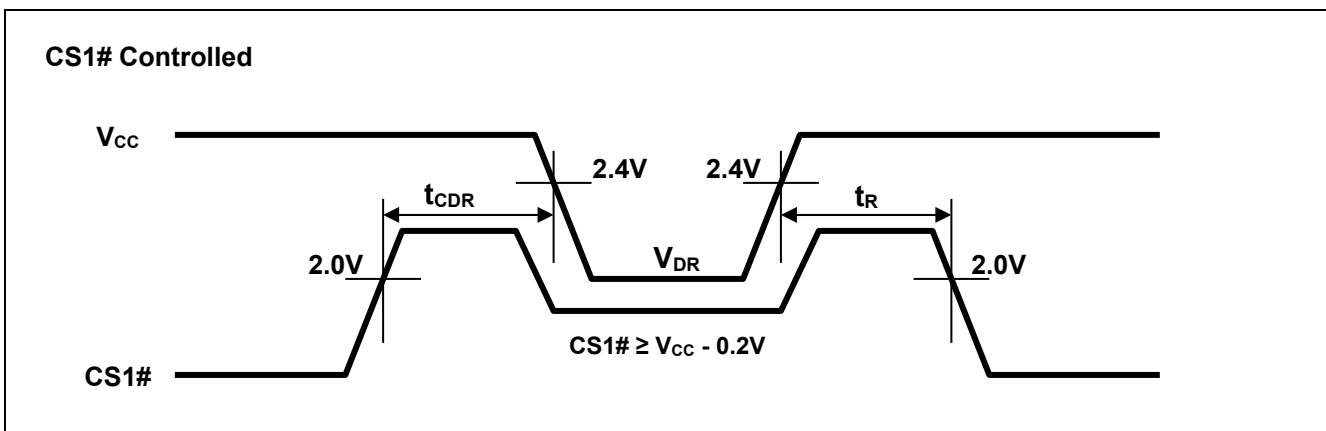
| Parameter                            | Symbol            | Min. | Typ.                | Max. | Unit | Test conditions <sup>*28</sup>  |
|--------------------------------------|-------------------|------|---------------------|------|------|---|
| V <sub>CC</sub> for data retention   | V <sub>DR</sub>   | 1.5  | —                   | 3.6  | V    | V <sub>in</sub> ≥ 0V,<br>(1) CS2 ≤ 0.2V or<br>(2) CS1# ≥ V <sub>CC</sub> -0.2V, CS2 ≥ V <sub>CC</sub> -0.2V |
| Data retention current               | I <sub>CCDR</sub> | —    | 0.45 <sup>*26</sup> | 2    | μA   | ~+25°C  |
|                                      |                   | —    | 0.6 <sup>*27</sup>  | 4    | μA   | ~+40°C  |
|                                      |                   | —    | —                   | 7    | μA   | ~+70°C  |
|                                      |                   | —    | —                   | 10   | μA   | ~+85°C  |
| Chip deselect time to data retention | t <sub>CDR</sub>  | 0    | —                   | —    | ns   | See retention waveform.   |
| Operation recovery time              | t <sub>R</sub>    | 5    | —                   | —    | ms   |   |

Note 26. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub>=25°C), and not 100% tested.

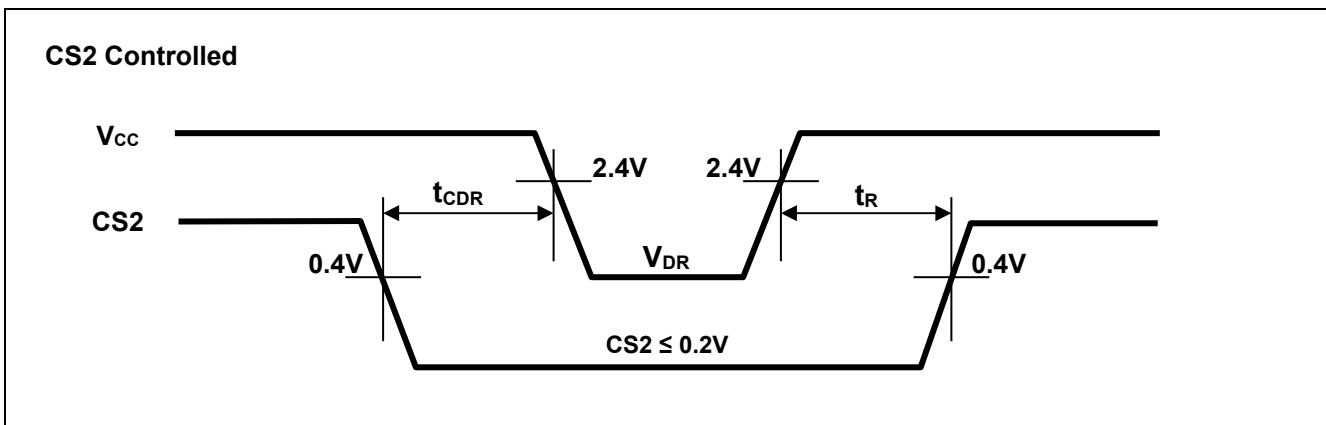
27. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub>=40°C), and not 100% tested.

28. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer and DQ buffer. If CS2 controls data retention mode, V<sub>in</sub> levels (address, WE#, CS1#, OE#, DQ) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 ≥ V<sub>CC</sub>-0.2V or CS2 ≤ 0.2V. The other inputs levels (address, WE#, OE#, DQ) can be in the high-impedance state.

Low V<sub>CC</sub> Data Retention Timing Waveforms (CS1# controlled)



Low V<sub>CC</sub> Data Retention Timing Waveforms (CS2 controlled)



|                  |                         |
|------------------|-------------------------|
| Revision History | RMLV0808BGSB Data Sheet |
|------------------|-------------------------|

| Rev. | Date       | Description                  |   |
|------|------------|------------------------------|---|
|      |            | Page                         | Summary   |
| 1.00 | 2014.11.28 | —                            | First Edition issued  |
| 2.00 | 2015.06.26 | P.1, 4<br>P.2<br>P.4<br>P.11 | Standby current $I_{SB1}$ : 25°C 0.6μA ->0.45μA (typ.), 40°C 2μA ->0.6μA (typ.)<br>Modify Pin Arrangement : Add 1pin Mark<br>Average operating current $I_{CC2}$ : 25°C 2mA ->1.5mA (typ.)<br>Data retention current $I_{CCDR}$ : 25°C 0.6μA ->0.45μA (typ.), 40°C 2μA ->0.6μA (typ.) |
| 2.01 | 2020.02.20 | Last page                    | Updated the Notice to the latest version  |
|      |            |                              |   |

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(Rev.1.0 Mar 2020)

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(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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