

# 74AVC8T245

## 8-bit dual supply translating transceiver with configurable voltage translation; 3-state

Rev. 6 — 31 March 2020

Product data sheet

### 1. General description

The 74AVC8T245 is an 8-bit, dual supply transceiver that enables bidirectional level translation. It features two 8-bit input-output ports (An and Bn), a direction control input (DIR), a output enable input ( $\overline{OE}$ ) and dual supply pins ( $V_{CC(A)}$  and  $V_{CC(B)}$ ). Both  $V_{CC(A)}$  and  $V_{CC(B)}$  can be supplied at any voltage between 0.8 V and 3.6 V making the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V). Pins An,  $\overline{OE}$  and DIR are referenced to  $V_{CC(A)}$  and pins Bn are referenced to  $V_{CC(B)}$ . A HIGH on DIR allows transmission from An to Bn and a LOW on DIR allows transmission from Bn to An. The output enable input ( $\overline{OE}$ ) can be used to disable the outputs so the buses are effectively isolated.

The device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either  $V_{CC(A)}$  or  $V_{CC(B)}$  are at GND level, both An and Bn are in the high-impedance OFF-state.

### 2. Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$ : 0.8 V to 3.6 V
  - $V_{CC(B)}$ : 0.8 V to 3.6 V
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114E Class 3B exceeds 8000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101C exceeds 1000 V
- Maximum data rates:
  - 380 Mbit/s ( $\geq 1.8$  V to 3.3 V translation)
  - 260 Mbit/s ( $\geq 1.1$  V to 3.3 V translation)
  - 260 Mbit/s ( $\geq 1.1$  V to 2.5 V translation)
  - 210 Mbit/s ( $\geq 1.1$  V to 1.8 V translation)
  - 150 Mbit/s ( $\geq 1.1$  V to 1.5 V translation)
  - 100 Mbit/s ( $\geq 1.1$  V to 1.2 V translation)
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AVC8T245PW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74AVC8T245BQ	-40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm	SOT815-1

### 4. Functional diagram

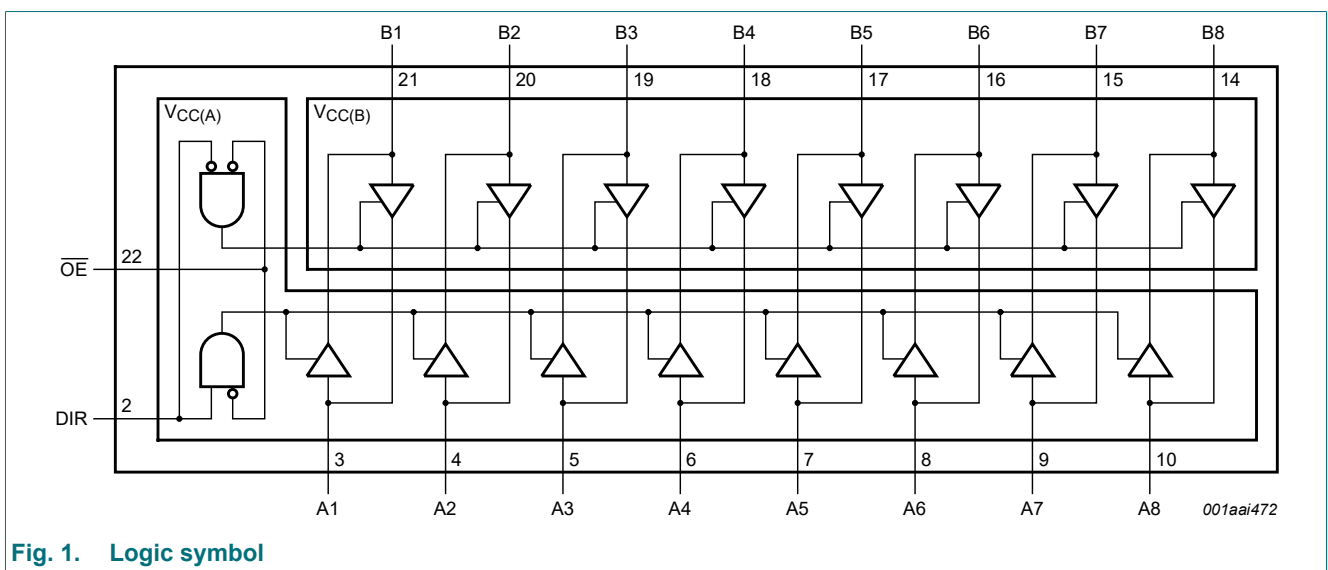


Fig. 1. Logic symbol

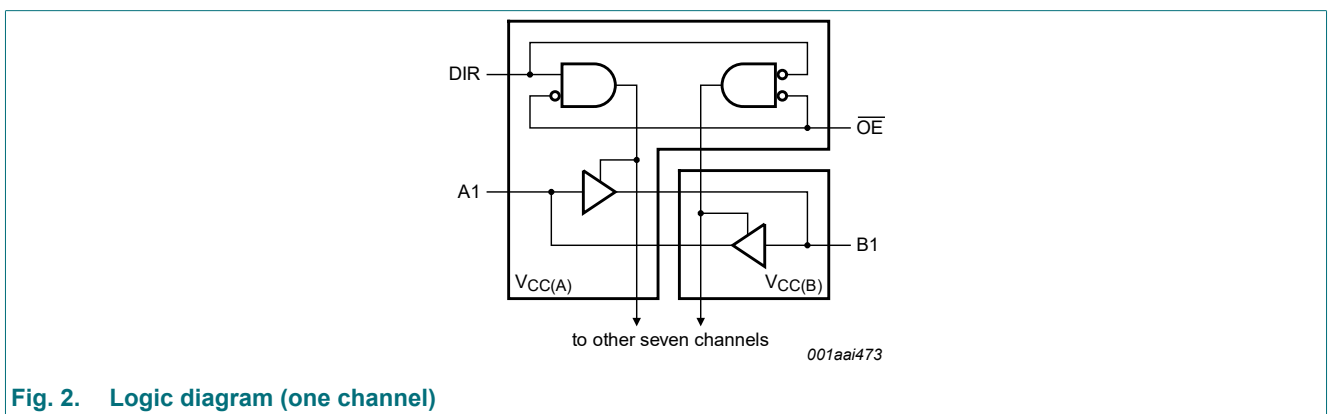


Fig. 2. Logic diagram (one channel)

## 5. Pinning information

### 5.1. Pinning

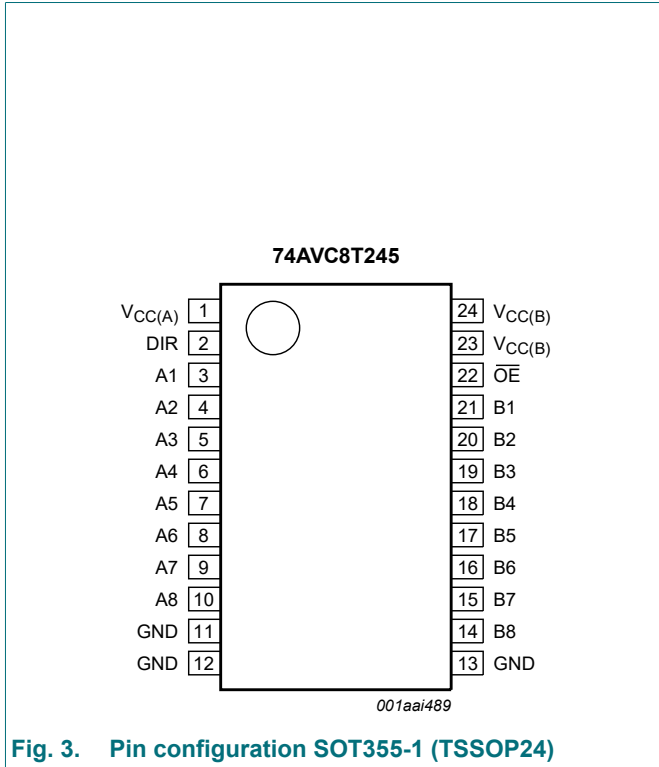


Fig. 3. Pin configuration SOT355-1 (TSSOP24)

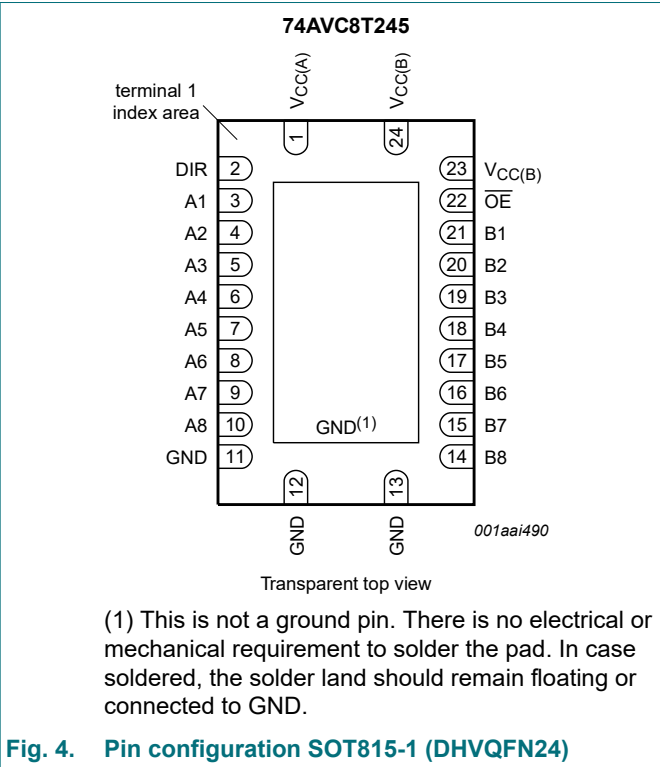


Fig. 4. Pin configuration SOT815-1 (DHVQFN24)

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
V <sub>CC(A)</sub>	1	supply voltage A (An, OE and DIR inputs are referenced to V <sub>CC(A)</sub> )
DIR	2	direction control
A1, A2, A3, A4, A5, A6, A7, A8	3, 4, 5, 6, 7, 8, 9, 10	data input or output
GND [1]	11, 12, 13	ground (0 V)
B1, B2, B3, B4, B5, B6, B7, B8	21, 20, 19, 18, 17, 16, 15, 14	data input or output
OE	22	output enable input (active LOW)
V <sub>CC(B)</sub>	23, 24	supply voltage B (Bn inputs are referenced to V <sub>CC(B)</sub> )

[1] All GND pins must be connected to ground (0 V).

## 6. Functional description

**Table 3. Function table**

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Supply voltage	Input		Input/output [1]	
$V_{CC(A)}$ , $V_{CC(B)}$	OE [2]	DIR [2]	An [2]	Bn
0.8 V to 3.6 V	L	L	An = Bn	input
0.8 V to 3.6 V	L	H	input	Bn = An
0.8 V to 3.6 V	H	X	Z	Z
GND [1]	X	X	Z	Z

[1] If at least one of  $V_{CC(A)}$  or  $V_{CC(B)}$  is at GND level, the device goes into suspend mode.

[2] The An, DIR and OE input circuit is referenced to  $V_{CC(A)}$ ; The Bn input circuit is referenced to  $V_{CC(B)}$ .

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+4.6	V
$V_{CC(B)}$	supply voltage B		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage	[1]	-0.5	+4.6	V
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$V_O$	output voltage	Active mode [1] [2] [3]	-0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode [1]	-0.5	+4.6	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current	per $V_{CC(A)}$ or $V_{CC(B)}$ pin	-	100	mA
$I_{GND}$	ground current	per GND pin	-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C [4]	-	500	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $V_{CCO}$  is the supply voltage associated with the output port.

[3]  $V_{CCO} + 0.5$  V should not exceed 4.6 V.

[4] For SOT355-1 (TSSOP24) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C.  
For SOT815-1 (DHVQFN24) package:  $P_{tot}$  derates linearly with 15.0 mW/K above 117 °C.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		0.8	3.6	V
$V_{CC(B)}$	supply voltage B		0.8	3.6	V
$V_I$	input voltage		0	3.6	V
$V_O$	output voltage	Active mode [1]	0	$V_{CCO}$	V
		Suspend or 3-state mode	0	3.6	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CCI} = 0.8\text{ V to }3.6\text{ V}$ [2]	-	5	ns/V

[1]  $V_{CCO}$  is the supply voltage associated with the output port.

[2]  $V_{CCI}$  is the supply voltage associated with the input port.

## 9. Static characteristics

Table 6. Typical static characteristics at  $T_{amb} = 25\text{ °C}$

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

$V_{CCI}$  is the supply voltage associated with the data input port;  $V_{CCO}$  is the supply voltage associated with the output port.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $I_O = -1.5\text{ mA}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V}$	-	0.69	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 1.5\text{ mA}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V}$	-	0.07	-	V
$I_I$	input leakage current	DIR, $\overline{OE}$ input; $V_I = 0\text{ V or }3.6\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V to }3.6\text{ V}$	-	$\pm 0.025$	$\pm 0.25$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	A or B port; $V_O = 0\text{ V or }V_{CCO}$ ; $V_{CC(A)} = V_{CC(B)} = 3.6\text{ V}$ [1]	-	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
		suspend mode A port; $V_O = 0\text{ V or }V_{CCO}$ ; $V_{CC(A)} = 3.6\text{ V}$ ; $V_{CC(B)} = 0\text{ V}$ [1]	-	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
		suspend mode B port; $V_O = 0\text{ V or }V_{CCO}$ ; $V_{CC(A)} = 0\text{ V}$ ; $V_{CC(B)} = 3.6\text{ V}$ [1]	-	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	A port; $V_I$ or $V_O = 0\text{ V to }3.6\text{ V}$ ; $V_{CC(A)} = 0\text{ V}$ ; $V_{CC(B)} = 0.8\text{ V to }3.6\text{ V}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
		B port; $V_I$ or $V_O = 0\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 0\text{ V}$ ; $V_{CC(A)} = 0.8\text{ V to }3.6\text{ V}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
$C_I$	input capacitance	DIR, $\overline{OE}$ input; $V_I = 0\text{ V or }3.3\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$	-	1.5	-	pF
$C_{I/O}$	input/output capacitance	A and B port; $V_O = 3.3\text{ V or }0\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$	-	4.3	-	pF

[1] For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

## 8-bit dual supply translating transceiver with configurable voltage translation; 3-state

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

$V_{CCI}$  is the supply voltage associated with the data input port;  $V_{CCO}$  is the supply voltage associated with the output port.

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	data input					
		$V_{CCI} = 0.8\text{ V}$	$0.70V_{CCI}$	-	$0.70V_{CCI}$	-	V
		$V_{CCI} = 1.1\text{ V to }1.95\text{ V}$	$0.65V_{CCI}$	-	$0.65V_{CCI}$	-	V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$	1.6	-	1.6	-	V
		$V_{CCI} = 3.0\text{ V to }3.6\text{ V}$	2	-	2	-	V
		DIR, $\overline{OE}$ input					
		$V_{CC(A)} = 0.8\text{ V}$	$0.70V_{CC(A)}$	-	$0.70V_{CC(A)}$	-	V
		$V_{CC(A)} = 1.1\text{ V to }1.95\text{ V}$	$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
		$V_{CC(A)} = 2.3\text{ V to }2.7\text{ V}$	1.6	-	1.6	-	V
$V_{CC(A)} = 3.0\text{ V to }3.6\text{ V}$	2	-	2	-	V		
$V_{IL}$	LOW-level input voltage	data input					
		$V_{CCI} = 0.8\text{ V}$	-	$0.30V_{CCI}$	-	$0.30V_{CCI}$	V
		$V_{CCI} = 1.1\text{ V to }1.95\text{ V}$	-	$0.35V_{CCI}$	-	$0.35V_{CCI}$	V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$	-	0.7	-	0.7	V
		$V_{CCI} = 3.0\text{ V to }3.6\text{ V}$	-	0.8	-	0.8	V
		DIR, $\overline{OE}$ input					
		$V_{CC(A)} = 0.8\text{ V}$	-	$0.30V_{CC(A)}$	-	$0.30V_{CC(A)}$	V
		$V_{CC(A)} = 1.1\text{ V to }1.95\text{ V}$	-	$0.35V_{CC(A)}$	-	$0.35V_{CC(A)}$	V
		$V_{CC(A)} = 2.3\text{ V to }2.7\text{ V}$	-	0.7	-	0.7	V
$V_{CC(A)} = 3.0\text{ V to }3.6\text{ V}$	-	0.8	-	0.8	V		
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$					
		$I_O = -100\text{ }\mu\text{A};$ $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V to }3.6\text{ V}$	$V_{CCO} - 0.1$	-	$V_{CCO} - 0.1$	-	V
		$I_O = -3\text{ mA};$ $V_{CC(A)} = V_{CC(B)} = 1.1\text{ V}$	0.85	-	0.85	-	V
		$I_O = -6\text{ mA};$ $V_{CC(A)} = V_{CC(B)} = 1.4\text{ V}$	1.05	-	1.05	-	V
		$I_O = -8\text{ mA};$ $V_{CC(A)} = V_{CC(B)} = 1.65\text{ V}$	1.2	-	1.2	-	V
		$I_O = -9\text{ mA};$ $V_{CC(A)} = V_{CC(B)} = 2.3\text{ V}$	1.75	-	1.75	-	V
		$I_O = -12\text{ mA};$ $V_{CC(A)} = V_{CC(B)} = 3.0\text{ V}$	2.3	-	2.3	-	V

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Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = 100 μA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	0.1	-	0.1	V
		I <sub>O</sub> = 3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	-	0.25	-	0.25	V
		I <sub>O</sub> = 6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	-	0.35	-	0.35	V
		I <sub>O</sub> = 8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	-	0.45	-	0.45	V
		I <sub>O</sub> = 9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	-	0.55	-	0.55	V
		I <sub>O</sub> = 12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	-	0.7	-	0.7	V
I <sub>I</sub>	input leakage current	DIR, $\overline{OE}$ input; V <sub>I</sub> = 0 V or 3.6 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±1	-	±5	μA
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.6 V [1]	-	±5	-	±30	μA
		suspend mode A port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V [1]	-	±5	-	±30	μA
		suspend mode B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V [1]	-	±5	-	±30	μA
I <sub>OFF</sub>	power-off leakage current	A port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±5	-	±30	μA
		B port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(B)</sub> = 0 V; V <sub>CC(A)</sub> = 0.8 V to 3.6 V	-	±5	-	±30	μA

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Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I <sub>CC</sub>	supply current	A port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
		V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	10	-	55	μA
		V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	8	-	50	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	8	-	50	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-2	-	-12	-	μA
		B port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
		V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	10	-	55	μA
		V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	8	-	50	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-2	-	-12	-	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-	8	-	50	μA
		A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	20	-	70	μA
		A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	16	-	65	μA

[1] For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

Table 8. Typical total supply current (I<sub>CC(A)</sub> + I<sub>CC(B)</sub>)

V <sub>CC(A)</sub>	V <sub>CC(B)</sub>							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	μA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	μA
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	μA
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	μA
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	μA
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	μA
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	μA



## 10. Dynamic characteristics

**Table 9. Typical dynamic characteristics at  $V_{CC(A)} = 0.8\text{ V}$  and  $T_{amb} = 25\text{ °C}$**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for wave forms see Fig. 5 and Fig. 6.

$t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	An to Bn	14.4	7.0	6.2	6.0	5.9	6.0	ns
		Bn to An	14.4	12.4	12.1	11.9	11.8	11.8	ns
$t_{dis}$	disable time	$\overline{OE}$ to An	16.2	16.2	16.2	16.2	16.2	16.2	ns
		$\overline{OE}$ to Bn	17.6	10.0	9.0	9.1	8.7	9.3	ns
$t_{en}$	enable time	$\overline{OE}$ to An	21.9	21.9	21.9	21.9	21.9	21.9	ns
		$\overline{OE}$ to Bn	22.2	11.1	9.8	9.4	9.4	9.6	ns

**Table 10. Typical dynamic characteristics at  $V_{CC(B)} = 0.8\text{ V}$  and  $T_{amb} = 25\text{ °C}$**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for wave forms see Fig. 5 and Fig. 6.

$t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	An to Bn	14.4	12.4	12.1	11.9	11.8	11.8	ns
		Bn to An	14.4	7.0	6.2	6.0	5.9	6.0	ns
$t_{dis}$	disable time	$\overline{OE}$ to An	16.2	5.9	4.4	4.2	3.1	3.5	ns
		$\overline{OE}$ to Bn	17.6	14.2	13.7	13.6	13.3	13.1	ns
$t_{en}$	enable time	$\overline{OE}$ to An	21.9	6.4	4.4	3.5	2.6	2.3	ns
		$\overline{OE}$ to Bn	22.2	17.7	17.2	17.0	16.8	16.7	ns

## 8-bit dual supply translating transceiver with configurable voltage translation; 3-state

Table 11. Typical power dissipation capacitance at  $V_{CC(A)} = V_{CC(B)}$  and  $T_{amb} = 25\text{ °C}$ 

Voltages are referenced to GND (ground = 0 V). [1] [2]

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$C_{PD}$	power dissipation capacitance	A port: (direction An to Bn); output enabled	0.2	0.2	0.2	0.3	0.4	0.5	pF
		A port: (direction An to Bn); output disabled	0.2	0.2	0.2	0.3	0.4	0.5	pF
		A port: (direction Bn to An); output enabled	9	9	10	10	11	13	pF
		A port: (direction Bn to An); output disabled	0.6	0.6	0.6	0.7	0.7	0.8	pF
		B port: (direction An to Bn); output enabled	9	9	10	10	11	13	pF
		B port: (direction An to Bn); output disabled	0.6	0.6	0.6	0.7	0.7	0.8	pF
		B port: (direction Bn to An); output enabled	0.2	0.2	0.2	0.3	0.4	0.5	pF
		B port: (direction Bn to An); output disabled	0.2	0.2	0.2	0.3	0.4	0.5	pF

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

 $f_i$  = input frequency in MHz; $f_o$  = output frequency in MHz; $C_L$  = load capacitance in pF; $V_{CC}$  = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.[2]  $f_i = 10\text{ MHz}$ ;  $V_i = \text{GND to } V_{CC}$ ;  $t_r = t_f = 1\text{ ns}$ ;  $C_L = 0\text{ pF}$ ;  $R_L = \infty\ \Omega$ .

## 8-bit dual supply translating transceiver with configurable voltage translation; 3-state

Table 12. Dynamic characteristics for temperature range -40 °C to +85 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for wave forms see Fig. 5 and Fig. 6.

$t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

Symbol	Parameter	Conditions	$V_{CC(B)}$										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b><math>V_{CC(A)} = 1.1 \text{ V to } 1.3 \text{ V}</math></b>													
$t_{pd}$	propagation delay	An to Bn	0.5	9.0	0.5	6.7	0.5	5.8	0.5	4.9	0.5	4.8	ns
		Bn to An	0.5	9.0	0.5	8.5	0.5	8.3	0.5	8.0	0.5	7.8	ns
$t_{dis}$	disable time	$\overline{OE}$ to An	0.5	11.8	0.5	11.8	0.5	11.8	0.5	11.8	0.5	11.8	ns
		$\overline{OE}$ to Bn	0.5	12.3	0.5	9.5	0.5	9.4	0.5	8.0	0.5	8.9	ns
$t_{en}$	enable time	$\overline{OE}$ to An	1.1	14.4	1.1	14.4	1.1	14.4	1.1	14.4	1.1	14.4	ns
		$\overline{OE}$ to Bn	1.1	14.2	1.1	10.4	1.1	9.0	1.0	7.7	1.0	7.3	ns
<b><math>V_{CC(A)} = 1.4 \text{ V to } 1.6 \text{ V}</math></b>													
$t_{pd}$	propagation delay	An to Bn	0.5	8.5	0.5	5.6	0.5	4.7	0.5	4.4	0.5	4.1	ns
		Bn to An	0.5	6.7	0.5	5.6	0.5	5.3	0.5	5.2	0.5	5.0	ns
$t_{dis}$	disable time	$\overline{OE}$ to An	0.5	8.6	0.5	8.6	0.5	8.6	0.5	8.6	0.5	8.6	ns
		$\overline{OE}$ to Bn	0.5	11.2	0.5	8.4	0.5	7.6	0.5	7.2	0.5	7.8	ns
$t_{en}$	enable time	$\overline{OE}$ to An	1.1	8.7	1.1	8.7	1.1	8.7	1.1	8.7	1.1	8.7	ns
		$\overline{OE}$ to Bn	1.1	12.8	1.1	8.1	1.1	7.1	1.0	5.6	1.0	5.2	ns
<b><math>V_{CC(A)} = 1.65 \text{ V to } 1.95 \text{ V}</math></b>													
$t_{pd}$	propagation delay	An to Bn	0.5	8.3	0.5	5.3	0.5	4.5	0.5	3.8	0.5	3.5	ns
		Bn to An	0.5	5.8	0.5	4.7	0.5	4.5	0.5	4.3	0.5	4.1	ns
$t_{dis}$	disable time	$\overline{OE}$ to An	0.5	7.1	0.5	7.1	0.5	7.1	0.5	7.1	0.5	7.1	ns
		$\overline{OE}$ to Bn	0.5	10.9	0.5	7.8	0.5	6.9	0.5	6.0	0.5	5.8	ns
$t_{en}$	enable time	$\overline{OE}$ to An	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	ns
		$\overline{OE}$ to Bn	1.1	12.4	1.1	8.2	1.0	6.7	0.5	5.1	0.5	4.5	ns
<b><math>V_{CC(A)} = 2.3 \text{ V to } 2.7 \text{ V}</math></b>													
$t_{pd}$	propagation delay	An to Bn	0.5	8.0	0.5	5.2	0.5	4.3	0.5	3.3	0.5	2.9	ns
		Bn to An	0.5	4.9	0.5	4.4	0.5	3.8	0.5	3.3	0.5	3.1	ns
$t_{dis}$	disable time	$\overline{OE}$ to An	0.5	5.1	0.5	5.1	0.5	5.1	0.5	5.1	0.5	5.1	ns
		$\overline{OE}$ to Bn	0.5	10.4	0.5	7.1	0.5	6.3	0.5	5.1	0.5	5.2	ns
$t_{en}$	enable time	$\overline{OE}$ to An	0.5	4.8	0.5	4.8	0.5	4.8	0.5	4.8	0.5	4.8	ns
		$\overline{OE}$ to Bn	1.1	11.9	1.1	7.9	0.5	6.4	0.5	4.6	0.5	4.0	ns
<b><math>V_{CC(A)} = 3.0 \text{ V to } 3.6 \text{ V}</math></b>													
$t_{pd}$	propagation delay	An to Bn	0.5	7.8	0.5	5.0	0.5	4.1	0.5	3.1	0.5	2.7	ns
		Bn to An	0.5	4.8	0.5	4.1	0.5	3.5	0.5	2.9	0.5	2.7	ns
$t_{dis}$	disable time	$\overline{OE}$ to An	0.5	4.9	0.5	4.9	0.5	4.9	0.5	4.9	0.5	4.9	ns
		$\overline{OE}$ to Bn	0.5	10.1	0.5	6.9	0.5	6.0	0.5	4.8	0.5	5.0	ns
$t_{en}$	enable time	$\overline{OE}$ to An	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	ns
		$\overline{OE}$ to Bn	1.1	11.7	1.1	7.8	0.5	6.2	0.5	4.5	0.5	3.9	ns

## 8-bit dual supply translating transceiver with configurable voltage translation; 3-state

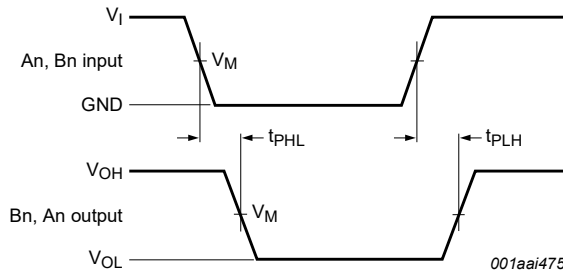
Table 13. Dynamic characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for wave forms see Fig. 5 and Fig. 6

$t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

Symbol	Parameter	Conditions	$V_{CC(B)}$										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b><math>V_{CC(A)} = 1.1 \text{ V to } 1.3 \text{ V}</math></b>													
$t_{pd}$	propagation delay	An to Bn	0.5	9.9	0.5	7.4	0.5	6.4	0.5	5.4	0.5	5.3	ns
		Bn to An	0.5	9.9	0.5	9.4	0.5	9.2	0.5	8.8	0.5	8.6	ns
$t_{dis}$	disable time	$\overline{OE}$ to An	0.5	13.0	0.5	13.0	0.5	13.0	0.5	13.0	0.5	13.0	ns
		$\overline{OE}$ to Bn	0.5	13.6	0.5	10.5	0.5	10.4	0.5	8.8	0.5	9.8	ns
$t_{en}$	enable time	$\overline{OE}$ to An	1.1	15.9	1.1	15.9	1.1	15.9	1.1	15.9	1.1	15.9	ns
		$\overline{OE}$ to Bn	1.1	15.7	1.1	11.5	1.1	9.9	1.0	8.5	1.0	8.1	ns
<b><math>V_{CC(A)} = 1.4 \text{ V to } 1.6 \text{ V}</math></b>													
$t_{pd}$	propagation delay	An to Bn	0.5	9.4	0.5	6.2	0.5	5.2	0.5	4.9	0.5	4.6	ns
		Bn to An	0.5	7.4	0.5	6.2	0.5	5.9	0.5	5.8	0.5	5.5	ns
$t_{dis}$	disable time	$\overline{OE}$ to An	0.5	9.5	0.5	9.5	0.5	9.5	0.5	9.5	0.5	9.5	ns
		$\overline{OE}$ to Bn	0.5	12.4	0.5	9.3	0.5	8.4	0.5	8.0	0.5	8.6	ns
$t_{en}$	enable time	$\overline{OE}$ to An	1.1	9.6	1.1	9.6	1.1	9.6	1.1	9.6	1.1	9.6	ns
		$\overline{OE}$ to Bn	1.1	14.1	1.1	9.0	1.1	7.9	1.0	6.2	1.0	5.8	ns
<b><math>V_{CC(A)} = 1.65 \text{ V to } 1.95 \text{ V}</math></b>													
$t_{pd}$	propagation delay	An to Bn	0.5	9.2	0.5	5.9	0.5	5.0	0.5	4.2	0.5	3.9	ns
		Bn to An	0.5	6.4	0.5	5.2	0.5	5.0	0.5	4.8	0.5	4.6	ns
$t_{dis}$	disable time	$\overline{OE}$ to An	0.5	7.9	0.5	7.9	0.5	7.9	0.5	7.9	0.5	7.9	ns
		$\overline{OE}$ to Bn	0.5	12.0	0.5	8.6	0.5	7.6	0.5	6.6	0.5	6.4	ns
$t_{en}$	enable time	$\overline{OE}$ to An	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	ns
		$\overline{OE}$ to Bn	1.1	13.7	1.1	9.1	1.0	7.4	0.5	5.7	0.5	5.0	ns
<b><math>V_{CC(A)} = 2.3 \text{ V to } 2.7 \text{ V}</math></b>													
$t_{pd}$	propagation delay	An to Bn	0.5	8.8	0.5	5.8	0.5	4.8	0.5	3.7	0.5	3.2	ns
		Bn to An	0.5	5.4	0.5	4.9	0.5	4.2	0.5	3.7	0.5	3.5	ns
$t_{dis}$	disable time	$\overline{OE}$ to An	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	ns
		$\overline{OE}$ to Bn	0.5	11.5	0.5	7.9	0.5	7.0	0.5	5.7	0.5	5.8	ns
$t_{en}$	enable time	$\overline{OE}$ to An	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	ns
		$\overline{OE}$ to Bn	1.1	13.1	1.1	8.7	0.5	7.1	0.5	5.1	0.5	4.4	ns
<b><math>V_{CC(A)} = 3.0 \text{ V to } 3.6 \text{ V}</math></b>													
$t_{pd}$	propagation delay	An to Bn	0.5	8.6	0.5	5.5	0.5	4.6	0.5	3.5	0.5	3.0	ns
		Bn to An	0.5	5.3	0.5	4.6	0.5	3.9	0.5	3.2	0.5	3.0	ns
$t_{dis}$	disable time	$\overline{OE}$ to An	0.5	5.4	0.5	5.4	0.5	5.4	0.5	5.4	0.5	5.4	ns
		$\overline{OE}$ to Bn	0.5	11.2	0.5	7.6	0.5	6.6	0.5	5.3	0.5	5.5	ns
$t_{en}$	enable time	$\overline{OE}$ to An	0.5	4.4	0.5	4.4	0.5	4.4	0.5	4.4	0.5	4.4	ns
		$\overline{OE}$ to Bn	1.1	12.9	1.1	8.6	0.5	6.9	0.5	5.0	0.5	4.3	ns

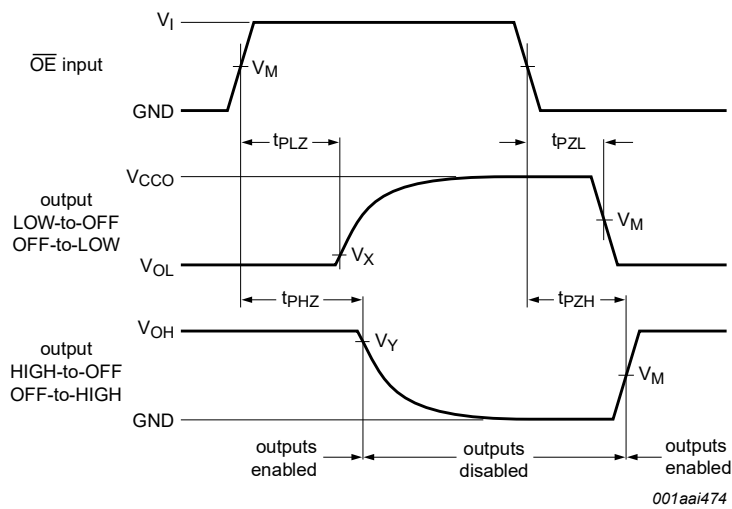
10.1. Waveforms and test circuit



Measurement points are given in [Table 14](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 5. The data input (An, Bn) to output (Bn, An) propagation delay times



Measurement points are given in [Table 14](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 6. Enable and disable times

Table 14. Measurement points

Supply voltage	Input [1]	Output [2]		
	$V_M$	$V_M$	$V_X$	$V_Y$
0.8 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1 V$	$V_{OH} - 0.1 V$
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.

[2]  $V_{CCO}$  is the supply voltage associated with the output port.

8-bit dual supply translating transceiver with configurable voltage translation; 3-state

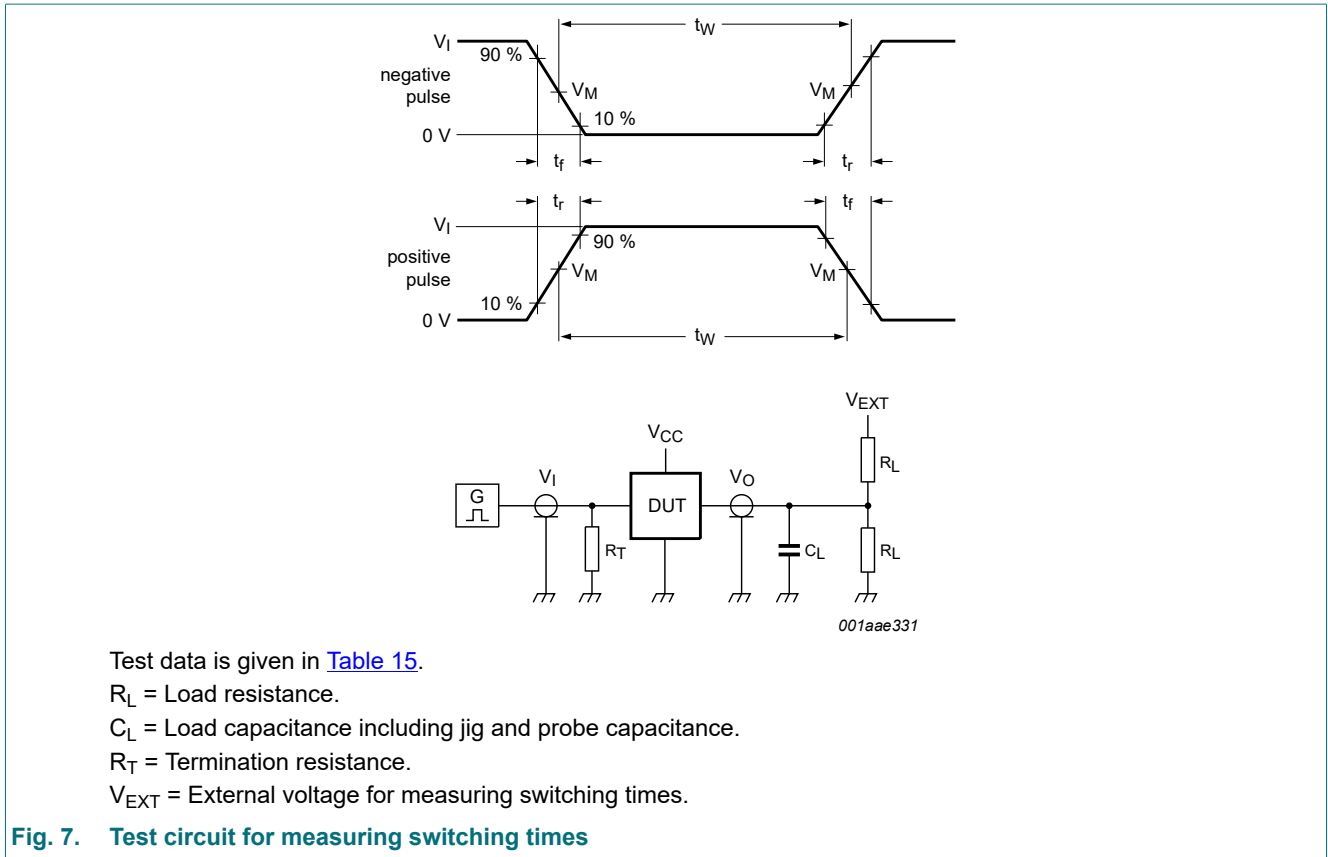
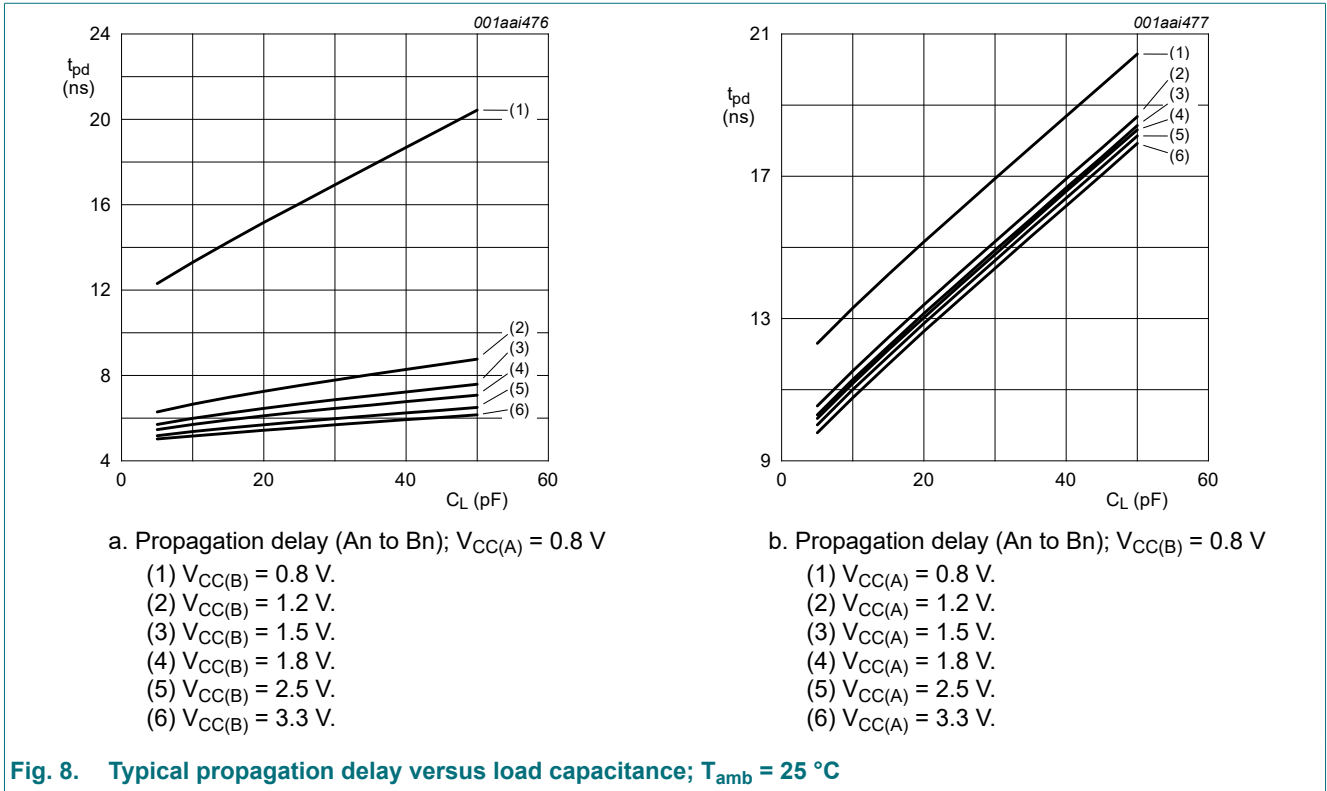


Table 15. Test data

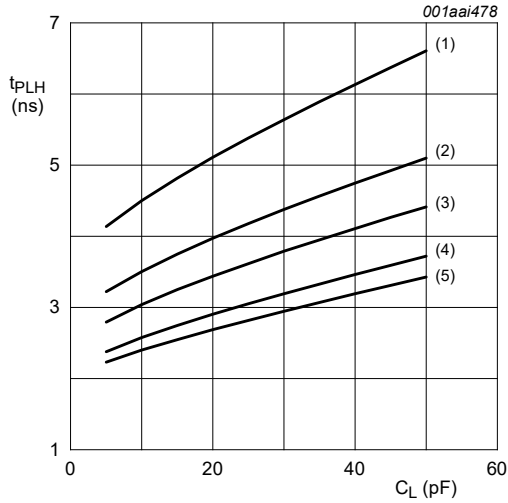
Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC(A)}, V_{CC(B)}$	$V_I$ [1]	$\Delta t/\Delta V$ [2]	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$ [3]
0.8 V to 1.6 V	$V_{CCI}$	$\leq 1.0$ ns/V	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	$V_{CCI}$	$\leq 1.0$ ns/V	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	$V_{CCI}$	$\leq 1.0$ ns/V	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.  
 [2]  $dV/dt \geq 1.0$  V/ns  
 [3]  $V_{CCO}$  is the supply voltage associated with the output port.

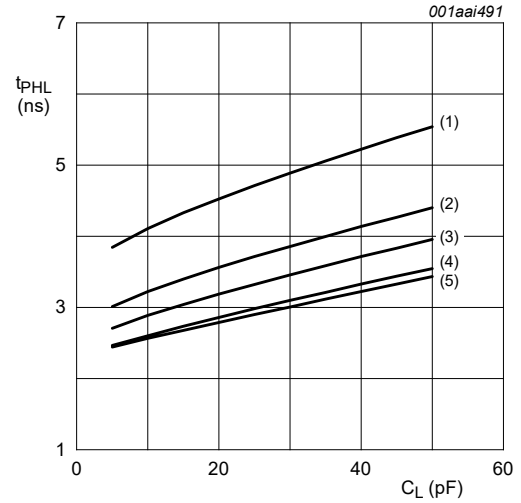
10.2. Typical propagation delay characteristics



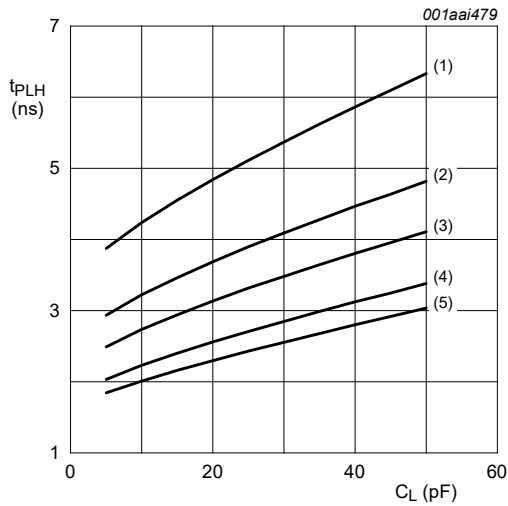
8-bit dual supply translating transceiver with configurable voltage translation; 3-state



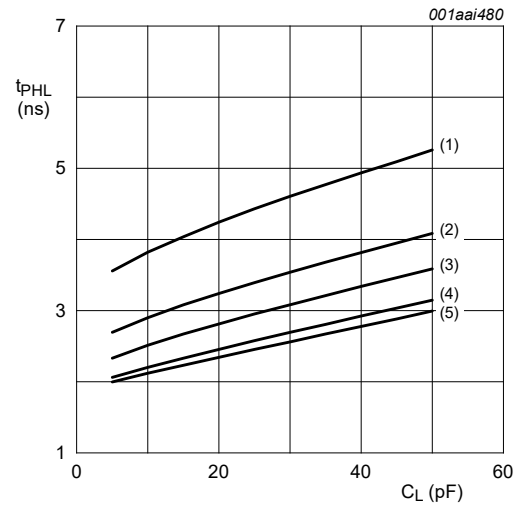
a. LOW to HIGH propagation delay (An to Bn);  $V_{CC(A)} = 1.2\text{ V}$



b. HIGH to LOW propagation delay (An to Bn);  $V_{CC(A)} = 1.2\text{ V}$



c. LOW to HIGH propagation delay (An to Bn);  $V_{CC(A)} = 1.5\text{ V}$



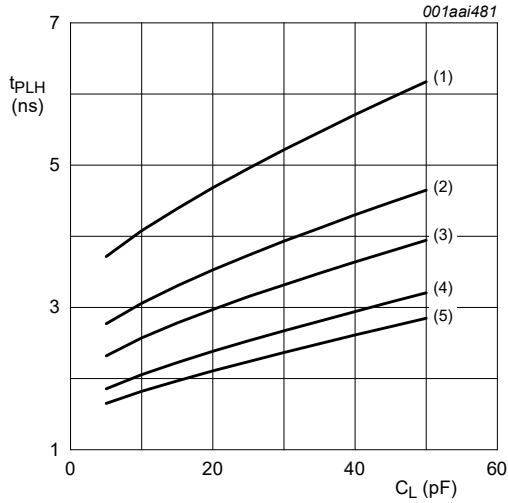
d. HIGH to LOW propagation delay (An to Bn);  $V_{CC(A)} = 1.5\text{ V}$

- (1)  $V_{CC(B)} = 1.2\text{ V}$ .
- (2)  $V_{CC(B)} = 1.5\text{ V}$ .
- (3)  $V_{CC(B)} = 1.8\text{ V}$ .
- (4)  $V_{CC(B)} = 2.5\text{ V}$ .
- (5)  $V_{CC(B)} = 3.3\text{ V}$ .

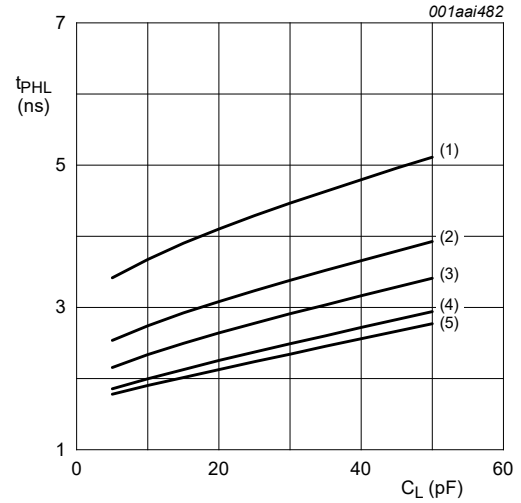
Fig. 9. Typical propagation delay versus load capacitance;  $T_{amb} = 25\text{ }^\circ\text{C}$



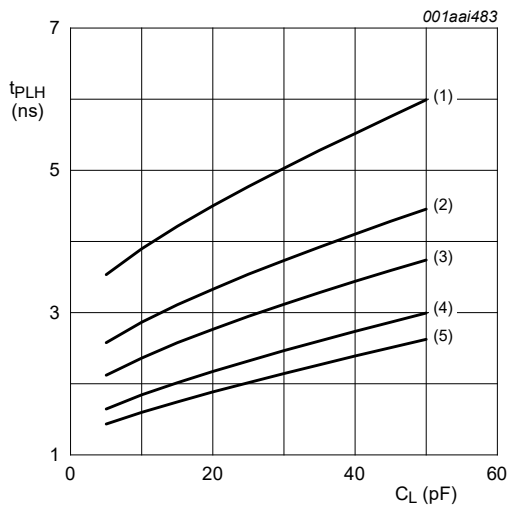
8-bit dual supply translating transceiver with configurable voltage translation; 3-state



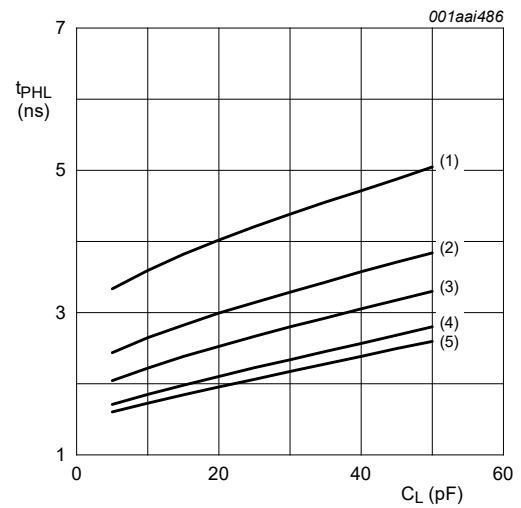
a. LOW to HIGH propagation delay (An to Bn);  $V_{CC(A)} = 1.8\text{ V}$



b. HIGH to LOW propagation delay (An to Bn);  $V_{CC(A)} = 1.8\text{ V}$



c. LOW to HIGH propagation delay (An to Bn);  $V_{CC(A)} = 2.5\text{ V}$

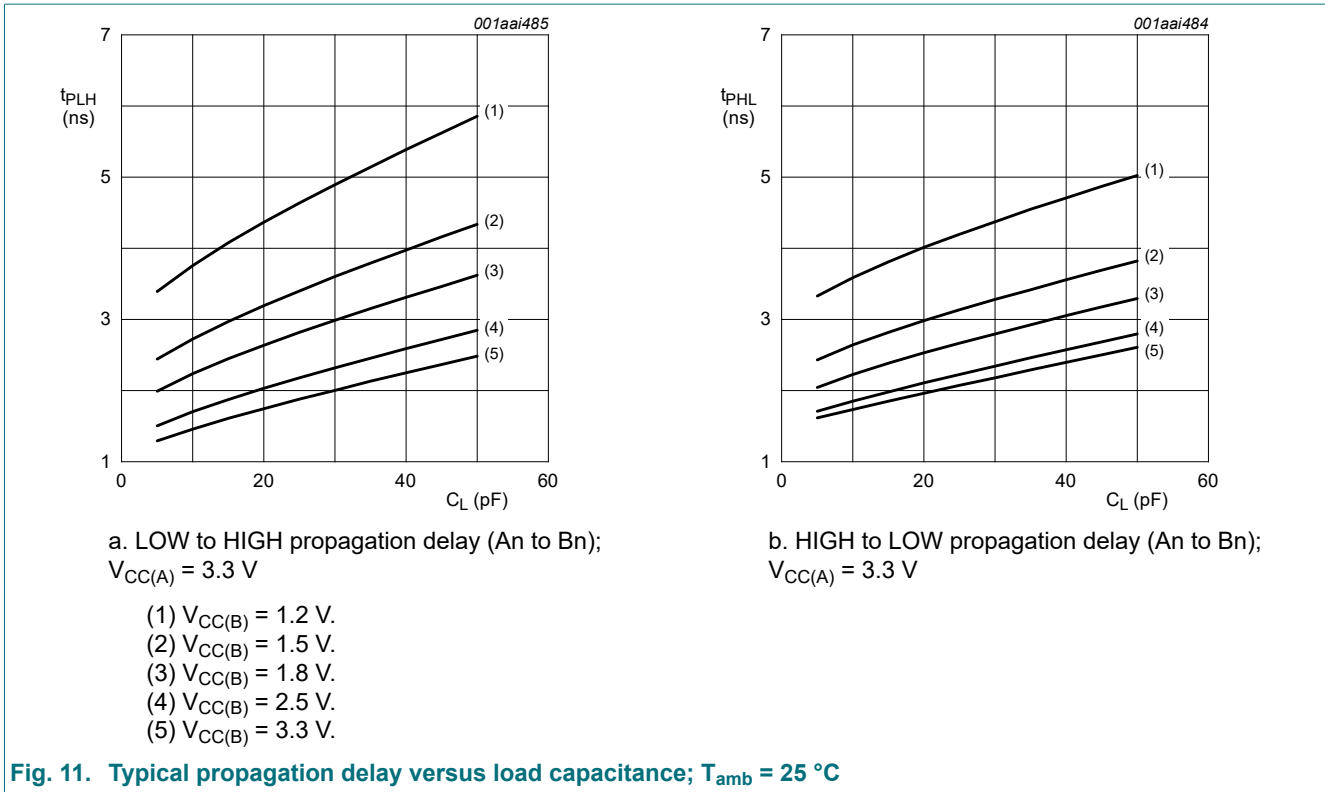


d. HIGH to LOW propagation delay (An to Bn);  $V_{CC(A)} = 2.5\text{ V}$

- (1)  $V_{CC(B)} = 1.2\text{ V}$ .
- (2)  $V_{CC(B)} = 1.5\text{ V}$ .
- (3)  $V_{CC(B)} = 1.8\text{ V}$ .
- (4)  $V_{CC(B)} = 2.5\text{ V}$ .
- (5)  $V_{CC(B)} = 3.3\text{ V}$ .

Fig. 10. Typical propagation delay versus load capacitance;  $T_{amb} = 25\text{ }^\circ\text{C}$

8-bit dual supply translating transceiver with configurable voltage translation; 3-state



### 11. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

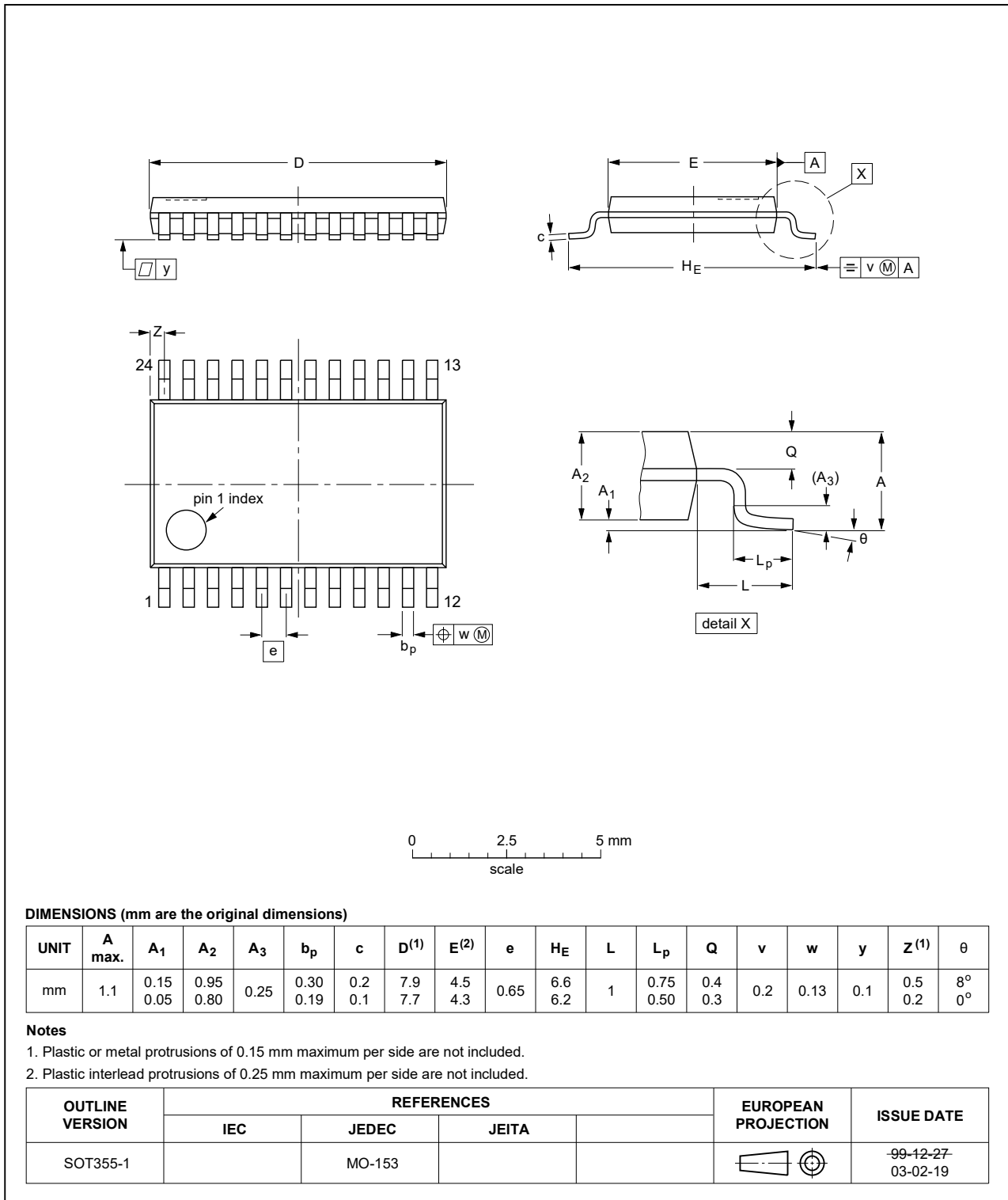


Fig. 12. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package;  
no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

SOT815-1

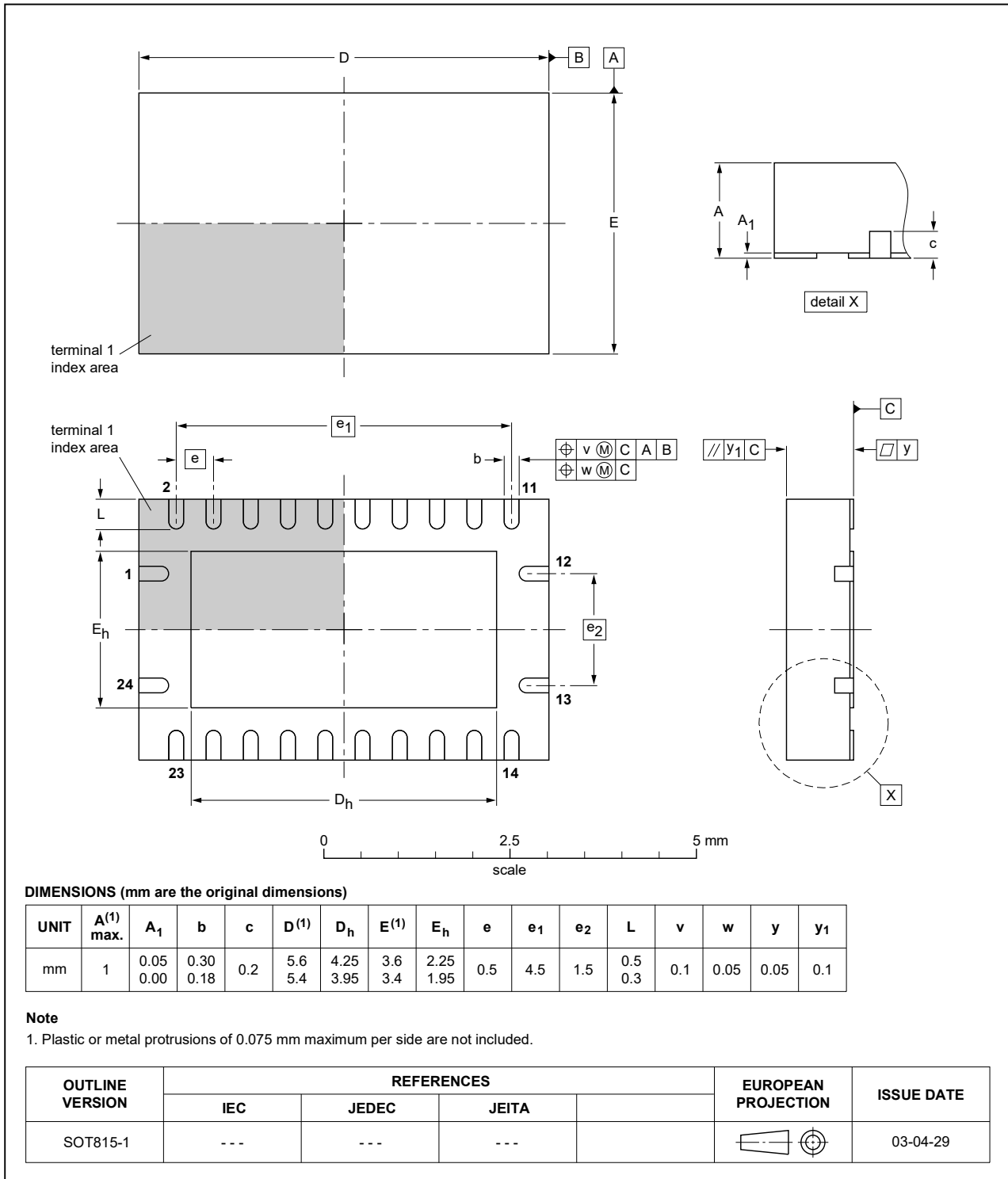


Fig. 13. Package outline SOT815-1 (DHVQFN24)

## 12. Abbreviations

Table 16. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 13. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC8T245 v.6	20200331	Product data sheet	-	74AVC8T245 v.5
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74AVC8T245 v.5	20121227	Product data sheet	-	74AVC8T245 v.4
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 4</a>: conditions <math>I_{CC}</math> and <math>I_{GND}</math> changed (errata).</li> </ul>			
74AVC8T245 v.4	20111208	Product data sheet	-	74AVC8T245 v.3
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
74AVC8T245 v.3	20110928	Product data sheet	-	74AVC8T245 v.2
74AVC8T245 v.2	20090428	Product data sheet	-	74AVC8T245 v.1
74AVC8T245 v.1	20080711	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: [ocean@oceanchips.ru](mailto:ocean@oceanchips.ru)

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А