NCN5120

Transceiver for KNX Twisted Pair Networks

Introduction

NCN5120 is a receiver−transmitter IC suitable for use in KNX twisted pair networks (KNX TP1−256). It supports the connection of actuators, sensors, microcontrollers, switches or other applications in a building network.

NCN5120 handles the transmission and reception of data on the bus. It generates from the unregulated bus voltage stabilized voltages for its own power needs as well as to power external devices, for example, a microcontroller.

NCN5120 assures safe coupling to and decoupling from the bus. Bus monitoring warns the external microcontroller for loss of power so that critical data can be stored in time.

Key Features

- 9600 baud KNX Communication Speed
- Supervision of KNX Bus Voltage
- Supports Bus Current Consumption up to 13 and 26 mA
- Selectable KNX Bus Current (0.5 mA/ms and 1.0 mA/ms)
- High Efficient DC−DC Converters
    - 3.3 V Fixed
    - 3.3 V to 21 V Selectable
- Control and Monitoring of Power Regulators
- Linear 20 V Regulator
- Prepared for Sleep Mode
- Buffering of Sent Data Frames (Extended Frames Supported)
- Selectable UART or SPI Interface to Host Controller
- Selectable UART and SPI baud Rate to Host Controller
- Optional CRC on UART to the Host
- Optional Received Frame−end with MARKER Service
- Optional Direct Coupling of RxD and TxD to Host (analog mode)
- Operates with Industry Standard Low Cost 16 MHz Quartz
- Generates Clock of 8 or 16 MHz for External Devices
- Auto Acknowledge (optional)
- Auto Polling (optional)
- Temperature Monitoring
- Operating Temperature Range −25°C to +85°C
- These Devices are Pb−Free and are RoHS Compliant

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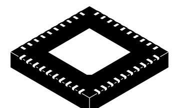
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QFN40
MN SUFFIX
CASE 485AU

MARKING DIAGRAM

NCN5120
21245−XXX
AWLYYWWG

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package
XXX	= Product Variant (contact ON Semiconductor if Product Variant is 001)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 54 of this data sheet.

August, 2014 − Rev. 5

Publication Order Number:
NCN5120/D

BLOCK DIAGRAM

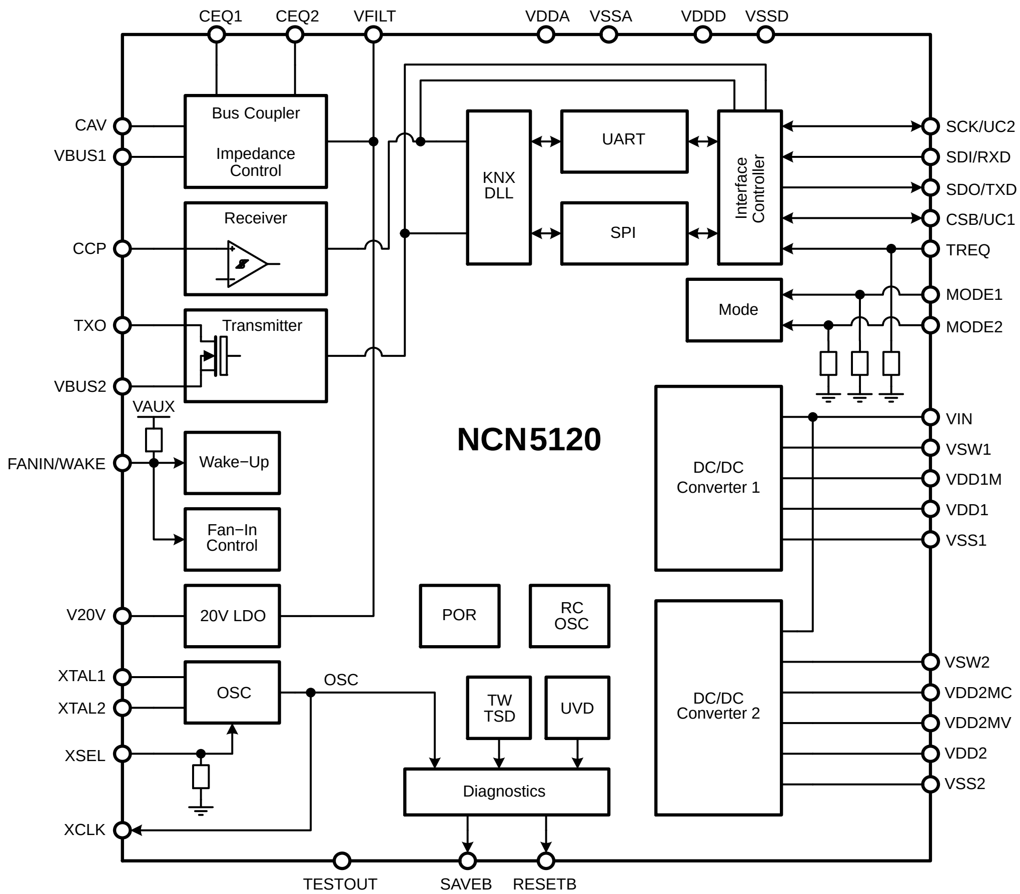


Figure 1. Block Diagram NCN5120

PIN OUT

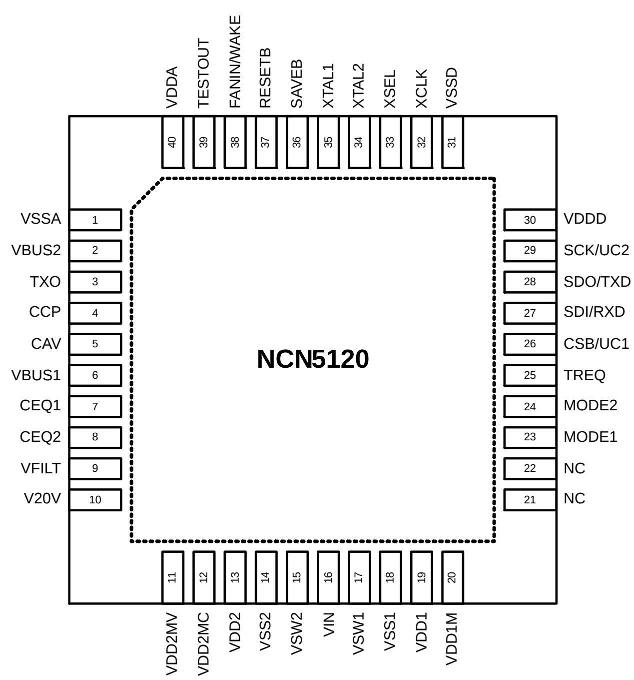


Figure 2. Pin Out NCN5120 (Top View)

PIN DESCRIPTION

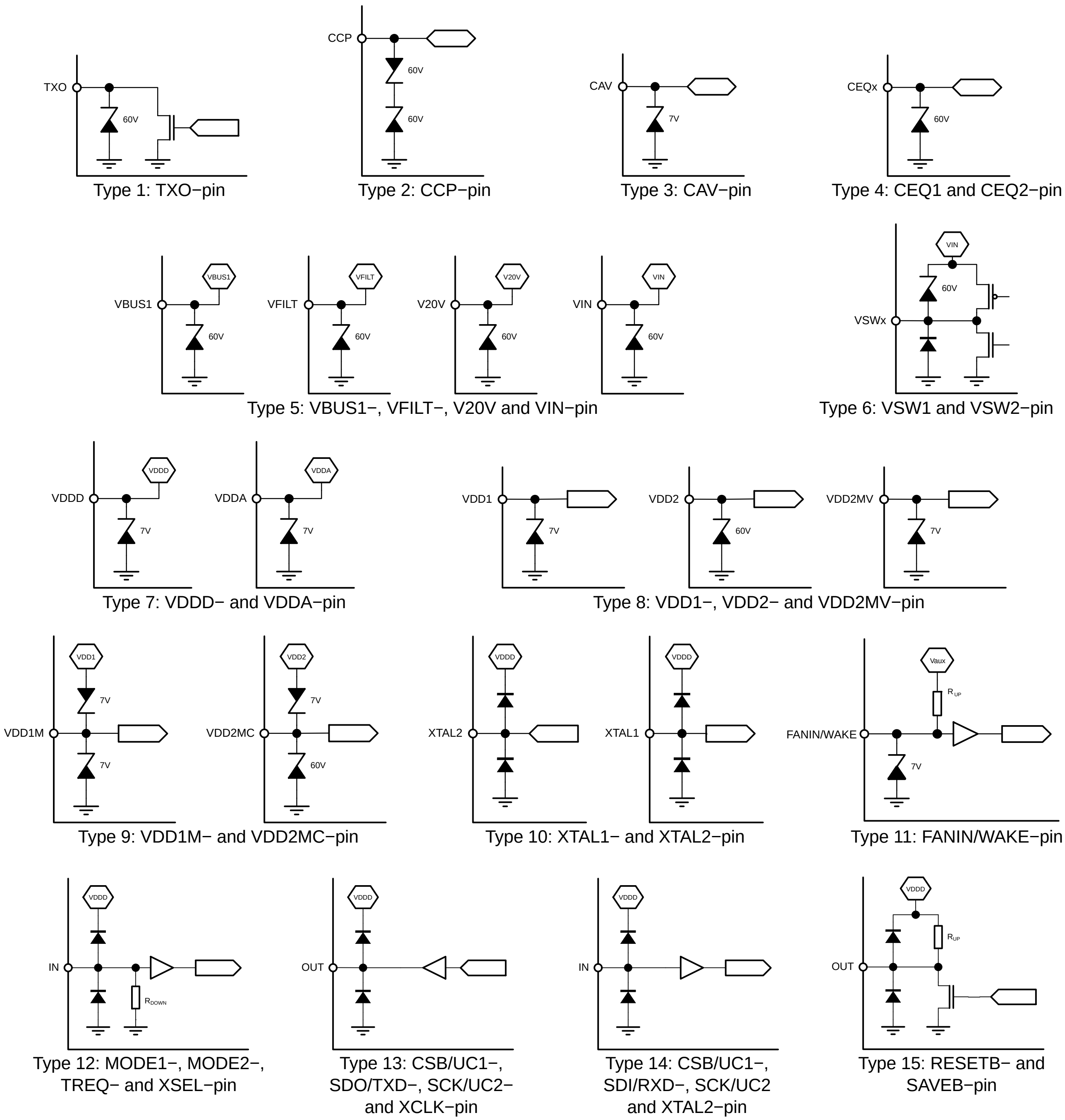
Table 1. PIN LIST AND DESCRIPTION

Name	Pin	Description	Type	Equivalent Schematic
VSSA	1	Analog Supply Voltage Ground	Supply	
VBUS2	2	Ground for KNX Transmitter	Supply	
TX0	3	KNX Transmitter Output	Analog Output	Type 1
CCP	4	AC coupling external capacitor connection	Analog I/O	Type 2
CAV	5	Capacitor connection to average bus DC voltage	Analog I/O	Type 3
VBUS1	6	KNX power supply input	Supply	Type 5
CEQ1	7	Capacitor connection 1 for defining equalization pulse	Analog I/O	Type 4
CEQ2	8	Capacitor connection 2 for defining equalization pulse	Analog I/O	Type 4
VFILT	9	Filtered bus voltage	Supply	Type 5
V20V	10	20V supply output	Supply	Type 5
VDD2MV	11	Voltage monitor of Voltage Regulator 2	Analog Input	Type 8
VDD2MC	12	Current monitor input 1 of Voltage Regulator 2	Analog Input	Type 9
VDD2	13	Current monitor input 2 of Voltage Regulator 2	Analog Input	Type 8
VSS2	14	Voltage Regulator 2 Ground	Supply	
VSW2	15	Switch output of Voltage Regulator 2	Analog Output	Type 6
VIN	16	Voltage Regulator 1 and 2 Power Supply Input	Supply	Type 5
VSW1	17	Switch output of Voltage Regulator 1	Analog Output	Type 6
VSS1	18	Voltage Regulator 1 Ground	Supply	
VDD1	19	Current Input 2 and Voltage Monitor Input of Voltage Regulator 1	Analog Input	Type 8
VDD1M	20	Current Monitor Input 1 of Voltage Monitor 1	Analog Input	Type 9
NC	21, 22	Not connected (do not connect)		
MODE1	23	Mode Selection Input 1	Digital Input	Type 12
MODE2	24	Mode Selection Input 2	Digital Input	Type 12
TREQ	25	Transmit Request Input	Digital Input	Type 12
CSB/UC1	26	Chip Select Output (SPI) or Configuration Input (UART)	Digital Output or Digital Input	Type 13 or 14
SDI/RXD	27	Serial Data Input (SPI) or Receive Input (UART)	Digital Input	Type 14
SDO/TXD	28	Serial Data Output (SPI) or Transmit Output (UART)	Digital Output	Type 13
SCK/UC2	29	Serial Clock Output (SPI) or Configuration Input (UART)	Digital Output or Digital Input	Type 13 or 14
VDDD	30	Digital Supply Voltage Input	Supply	Type 7
VSSD	31	Digital Supply Voltage Ground	Supply	
XCLK	32	Oscillator Clock Output	Digital Output	Type 13
XSEL	33	Clock Selection (Quartz or Digital Clock)	Digital Input	Type 12
XTAL2	34	Clock Generator Output (Quartz) or Input (Digital Clock)	Analog Output or Digital Input	Type 10 or 14
XTAL1	35	Clock Generator Input (Quartz)	Analog Input	Type 10
SAVEB	36	Save Signal (open drain with pull−up)	Digital Output	Type 15
RESETB	37	Reset Signal (open drain with pull−up)	Digital Output	Type 15
FANIN/WAKE	38	Fan−In and Wake−Up Input	Digital Input	Type 11
TESTOUT	39	Test Output (do not connect)	Analog Output	
VDDA	40	Analog Supply Voltage Input	Supply	Type 7

NOTE: Type of CSB/UC1 and SCK/UC2 is depending on status MODE1 − MODE2 pin
Type of XTAL1 and XTAL2 pin is depending on status XSEL pin.

EQUIVALENT SCHEMATICS

Following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.



NOTE: Type of CSB/UC1 and SCK/UC2 is depending on status MODE1 − MODE2 pin
Type of XTAL1 and XTAL2 pin is depending on status XSEL pin.

Figure 3. In− and Output Equivalent Diagrams

ELECTRICAL SPECIFICATION

Table 2. ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Symbol	Parameter	Min	Max	Unit
V_{TXO}	KNX Transmitter Output Voltage	−0.3	+45	V
I_{TXO}	KNX Transmitter Output Current (Note 3)		250	mA
V_{CCP}	Voltage on CCP−pin	−10.5	+14.5	V
V_{CAV}	Voltage on CAV−pin	−0.3	+3.6	V
V_{BUS1}	Voltage on VBUS1−pin	−0.3	+45	V
I_{BUS1}	Current Consumption VBUS1−pin	0	60	mA
V_{CEQ}	Voltage on pins CEQ1 and CEQ2	−0.3	+45	V
V_{FILT}	Voltage on VFILT−pin	−0.3	+45	V
V_{20V}	Voltage on V20V−pin	−0.3	+25	V
V_{DD2MV}	Voltage on VDD2MV−pin	−0.3	+3.6	V
V_{DD2MC}	Voltage on VDD2MC−pin	−0.3	+45	V
V_{DD2}	Voltage on VDD2−pin	−0.3	+45	V
V_{SW}	Voltage on VSW1− and VSW2−pin	−0.3	+45	V
V_{IN}	Voltage on VIN−pin	−0.3	+45	V
V_{DD1}	Voltage on VDD1−pin	−0.3	+3.6	V
V_{DD1M}	Voltage on VDD1M−pin	−0.3	+3.6	V
V_{DIG}	Voltage on pins MODE1, MODE2, TREQ, CSB/UC1, SDI/TXD, SDO/RXD, SCK/UC2, XCLK, XSEL, SAVEB, RESETB and FANIN/WAKE	−0.3	+3.6	V
V_{DD}	Voltage on VDDD− and VDDA−pin	−0.3	+3.6	V
V_{XTAL}	Voltage on XTAL1− and XTAL2−pin	−0.3	+3.6	V
T_{ST}	Storage temperature	−55	+150	°C
T_J	Junction Temperature (Note 4)	−25	+155	°C
V_{HBM}	Human Body Model electronic discharge immunity (Note 5)	−2	+2	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Convention: currents flowing in the circuit are defined as positive.
2. VBUS2, VSS1, VSS2, VSSA and VSSD form the common ground. They are hard connected to the PCB ground layer.
3. Room temperature, 27 Ω shunt resistor for transmitter, 250 mA over temperature range.
4. Normal performance within the limitations is guaranteed up to the Thermal Warning level. Between Thermal Warning and Thermal Shutdown temporary loss of function or degradation of performance (which ceases after the disturbance ceases) is possible.
5. According to JEDEC JESD22−A114.

Recommend Operation Conditions

Operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the chip outside these operating ranges is not guaranteed. Operating outside the recommended operating ranges for extended periods of time may affect device reliability.

Table 3. OPERATING RANGES

Symbol	Parameter	Min	Max	Unit
V_{BUS1}	VBUS1 Voltage (Note 6)	+20	+33	V
V_{DD}	Digital and Analog Supply Voltage (VDDD− and VDDA−pin)	+3.13	+3.47	V
V_{IN}	Input Voltage DC−DC Converter 1 and 2 (Note 7)	+8.47	+33	V
V_{CCP}	Input Voltage at CCP−pin	−10.5	+14.5	V
V_{DD1}	Input Voltage on VDD1−pin	+3.13	+3.47	V
V_{DD1M}	Input Voltage on VDD1M−pin	+3.13	+3.57	V
V_{DD2}	Input Voltage on VDD2−pin	+3.1	+21	V
V_{DD2MC}	Input Voltage on VDD2MC−pin	+3.1	+21.1	V
V_{DD2MV}	Input Voltage on VDD2MV−pin	+1.2	VDD	V
V_{DIG}	Input Voltage on pins MODE1, MODE2, TREQ, CSB/UC1, SDI/RXD, SCK/UC2, and XSEL	0	VDD	V
V_{WAKE}	Input Voltage on FANIN/WAKE−pin	0	3.6	V
f_{clk}	Clock Frequency External Quartz	16		MHz
T_A	Ambient Temperature	−25	+85	°C
T_J	Junction Temperature (Note 8)	−25	+125	°C

6. Voltage indicates DC value. With equalization pulse bus voltage must be between 11 V and 45 V.
7. Minimum operating voltage on VIN−pin should be equal to the lowest value of VDD1 and VDD2.
8. Higher junction temperature can result in reduced lifetime.

Table 4. DC PARAMETERS The DC parameters are given for a device operating within the Recommended Operating Conditions unless otherwise specified. Convention: currents flowing in the circuit are defined as positive.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY							
V_{BUS1}	VBUS1	Bus DC voltage	Excluding active and equalization pulse	20		33	V
I_{BUS1_Int}	VBUS1	Bus Current Consumption	Normal operating mode. No external load, DC1 and DC2 enabled, continuous trans−mission of ‘0’ on the KNX bus by another KNX device (50% bus load), based on Figure 14		5		mA
I_{SLEEP}	VBUS1	Sleep Mode Current Consumption			1.35	1.8	mA
V_{BUSH}	VBUS1	Undervoltage release level	V_{BUS1} rising, see Figure 4	17.1	18.0	18.9	V
V_{BUSL}	VBUS1	Undervoltage trigger level	V_{BUS1} falling, see Figure 4	15.9	16.8	17.7	V
V_{BUS_Hyst}	VBUS1	Undervoltage hysteresis		0.6			V
V_{DDD}	VDDD	Digital Power Supply		3.13	3.3	3.47	V
V_{DDA}	VDDA	Analog Power Supply		3.13	3.3	3.47	V
V_{AUX}		Auxiliary Supply		2.8	3.3	3.6	V
KNX BUS COUPLER							
$I_{coupler\_lim}$		Bus Coupler Current Limitation	FANIN/WAKE = 1, V_{FILT} > V_{FILTH}	13		30	mA
			FANIN/WAKE = 0, V_{FILT} > V_{FILTH}	26		60	mA

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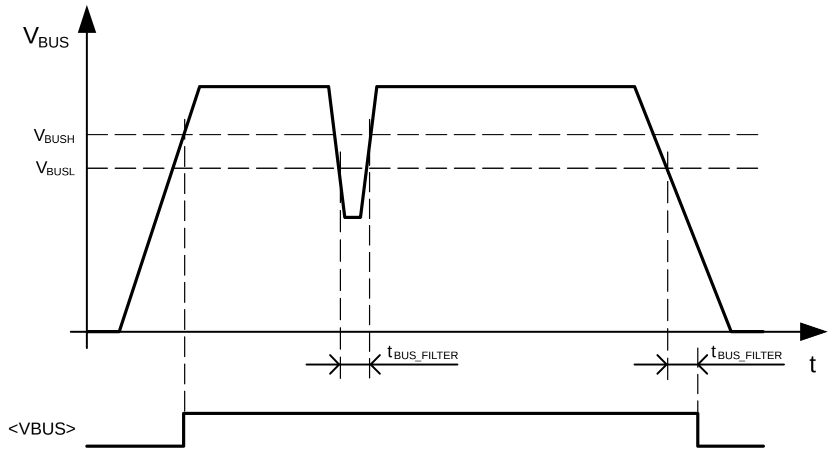
Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
KNX BUS COUPLER							
$V_{coupler\_drop}$	VBUS1, VFILT	Coupler Voltage Drop	I_{BUS1} = 12 mA $V_{coupler\_drop} = V_{BUS1} - V_{FILT}$	3.5		6.5	V
			I_{BUS1} = 24 mA $V_{coupler\_drop} = V_{BUS1} - V_{FILT}$	4.5		8	V
V_{FILTH}	VFILT	Undervoltage release level	V_{FILT} rising, see Figure 5	10.1	10.6	11.2	V
V_{FILTL}		Undervoltage trigger level	V_{FILT} falling, see Figure 5	8.4	8.9	9.4	V
FIXED DC−DC CONVERTER							
V_{IN}	VIN	Input Voltage		8.47		33	V
V_{DD1}	VDD1	Output Voltage		3.13	3.3	3.47	V
V_{DD1_rip}		Output Voltage Ripple	V_{IN} = 25 V, I_{DD1} = 40 mA		40		mV
I_{DD1_lim}		Overcurrent Threshold	R_2 = 1 Ω, see Figure 14	−100		−200	mA
η_{VDD1}		Power Efficiency (DC Converter Only)	V_{in} = 25 V, I_{DD1} = 35 mA, L_1 = 220 μH (1.26 Ω ESR), see Figure 13		90		%
$R_{DS(on)\_p1}$		$R_{DS(on)}$ of power switch	See Figure 17			8	Ω
$R_{DS(on)\_n1}$		$R_{DS(on)}$ of flyback switch	See Figure 17			4	Ω
V_{DD1M}	VDD1M	Input voltage VDD1M−pin				3.57	V
ADJUSTABLE DC−DC CONVERTER							
V_{IN}	VIN	Input Voltage		V_{DD2}		33	V
V_{DD2}	VDD2	Output Voltage	$V_{IN} \geq V_{DD2}$	3.3		21	V
V_{DD2H}		Undervoltage release level	V_{DD2} rising, see Figure 6		0.9 x V_{DD2}		V
V_{DD2L}		Undervoltage trigger level	V_{DD2} falling, see Figure 6		0.8 x V_{DD2}		V
V_{DD2_rip}		Output Voltage Ripple	V_{IN} = 25 V, V_{DD2} = 3.3 V, I_{DD2} = 40 mA		40		mV
I_{DD2_lim}		Overcurrent Threshold	R_3 = 1 Ω, see Figure 14	−100		−200	mA
η_{VDD2}		Power Efficiency (DC Converter Only)	V_{in} = 25 V, V_{DD2} = 3.3 V, I_{DD2} = 35 mA, L_2 = 220 μH (1.26 Ω ESR), see Figure 14		90		%
$R_{DS(on)\_p2}$		$R_{DS(on)}$ of power switch	See Figure 17			8	Ω
$R_{DS(on)\_n2}$		$R_{DS(on)}$ of flyback switch	See Figure 17			4	Ω
V_{DD2M}	VDD2MC	Input voltage VDD2MC−pin				21.1	V
R_{VDD2M}	VDD2MV	Input Resistance VDD2MV−pin		60	100	140	kΩ
V20V REGULATOR							
V_{20V}	V20V	V20V Output Voltage	I_{20V} < 4 mA, $V_{FILT} \geq$ 21 V	18	20	22	V
I_{20V}		V20V Output Current		0		−4	mA
I_{20V_lim}		V20V Output Current Limitation				−11	mA
V_{20VH}		V20V Undervoltage release level	V_{20V} rising, see Figure 7	12.6	13.4	14.2	V
V_{20VL}		V20V Undervoltage trigger level	V_{20V} falling, see Figure 7	11.8	12.6	13.4	V
V_{20V_hyst}		V20V Undervoltage hysteresis	$V_{20V\_hyst} = V_{20VH} - V_{20VL}$		0.8		V

Table 4. DC PARAMETERS The DC parameters are given for a device operating within the Recommended Operating Conditions unless otherwise specified. Convention: currents flowing in the circuit are defined as positive.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
XTAL OSCILLATOR							
V_{XTAL}	XTAL1, XTAL2	Voltage on XTAL−pin				V_{DDD}	V
FAN−IN AND WAKE−UP CONTROL							
V_{WAKE_H}	FANIN/ WAKE	FANIN/WAKE−pin release level	See Figure 8	1.5	1.8	2.1	V
V_{WAKE_L}		FANIN/WAKE−pin active level	See Figure 8	0.9	1.2	1.4	V
V_{WAKE_hyst}		Hysteresis on FANIN/WAKE−pin	See Figure 8		0.6		V
R_{WAKE}		Pull−Up Resistor FANIN/ WAKE−pin	Pull−up connected to V_{AUX}	80	165	270	Ω
DIGITAL INPUTS							
V_{IL}	SCK/UC2, SDI/RXD, CSB/UC1, TREQ, MODE1, MODE2, XSEL	Logic Low Threshold		0		0.7	V
V_{IH}		Logic High Threshold		2.65		V_{DDD}	V
R_{DOWN}		Internal Pull−Down Resistor	SCK/UC2−, SDI/RXD− and CSB/UC1 pin excluded. Only valid in Normal State.	5	10	28	kΩ
DIGITAL OUTPUTS							
V_{OL}	SCK/UC2, SDO/TXD, CSB/UC1, XCLK	Logic low output level		0		0.4	V
V_{OH}		Logic high output level		V_{DDD} − 0.45		V_{DDD}	V
I_L	SCK/UC2, XCLK	Load Current				−8	mA
	SDO/TXD, CSB/UC1					−4	mA
V_{OL}	SAVEB, RESETB	Logic low level open drain	I_{OL} = 4 mA			0.4	V
R_{up}		Internal Pull−up Resistor		20	40	80	kΩ
TEMPERATURE MONITOR							
T_{TW}		Thermal Warning	Rising temperature See Figure 9	105	115	135	°C
T_{TSD}		Thermal shutdown	Rising temperature See Figure 9	125	140	155	°C
T_{Hyst}		Thermal Hysteresis	See Figure 9	5	11	15	°C
ΔT		Delta T_{TSD} and T_{TW}	See Figure 9		25		°C
PACKAGE THERMAL RESISTANCE VALUE							
Rth_{ja}		Thermal Resistance Junction−to−Ambient	Simulated Conform JEDEC JESD−51, (2S2P)		30		K/W
			Simulated Conform JEDEC JESD−51, (1S0P)		60		K/W
Rth_{jp}		Thermal Resistance Junction−to−Exposed Pad			0.95		K/W

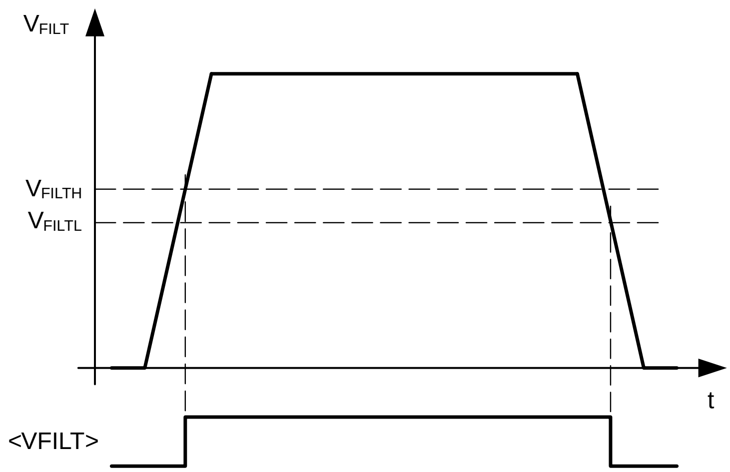
Table 5. AC PARAMETER The AC parameters are given for a device operating within the Recommended Operating Conditions unless otherwise specified.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY							
t_{BUS_FILTER}	VBUS1	VBUS1 filter time	See Figure 4		2		ms
FIXED DC−DC CONVERTER							
t_{VSW1_rise}	VSW1	Rising slope at VSW1−pin			0.45		V/ns
t_{VSW1_fall}		Falling slope at VSW1−pin			0.6		V/ns
ADJUSTABLE DC−DC CONVERTER							
t_{VSW2_rise}	VSW2	Rising slope at VSW2−pin			0.45		V/ns
t_{VSW2_fall}		Falling slope at VSW2−pin			0.6		V/ns
XTAL OSCILLATOR							
f_{XTAL}	XTAL1, XTAL2	XTAL Oscillator Frequency			16		MHz
FAN−IN AND WAKE−UP CONTROL							
t_{WAKE}	FANIN/ WAKE	Debounce Time on FANIN/ WAKE−pin	See Figure 8			100	ms
WATCHDOG							
t_{WDPR}		Prohibited Watchdog Acknowledge Delay	See Watchdog, p19	2		33	ms
t_{WDTO}		Watchdog Timeout Interval	Selectable over UART or SPI	33		524	ms
t_{WDTO_acc}		Watchdog Timeout Interval Accuracy		=Xtal accuracy			
t_{WDRD}		Watchdog Reset Delay			0		ns
t_{RESET}		Reset Duration			8		μs
MASTER SERIAL PERIPHERAL INTERFACE (MASTER SPI)							
t_{sck}	SCK	SPI Clock period	SPI Baudrate depending on configuration input bits (see Interface Mode, p24). Tolerance is equal to Xtal oscillator tolerance. See also Figure 11		2		μs
					8		μs
t_{SCK_HIGH}		SPI Clock high time			t_{SCK} / 2		
t_{SCK_LOW}		SPI Clock low time			t_{SCK} / 2		
t_{SDI_SET}	SDI	SPI Data Input setup time		125			ns
t_{SDI_HOLD}		SPI Data Input hold time		125			ns
t_{SDO_VALID}	SDO	SPI Data Output valid time	C_L = 20 pF, See Figure 11			100	ns
t_{CS_HIGH}	CSB	SPI Chip Select high time	See Figure 11	0.5 x t_{SCK}			
t_{CS_SET}		SPI Chip Select setup time		0.5 x t_{SCK}			
t_{CS_HOLD}		SPI Chip Select hold time		0.5 x t_{SCK}			
t_{TREQ_LOW}	TREQ	TREQ low time	See Figure 12	125			ns
t_{TREQ_HIGH}		TREQ high time		125			ns
t_{TREQ_SET}		TREQ setup time		125			ns
t_{TREQ_HOLD}		TREQ hold time		125			ns
UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)							
f_{UART}	TXD, RXD	UART Interface Baudrate	Baudrate depending on configuration input pins (see *Interface Mode*, p24). Tolerance is equal to tolerance of Xtal oscillator tolerance.		19200		Baud
					38400		Baud



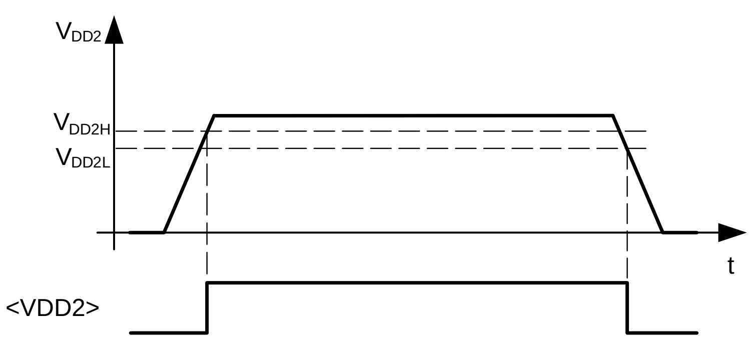
Comments:
<VBUS> is an internal signal which can be verified with the Internal State Service.

Figure 4. Bus Voltage Undervoltage Threshold



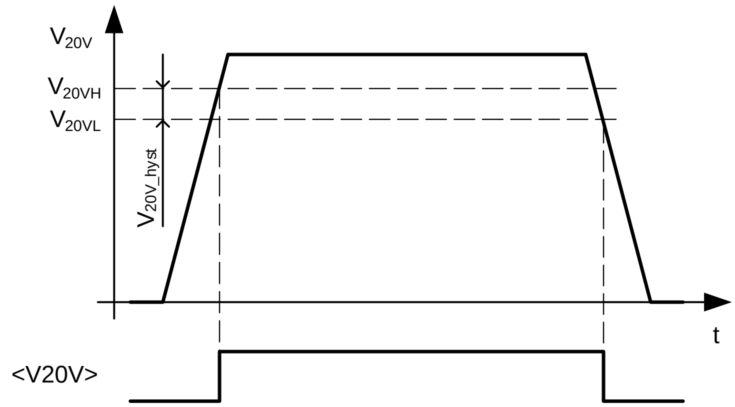
Comments:
<VFILT> is an internal signal which can be verified with the System State Service

Figure 5. VFILT Undervoltage Threshold



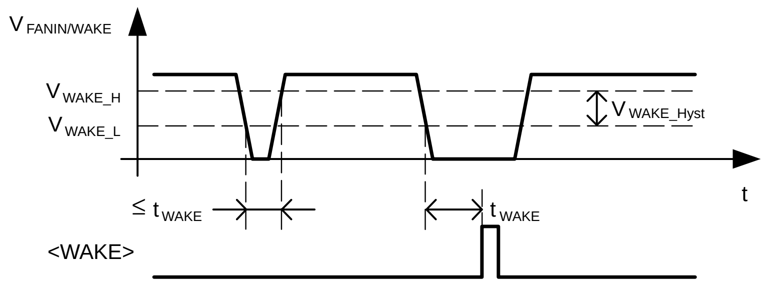
Comments:
<VDD2> is an internal signal which can be verified with the System State Service

Figure 6. VDD2 Undervoltage Thresholds



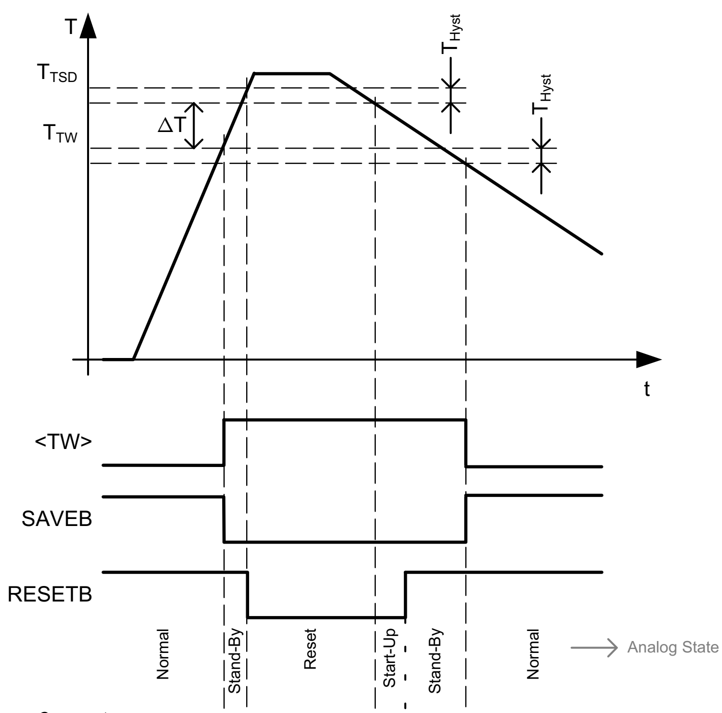
<u>Comments:</u>
<V20V> is an internal signal which can be verified with the System State Service.

Figure 7. V20V Undervoltage Threshold levels



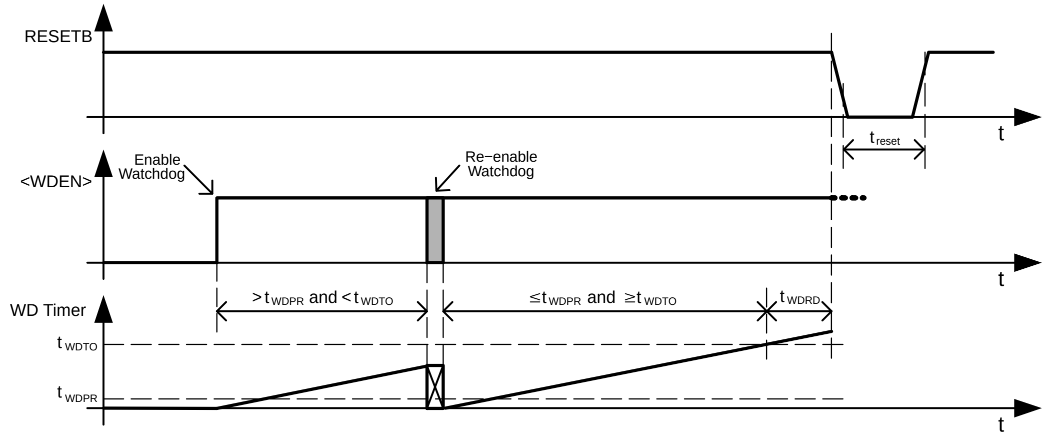
<u>Comments:</u>
−<WAKE> is an internal signal indicating a wake up
−Wake functionality only possible when FANIN/WAKE−pin is high during normal operation

Figure 8. Wake−Up Threshold Levels and Timing



<u>Comments:</u>
- <TW> is an internal signal which can be verified with the System State Service.
- No SPI/UART communication possible when RESETB is low!
- It's assumed all voltage supplies are within their operating condition.

Figure 9. Temperature Monitoring Levels



Remarks:
- WD Timer is an internal timer
- t_{WDTO} = <WDT[3:0]>
- <WDEN> and <WDT[3:0]> are Watchdog Register bits

Figure 10. Watchdog Timing Diagram

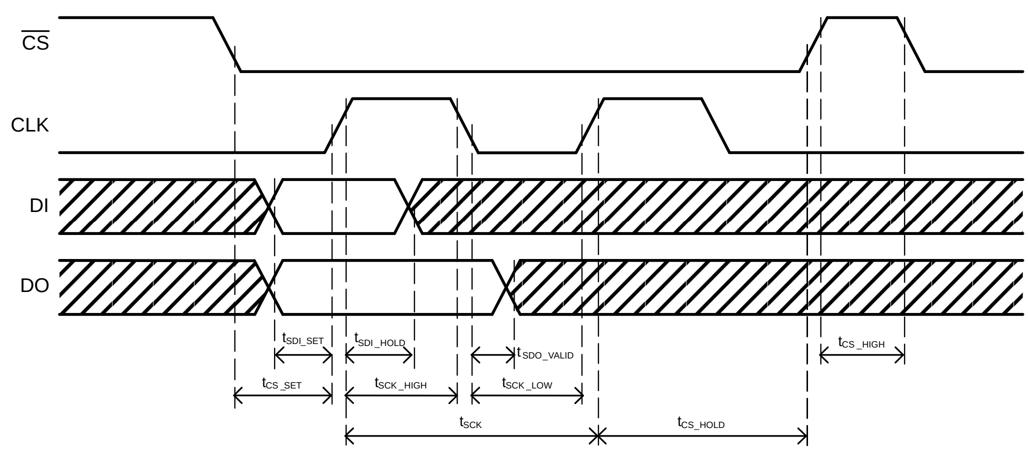


Figure 11. SPI Bus Timing Diagram

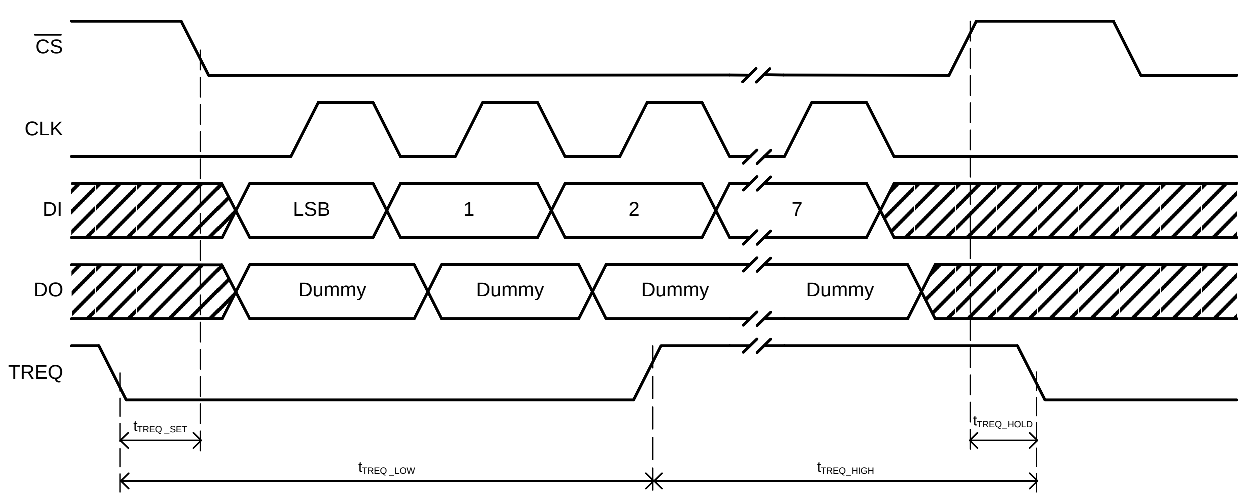


Figure 12. TREQ Timing Diagram

TYPICAL APPLICATION SCHEMATICS

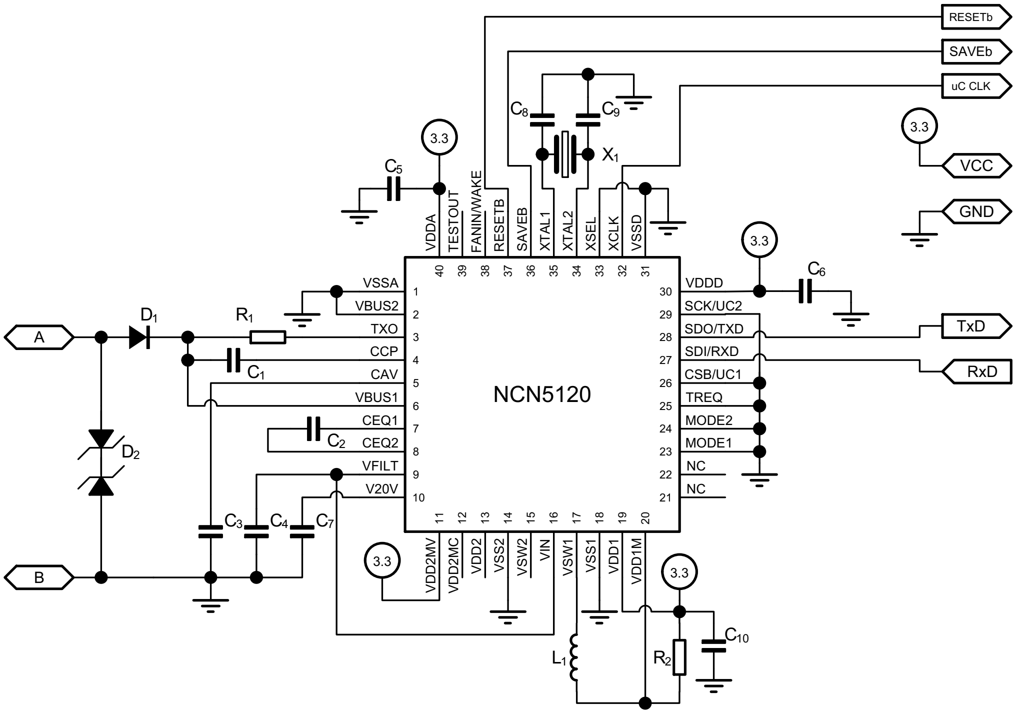


Figure 13. Typical Application Schematic NCN5120, 9−bit UART Mode (19200bps), Single Supply

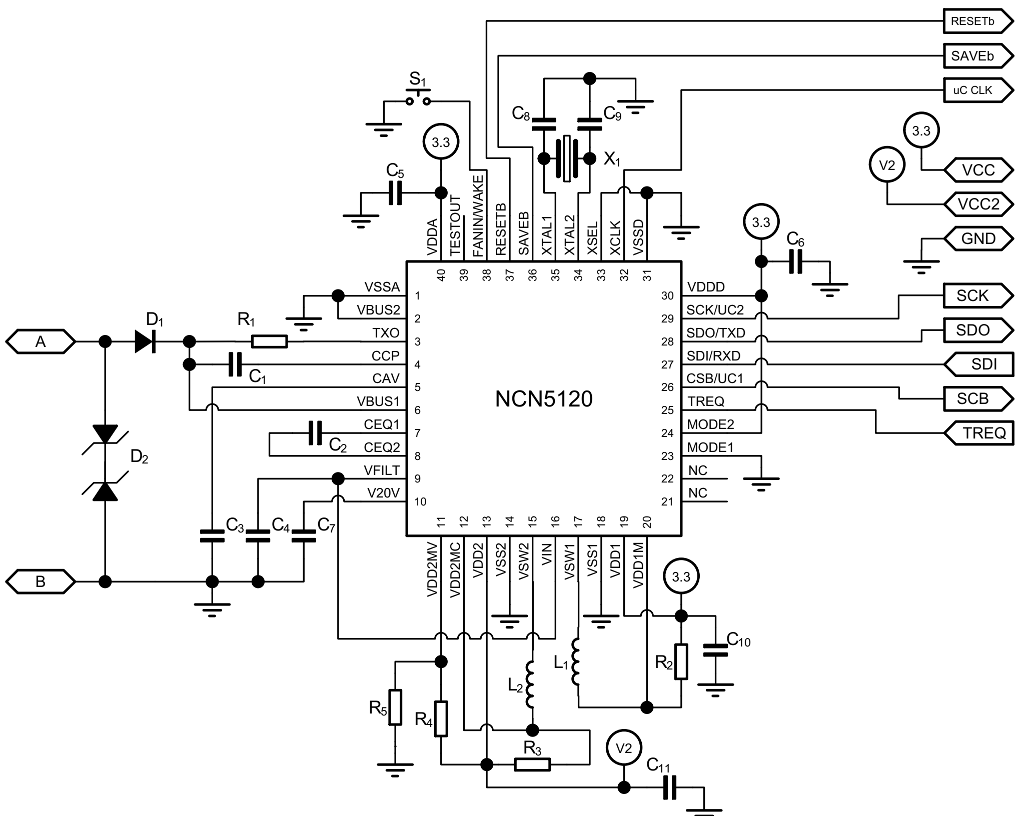


Figure 14. Typical Application Schematic NCN5120, SPI (500 kbps), Dual Supply and Wake−up

TYPICAL APPLICATION SCHEMATICS

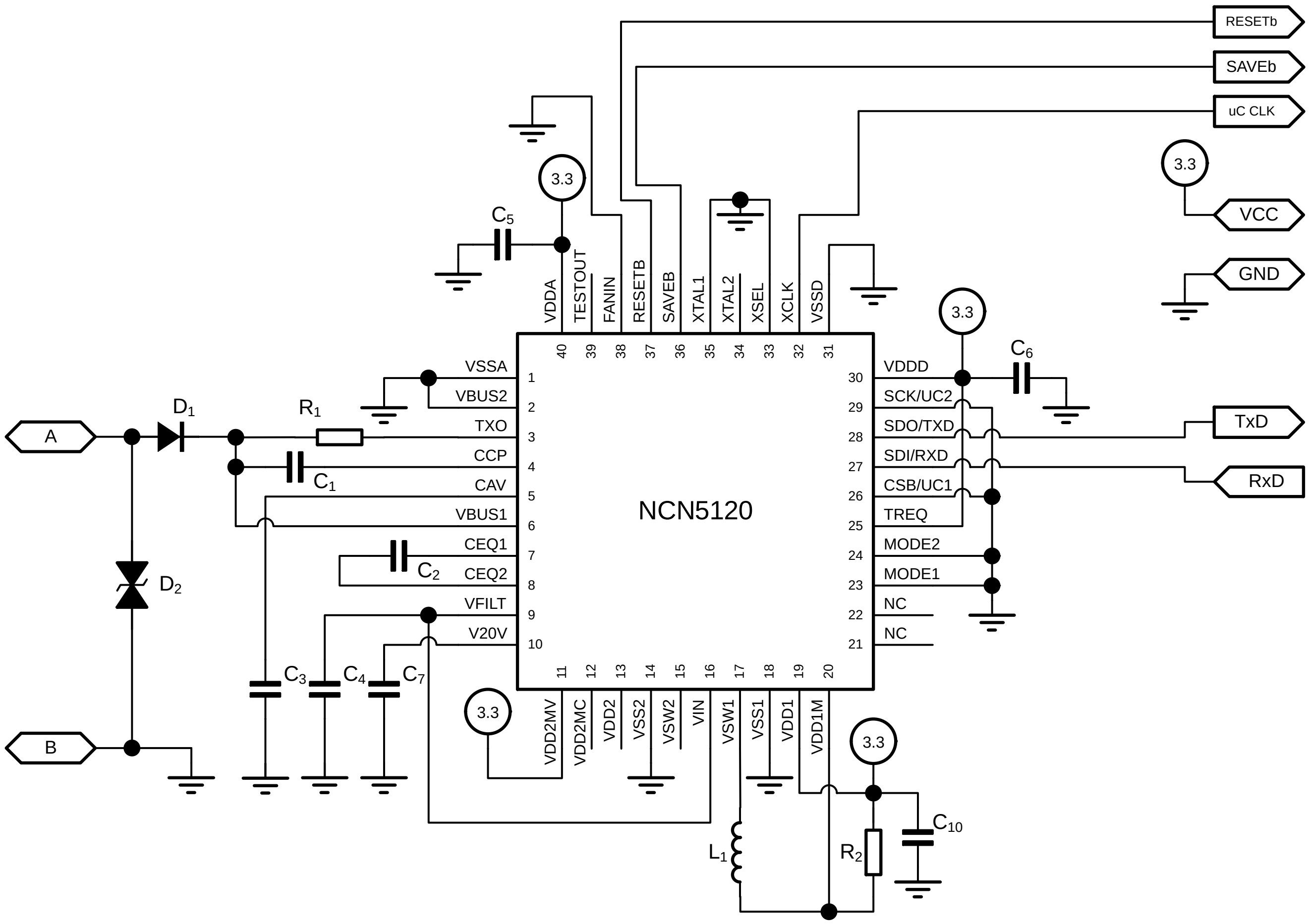


Figure 15. Typical Application Schematic NCN5120, Analog Mode, Single Supply, 1.0 mA/ms Current Slope (FANIN/WAKE−pin Pulled to Ground)

Table 6. EXTERNAL COMPONENTS LIST AND DESCRIPTION

Comp.	Function	Min	Value	Max	Unit	Remarks	Notes
C_1	AC coupling capacitor	38	47	56	nF	50 V, Ceramic	9
C_2	Equalization capacitor	4.2	4.7	5.2	nF	25 V, Ceramic	9
C_3	Capacitor to average bus DC voltage	80	100	120	nF	50 V, Ceramic	9
C_4	Storage and filter capacitor VFILT	80	100	1000	μF	35 V	9
C_5	VDDA HF rejection capacitor	80	100		nF	6.3 V, Ceramic	
C_6	VDDD HF rejection capacitor	80	100		nF	6.3 V, Ceramic	
C_7	Load Capacitor V20V		1		μF	35 V, Ceramic, ESR < 2 Ω	14, 15
C_8, C_9	Parallel capacitor X−tal	8	10	12	pF	6.3 V, Ceramic	10
C_{10}	Load capacitor VDD1	8	10		μF	6.3 V, Ceramic, ESR < 0.1 Ω	
C_{11}	Load capacitor VDD2	8	10		μF	Ceramic, ESR < 0.1 Ω	11
R_1	Shunt resistor for transmitting	19.8	22	24.2	Ω	1 W	9
R_2	DC1 sensing resistor	0	1	10	Ω	1/16 W	
R_3	DC2 sensing resistor	0	1	10	Ω	1/16 W	
R_4	Voltage divider to specify VDD2		10		kΩ	1/16 W, see p17 for calculating the exact value	
R_5			27		kΩ		
L_1, L_2	DC1/DC2 inductor		220		μH		
D_1	Reverse polarity protection diode		SS16				12
D_2	Voltage suppressor		1SMA40CA				
X_1	Crystal oscillator		FA−238				13
S_1	Push Button						

9. Component must be between minimum and maximum value to fulfill the KNX requirement.
10. Actual capacitor value depends on X1. If an crystal oscillator is chosen, the capacitors need to be chosen in such a way that the frequency equals 16 MHz. Capacitors are not required if external clock signal is supplied.
11. Voltage of capacitor depends on VDD2 value defined by R4 and R5. See p16 for more details on defining VDD2 voltage value.
12. Reverse polarity diode is mandatory to fulfill the KNX requirement.
13. A clock signal of 16 MHz (50 ppm or less) is mandatory to fulfill the KNX requirements. Or a crystal oscillator of 16 MHz, 50 ppm is used (C8 and C9 need to be of the correct value based on the crystal datasheet), or an external 16 MHz clock is used.
14. It’s allowed to short this pin to VFILT−pin.
15. High capacitor value might affect the start up time.

ANALOG FUNCTIONAL DESCRIPTION

Because NCN5120 follows the KNX standard only a brief description of the KNX related blocks is given in this datasheet. Detailed information on the KNX Bus can be found on the KNX website (www.knx.org) and in the KNX standards.

KNX Bus Interfacing

Each bit period is 104 μs. Logic 1 is simply the DC level of the bus voltage which is between 20 V and 33 V. Logic 0 is encoded as a drop in the bus voltage with respect to the DC level. Logic 0 is known as the active pulse.

The active pulse is produced by the transmitter and is ideally rectangular. It has a duration of 35 μs and a depth between 6 and 9 V (V_{act}). Each active pulse is followed by an equalization pulse with a duration of 69 μs. The latter is an abrupt jump of the bus voltage above the DC level followed by an exponential decay down to the DC level. The equalization pulse is characterized by its height V_{eq} and the voltage V_{end} reached at the end of the equalization pulse.

See the KNX Twisted Pair Standard (KNX TP1−256) for more detailed KNX information.

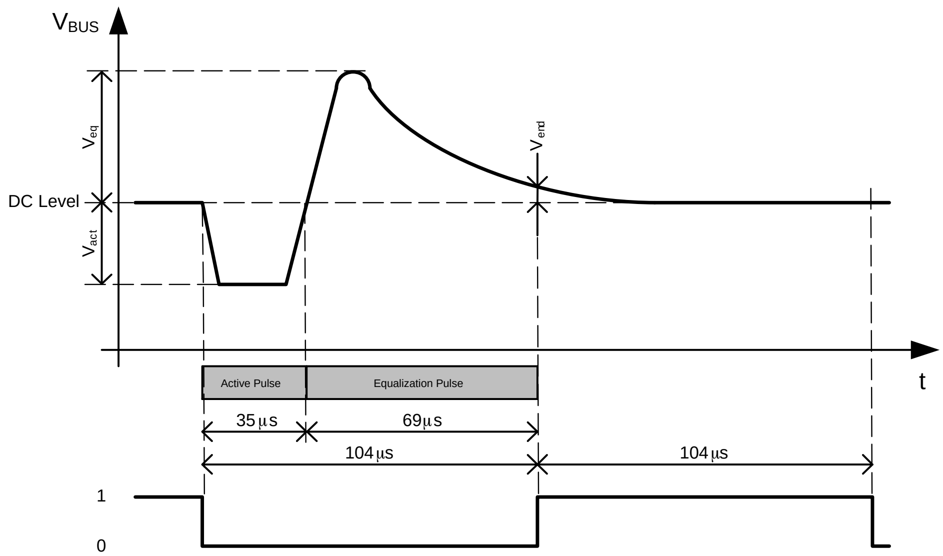


Figure 16. KNX Bus Voltage versus Digital Value

KNX Bus Transmitter

The purpose of the transmitter is to produce an active pulse (see Figure 16) between 6 V and 9 V regardless of the bus impedance (Note 1). In order to do this the transmitter will sink as much current as necessary until the bus voltage drops by the desired amount.

KNX Bus Receiver

The receiver detects the beginning and the end of the active pulse. The detection threshold for the start of the active pulse is −0.45 V (typ.) below the average bus voltage. The detection threshold for the end of the active pulse is −0.2 V (typ.) below the average bus voltage giving a hysteresis of 0.25 V (typ.).

Bus Coupler

The role of the bus coupler is to extract the DC voltage from the bus and provide a stable voltage supply for the purpose of powering the NCN5120. This stable voltage supplied by the bus coupler will follow the average bus voltage. The bus coupler also makes sure that the current drawn from the bus changes very slowly. For this a large filter capacitor is used on the VFILT−pin. Abrupt load current steps are absorbed by the filter capacitor. Long−term stability requires that the average bus coupler input current is equal to the average (bus coupler) load current

The bus coupler is implemented as a linear voltage regulator. For efficiency purpose, the voltage drop over the bus coupler is kept minimal (see Table 4).

KNX Impedance Control

The impedance control circuit defines the impedance of the bus device during the active and equalization pulses. The impedance can be divided into a static and a dynamic component, the latter being a function of time. The static impedance defines the load for the active pulse current and the equalization pulse current. The dynamic impedance is produced by a block, called an equalization pulse generator, that reduces the device current consumption (i.e. increases the device impedance) as a function of time during the equalization phase so as to return energy to the bus.

1. Maximum bus impedance is specified in the KNX Twisted Pair Standard

Fixed and Adjustable DC−DC Converter

The device contains two DC−DC buck converters, both supplied from VFILT.

DC1 provides a fixed voltage of 3.3 V. This voltage is used as an internal low voltage supply (V_{DDA} and V_{DDD}) but can also be used to power external devices (VDD1−pin). DC1 is automatically enabled during the power−up procedure (see Analog State Diagram, p20).

DC2 provides a programmable voltage by means of an external resistor divider. It is not used as an internal voltage supply making it not mandatory to use this DC−DC converter (if not needed, tie the VDD2MV pin to VDD1, see also Figure 13).

DC2 can be monitored (<VDD2>, see System Status Service, p34), and/or disabled by a command from the host controller (<DC2EN>, see Analog Control Register 0, p51). DC2 will only be enabled when VFILT−bit is set (<VFILT>, see System Status Service, p34). The status of DC2 can be monitored (<VDD2>, see System Status Service, p34).

The voltage divider can be calculated as next:

$$R_4 = \frac{R_5 \times R_{VDD2M}}{R_5 + R_{VDD2M}} \times \frac{V_{DD2} - 3.3}{3.3} \qquad \text{(eq. 1)}$$

Both DC−DC converters make use of slope control to improve EMC performance (see Table 5).

To operate DC1 and DC2 correctly, the voltage on the VIN−pin should be higher than the highest value of DC1 and DC2.

Although both DC−DC converters are capable of delivering 100 mA, the maximum current capability will not always be usable. One always needs to make sure that the KNX bus power consumption stays within the KNX specification. The maximum allowed current for the DC−DC converters and V20V regulator can be estimated as next:

$$\frac{V_{BUS} \times \left(I_{BUS} - I_{20V}\right)}{2 \times \left[\left(V_{DD1} \times I_{DD1}\right) + \left(V_{DD2} \times I_{DD2}\right)\right]} \geq 1 \qquad \text{(eq. 2)}$$

I_{BUS} will be limited by the KNX standard and should be lower or equal to $I_{coupler}$ (see Table 4). Minimum V_{BUS} is 20 V (see KNX standard). V_{DD1} and V_{DD2} can be found back in Table 4. I_{DD1}, I_{DD2} and I_{20V} must be chosen in a correct way to be in line with the KNX specification (Note 2).

Although DC2 can operate up to 21V, it will not be possible to generate this 21V under all operating conditions. For relay applications this could give certain limitations. See application note AND9149 for more info on draving relays.

See application note AND9135 for defining the optimum inductor and capacitor of the DC-DC converters.

V20V Regulator

This is the 20 V low drop linear voltage regulator used to supply external devices. As it draws current from VFILT, this current is seen without any power conversion directly at the VBUS1 pin.

The V20V regulator starts up by default but can be disabled by a command from the host controller (<V20VEN>, see Analog Control Register 0, p51). When the V20V regulator is not used, no load capacitor needs to be connected (see C7 of Figures 13, 14 and 15). Connect V20V−pin with VFILT−pin in this case.

V20V regulator will only be enabled when VFILT−bit is set (<VFILT>, see System Status Service, p34). The host controller can also monitor the status of the regulator (<V20V>, see System Status Service, p34).

Xtal Oscillator

An analog oscillator cell generates the main clock of 16 MHz. This clock is directly provided to the digital block to generate all necessary clock domains.

An input pin XSEL is foreseen to enable the use of a quartz crystal (see Figure 18) or an external clock generator (see Figure 19) to generate the main clock.

The XCLK−pin can be used to supply a clock signal of 8 MHz to the host controller. The frequency of this clock signal can be doubled or switched off by a command from the host controller (<XCLKFREQ> and <XCLKEN>, see Analog Control Register 0, p51).

After power−up, a 4 MHz (Note 3) clock signal will be present on the XCLK−pin during Stand−By. When Normal State is entered, a 8 or 16 MHz clock signal will be present on the XCLK−pin. See also Figure 21.

When Normal State is left and Stand−By State is entered due to an issue different than an Xtal issue, the 8 or 16 MHz clock signal will still be present on the XCLK−pin during the Stand−By State. If however Stand−By is entered from Normal State due to an Xtal issue, the 4 MHz clock signal will be present on the XCLK−pin. See also Table 7.

FANIN/WAKE−pin

The FANIN/WAKE−pin has a double purpose. First of all it defines the maximum allowed bus current and bus current slopes. If the FANIN/WAKE−pin is kept floating or pulled high, NCN5120 will limit the KNX bus current slopes to 0.5 mA/ms at all times. NCN5120 will also limit the KNX bus current to 30mA during start−up. During normal operation, NCN5120 is capable of taking up to 13 mA (= Icoupler) from the KNX bus for supplying external loads (DC1, DC2 and V20V). Because NCN5120 will not limit the KNX bus current to 13 mA during normal operation, it's up to the user to make sure that the Icoupler bus current does not go above 13 mA (for FANIN/WAKE−pin floating or high).

2. The formula is for a typical KNX application. It's only given as guidance and does not guarantee compliance with the KNX standard.
3. The 4 MHz clock signal is internally generated and will be less accurate as the crystal generated clock signal of 8 or 16 MHz.

If the FANIN/WAKE−pin is pulled to ground the operation is similar as above with the exception that the KNX bus current slopes will be limited to 1 mA/ms at all times, the KNX bus current will be limited to 60 mA during start−up and the up to 26 mA (Icoupler) can be taken from the KNX bus during normal operation. Definitions for Start−Up and Normal Operation (as given above) can be found in the KNX Specification.

The FANIN/WAKE−pin can also be used to exit from Sleep Mode (see p19). When in Sleep Mode, a low level on the FANIN/WAKE−pin initiates the power−up procedure of the device. Because FANIN/WAKE−pin has an internal pull−up a simple push button can be used to exit Sleep Mode (see also Figure 14). This functionality is not available when the FANIN/Wake−pin is pulled to ground.

When using the FANIN/WAKE−pin, timings must be respected (see Table 5 and Figure 8).

RESETB− and SAVEB−pin

The RESETB signal can be used to keep the host controller in a reset state. When RESETB is low this indicates that the bus voltage is too low for normal operation and that the fixed DC−DC converter has not started up. It could also indicate a Thermal Shutdown (TSD). The RESETB signal also indicates if communication between host and NCN5120 is possible.

The SAVEB signal indicates correct operation. When SAVEB goes low, this indicates a possible issue (loss of bus power or too high temperature) which could trigger the host controller to save critical data or go to a save state.

RESETB− and SAVEB−pin are open−drain pins with an internal pull−up resistor to V_{DDD}.

Voltage Supervisors

NCN5120 has different voltage supervisors monitoring VBUS, VFILT, VDD2 and V20V. The general function of a voltage supervisor is to detect when a voltage is above or below a certain level. The levels for the different voltages monitored can be found back in Table 4 (see also Figures 4, 5, 6 and 7).

The status of the voltage supervisors can be monitored by the host controller (see System Status Service, p34).

Depending on the voltage supervisor outputs, the device can enter different states (see Analog State Diagram, p20).

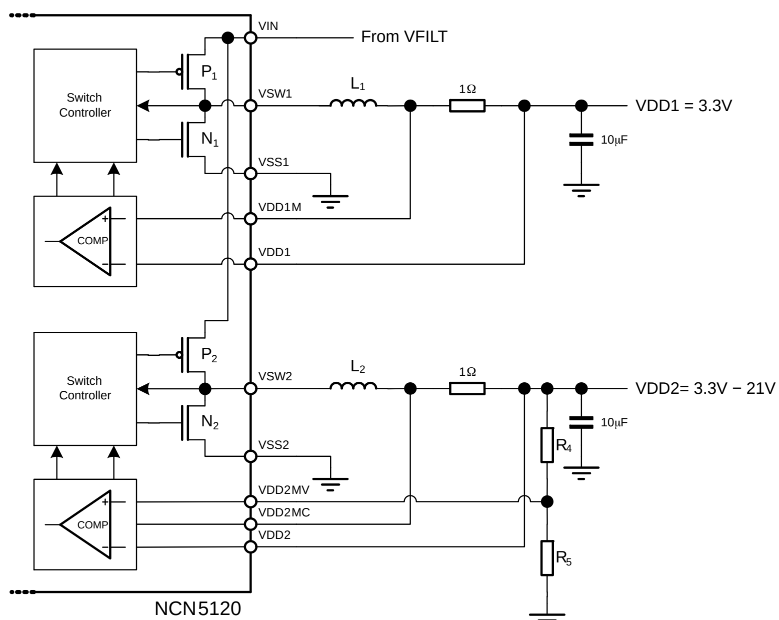


Figure 17. Fixed (VDD1) and Adjustable (VDD2) DC−DC Converter

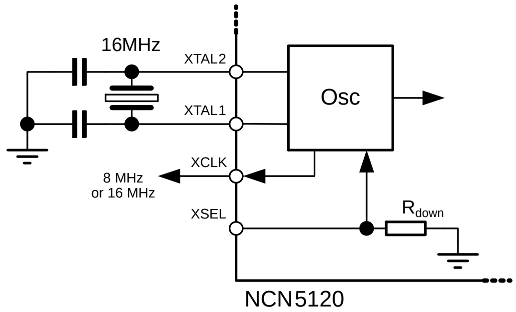


Figure 18. XTAL Oscillator

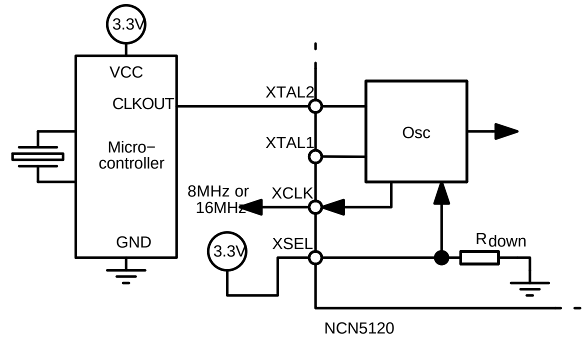


Figure 19. External Clock Generator

Table 7. STATUS OF SEVERAL BLOCKS DURING THE DIFFERENT (ANALOG) STATES

State	Osc	XCLK	VDD1	VDD2/V20V	SPI/UART	KNX
Reset	Off	Off	Off	Off	Inactive	Inactive
Start−Up	Off	Off	Start−up	Off	Inactive	Inactive
Stand−By (Note 16)	Off	4 MHz	On	Start−Up	Active	Inactive (Note 21)
Stand−By (Note 17)	On (Note 19)	On (Note 19)	On	On (Note 20)	Active	Inactive (Note 21)
Normal	On	On (Note 18)	On	On	Active	Active
Sleep	Off	Off	Off	Off	Inactive	Inactive

16. Only valid when entering Stand−By from Start−Up State.
17. Only valid when entering Stand−By from Normal State.
18. 8 MHz
19. 4 MHz signal if Stand−By state was entered due to oscillator issue. Otherwise 8 MHz clock signal.
20. Only operational if Stand−By state was not entered due to VDD2 or V20V issue.
21. Under certain conditions KNX bus is (partly) active. See Digital State Diagram for more details.

Temperature Monitor

The device produces an over−temperature warning (TW) and a thermal shutdown warning (TSD). Whenever the junction temperature rises above the Thermal Warning level (T_{TW}), the SAVEB−pin will go low to signal the issue to the host controller. Because the SAVEB−pin will not only go low on a Thermal Warning (TW), the host controller needs to verify the issue by requesting the status (<TW>, see System Status Service, p34). When the junction temperature is above TW, the host controller should undertake actions to reduce the junction temperature and/or store critical data.

When the junction temperature reaches Thermal Shutdown (T_{TSD}), the device will go to the Reset State. The Thermal Shutdown will be stored (<TSD>, see Analog Status Register, p52) and the analog and digital power supply will be stopped (to protect the device). The device will stay in the Reset State as long as the temperature stays above T_{TSD}.

If the temperature drops below T_{TSD}, Start−Up State will be entered (see also Figure 20). At the moment VDD1 is back up and the OTP memory is read, Stand−By State will be entered and RESETB will go high. The Xtal oscillator will be started. Once the temperature has dropped below T_{TW} and all voltages are high enough, Normal State will be entered. SAVEB will go high and KNX communication is back possible.

The TW−bit will be reset at the moment the junction temperature drops below T_{TW}. The TSD−bit will only be reset when the junction temperature is below T_{TSD} and the <TSD> bit is read (see Analog Status Register, p52).

Figure 9 gives a better view on the temperature monitor.

Sleep Mode

Sleep Mode can be entered by setting the SLP−bit (<SLP>, see Analog Control Register 1, p52). Leaving Sleep Mode can only be done by means of a (wake) pulse on the FANIN/WAKE−pin (or a POR). An exit from Sleep Mode can be verified by the host controller (<SLP>, see Analog Status Register, p52).

It's not possible to enter Sleep Mode when the FANIN/WAKE−pin is pulled low (see p17).

See Table 7 for the status of several blocks during Sleep Mode.

Watchdog

NCN5120 provides a Watchdog function to the host controller. The Watchdog function can be enabled by means of the WDEN−bit (<WDEN>, see Watchdog Register, p51).

Once this bit is set to ‘1’, the host controller needs to re−write this bit to clear the internal timer before the Watchdog Timeout Interval expires (Watchdog Timeout Interval = <WDT>, see Watchdog Register, p51).

In case the Watchdog is acknowledged too early (before t_{WDPR}) or not within the Watchdog Timeout Interval (t_{WDTO}), the RESETB−pin will be made low (= reset host controller).

Table 8 gives the Watchdog timings t_{WDTO} and t_{WDPR}. Details on <WDT> can be found in the Watchdog Register, p51.

Table 8. WATCHDOG TIMINGS

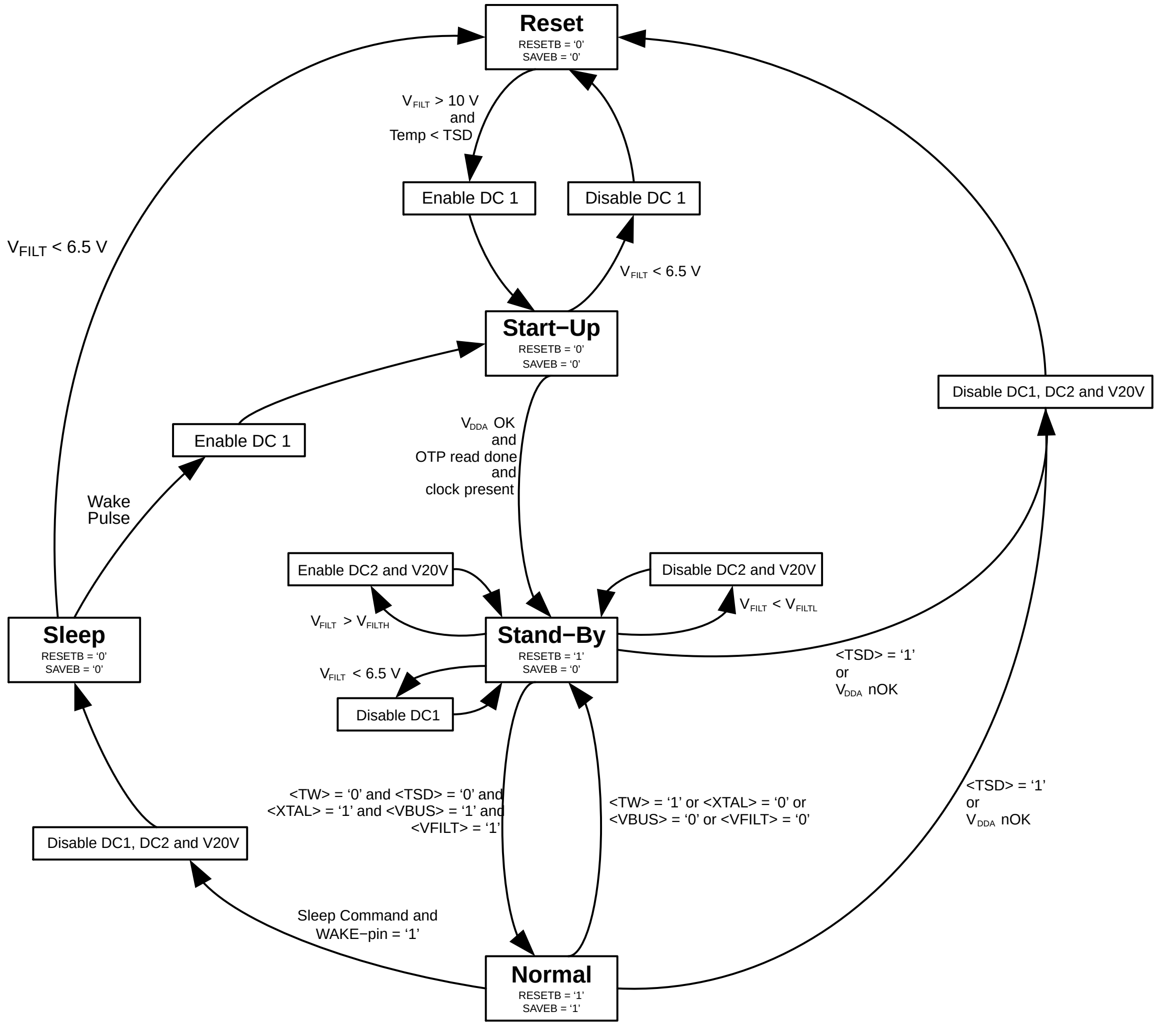
WDT[3:0]	t_{WDTO} [ms]	t_{WDPR} [ms]
0000	33	2
0001	66	4
0010	98	6
0011	131	8
0100	164	10
0101	197	12
0110	229	14
0111	262	16
1000	295	18
1001	328	20
1010	360	23
1011	393	25
1100	426	27
1101	459	29
1110	492	30
1111	524	31

Analog State Diagram

The analog state diagram of NCN5120 is given in Figure 20. The status of the oscillator, XCLK−pin, DC−DC converters, V20V regulator, serial and KNX communication during the different (analog) states is given in Table 7.

Figure 21 gives a detailed view on the start−up behavior of NCN5120. After applying the bus voltage, the filter capacitor starts to charge. During this Reset State, the current drawn from the bus is limited to $I_{coupler}$ (for details see the KNX Standards). Once the voltage on the filter capacitor reaches 10 V (typ.), the fixed DC−DC converter (powering VDDA) will be enabled and the device enters the Start−Up State. When V_{DD1} gets above 2.8 V (typ.), the OTP memory is read out to trim some analog parameters (OTP memory is not accessible by the user). When done, the Stand−By State is entered and the RESETB−pin is made high. If at this moment V_{BUS} is above V_{BUSH}, the VBUS−bit will be set (<VBUS>, see System Status Service, p34). After aprox. 2 ms the Xtal oscillator will start. When V_{FILT} is above V_{FILTH} DC2 and V20V will be started. When the Xtal oscillator has started, no Thermal Warning (TW) or Thermal Shutdown (TSD) was detected and the VBUS−, VFILT−, VDD2− and V20V−bits are set, the Normal State will be entered and SAVEB−pin will go high.

Figure 22 gives a detailed view on the shut−down behavior. If the KNX bus voltage drops below V_{BUSL} for more than t_{bus_filter}, the VBUS−bit will be reset (<VBUS>, see System Status Service, p34) and the Standy−By State is entered. SAVEB will go low to signal this. When VFILT drops below V_{FILTL}, DC2 and the V20V regulator will be switched off. When VFILT drops below 6.5 V (typ), DC1 will be switched off and V_{DD1} drops below 2.8 V (typ.) the device goes to Reset State (RESETB low).



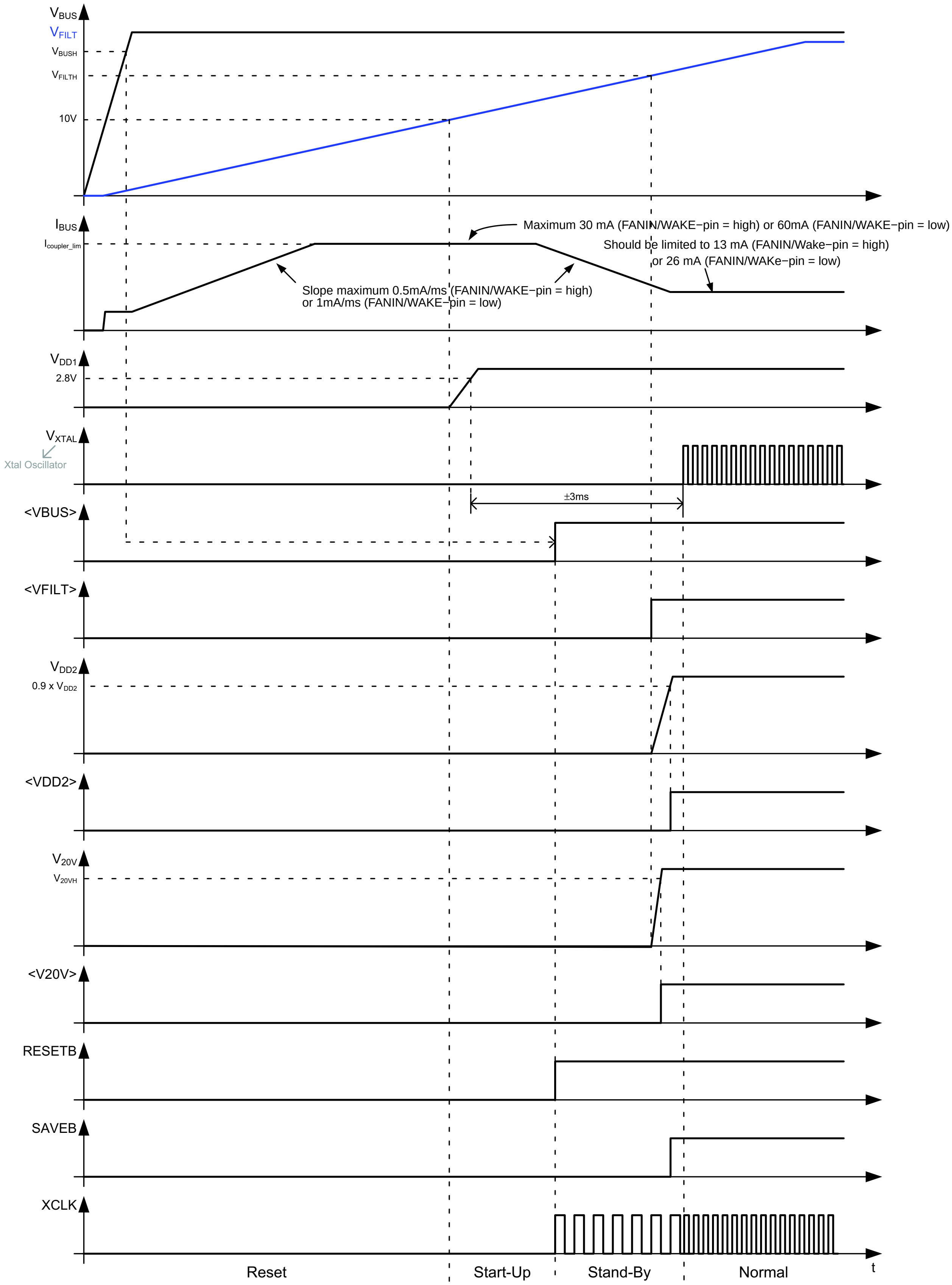
Remarks:

− <TW>, <TSD>, <XTAL, <VBUS> and <VFILT> are internal status bits which can be verified with the System State Service (with exception of <TSD> for which Internal Register Read should be used).

− Although Reset State could be entered from Normal State on a TSD, Stand−By State will be entered first due to a TW.

− Enabling of DC2 and V20V will depend on the <DC2EN> and <V20VEN> bits in Analog Control Register 0.

Figure 20. Analog State Diagram



Remarks:
VDD1 directly connected to VDDA.

Figure 21. Start−Up Behavior

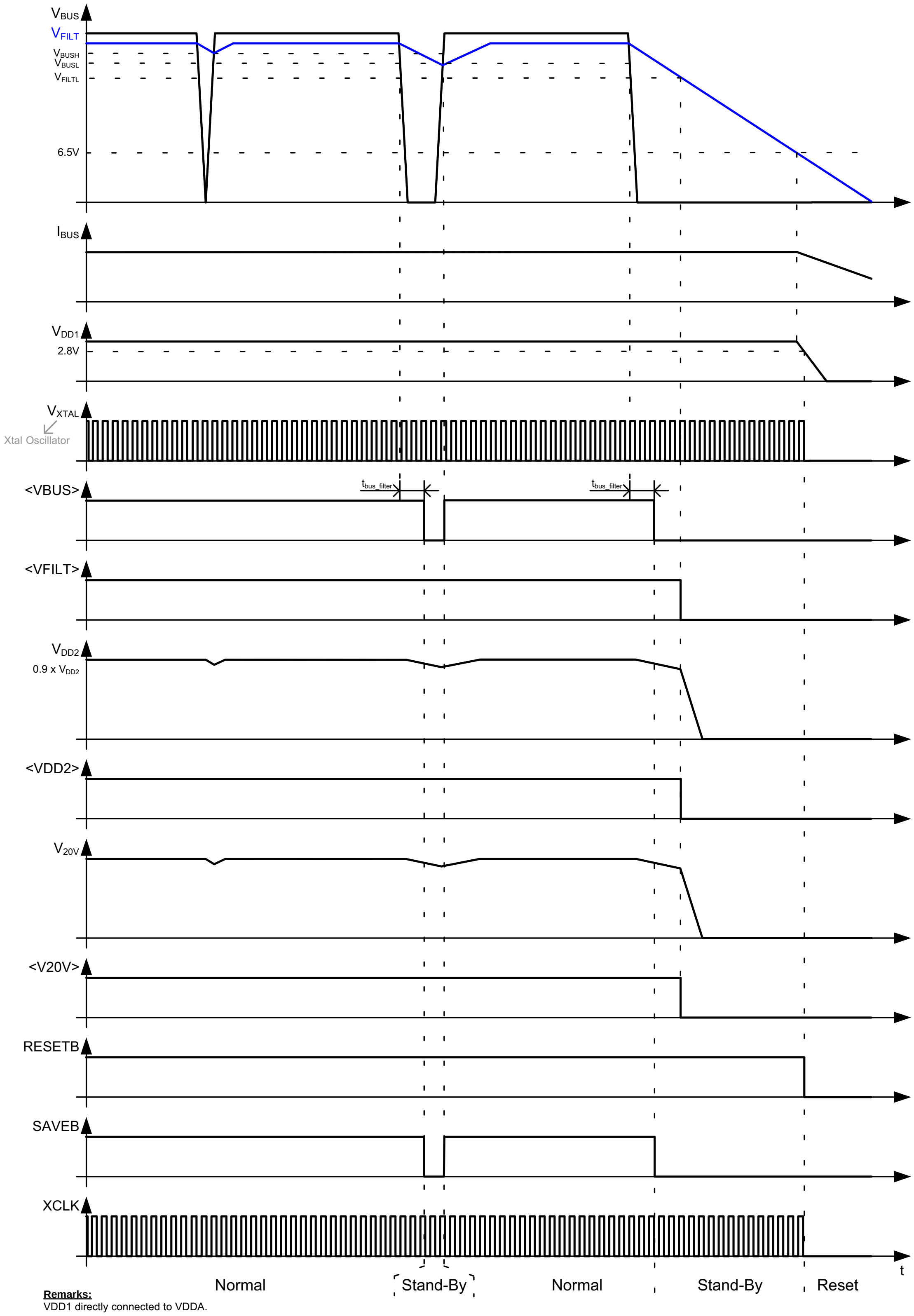


Figure 22. Shut−Down Behavior

Interface Mode

The device can communicate with the host controller by means of a UART interface or an SPI interface. The selection of the interface is done by the pins MODE1, MODE2, TREQ, SCK/UC2 and CSB/UC1.

Table 9. INTERFACE SELECTION

TREQ	MODE2	MODE1	SCK/UC2	CSB/UC1	SDI/RXD	SDO/TXD	Description
0	0	0	0	0	RXD	TXD	9−bit UART−Mode, 19200 bps
0	0	0	0	1			9−bit UART−Mode, 38400 bps
0	0	0	1	0			8−bit UART−Mode, 19200 bps
0	0	0	1	1			8−bit UART−Mode, 38400 bps
1	0	0	X	X	Driver	Receiver	Analog Mode
TREQ	0	1	SCK (out)	CSB (out)	SDI	SDO	SPI Master, 125 kbps
TREQ	1	0					SPI Master, 500 kbps

NOTE: X = Don't Care

UART Interface

The UART interface is selected by pulling pins TREQ, MODE1 and MODE2 to ground. Pin UC2 is used to select the UART Mode (‘0’ = 9−bit, ‘1’ = 8−bit) and pin UC1 is used to select the baudrate (‘0’ = 19200 bps, ‘1’ = 38400 bps). The UART interface allows full duplex, asynchronous communication.

The difference between 8−bit mode and 9−bit mode is that in 9−bit an additional even parity bit is transmitted (with exception of the internal register read and write services where the parity bit is meaningless and should be ignored). In 8−bit mode one extra service is available (U_FrameState.ind). The SDI/RXD−pin is the NCN5120 UART receive pin and is used to send data from the host controller to the device. Pin SDO/TXD is the NCN5120 UART transmit pin and is used to transmit data between the device and the host controller. Figure 13 gives an UART application example (9−bit, 19200 bps). Data is transmitted LSB first.

Start (= 0)	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Stop (= 1)

Figure 23. 8−bit UART Mode

Start (= 0)	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Parity	Stop (= 1)

Figure 24. 9−bit UART Mode

One special UART Mode is foreseen called Analog Mode. When this mode is selected (TREQ = ‘1’, MODEx = ‘0’) an immediate connection is made with the KNX transmitter receiver (see Figure 25). Bit level coding/decoding has to be done by the host controller. Keep in mind that the signals on the SDI/RXD− and SDO/TXD−pin are inverted. Figure 15 gives an Analog Mode application example. When using the device in Analog Mode, no clock needs to be provided to the device.

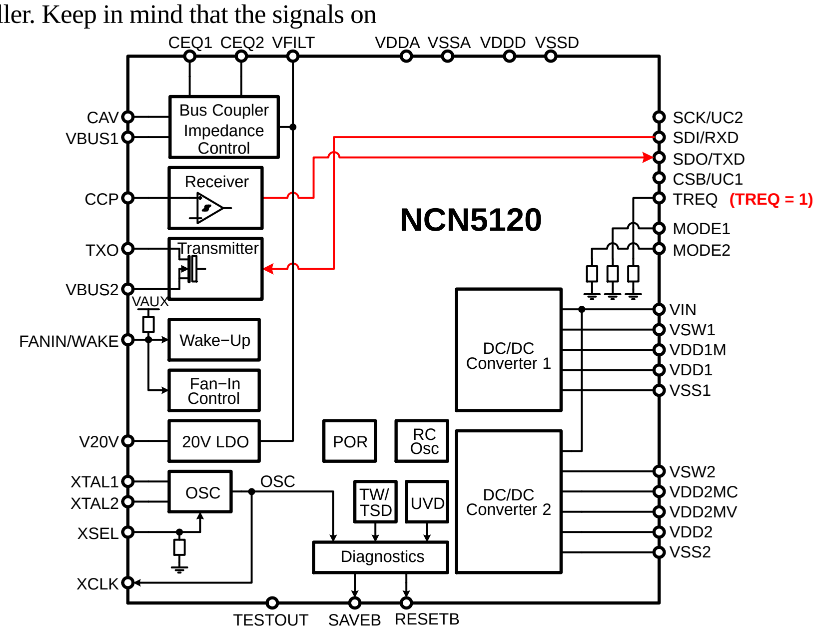


Figure 25. Analog UART Mode

SPI Interface

The SPI interface is selected by MODE1− and MODE2−pin. The baudrate is determined by which MODE−pin is pulled high (MODE1 pulled high = 125 kbps, MODE2 pulled high = 500 kbps).

The SPI interface allows full duplex synchronous communication between the device and the host controller. The interface operates in Mode 0 (CPOL and CPHA = ‘0’) meaning that the data is clocked out on the falling edge and sampled on the rising edge. The LSB is transmitted first.

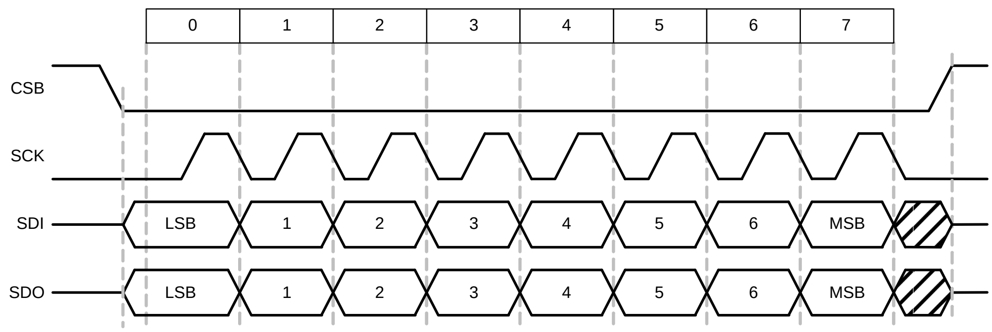


Figure 26. SPI Transfer

During SPI transmission, data is transmitted (shifted out serially) on the SDO/TXD−pin and received (shifted in serially) on the SDI/RXD−pin simultaneously. SCK/UC2 is set as output and is used as the serial clock (SCK) to synchronize shifting and sampling of the data on the SDI− and SDO−pin. The speed of this clock signal is selectable (see Table 9). The slave select line (CSB/UC1−pin) will go low during each transmission allowing to selection the host controller (CSB−pin is high when SPI is in idle state).

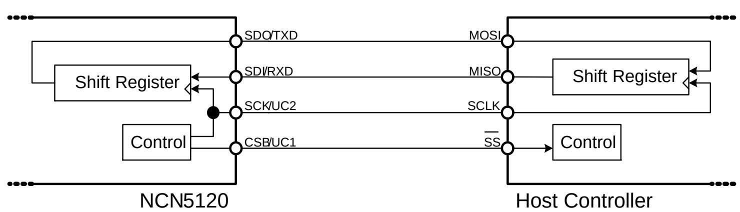


Figure 27. SPI Master

In an SPI network only one SPI Master is allowed (in this case NCN5120). To allow the host controller to communicate with the device the TREQ−pin can be used (Transmit Request). When NCN5120 detects a negative edge on TREQ, the device will issue dummy transmission of 8 bits which will result in a transmission of data byte from the host controller to the device. See Figure 12 for details on the timings. See Figure 14 for an SPI application example.

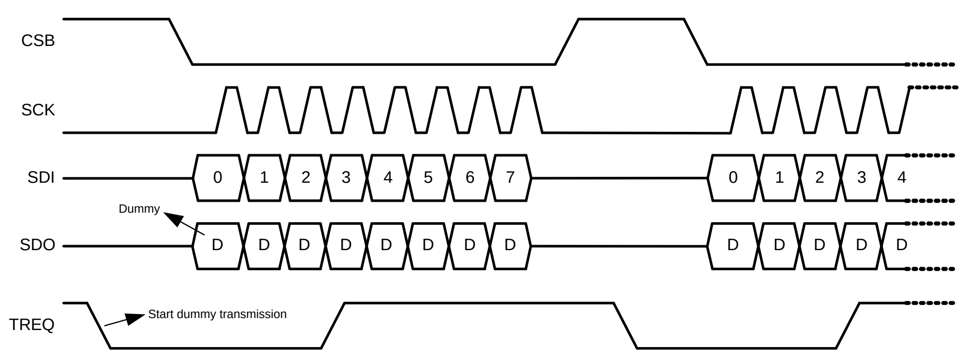


Figure 28. Transmission Request

DIGITAL FUNCTIONAL DESCRIPTION

The implementation of the Data Link Layer as specified in the KNX standard is divided in two parts. All functions related to communication with the Physical Layer and most of the Data Link Layer services are inside NCN5120, the rest of the functions and the upper communication layers are implemented into the host controller (see Figure 29).
The host controller is responsible for handling:

- Checksum
- Parity
- Addressing
- Length

The NCN5120 is responsible for handling:

- Checksum
- Parity
- Acknowledge
- Repetition
- Timing

Digital State Diagram

The digital state diagram is given in Figure 30.

The current mode of operation can be retrieved by the host controller at any time (when RESETB−pin is high) by issuing the U_SystemStat.req service and parsing back U_SystemStat.ind service (see System Status Service, p34).

Table 10. NCN5120 DIGITAL STATES

State	Explanation
RESET	Entered after Power On Reset (POR) or in response to a U_Reset.req service issued by the host controller. In this state NCN5120 gets initialized, all features disabled and services are ignored and not executed.
POWER−UP / POWER−UP STOP	Entered after Reset State or when VBUS, VFILT or Xtal are not operating correctly (operation of VBUS, VFILT and XTAL can be verified by means of the System Status Service, p34). Communication with KNX bus is not allowed. U_SystemStat.ind can be used to verify this state (code 00).
SYNC	NCN5120 remains in this state until it detects silence on the KNX bus for at least 40 Tbits. Although the receiver of NCN5120 is on, no frames are transmitted to the host controller. U_SystemStat.ind can be used to verify this state (code 01).
STOP	This state is useful for setting−up NCN5120 safely or temporarily interrupting reception from the KNX bus. U_SystemStat.ind can be used to verify this state (code 10).
NORMAL	In this state the device is fully functional. Communication with the KNX bus is allowed. U_SystemStat.ind can be used to verify this state (code 11).

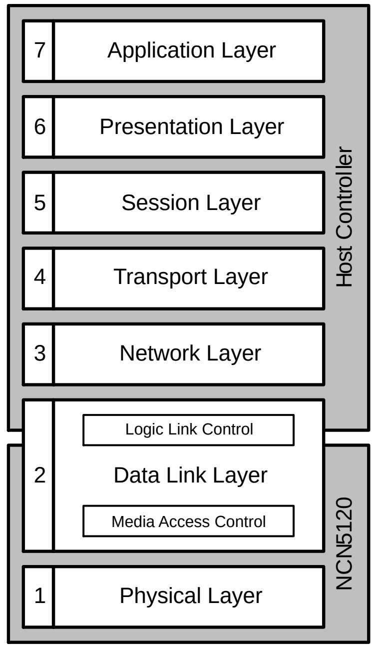


Figure 29. OSI Model Reference

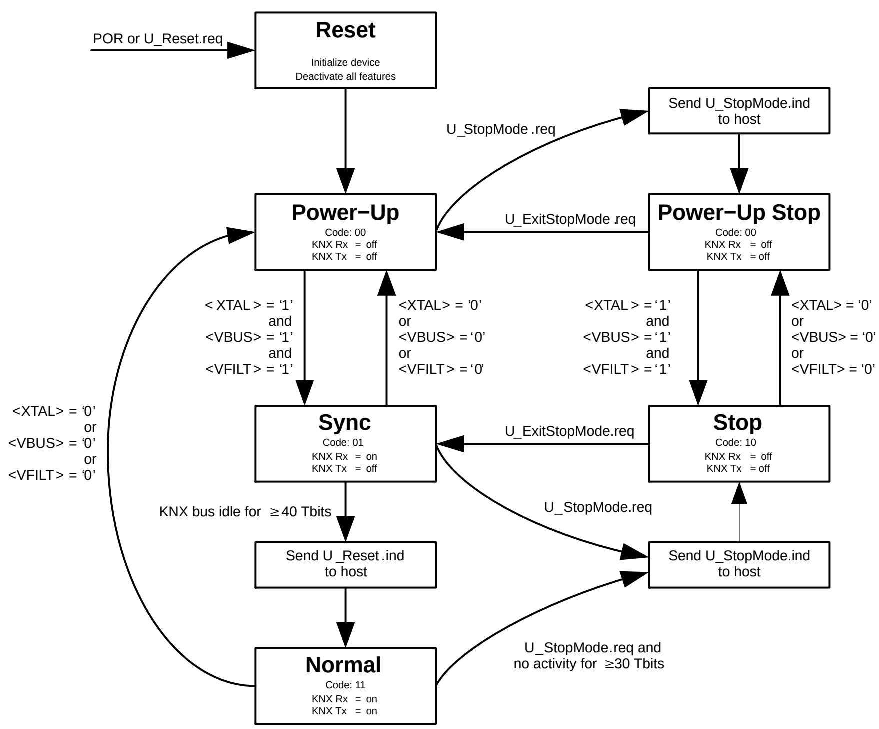


Figure 30. Digital State Diagram

Services

Execution of services depends on the digital state (Figure 30). Certain services are rejected if received outside the Normal State. The following table gives a view of all services and there acceptance during the different digital states.

Table 11. ACCEPTANCE OF SERVICES

Service	State				
	Normal	Stop	Sync	Power−Up	Bus Monitor
U_Reset.req	E	E	E	E	E
U_State.req	E	E	E	E	I
U_SetBusy.req	E	E	E	E	I
U_QuitBusy.req	E	E	E	E	I
U_Busmon.req	E	E	E	E	I
U_SetAddress.req	E	E	E	E	I
U_SetRepetition.req	E	E	E	E	I
U_L_DataOffset.req	E	E	E	E	I
U_SystemStat.req	E	E	E	E	I
U_StopMode.req	E	I	E	E	E
U_ExitStopMode.req	I	E	I	I	E
U_Ackn.req	E	R	R	R	I
U_Configure.req	E	E	E	E	I
U_IntRegWr.req	E	E	E	E	E
U_IntRegRd.req	E	E	E	E	E
U_L_DataStart.req	E	R	R	R	I
U_L_DataCont.req	E	R	R	R	I
U_L_DataEnd.req	E	R	R	R	I
U_PollingState.req	E	E	E	E	I

NOTE:

Bus Monitor state is not a separate state. It is applied on top of Normal, Stop, Sync or Power−Up State.

Legend: E = service is executed

I = service is ignored (not executed and no feedback sent to the host controller)

R = service is rejected (not executed, protocol error is sent back to the host controller through U_State.ind)

See Internal Register Read Service (p36) for limitations of U_IntRegRd.req

Table 12. SERVICES FROM HOST CONTROLLER

Control Field								Service Name	Hex	Remark	Extra Following Bytes	Total Bytes
7	6	5	4	3	2	1	0					
INTERNAL COMMANDS – DEVICE SPECIFIC												
0	0	0	0	0	0	0	1	U_Reset.req	01			1
0	0	0	0	0	0	1	0	U_State.req	02			1
0	0	0	0	0	0	1	1	U_SetBusy.req	03			1
0	0	0	0	0	1	0	0	U_QuitBusy.req	04			1
0	0	0	0	0	1	0	1	U_Busmon.req	05			1
1	1	1	1	0	0	0	1	U_SetAddress.req	F1		AddrHigh AddrLow X (don't care)	4
1	1	1	1	0	0	1	0	U_SetRepetition.req	F2		RepCntrs X (don't care) X (don't care)	4
0	0	0	0	1	i	i	i	U_L_DataOffset.req	08−0C	iii = MSB byte index (0…4)		1
0	0	0	0	1	1	0	1	U_SystemState.req	0D			1
0	0	0	0	1	1	1	0	U_StopMode.req	0E			1
0	0	0	0	1	1	1	1	U_ExitStopMode.req	0F			1
0	0	0	1	0	n	b	a	U_Ackn.req	10−17	n = nack b = busy a = addressed		1
0	0	0	1	1	p	c	m	U_Configure.req	18−1F	p = auto−polling c = CRC−CCITT m = frame end with MARKER		1
0	0	1	0	1	0	a	a	U_IntRegWr.req	28−2B	aa = address of internal register	Data to be written	2
0	0	1	1	1	0	a	a	U_IntRegRd.req	38−3B			1
1	1	1	0	s	s	s	s	U_PollingState.req	E0−EE	s = slot number (0 … 14)	PollAddrHigh PollAddrLow PollState	4
KNX TRANSMIT DATA COMMANDS												
1	0	0	0	0	0	0	0	U_L_DataStart.req	80		Control Octet (CTRL)	2
1	0	i	i	i	i	i	i	U_L_DataCont.req	81−BF	i = index (1…63)	Data octet (CTRLE, SA, DA, AT, NPCI, LG, TPDU)	2
0	1	l	l	l	l	l	l	U_L_DataEnd.req	47−7F	l = last index + 1 (7 … 63)	Check Octet (FCS)	2

With respect to command length, there are two types of services from the host controller:

- Single−byte commands: the control byte is the only data sent from the host controller to NCN5120.
- Multiple−byte commands: the following data byte(s) need to be handled according to the already received control byte.

With respect to command purpose there are two types of services from the host controller:

- Internal command: does not initiate any communication on the KNX bus.
- KNX transmit data command: initiates KNX communication

Table 13. SERVICES TO HOST CONTROLLER

Control Field								Service Name	Remark	Extra Following Bytes	Total Bytes
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**				
DLL (LAYER 2) SERVICES (DEVICE IS TRANSPARENT)											
1	0	r	1	p1	p0	0	0	L_Data_Standard.ind	r = not repeated (‘1’) or repeated L_Data frame (‘0’) p1, p0 = priority		n
0	0	r	1	p1	p0	0	0	L_Data_Extended.ind			n
1	1	1	1	0	0	0	0	L_Poll_Data.ind			n
ACKNOWLEDGE SERVICES (DEVICE IS TRANSPARENT IN BUS MONITOR MODE)											
x	x	0	0	x	x	0	0	L_Ackn.ind	x = acknowledge frame		1
z	0	0	0	1	0	1	1	L_Data.con	z = positive (‘1’) or negative (‘0’) confirmation		1
CONTROL SERVICES – DEVICE SPECIFIC											
0	0	0	0	0	0	1	1	U_Reset..ind			1
sc	re	te	pe	tw	1	1	1	U_State.ind	sc = slave collision re = receive error te = transmit error pe = protocol error tw = temperature warning		1
re	ce	te	1	res	0	1	1	U_FrameState.ind	re = parity or bit error ce = checksum or length error te = timing error res = reserved		1
0	b	aa	ap	c	m	0	1	U_Configure.ind	b = reserved aa = auto−acknowledge ap = auto−polling c = CRC−CCITT m = frame end with MARKER		1
1	1	0	0	1	0	1	1	U_FrameEnd.ind			1
0	0	1	0	1	0	1	1	U_StopMode.ind			1
0	1	0	0	1	0	1	1	U_SystemStat.ind		V20V, VDD2, VBUS, VFILT, XTAL, TW, Mode	2

Each data byte received from the KNX bus is transparently transmitted to the host controller. An exception is the Acknowledge byte which is transmitted to the host controller only in bus monitoring mode. Other useful information can be transmitted to the host controller by request using internal control services.

A detailed description of the services is given on the next pages. For all figures, the MSB bit is always given on the left side no matter how the arrow is drawn.

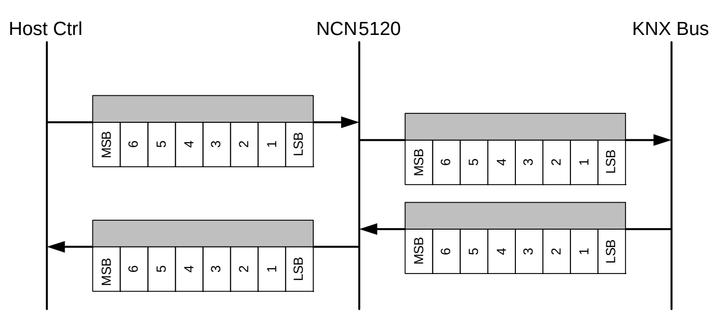


Figure 31. Bit Order of Services

Reset Service
Reset the device to the initial state.

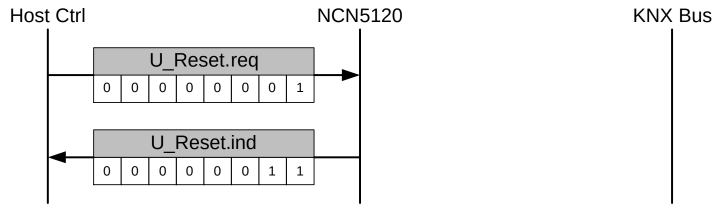


Figure 32. Reset Service

Remark: U_Reset.Ind will be send when entering Normal State (see Digital State Diagram, p26).

State Service
Get internal communication state of the device.

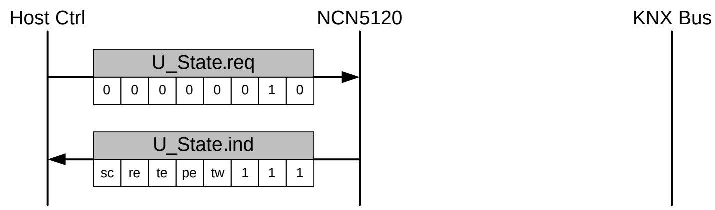


Figure 33. State Service

sc (slave collision):	'1' if collision is detected during transmission of polling state
re (receive error):	'1' if corrupted bytes were sent by the host controller. Corruption involves incorrect parity (9−bit UART only) and stop bit of every byte as well as incorrect control octet, length or checksum of frame for transmission.
te (transceiver error):	'1' if error detected during frame transmission (sending '0' but receiving '1').
pe (protocol error):	'1' if an incorrect sequence of commands sent by the host controller is detected.
tw (thermal warning):	'1' if thermal warning condition is detected.

Set Busy Service
Activate BUSY mode.

During this time and when autoacknowledge is active (see *Set Address Service* p32), NCN5120 rejects the frames whose destination address corresponds to the stored physical address by sending the BUSY acknowledge. This service has no effect if autoacknowledge is not active.

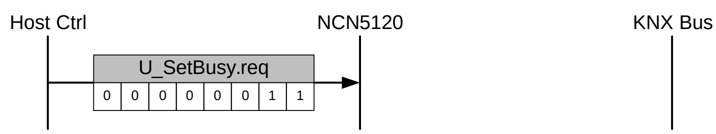


Figure 34. Set Busy Service

Remark: BUSY mode is deactivated immediately if the host controller confirms a frame by sending U_Ackn.req service.

Quit Busy Service
Deactivate the BUSY mode.

Restores back to the normal autoacknowledge behavior with ACK sent on the bus in response to addressing frame (only if autoacknowledge is active). This service has no effect if autoacknowledge is not active or BUSY mode was not set.

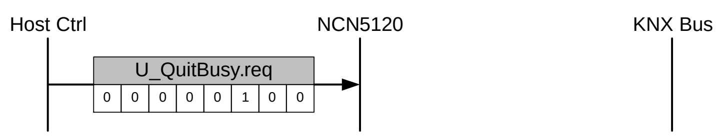


Figure 35. Quit Busy Service

Bus Monitor Service

Activate bus monitoring state.

In this mode all data received from the KNX bus is sent to the host controller without performing any filtering on Data Link Layer. Acknowledge Frames are also transmitted transparently. This state can only be exited by the Reset Service (see p31).

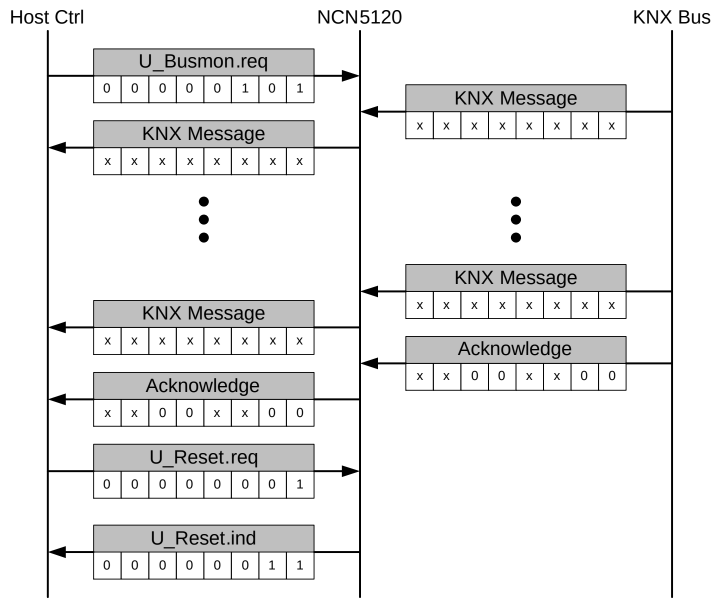


Figure 36. Bus Monitor Service

Remark:
x = don‘t care

Set Address Service

Sets the physical address of the device and activates the auto−acknowledge function.

NCN5120 starts accepting all frames whose destination address corresponds to the stored physical address or whose destination address is the group address by sending IACK on the bus. In case of an error detected during such frame reception, NCN5120 sends NACK instead of IACK.

When issued several times after each other, the first call will set the physical address and activate the auto−acknowledge. Following calls will only set the physical address because auto−acknowledge is already activated.

NCN5120 confirms activation of auto−acknowledge function by sending the U_Configure.ind service to the host controller.

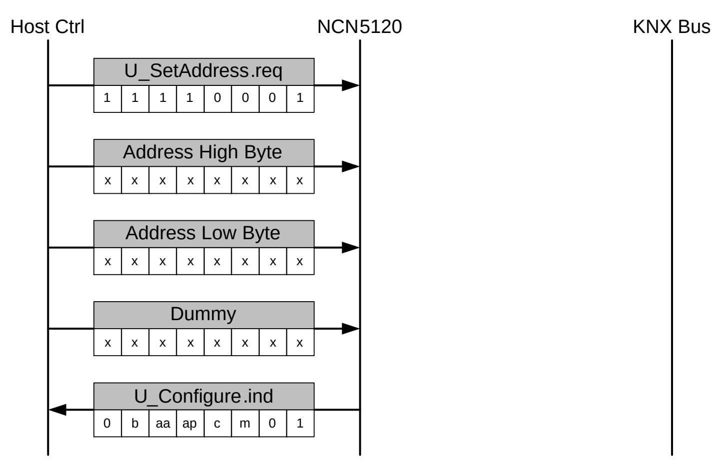


Figure 37. Set Address Service

b (busy mode): '1' if busy mode is active. Can be enabled with U_SetBusy.req (see Set Busy Service, p31) and disabled with U_QuitBusy.req service (see *Quit Busy Service,* p31) or U_Ackn.req service (see *Receive Frame Service*, p44).

aa (auto−acknowledge): '1' if auto−acknowledge feature is active. Can be enabled with U_SetAddress.req service (see *Set Address Service*, p32).

ap (auto−polling): '1' if auto−polling feature is active. This feature can be enabled with U_Configure.req service (see *Configure Service*, p35).

c (CRC−CCITT): '1' if CRC−CCITT feature is active. This feature can be enabled with U_Configure.req service (see *Configure Service*, p35).

m (frame end with MARKER): '1' when feature is active. This feature can be enabled with U_Configure.req service (see *Configure Service*, p35).

Remarks:

- Set Address Service can be issued any time but the new physical address and the autoacknowledge function will only get active after the KNX bus becomes idle.
- Autoacknowledge can only be deactivated by a Reset Service (p31)
- x = don't care
- Dummy byte can be anything. NCN5120 completely disregards this information.

Set Repetition Service

Specifies the maximum repetition count for transmitted frames when not acknowledged with IACK.

Separate counters can be set for NACK and BUSY frames. Initial value of both counters is 3.

If the acknowledge from remote Data Link Layer is BUSY during frame transmission, NCN5120 tries to repeat after at least 150 bit times KNX bus idle. The BUSY counter determines the maximum amount of times the frame is repeated. If the BUSY acknowledge is still received after the last try, an L_Data.con with a negative conformation is sent back to the host controller.

For all other cases (NACK acknowledgment received, invalid/corrupted acknowledge received or time−out after 30 bit times) NCN5120 will repeat after 50 bit times of KNX bus idle. The NACK counter determines the maximum retries. L_Data.con with a negative confirmation is send back to the host controller when the maximum retries were reached.

In worst case, the same request is transmitted (NACK + BUSY + 1) times before NCN5120 stops retransmission.

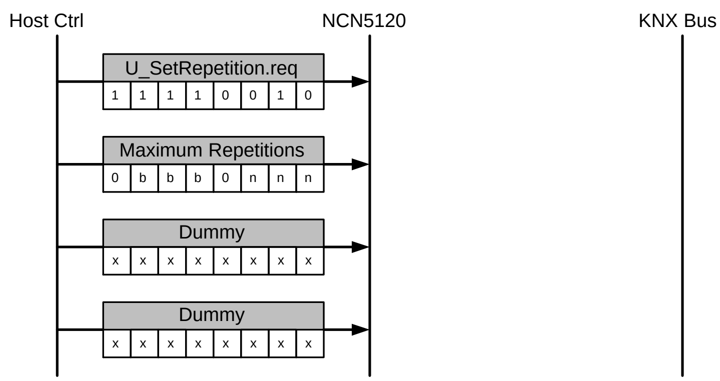


Figure 38. Set Repetition Service

bbb: BUSY counter (a frame will be retransmitted bbb−times if acknowledge with BUSY).
nnn: NACK counter (a frame will be retransmitted nnn−times if acknowledge with NACK).

Remark: Bit 3 and 7 of the second byte need to be zero ('0')!

System Status Service

Request the internal system state of the device.

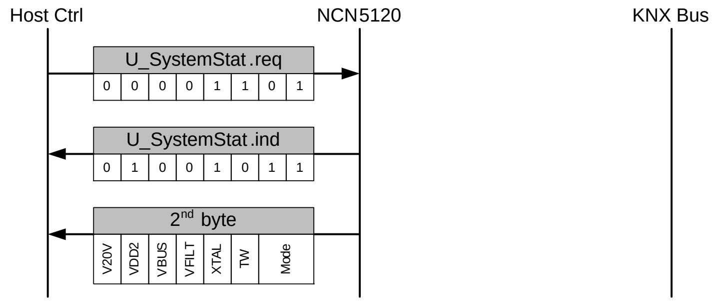


Figure 39. System State Service

V20V: ‘1’ if V20V linear voltage regulator is within normal operating range
VDD2: ‘1’ if DC2 regulator is within normal operating range
VBUS: ‘1’ if KNX bus voltage is within normal operating range
VFILT: ‘1’ if voltage on tank capacitor is within normal operating range State Service
XTAL: ‘1’ if crystal oscillator frequency is within normal operating range
TW: ‘1’ if thermal warning condition is present (can also be verified with U_State.ind service (see State Service, p31)
Mode: Operation mode (see also Digital State Diagram, p26).

Bit		Mode
1	**0**	
0	0	Power−Up
0	1	Sync
1	0	Stop
1	1	Normal

Note: SAVEB−pin is low if any of bits 3 to 7 is ‘0’ (zero) or bit 2 is ‘1’.

Stop Mode Service

Go to Stop State. A confirmation is sent to indicate that device has switched to the Stop State. See also Digital State Diagram, p26

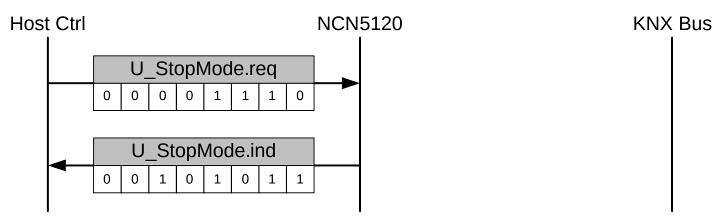


Figure 40. Stop Mode Service

Exit Stop Mode Service

Request transition from Stop to Sync State. An acknowledge service is send later to confirm that device has switched from Sync to Normal State. See also Digital State Diagram, p26.

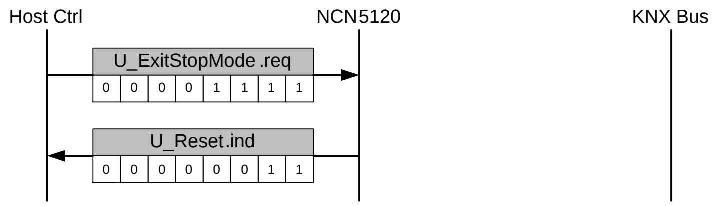


Figure 41. Exit Stop Mode Service

Configure Service

Activate additional features (which are disabled after reset).

U_Configure.ind service is send back to the host controller at the exact moment when the new features get activated. This is done during bus idle or outside the Normal State. It confirms the execution of the request service.

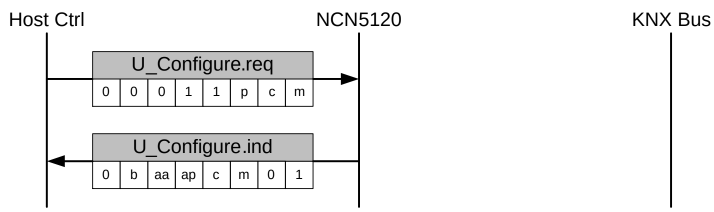


Figure 42. Configure Service

p (auto polling):	when active, NCN5120 automatically fills in corresponding poll slot of polling telegrams. Host controller is responsible to provide appropriate polling information with the U_PollingState.req service (See Slave Polling Frame Service and Master Polling Frame Service, p47 and 48).
c (CRC−CCITT):	when active, NCN5120 accompanies every received frame with a 2−byte CRC−CCITT value. CRC−CCITT is also known as CRC−16−CCITT.
m (frame end with MARKER):	End of received frames is normally reported with a silence of 2.6 ms on the Tx line to the host controller. With this feature active, NCN5120 marks end of frame with U_FrameEnd.ind + U_FrameState.ind services (See Send Frame Service and Receive Frame Service, p36 and 44).
b:	‘1’ if busy mode is active. Can be enabled with U_SetBusy.req (see Set Busy Service, p31) and disabled with U_QuitBusy.req service (see Quit Busy Service, p31) or U_Ackn.req service (see Receive Frame Service, p44).
aa:	‘1’ if auto−acknowledge feature is active. Can be enabled with U_SetAddress.req service (see Set Address Service, p32).
ap (auto−polling):	‘1’ if auto−polling feature is active. This feature can be enabled with U_Configure.req service.
c (CRC−CCITT):	‘1’ if CRC−CCITT feature is active. See p50 for info on CRC−CCITT. This feature can be enabled with U_Configure.req service.
m (frame end with MARKER):	‘1’ when feature is active. This feature can be enabled with U_Configure.req service.

<u>Remark:</u>

Activation of the additional features is done by setting the corresponding bit to ‘1’. Setting the bit to ‘0’ (zero) has no effect (will not deactivate feature). Features can only be deactivated by a reset. Set all bits (m, c and p) to ‘0‘ (zero) to poll the current configuration status.

Internal Register Write Service

Write a byte to an internal device−specific register (see *Internal Device−Specific Registers*, p51). The address of the register is specified in the request. The data to be written is transmitted after the request.

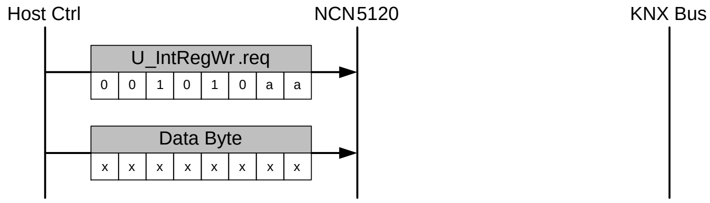


Figure 43. Internal Register Write Service

aa: address of the internal register

Remark: x = don’t care (in line with *Internal Device−Specific Registers*, p51).

* Note: Internal Register Write is not synchronized with other services. One should only use this service when all previous services are ended. When using communication over SPI, it is recommended to go to stop mode when performing a register write. When communicating over UART, this is not required.

Internal Register Read Service

Read a byte from an internal device−specific register (see *Internal Device−Specific Registers*, p51). The address of the register is specified in the request. The next byte returns the data of the addressed register.

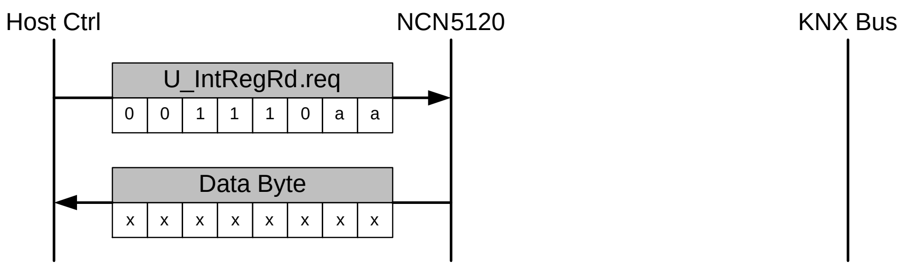


Figure 44. Internal Register Read Service

aa: address of the internal register

Remarks:

- x = don’t care (in line with *Internal Device−Specific Registers*, p51).
- It’s advised to only use this service in Stop, Power−Up Stop or Power−Up State. In the other state erroneous behavior could occur.

* Note: Internal Register Read is not synchronized with other services. One should only use this service when all previous services are ended. When using communication over SPI or UART, it is recommended to go to stop mode when performing a register write.

Send Frame Service

Send data over the KNX bus.

The U_L_DataStart.req is used to start transmission of a new frame. The byte following this request is the control byte of the KNX telegram.

The different bytes following the control byte are assembled by using U_L_DataCont.req. The byte following U_L_DataCont.req is the data byte of the KNX telegram. U_L_DataCont.req contains the index which specifies the position of the data byte inside the KNX telegram. It‘s allowed to transmit bytes in random order and even overwrite bytes (= write several times into the same index). It‘s up to the host controller to correctly populate all data bytes of the KNX telegram.

U_L_DataEnd.req is used to finalize the frame and start the KNX transfer. The byte following U_L_DataEnd.req is the checksum of the KNX telegram. If the checksum received by the device corresponds to the calculated checksum, the device starts the transmission on the KNX bus. If not, the device returns U_State.ind message to the host controller with Receive Error flag set (see *State Service* p31 for U_State.ind).

U_L_DataStart/DataCont/DataEnd only provides space for 6 index bits. Because an extended frame can consist out of

263 bytes, an index of 9 bits long is needed. U_DataOffset.req provides the 3 most significant bits of the data byte index. The value is stored internally until a new offset is provided with another call.

Each transmitted data octet on the KNX bus will also be transmitted back to the host controller.

Each transmission is ended with a L_Data.con service where the MSB indicates if an acknowledgment was received or not. When operating in SPI or UART 8−bit Mode, L_Data.con is preceded with U_FrameState.ind.

Depending on the activated features, a CRC−CCITT service and/or a MARKER could be included.

Next figures give different examples of send frames.

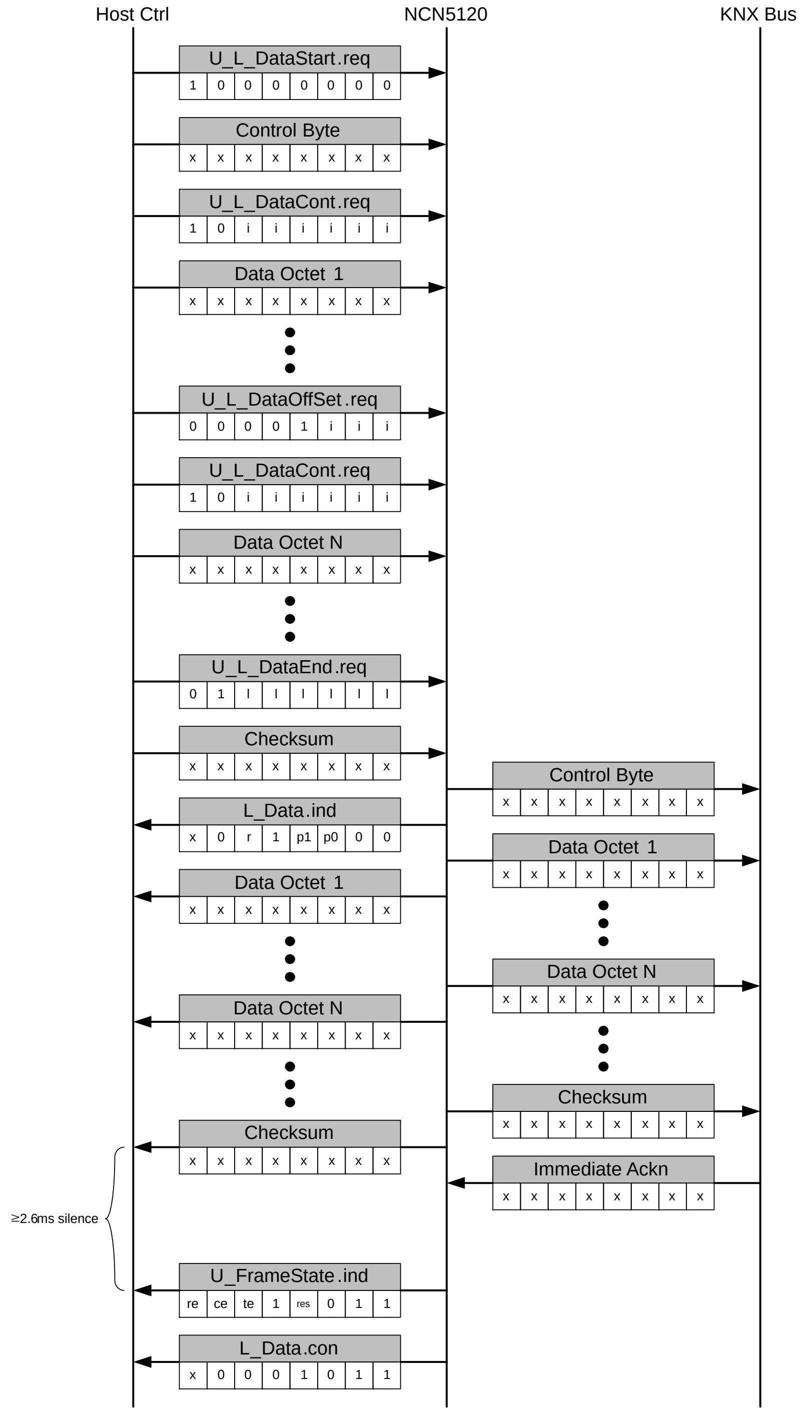


Figure 45. Send Frame, SPI or 8−bit UART Mode, Frame End with Silence, No CRC−CCITT

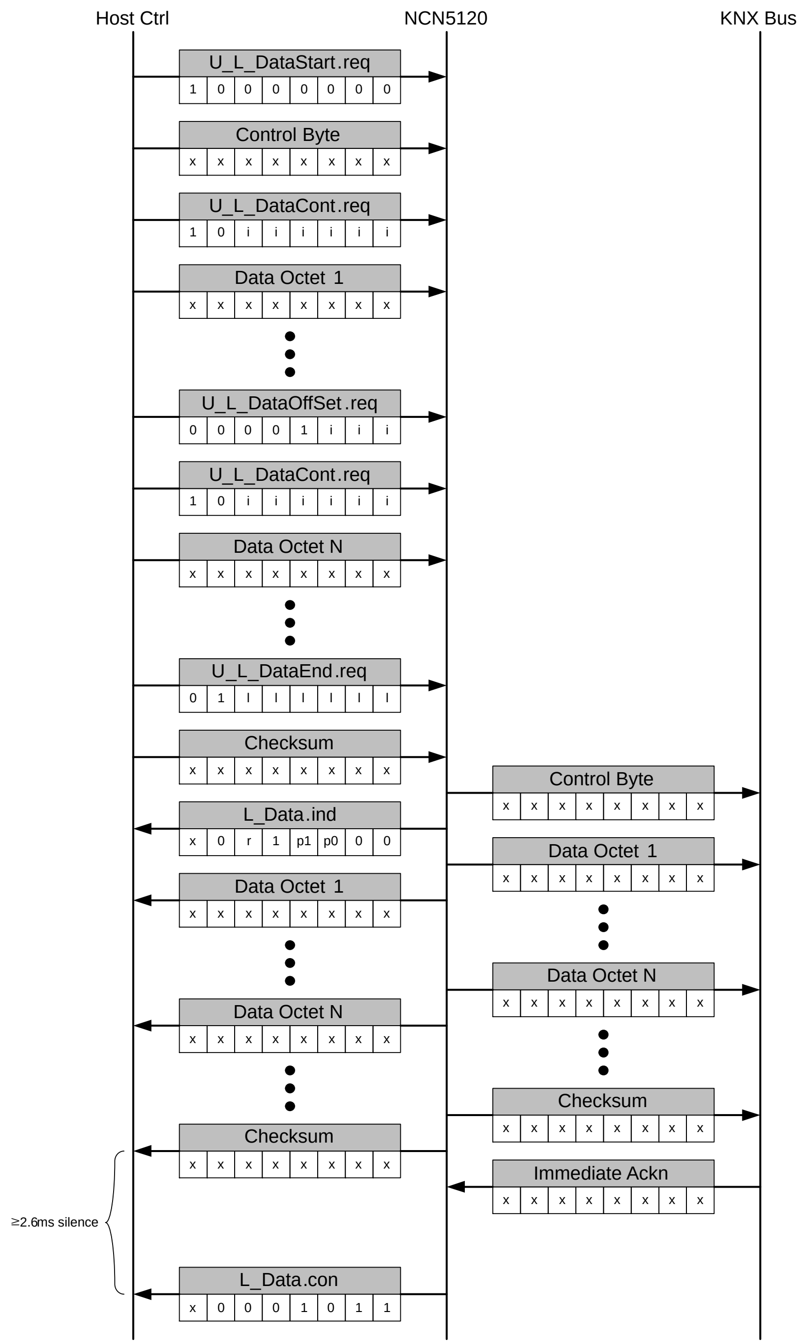


Figure 46. Send Frame, 9−bit UART Mode, Frame End with Silence, No CRC−CCITT

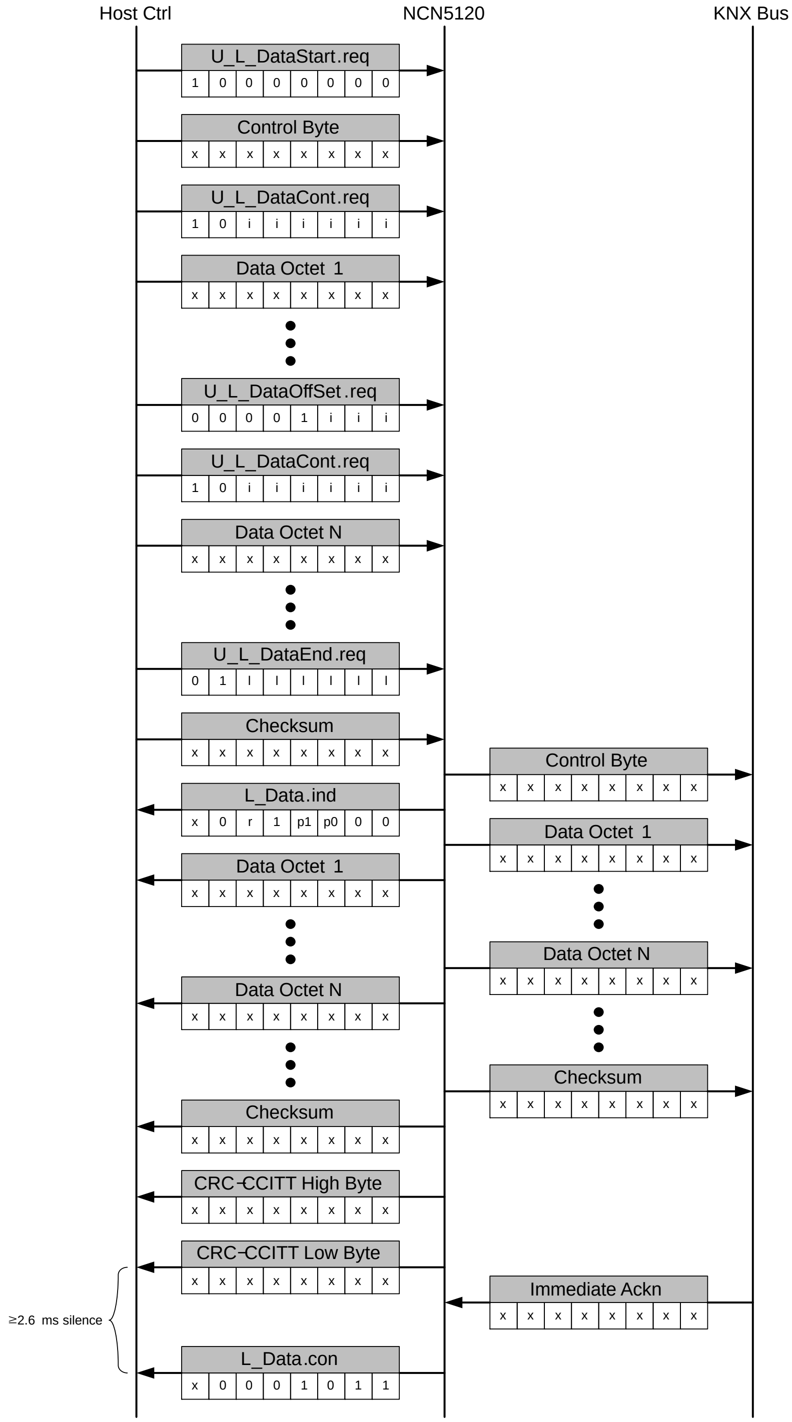


Figure 47. Send Frame, 9−bit UART Mode, Frame End with Silence, with CRC−CCITT

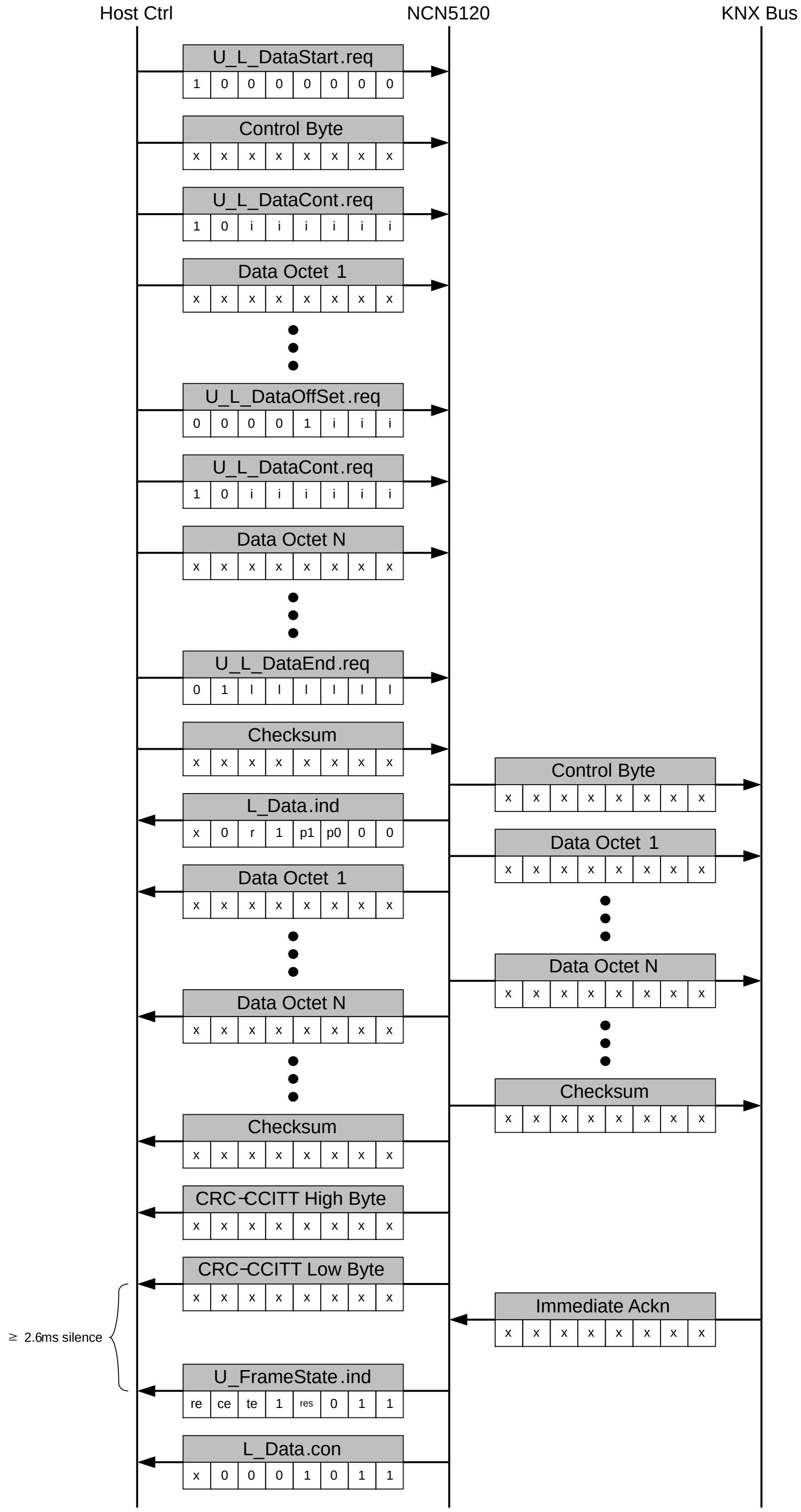


Figure 48. Send Frame, SPI or 8−bit UART Mode, Frame End with Silence, with CRC−CCITT

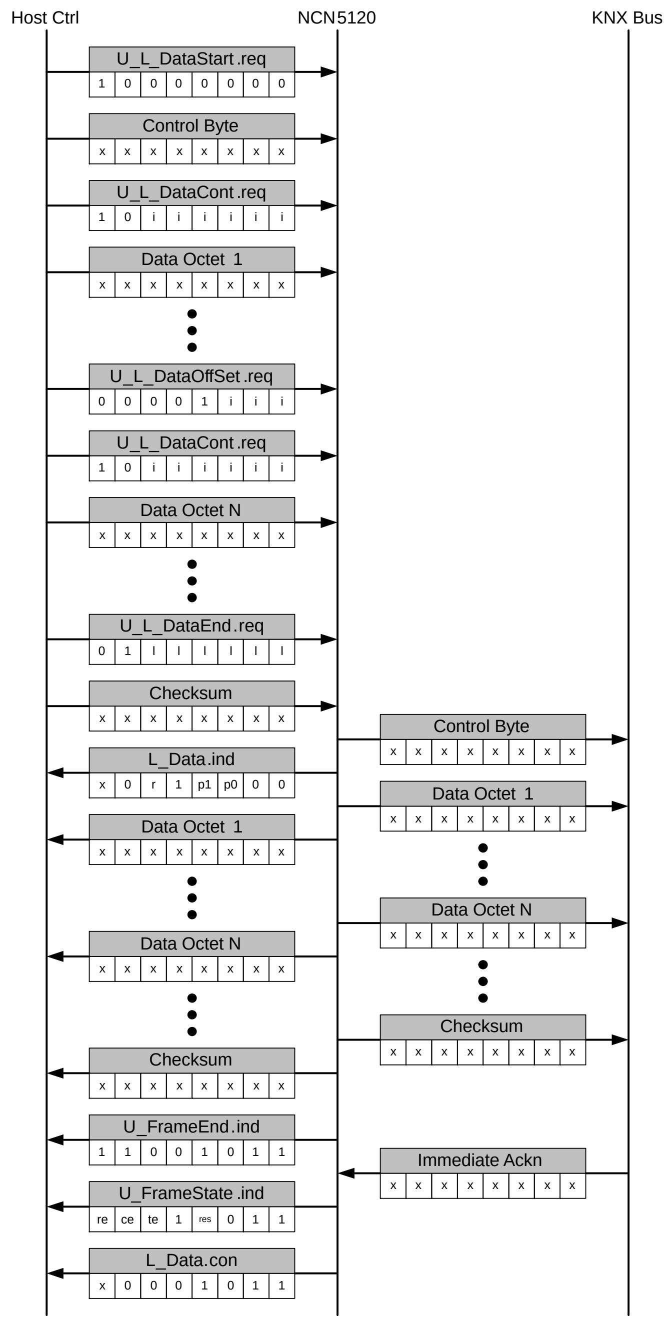


Figure 49. Send Frame, All Modes, Frame End with MARKER, No CRC−CCITT

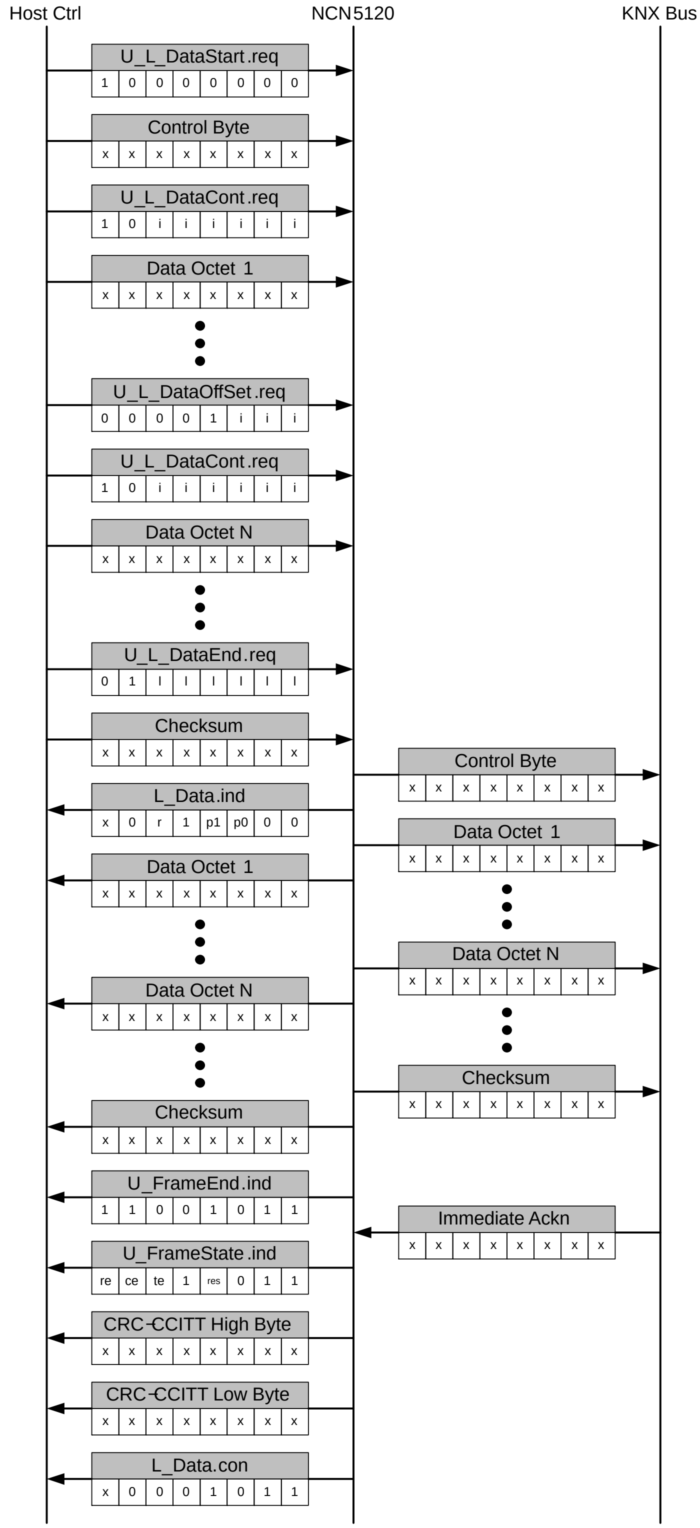


Figure 50. Send Frame, All Modes, Frame End with MARKER and with CRC−CCITT

re (receive error):	‘1’ if newly received frame contained corrupted bytes (wrong parity, wrong stop bit or incorrect bit timings)
ce (checksum or length error):	‘1’ if newly received frame contained wrong checksum or length which does not correspond to the number of received bytes
te (timing error):	‘1’ if newly received frame contained bytes whose timings do not comply with the KNX standard
res (reserved):	Reserved for future use (will be ‘0’).

Remarks:

− If the repeat flag is not set (see Set Repetition Service p33), the device will only perform one attempt to send the KNX telegram.
− Sending of the KNX telegram over the KNX bus is only started after all data bytes are received and the telegram is assembled.
− When starting transmission of a new frame with U_L_DataStart.req, the device automatically resets the internal offset of the data index to zero.
− Data offsets of 5, 6 and 7 are forbidden (U_L_DataOffset.req)!

Remarks on Figures 45 to 50:

− x = don‘t care (in respect with KNX standard)
− See Tables 12 and 13 for more details on all the bits
− Code of U_FrameEnd.ind (0xCB) can also be part of the KNX frame content (Data Octet). When NCN5120 transmits the data octet (0xCB) on the KNX bus, 2 bytes (2 times 0xCB) will be transmitted back to the host controller to make it possible for the host controller to distinguish between a data octet (0xCB) and U_FrameEnd.ind. This remark is only valid if frame end with MARKER is enabled.
− See p50 for info on CRC−CCITT.

Receive Frame Service

Receive data over the KNX bus.

Upon reception from the control byte, the control byte is checked by the device. If correct, the control byte is transmitted back to the host (L_Data_Standard.ind or L_Data_Extended.ind depending if standard or extended frame type is received). After the control byte, all data bytes are transparently transmitted back to the host controller. Handling of this data is a task for the Data Link Layer which should be implemented in the host controller.

The host controller can indicate if the device is addressed by setting the NACK, BUSY or ACK flag (U_Ackn.req).

When working in SPI or 8−bit UART Mode, each frame is ended with an U_FrameState.ind. Depending on the activated features, a CRC−CCITT or MARKER could be added to the complete frame.

Below figures give different examples of receive frames.

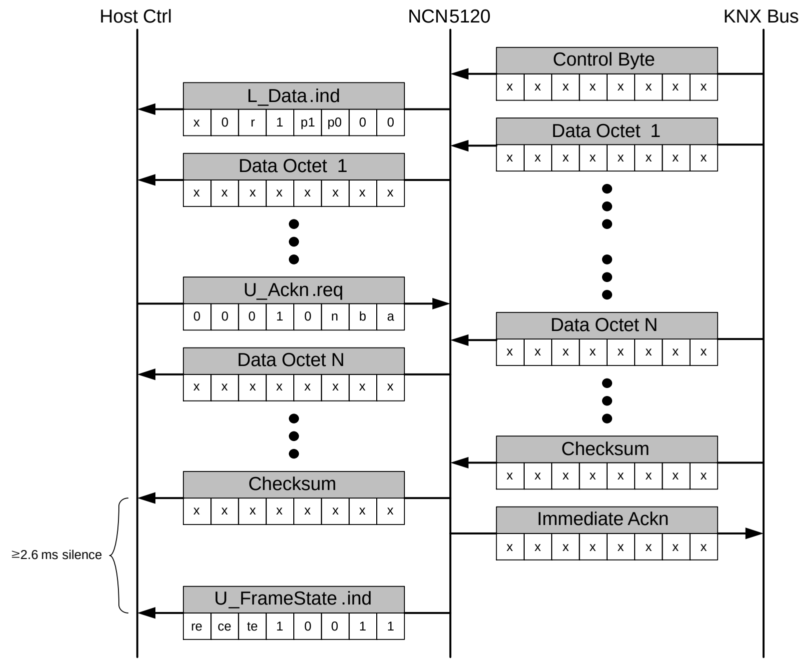


Figure 51. Receive Frame, SPI or 8−bit UART Mode, Frame End with Silence, No CRC−CCITT

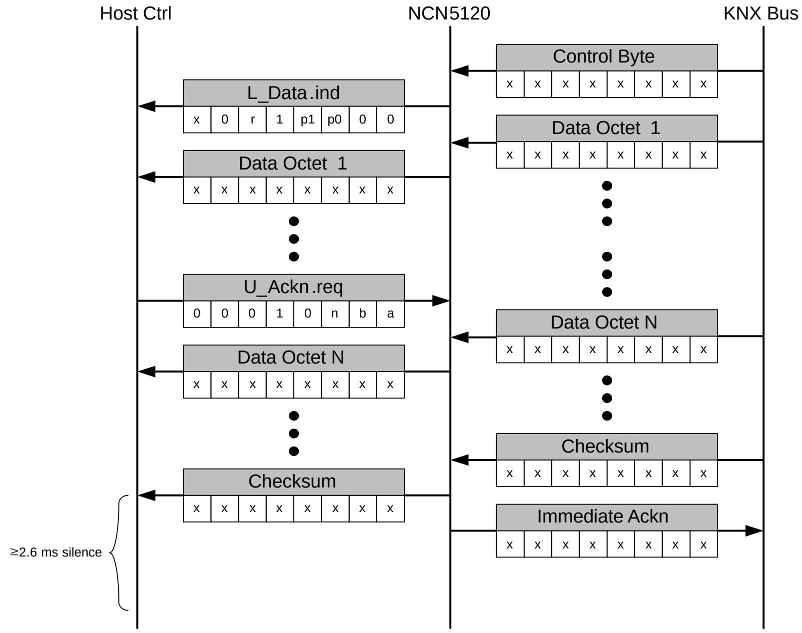


Figure 52. Receive Frame, 9−bit UART Mode, Frame End with Silence, No CRC−CCITT

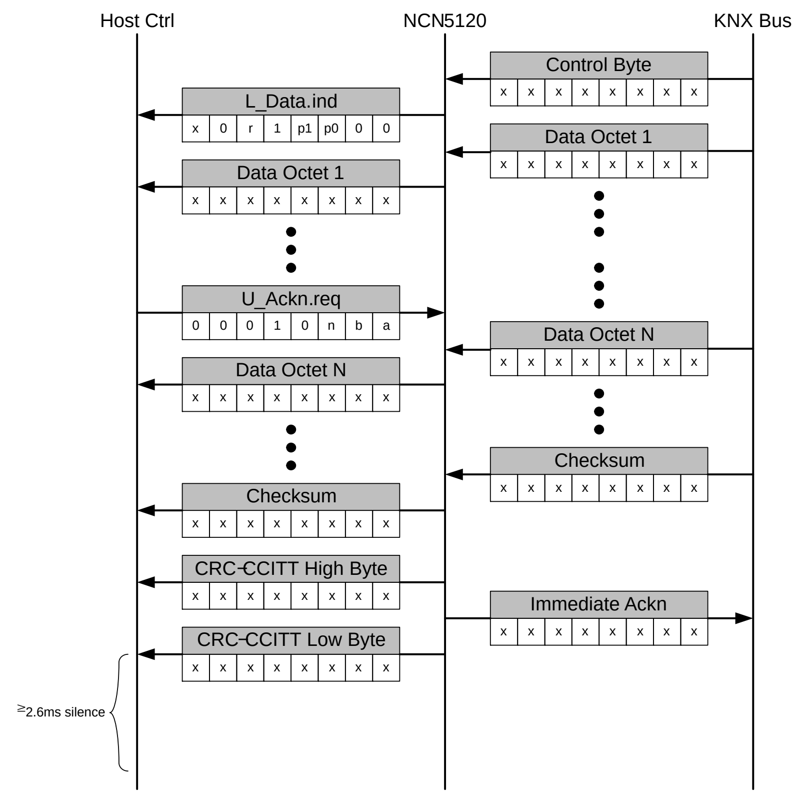


Figure 53. Receive Frame, 9−bit UART Mode, Frame End with Silence, with CRC−CCITT

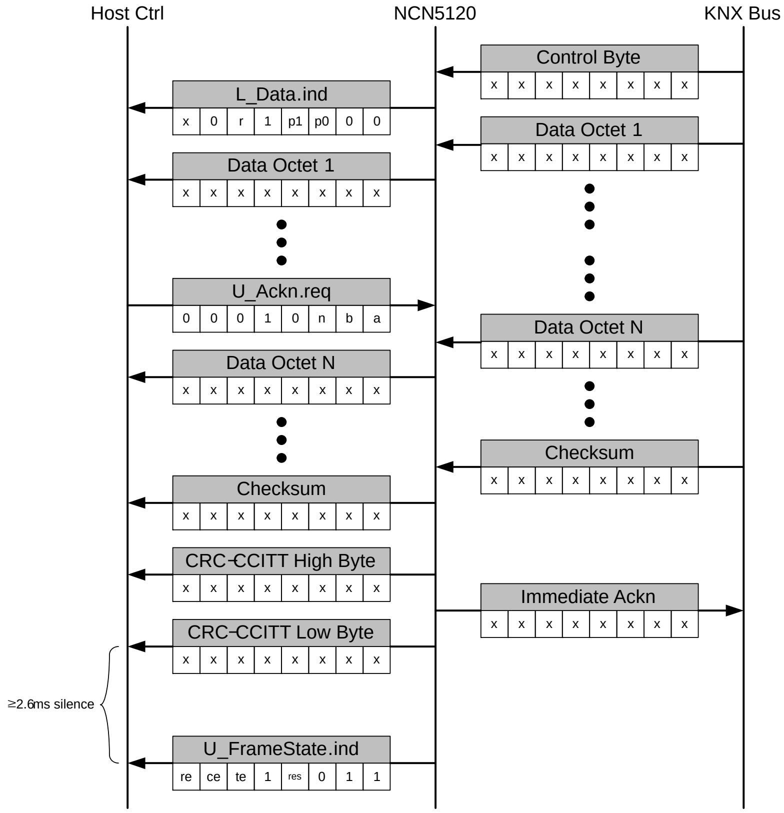


Figure 54. Receive Frame, SPI or 8−bit UART Mode, Frame End with Silence, with CRC−CCITT

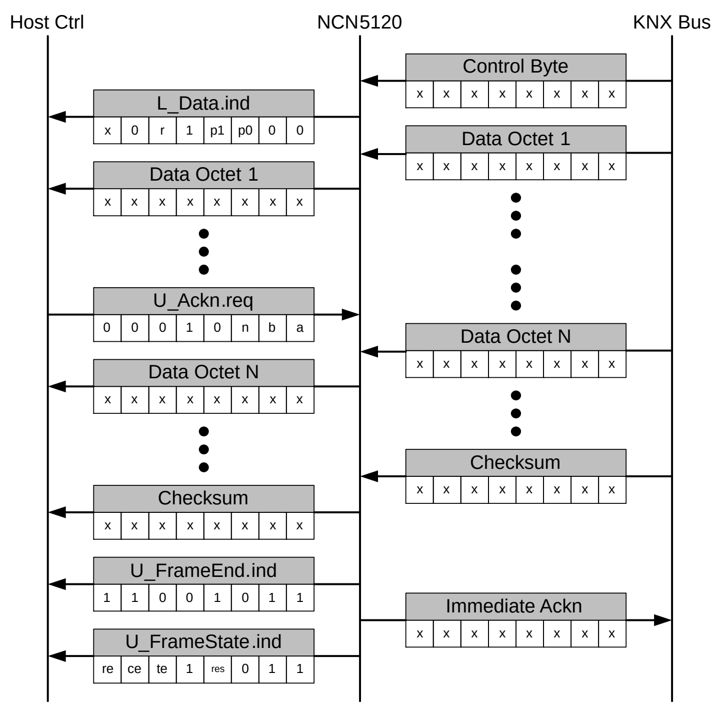


Figure 55. Receive Frame, All Modes, Frame End with MARKER, No CRC−CCITT

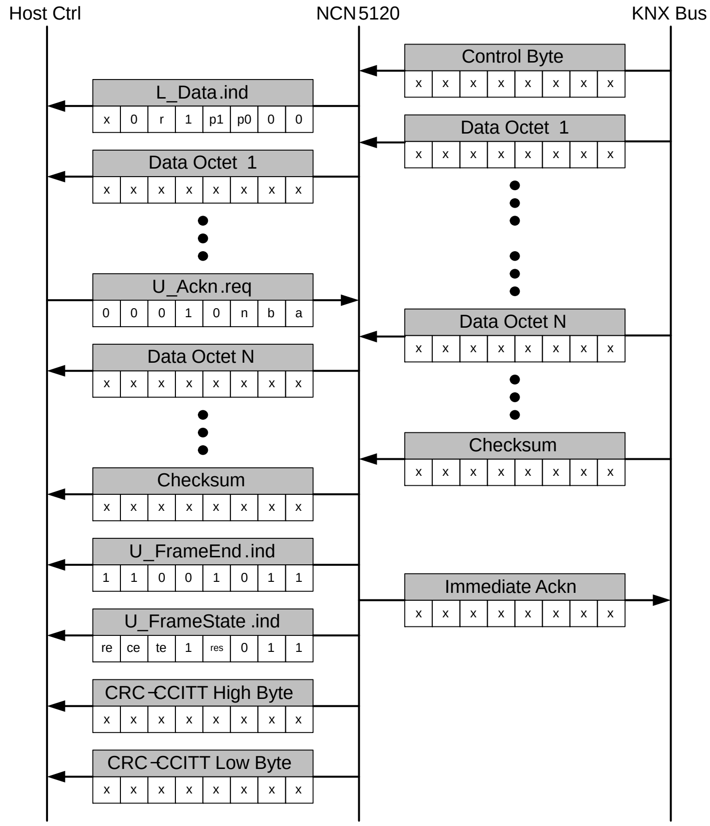


Figure 56. Receive Frame, All Modes, Frame End with MARKER, with CRC−CCITT

re (receive error): ‘1’ if newly received frame contained corrupted bytes (wrong parity, wrong stop bit or incorrect bit timings)
ce (checksum or length error): ‘1’ if newly received frame contained wrong checksum or length which does not correspond to the number of received bytes
te (timing error) : ‘1’ if newly received frame contained bytes whose timings do not comply with the KNX standard
res (reserved) : Reserved for future use (will be ‘0’).

Remarks on Figures 51 to 56:

− x = don‘t care (in respect with KNX standard)
− See Tables 12 and 13 for more details on all the bits
− Code of U_FrameEnd.ind (0xCB) can also be part of the KNX frame content (Data Octet). To make a distinguish between a data octet and U_FrameEnd.ind, NCN5120 duplicates the data content (if 0xCB). This will result in 2 bytes transmitted to the host controller (two times 0xCB) corresponding to 1 byte received on the KNX bus.
  Above is only valid if frame end with MARKER is enabled.
− See p50 for info on CRC−CCITT.

Slave Polling Frame Service

Upon reception and consistency check of the polling control byte, the control byte is send back to the host controller (L_Poll_Data.ind). The host controller will send the slot number to the device (U_PollingState.req), followed by the polling address and the polling state. At the same time the source address, polling address, slot count and checksum is received over the KNX bus. If the polling address received from the KNX bus is equal to the polling address received from the host controller, NCN5120 will send the polling data in the slot as define by U_PollingState.req (only if the slotcount is higher as the define slot).

U_PollingState.req can be sent at any time (not only during a transmission of a polling telegram). The information is stored internally in NCN5120 and can be reused for further polling telegrams if auto−polling function gets activated.

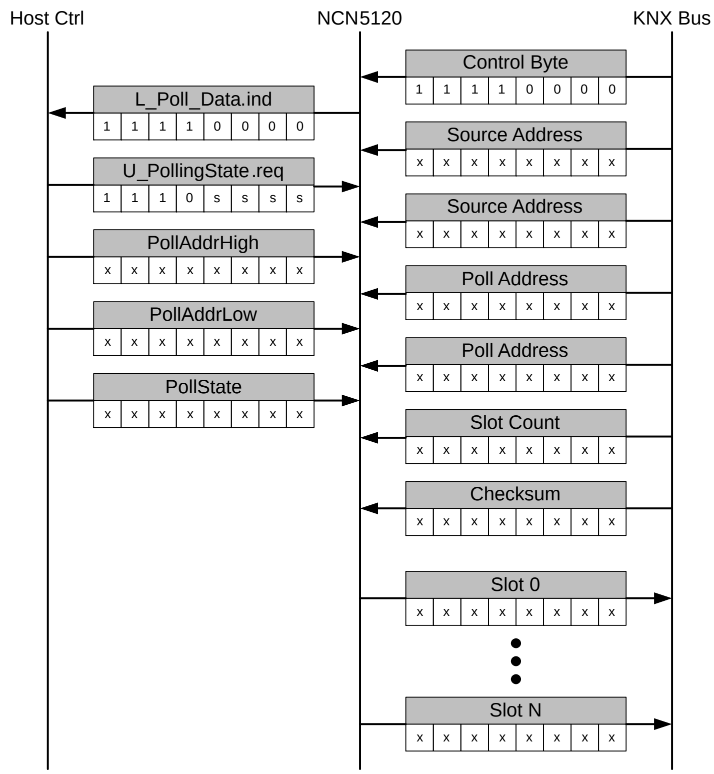


Figure 57. Slave Polling Frame Service

Remarks:

x = don't care (in respect with KNX standard)
ssss = slot number

Master Polling Frame Service

When NCN5120 receives the polling frame from the host controller, the polling frame will be transmitted over the KNX bus.

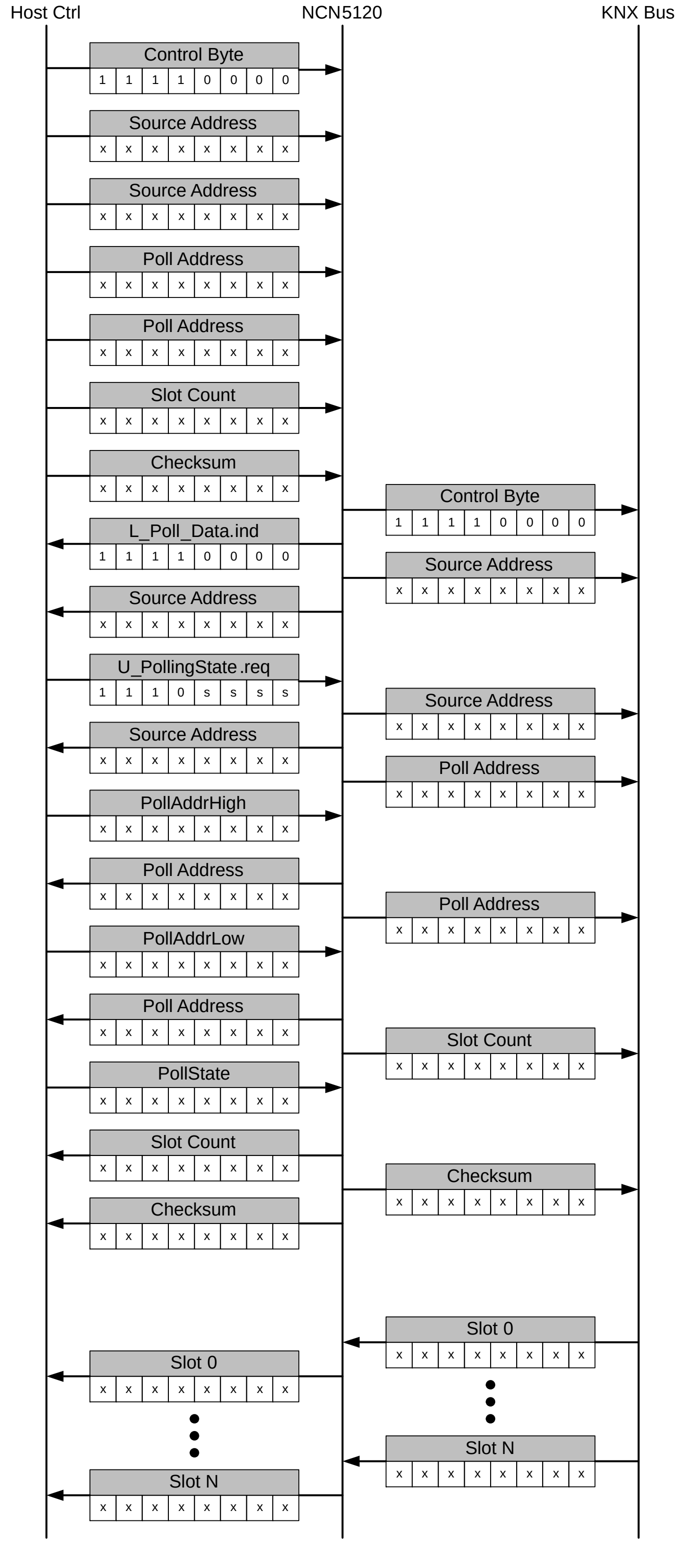


Figure 58. Master Polling Frame Service

Remarks:

x = don‘t care (in respect with KNX standard)
ssss = slot number

CRC−CCITT
CRC order - 16 bit
CRC polynom (hex) - 1021
Initial value (hex) − FFFF
Final XOR value (hex) − 0
No reverse on output CRC

Test string „123456789“ is 29B1h

CRC−CCITT value over a buffer of bytes can be calculated with following code fragment in C, where
pBuf is pointer to the start of frame buffer
uLength is the frame length in bytes

```
unsigned short calc_CRC_CCITT(unsigned char* pBuf, unsigned short uLength)
{
    unsigned short u_crc_ccitt;
    for (u_crc_ccitt = 0xFFFF; uLength−−; p++)
    {
        u_crc_ccitt = get_CRC_CCITT(u_crc_ccitt, *p);
    }
    return u_crc_ccitt;
}

unsigned short get_CRC_CCITT(unsigned short u_crc_val, unsigned char btVal)
{
    u_crc_val = ((unsigned char)(u_crc_val >> 8)) | (u_crc_val << 8);
    u_crc_val ^= btVal;
    u_crc_val ^= ((unsigned char)(u_crc_val & 0xFF)) >> 4;
    u_crc_val ^= u_crc_val << 12;
    u_crc_val ^= (u_crc_val & 0xFF) << 5;
    return u_crc_val;
}
```

Internal Device−Specific Registers

In total 4 device-specific register are available:

- Watchdog Register (0x00)
- Analog Control Register 0 (0x01)
- Analog Control Register 1 (0x02)
- Analog Status Register 0 (0x03)

Watchdog Register

The Watchdog Register is located at address 0x00 and can be used to enable the watchdog and set the watchdog time.

Table 14. WATCHDOG REGISTER

ExtWatchdogCtrl (ExtWR)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x00	**Access**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	0	0	1	1	1	1
	Data	WDEN	-	-	-	WDT			

Table 15. WATCHDOG REGISTER PARAMETERS

Parameter	Value		Description	Info
WDEN	0	Disable	Enables/disables the watchdog	p19
	1	Enable		
WDT	0000	33 ms	Defines the watchdog time. The watchdog needs to be re-enabled (WDEN) within this time or a watchdog event will be triggered.	
	0001	66 ms		
	0010	98 ms		
	0011	131 ms		
	0100	164 ms		
	0101	197 ms		
	0110	229 ms		
	0111	262 ms		
	1000	295 ms		
	1001	328 ms		
	1010	360 ms		
	1011	393 ms		
	1100	426 ms		
	1101	459 ms		
	1110	492 ms		
	1111	524 ms		

Remark: Bit 4 … 6 are reserved.

Analog Control Register 0

The Analog Control Register 0 is located at address 0x01 and can be used to enable Sleep Mode, to disable the V20V and the DC2 regulator, to disable the XCLK-pin and to set the frequency of the XCLK output signal.

Table 16. ANALOG CONTROL REGISTER 0

Analog Control Register 0 (AnaCtrl0)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x01	**Access**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	1	1	1	0	0	0	0
	Data	SLPEN	V20VEN	DC2EN	XCLKEN	XCLKFREQ	-	-	-

Table 17. ANALOG CONTROL REGISTER 0 PARAMETERS

Parameter	Value		Description	Info
SLPEN	0	Disable	Enables/disables Sleep Mode (≠ going to Sleep Mode)	p 19
	1	Enable		
V20VEN	0	Disable	Enables/disables the V20V regulator	p 17
	1	Enable		
DC2EN	0	Disable	Enables/disables the DC2 converter	p 17
	1	Enable		
XCLKEN	0	Disable	Enables/disables the XCLK output signal	p 17
	1	Enable		
XCLKFREQ	0	8 MHz	Sets the frequency of the XCLK output signal (if enabled)	
	1	16 MHz		

Remark: Bit 0 … 2 are reserved.

Analog Control Register 1

The Analog Control Register 1 is located at address 0x02 and can be used to put the device in Sleep Mode.

Table 18. ANALOG CONTROL REGISTER 1

Analog Control Register 1 (AnaCtrl1)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x02	**Access**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	0	0	0	0	0	0
	Data	SLP	-	-	-	-	-	-	-

Table 19. ANALOG CONTROL REGISTER 1 PARAMETERS

Parameter	Value		Description	Info
SLP	0	Disable	If ‘1’, device goes to Sleep Mode (if SLPEN = ‘1’). Once in Sleep Mode, only way to get out is a Wake-Up Event on the FANIN/WAKE-pin.	p 17 and 19
	1	Enable		

Remark: Bit 0 … 6 are reserved.

Analog Status Register

The Analog Status Register is located at address 0x03 and can be used to verify the Sleep Mode, voltage monitors, Xtal and thermal status.

Table 20. ANALOG STATUS REGISTER

Analog Status Register (AnaStat)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x03	**Access**	R	R	R	R	R	R	R	R
	Reset	0	0	0	0	0	0	0	0
	Data	SLPMODE	V20V	VDD2	VBUS	VFILT	XTAL	TW	TSD

Table 21. ANALOG STATUS REGISTER PARAMETERS

Parameter	Value	Value	Description	Info
SLPMODE	0	Disabled	Contains information about the previous Sleep Mode of the device	p 19
	1	Enabled		
V20V	0	nOK	‘1’ if voltage on V20V-pin is above the V20V undervoltage level	p 17
	1	OK		
VDD2	0	nOK	‘1’ if voltage on VDD2-pin is above the VDD2 undervoltage level	p 17
	1	OK		
VBUS	0	nOK	‘1’ if bus voltage is above the VBUS undervoltage level	P 16
	1	OK		
VFILT	0	nOK	‘1’ if voltage on VFILT-pin is above the VFILT undervoltage level	p 16
	1	OK		
XTAL	0	nOK	‘1’ if XTAL is up and running	p 17
	1	OK		
TW	0	No TW	‘1’ if Thermal Warning detected	p 19
	1	TW		
TSD	0	No TSD	Contains information about the previous Thermal Shutdown situation	
	1	TSD		

PACKAGE THERMAL CHARACTERISTICS

The NCN5120 is available in a QFN40 package. For cooling optimizations, the QFN40 has an exposed thermal pad which has to be soldered to the PCB ground plane. The ground plane needs thermal vias to conduct the heat to the bottom layer.

Figure 59 gives an example of good heat transfer. The exposed thermal pad is soldered directly on the top ground layer (left picture of Figure 59). It‘s advised to make the top ground layer as large as possible (see arrows Figure 59). To improve the heat transfer even more, the exposed thermal pad is connected to a bottom ground layer by using thermal vias (see right picture of Figure 59). It‘s advised to make this bottom ground layer as large as possible and with as less as possible interruptions.

For precise thermal cooling calculations the major thermal resistances of the device are given (Table 4). The thermal media to which the power of the devices has to be given are:

− Static environmental air (via the case)
− PCB board copper area (via the exposed pad)

The major thermal resistances of the device are the Rth from the junction to the ambient (Rth_{ja}) and the overall Rth from the junction to exposed pad (Rth_{jp}). In Table 4 one can find the values for the Rth_{ja} and Rth_{jp}, simulated according to JESD−51.

The Rth_{ja} for 2S2P is simulated conform JEDEC JESD−51 as follows:

− A 4−layer printed circuit board with inner power planes and outer (top and bottom) signal layers is used
− Board thickness is 1.46 mm (FR4 PCB material)
− The 2 signal layers: 70 μm thick copper with an area of 5500 mm^2 copper and 20% conductivity
− The 2 power internal planes: 36 μm thick copper with an area of 5500 mm^2 copper and 90% conductivity

The Rth_{ja} for 1S0P is simulated conform to JEDEC JESD−51 as follows:

− A 1−layer printed circuit board with only 1 layer
− Board thickness is 1.46 mm (FR4 PCB material)
− The layer has a thickness of 70 μm copper with an area of 5500 mm^2 copper and 20% conductivity

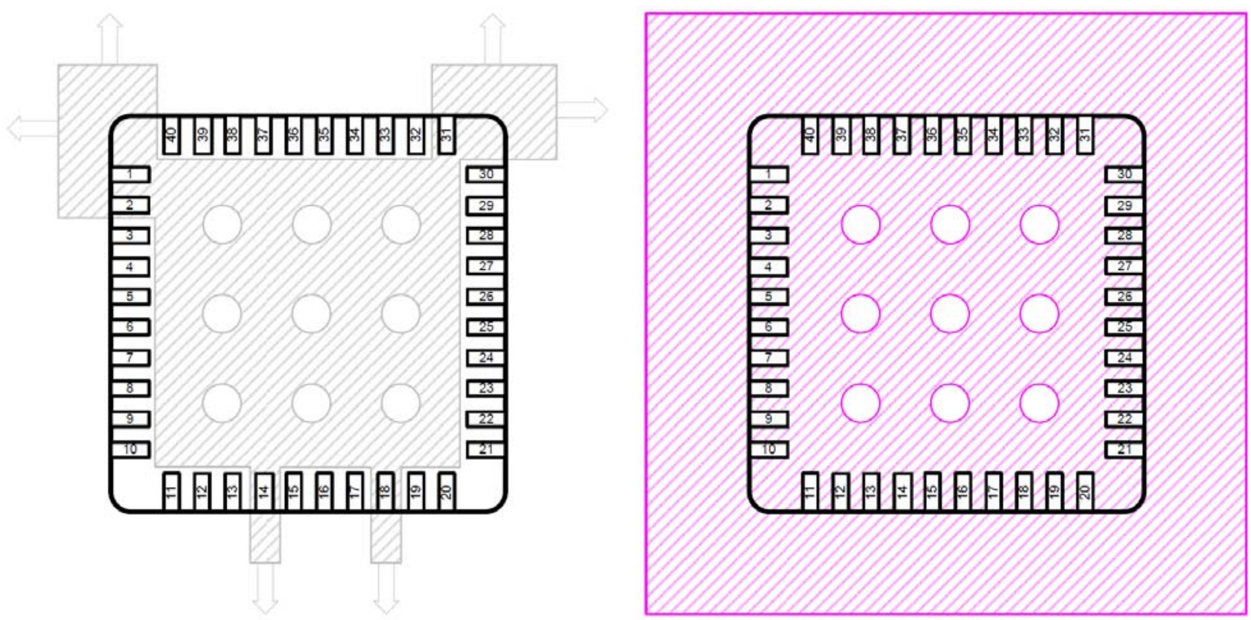


Figure 59. PCB Ground Plane Layout Condition (left picture displays the top ground layer, right picture displays the bottom ground layer)

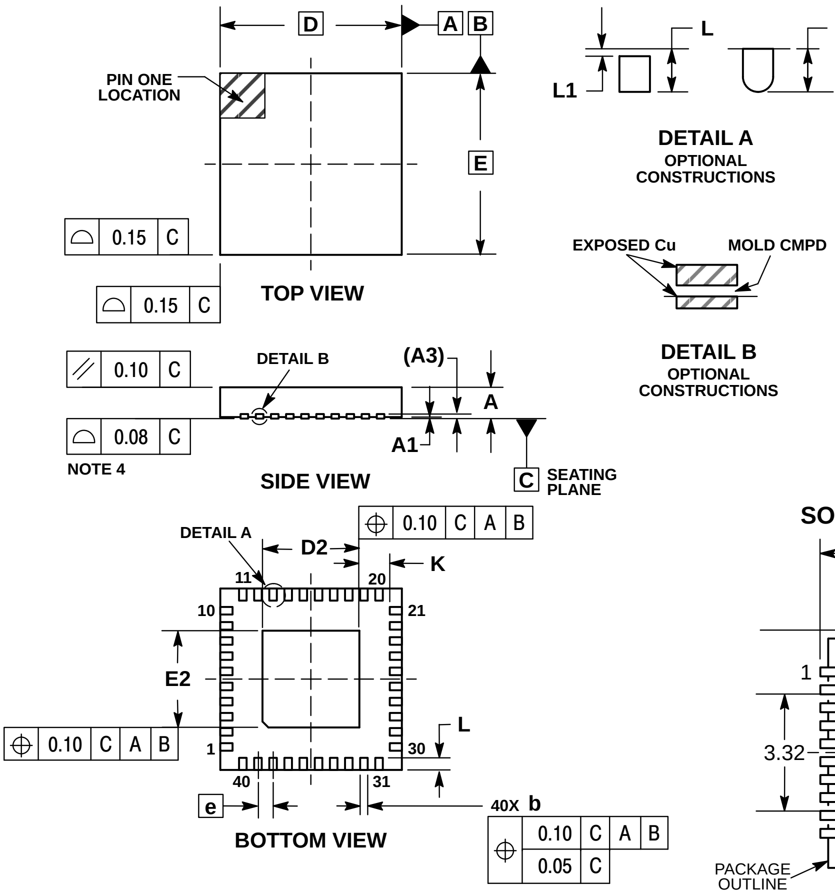
ORDERING INFORMATION

Device Number	Temperature Range	Package	Shipping†
NCN5120MNG	−25°C to 85°C	QFN−40 (Pb−Free)	50 Units / Tube 100 Tubes / Box
NCN5120MNTWG	−25°C to 85°C	QFN−40 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PACKAGE DIMENSIONS

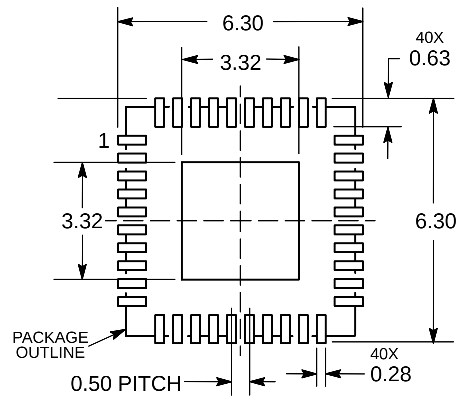
QFN40 6x6, 0.5P
CASE 485AU
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	3.10	3.30
E	6.00 BSC	
E2	3.10	3.30
e	0.50 BSC	
K	0.20 MIN	
L	0.30	0.50
L1	---	0.15

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PUBLICATION ORDERING INFORMATION

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