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December 2010

# NC7SV57 / NC7SV58 TinyLogic<sup>®</sup> ULP-A Universal Configurable Two-Input Logic Gates

### **Features**

- 0.9V to 3.6V V<sub>CC</sub> Supply Operation
- 3.6V Over-Voltage Tolerant I/Os at V<sub>CC</sub> from 0.9V to 3.6V
- Extremely High Speed tpd
  - 2.5ns: Typical for 2.7V to 3.6V V<sub>CC</sub>
  - 3.1ns: Typical for 2.3V to 2.7V  $V_{CC}$
  - 4.0ns: Typical for 1.65V to 1.95V  $V_{CC}$
  - 6.0ns: Typical for 1.4V to 1.6V V<sub>CC</sub>
  - 8.0ns: Typical for 1.1V to 1.3V V<sub>CC</sub>
  - 23.0ns: Typical for 0.9V V<sub>CC</sub>
- Power-Off High-Impedance Inputs and Outputs
- High Static Drive (I<sub>OH</sub>/I<sub>OL</sub>)
  - ±24mA at 3.00V V<sub>CC</sub>
  - ±18mA at 2.30V V<sub>CC</sub>
  - $\pm 6mA$  at 1.65V  $V_{CC}$
  - $\pm 4mA$  at 1.4V  $V_{\text{CC}}$
  - $\pm 2$ mA at 1.1V V<sub>CC</sub> -  $\pm 0.1$ mA at 0.9V V<sub>CC</sub>
- Proprietary Quiet Series™ Noise/EMI Reduction
- Ultra-Small MicroPak™ Package
- Ultra-Low Dynamic Power

### **Description**

The NC7SV57 and NC7SV58 are universal configurable two-input logic gates from Fairchild's Ultra-Low Power (ULP-A) series of TinyLogic $^{\tiny old N}$ . ULP-A is ideal for applications that require extreme high-speed, high drive, and low power. This product is designed for a wide low-voltage operating range (0.9V to 3.6V V $_{\rm CC}$ ) and applications that require more drive and speed than the TinyLogic ULP series, but still offer best-in-class, low-power operation.

Each device is capable of being configured for 1 of 5 unique two-input logic functions. Any possible two-input combinatorial logic function can be implemented, as shown in the *Function Selection Table*. Device functionality is selected by how the device is wired at the board level. *Figures 1 through 10* illustrate how to connect the NC7SV57 and NC7SV58, respectively, for the desired logic function. All inputs have been implemented with hysteresis.

The NC7SV57 and NC7SV58 are uniquely designed for optimized power and speed and are fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

### **Ordering Information**

Part Number	Top Mark	Package	Packing Method	
NC7SV57P6X	V57	6-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3000 Units on Tape & Reel	
NC7SV57L6X	H3 6-Lead Micropak™, 1.0mm Wide 50		5000 Units on	
NC7SV57FHX	H3	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	Tape & Reel	
NC7SV58P6X	V58	6-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3000 Units on Tape & Reel	
NC7SV58L6X	NC7SV58L6X H4 6-Lead Micropak™, 1.0mm Wide		5000 Units on	
NC7SV58FHX H4 6-L		6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	Tape & Reel	

### **Battery Life**

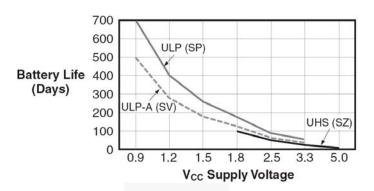


Figure 1. Battery Life vs. V<sub>CC</sub> Supply Voltage

#### Notes:

- 1. TinyLogic<sup>®</sup> ULP and ULP-A with up to 50% less power consumption can extend your battery life significantly. Battery Life = (V<sub>battery</sub>•I<sub>battery</sub>•.9)/(P<sub>device</sub>)/24hrs/day where P<sub>device</sub> = (I<sub>CC</sub>• V<sub>CC</sub>) + (C<sub>PD</sub> + C<sub>L</sub>) V<sub>CC</sub><sup>2</sup>• f.
- where  $P_{device} = (I_{CC} \cdot V_{CC}) + (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f$ .

  2. Assumes ideal 3.6V Lithium Ion battery with current rating of 900mAH and derated 90% and device frequency at 10MHz, with  $C_L = 15pF$  load.

### **Pin Configurations**

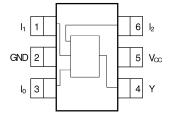


Figure 2. SC70 (Top View)

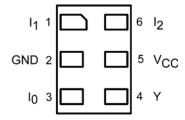


Figure 3. MicroPak™ (Top Through View)

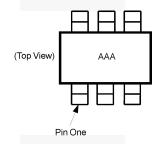


Figure 4. Pin 1 Orientation

#### Notes:

- 3. AAA represents product code top mark (see Ordering Information).
- 4. Orientation of top mark determines pin one location.
- 5. Reading the top mark left to right, pin one is the lower left pin.

#### **Pin Definitions**

Pin # SC70	Pin # MicroPak™	Name	Description
1	1	I <sub>1</sub>	Data Input
2	2	GND	Ground
3	3	I <sub>0</sub>	Data Input
4	4	Y	Output
5	5	V <sub>CC</sub>	Supply Voltage
6	6	l <sub>2</sub>	Data Input

### **Function Table**

	Inputs		NC7SV57	NC7SV58
l <sub>2</sub>	l <sub>1</sub>	I <sub>0</sub>	$Y = \overline{(I_0)} \bullet \overline{(I_2)} + (I_1) \bullet (I_2)$	$Y = (I_0) \bullet \overline{(I_2)} + \overline{(I_1)} \bullet (I_2)$
L	L	L	Н	L
L	L	Н	L	Н
L	Н	L	Н	L
L	Н	Н	L	Н
Н	L	L	L	Н
Н	L	Н	L	Н
Н	Н	L	Н	L
Н	Н	Н	Н	L

H = HIGH Logic Level L = LOW Logic Level

### **Function Selection Table**

2-Input Logic Function	<b>Device Selection</b>	Connection Configuration
2-Input AND	NC7SV57	Figure 5
2-Input AND with Inverted Input	NC7SV58	Figure 11, Figure 12
2-Input AND with Both Inputs Inverted	NC7SV57	Figure 8
2-Input NAND	NC7SV58	Figure 10
2-Input NAND with Inverted Input	NC7SV57	Figure 6, Figure 7
2-Input NAND with Both Inputs Inverted	NC7SV58	Figure 13
2-Input OR	NC7SV58	Figure 13
2-Input OR with Inverted Input	NC7SV57	Figure 6, Figure 7
2-Input OR with Both Inputs Inverted	NC7SV58	Figure 10
2-Input NOR	NC7SV57	Figure 8
2-Input NOR with Inverted Input	NC7SV58	Figure 10, Figure 11
2-Input NOR with Both Inputs Inverted	NC7SV57	Figure 5
2-Input XOR	NC7SV58	Figure 14
2-Input XNOR	NC7SV57	Figure 9

### **NC7SV57 Logic Configurations**

Figure 5 through Figure 9 show the logical functions that can be implemented using the NC7SV57. The diagrams show the DeMorgan's equivalent logic duals for a given two-input function. The logical

implementation is next to the board-level physical implementation of how the pins of the function should be connected.

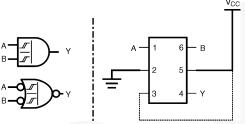


Figure 5. 2-Input AND Gate

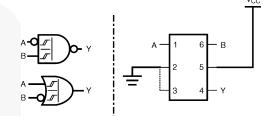


Figure 6. 2-Input NAND Gate with Inverted A Input

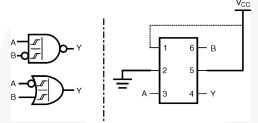


Figure 7. 2-Input NAND with Inverted B Input

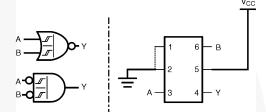


Figure 8. 2-Input NOR Gate

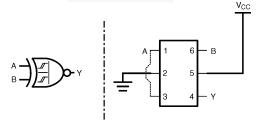


Figure 9. 2-Input XNOR Gate

### **NC7SV58 Logic Configurations**

Figure 10 through Figure 14 show the logical functions that can be implemented using the NC7SV58. The diagrams show the DeMorgan's equivalent logic duals for a given two-input function. The logical

implementation is next to the board-level physical implementation of how the pins of the function should be connected.

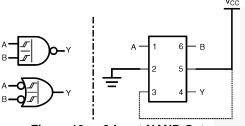


Figure 10. 2-Input NAND Gate

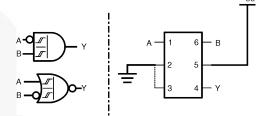


Figure 11. 2-Input AND Gate with Inverted A Input

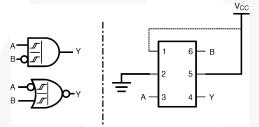


Figure 12. 2-Input AND with Inverted B Input

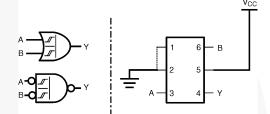


Figure 13. 2-Input OR Gate

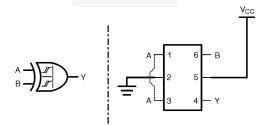


Figure 14. 2-Input XOR Gate

### **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Para	Parameter			Unit
V <sub>CC</sub>	Supply Voltage		-0.5	4.6	V
V <sub>IN</sub>	DC Input Voltage		-0.5	4.6	V
	DC Output Voltage	HIGH or LOW State <sup>(6)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
V <sub>OUT</sub>	DC Output Voltage	V <sub>CC</sub> =0V	-0.5	4.6	V
I <sub>IK</sub>	DC Input Diode Current	V <sub>IN</sub> < 0V		±50	mA
	DC Output Diada Current	V <sub>OUT</sub> < 0V		-50	m ^
I <sub>OK</sub>	DC Output Diode Current	$V_{OUT} > V_{CC}$		+50	mA
I <sub>OH</sub> / I <sub>OL</sub>	DC Output Source / Sink Curre	ent		±50	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current per	Supply Pin		±50	mA
T <sub>STG</sub>	Storage Temperature Range		-65	+150	°C
		MicroPak™-6		130	
$P_{D}$	Power Dissipation at +85°C	SC70-6		150	mW
		MicroPak2™-6		120	
ESD	Human Body Model, JEDEC:JI	ESD22-A114		4000	V
ESD	Charged Device Model, JEDEO	C:JESD22-C101		2000	V

#### Note:

6. IO absolute maximum rating must be observed.

### **Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
Vcc	Supply Voltage Operating		0.9	3.6	V
V <sub>IN</sub>	Input Voltage		0	3.6	V
V	Output Voltage	V <sub>CC</sub> =0V	0	3.6	V
V <sub>OUT</sub>	Output Voltage	HIGH or LOW State	0	Vcc	7 V
		V <sub>CC</sub> =3.0V to 3.6V		±24.0	
		V <sub>CC</sub> =2.3V to 2.7V		±18.0	
1 /1	Output Current	V <sub>CC</sub> =1.65V to 1.95V		±6.0	mA
I <sub>OH</sub> /I <sub>OL</sub>	Output Current	V <sub>CC</sub> =1.4V to 1.6V		±4.0	
		V <sub>CC</sub> =1.1V to 1.3V		±2.0	
		V <sub>CC</sub> =0.9V		±0.1	μA
T <sub>A</sub>	Operating Temperature, Free Air		-40	+85	°C
Δt/ΔV	Minimum Input Edge Rate	V <sub>IN</sub> =0.8V to 2.0, V <sub>CC</sub> =3.0V		10	ns/V
		SC70-6		425	
$\theta_{\sf JA}$	Thermal Resistance	MicroPak™-6		500	°C/W
		MicroPak2™-6		560	7

#### Note:

7. Unused inputs must be held HIGH or LOW. They may not float.

### **DC Electrical Characteristics**

Compleal	Davamatar	V	Conditions	T <sub>A</sub> =2	5°C	T <sub>A</sub> =-40	to 85°C	l lmita
Symbol	Parameter	V <sub>CC</sub>	Conditions	Min.	Max.	Min.	Max.	Units
		0.90		0.30	0.70	0.30	0.70	
		1.10		0.40	1.00	0.40	1.00	
$V_{P}$	Positive Threshold	1.40		0.50	1.40	0.50	1.40	V
<b>V</b> P	Voltage	1.65		0.70	1.50	0.70	1.50	·
		2.30		1.00	1.80	1.00	1.80	
		2.70		1.30	2.20	1.30	2.20	
		0.90		0.10	0.60	0.10	0.60	
		1.10		0.15	0.70	0.15	0.70	
$V_N$	Negative Threshold	1.40		0.20	0.80	0.20	0.80	V
۷N	Voltage	1.65		0.25	0.90	0.25	0.90	v
		2.30		0.40	1.15	0.40	1.15	
		2.70		0.60	1.50	0.60	1.50	
		0.90		0.07	0.50	0.07	0.50	
		1.10		0.08	0.60	0.08	0.60	
V <sub>H</sub>	Hysteresis Voltage	1.40		0.10	0.80	0.10	0.80	V
VН	Trysteresis voltage	1.65		0.15	1.00	0.15	1.00	v
		2.30		0.25	1.10	0.25	1.10	
		2.70		0.40	1.20	0.40	1.20	
		0.90		V <sub>CC</sub> -0.1		V <sub>CC</sub> -0.1		
		$1.10 \leq V_{CC} \leq 1.30$		V <sub>CC</sub> -0.1		V <sub>CC</sub> -0.1		
		$1.40 \leq V_{CC} \leq 1.60$	I = 100A	V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		
		$1.65 \leq V_{C,C} \leq 1.95$	I <sub>OH</sub> =-100μA	V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		
		$2.30 \leq V_{CC} \leq 2.70$		V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		
		$2.70 \leq V_{CC} \leq ~3.60$	V	V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		
		$1.10 \le V_{CC} \le 1.30$	I <sub>OH</sub> =-2mA	.75 x V <sub>CC</sub>		.75 x V <sub>CC</sub>		
$V_{OH}$	HIGH Level Output Voltage	$1.40 \le V_{CC} \le 1.60$	I <sub>OH</sub> =-4mA	.75 x V <sub>CC</sub>		.75 x V <sub>CC</sub>		V
	Voltage	$1.65 \leq V_{CC} \leq 1.95$		1.25		1.25		1
		$2.30 \le V_{CC} \le 2.70$	I <sub>OH</sub> =-6mA	2.0	1	2.0		
		$2.30 \le V_{CC} \le 2.70$		1.8		1.8		
		$2.70 \le V_{CC} \le 3.60$	I <sub>OH</sub> =-12mA	2.2		2.2		1
		$2.30 \le V_{CC} \le 2.70$		1.7		1.7		1
		2.70 ≤ V <sub>CC</sub> ≤ 3.60	I <sub>OH</sub> =-18mA	2.4		2.4		1
		$2.70 \le V_{CC} \le 3.60$	I <sub>OH</sub> =-24mA	2.2		2.2		

Continued on following page....

### DC Electrical Characteristics (Continued)

		.,	0 1111	T <sub>A</sub> =	:25°C	T <sub>A</sub> =-40	to 85°C		
Symbol	Symbol Parameter	raiameter v <sub>CC</sub>	V <sub>CC</sub>	Conditions	Min.	Max.	Min.	Max.	Units
		0.90			0.1		0.1		
		$1.10 \leq V_{CC} \leq 1.30$			0.1		0.1		
		$1.40 \le V_{CC} \le 1.60$	1004		0.2		0.2		
		$1.65 \leq V_{CC} \leq 1.95$	Ι <sub>ΟL</sub> =100μΑ		0.2		0.2		
		$2.30 \leq V_{CC} \leq 2.70$			0.2		0.2		
		$2.70 \leq V_{CC} \leq 3.60$			0.2		0.2		
.,	LOW Level Output	$1.10 \le V_{CC} \le 1.30$	I <sub>OL</sub> =2mA		.25 x V <sub>CC</sub>		.25 x V <sub>CC</sub>	.,	
V <sub>OL</sub>	Voltage	$1.40 \le V_{CC} \le 1.60$	I <sub>OL</sub> =4mA		.25 x V <sub>CC</sub>		.25 x V <sub>CC</sub>	V	
		$1.65 \leq V_{CC} \leq 1.95$	I <sub>OL</sub> =6mA		0.3		0.3		
		$ \begin{array}{c c} 2.30 \le V_{CC} \le 2.70 \\ \hline 2.70 \le V_{CC} \le 3.60 \end{array}   I_{OL} = 120 $	L =40m A		0.4		0.4		
			I <sub>OL</sub> =IZMA		0.4		0.4		
		$2.30 \leq V_{CC} \leq 2.70$	L =40m A		0.6		0.6		
		$2.70 \leq V_{CC} \leq 3.60$	I <sub>OL</sub> =18mA		0.4		0.4		
	9	$2.70 \leq V_{CC} \leq 3.60$	I <sub>OL</sub> =24mA		0.55		0.55		
I <sub>IN</sub>	Input Leakage Current	0.90 to 3.60	$0 \leq V_{IN} \leq 3.6V$		±0.1		±0.5	μA	
I <sub>OFF</sub>	Power Off Leakage Current	0	$0 \leq (V_{IN}, V_O) \leq 3.60$		0.5		0.5	μA	
	Quiescent Supply	0.00 to 2.60	V <sub>IN</sub> =V <sub>CC</sub> or GND		0.9		0.9		
Icc	Current 0.90 to 3.60		$V_{CC} \leq V_{IN} \leq 3.6 V$				±0.9	μA	

### **AC Electrical Characteristics**

Complete	Downwater	W	Conditions		T <sub>A</sub> =25°(	<b>C</b>	T <sub>A</sub> =-40	to 85°C	Units	F:
Symbol	Parameter	V <sub>CC</sub>	Conditions	Min.	Тур.	Min.	Тур.	Min.	Units	Figure
		0.90	$C_L$ =15pF, $R_L$ =1M $\Omega$		15.0					
		$1.10 \leq V_{CC} \leq 1.30$	C =15nF D =2KO	4.0	8.0	16.5	3.3	31.0		7
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation	$1.40 \le V_{CC} \le 1.60$	$C_L=15pF, R_L=2K\Omega$	2.0	6.0	10.0	2.0	12.0		Figure 15 Figure 16
	Delay	$1.65 \leq V_{CC} \leq 1.95$	$C_L$ =30pF, R <sub>I</sub> =500 $\Omega$	2.0	4.0	9.1	1.9	10.0		
		$2.30 \leq V_{CC} \leq 2.70$		1.5	3.1	6.2	1.4	6.7		
		$2.70 \leq V_{CC} \leq 3.60$	11( 00011	1.2	2.5	5.4	1.2	6.1		
C <sub>IN</sub>	Input Capacitance	0			8				pF	
Соит	Output Capacitance	0			12				pF	K)
C <sub>PD</sub>	Power Dissipation Capacitance	0.90 to 3.60	V <sub>I</sub> =0V or V <sub>CC</sub> , f=10MHz		10				pF	

### **AC Loadings and Waveforms**

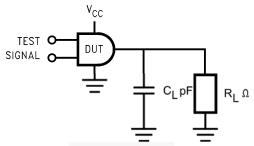


Figure 15. AC Test Circuit

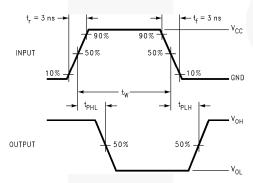


Figure 16. AC Waveforms

Symbol	V <sub>cc</sub>						
Symbol	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V	1.5V ± 0.10V	1.2V ± 0.10V	Ve.0	
V <sub>mi</sub>	1.5V	V <sub>CC</sub> /2					
$V_{mo}$	1.5V	V <sub>CC</sub> /2					

### **Physical Dimensions**

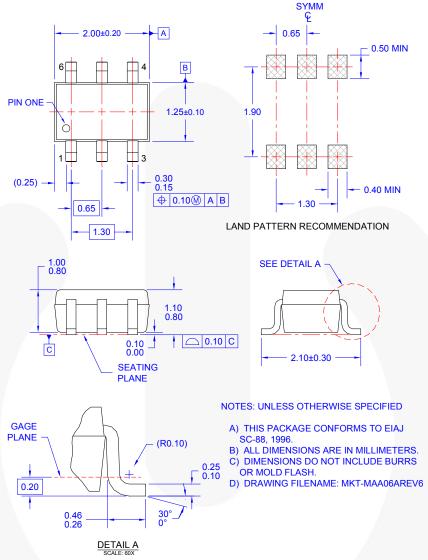


Figure 17. 6-Lead, SC70, EIAJ SC-88a, 1.25mm Wide

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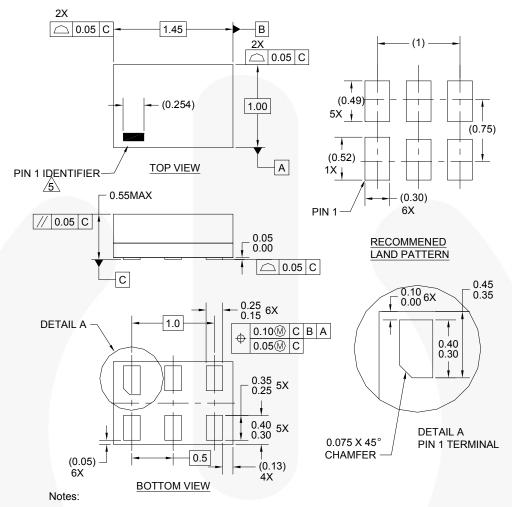
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#### **Tape and Reel Specifications**

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/products/analog/pdf/sc70-6 tr.pdf

Package Designator	Tape Section	<b>Cavity Number</b>	<b>Cavity Status</b>	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
P6X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

### **Physical Dimensions**



- 1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
- 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y14.5M-1994
- 4. FILENAME AND REVISION: MAC06AREV4
- 5 PIN ONE IDENTIFIER IS 2X LENGTH OF ANY

OTHER LINE IN THE MARK CODE LAYOUT.

Figure 18. 6-Lead, MicroPak™, 1.0mm Wide

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Package Designator	Tape Section	Cavity Number	<b>Cavity Status</b>	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
L6X	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

#### **Physical Dimensions** 0.89 ○ 0.05 C 0.35 1.00 2X 5X 0.40 PIN 1 0.66 MIN 250uM 1.00 1X 0.45 6X 0.19 ○ 0.05 C **TOP VIEW** RECOMMENDED LAND PATTERN 2X FOR SPACE CONSTRAINED PCB 0.90 // 0.05 C 0.35 0.55MAX С 5X 0 52 SIDE VIEW 0.73 1X 0.57 (0.08) 4X 0.09 6X 2 **DETAIL A** 0.19 - 0.20 6X

- ALTERNATIVE LAND PATTERN FOR UNIVERSAL APPLICATION 5X 0.35 0.25 0.60 0.10M C B A 0.35  $\oplus$ (80.0).05 C 4X **BOTTOM VIEW** A. COMPLIES TO JEDEC MO-252 STANDARD
  - 0.40 0.30 0.075X45° **DETAIL A CHAMFER** PIN 1 LEAD SCALE: 2X

(0.05)6X

- B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. LANDPATTERN RECOMMENDATION IS BASED ON FSC
- E. DRAWING FILENAME AND REVISION: MGF06AREV3

Figure 19. 6-Lead, MicroPak2, 1x1mm Body, .35mm Pitch

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#### **Tape and Reel Specifications**

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/packaging/MicroPAK2 6L tr.pdf

Package Designator	Tape Section	Cavity Number	<b>Cavity Status</b>	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed





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