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## FDMC8462

### N-Channel Power Trench® MOSFET

40V, 20A, 5.8mΩ

#### Features

- Max  $r_{DS(on)}$  = 5.8mΩ at  $V_{GS} = 10V$ ,  $I_D = 13.5A$
- Max  $r_{DS(on)}$  = 8.0mΩ at  $V_{GS} = 4.5V$ ,  $I_D = 11.8A$
- Low Profile - 1mm max in Power 33
- 100% UIL Tested
- RoHS Compliant

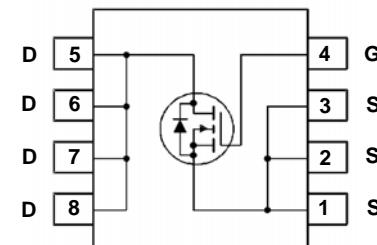
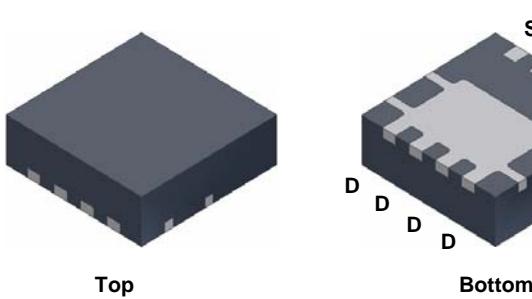


#### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

#### Application

- DC - DC Conversion



Power 33

#### MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	40	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ C$	20	A
	-Continuous (Silicon limited) $T_C = 25^\circ C$	64	
	-Continuous $T_A = 25^\circ C$ (Note 1a)	14	
	-Pulsed	50	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	mJ
$P_D$	Power Dissipation $T_C = 25^\circ C$	41	W
	Power Dissipation $T_A = 25^\circ C$ (Note 1a)	2.0	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

#### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	°C/W

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8462	FDMC8462	Power 33	13"	12mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$\text{BV}_{\text{DSS}}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	40			V
$\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		31		$\text{mV}/^\circ\text{C}$
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{V}, V_{DS} = 32\text{V}$ ,			1	$\mu\text{A}$
$I_{\text{GSS}}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-6.6		$\text{mV}/^\circ\text{C}$
$r_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 13.5\text{A}$		4.7	5.8	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 11.8\text{A}$		6.4	8.0	
		$V_{GS} = 10\text{V}, I_D = 13.5\text{A}, T_J = 125^\circ\text{C}$		7.1	9.3	
$g_{\text{FS}}$	Forward Transconductance	$V_{DD} = 5\text{V}, I_D = 13.5\text{A}$		60		S

### Dynamic Characteristics

$C_{\text{iss}}$	Input Capacitance	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		2000	2660	pF
$C_{\text{oss}}$	Output Capacitance			545	725	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance			80	120	pF
$R_g$	Gate Resistance	$f = 1\text{MHz}$		2.7		$\Omega$

### Switching Characteristics

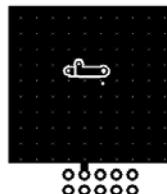
$t_{d(\text{on})}$	Turn-On Delay Time	$V_{DD} = 20\text{V}, I_D = 13.5\text{A}, V_{GS} = 10\text{V}, R_{\text{GEN}} = 6\Omega$		12	21	ns
$t_r$	Rise Time			4	10	ns
$t_{d(\text{off})}$	Turn-Off Delay Time			27	43	ns
$t_f$	Fall Time			3	10	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{V} \text{ to } 10\text{V}$		30	43	nC
	Total Gate Charge		$V_{DD} = 20\text{V}, I_D = 13.5\text{A}$	15	21	nC
$Q_{gs}$	Gate to Source Charge			6		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			5		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 13.5\text{A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\text{V}, I_S = 1.7\text{A}$ (Note 2)		0.7	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 13.5\text{A}, di/dt = 100\text{A}/\mu\text{s}$		35	57	ns
				20	32	

#### NOTES:

1.  $R_{\text{0JA}}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5$  in. board of FR-4 material.  $R_{\text{0JC}}$  is guaranteed by design while  $R_{\text{0CA}}$  is determined by the user's board design.



a.  $53^\circ\text{C}/\text{W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper



b.  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3. Starting  $T_J = 25^\circ\text{C}$ ; N-ch:  $L = 3\text{ mH}$ ,  $I_{AS} = 12\text{A}$ ,  $V_{DD} = 40\text{V}$ ,  $V_{GS} = 10\text{V}$

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

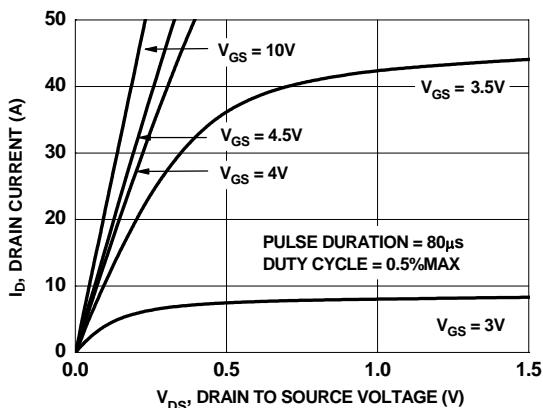


Figure 1. On-Region Characteristics

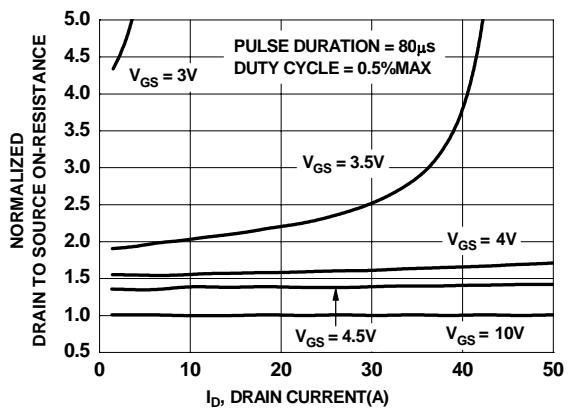


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

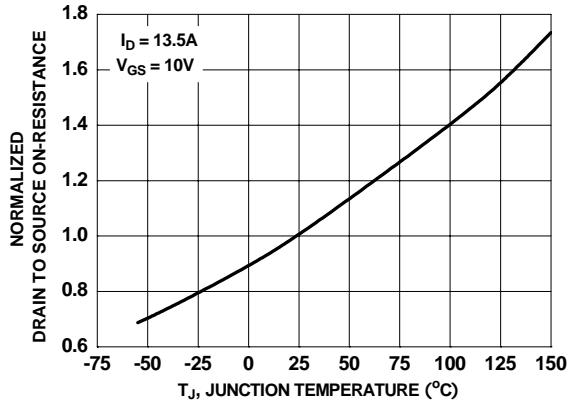


Figure 3. Normalized On-Resistance vs Junction Temperature

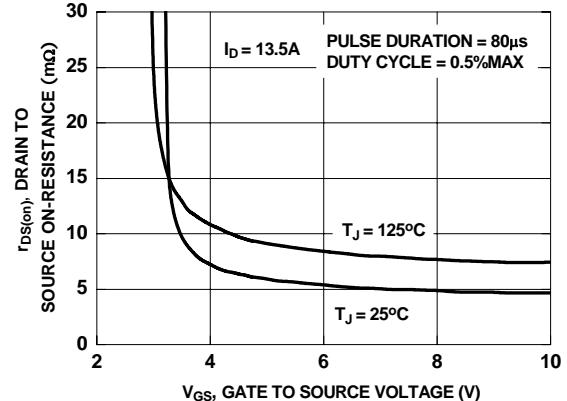


Figure 4. On-Resistance vs Gate to Source Voltage

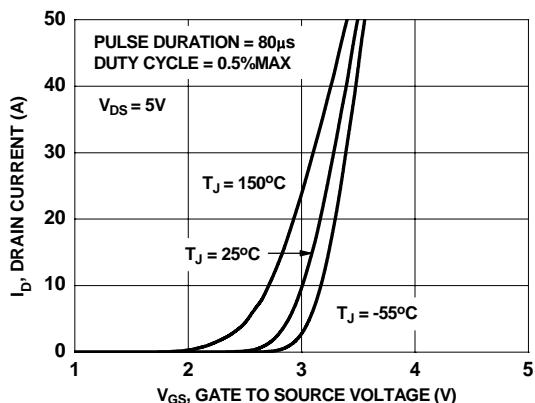


Figure 5. Transfer Characteristics

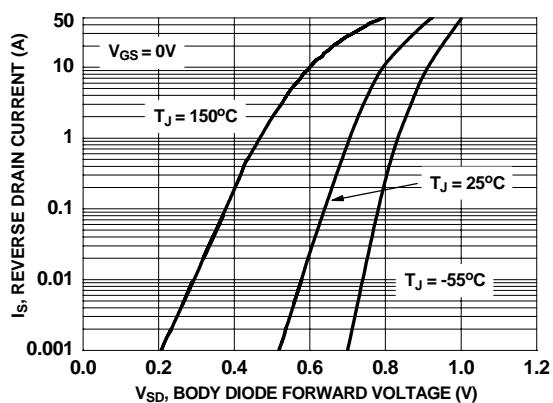


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

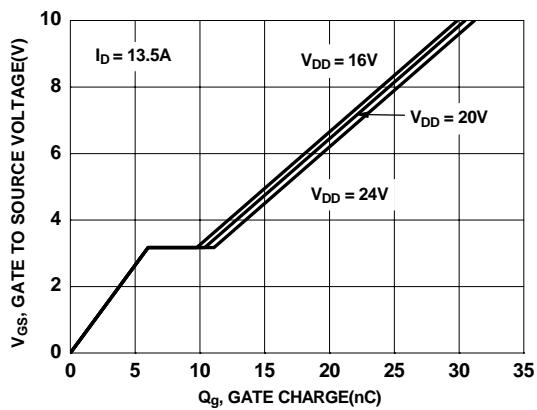


Figure 7. Gate Charge Characteristics

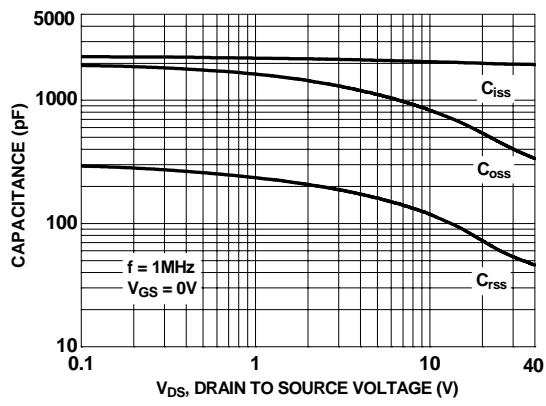


Figure 8. Capacitance vs Drain to Source Voltage

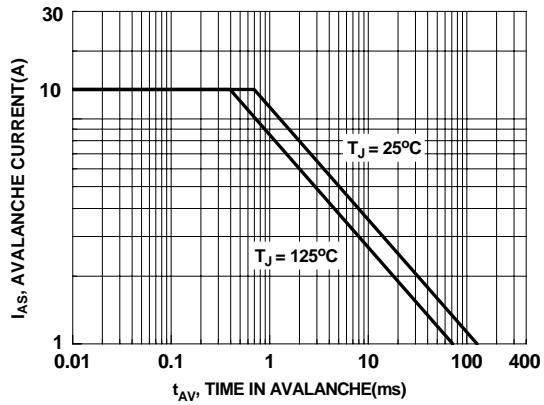


Figure 9. Unclamped Inductive Switching Capability

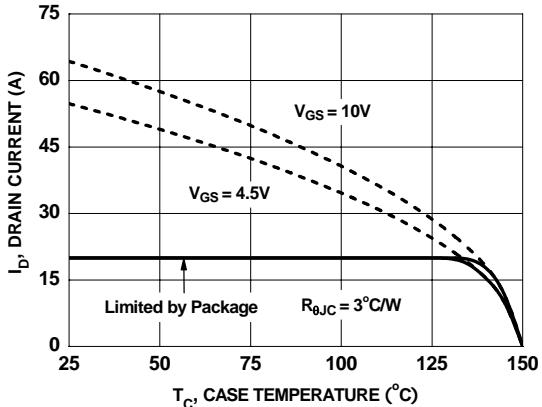


Figure 10. Maximum Continuous Drain Current vs Case Temperature

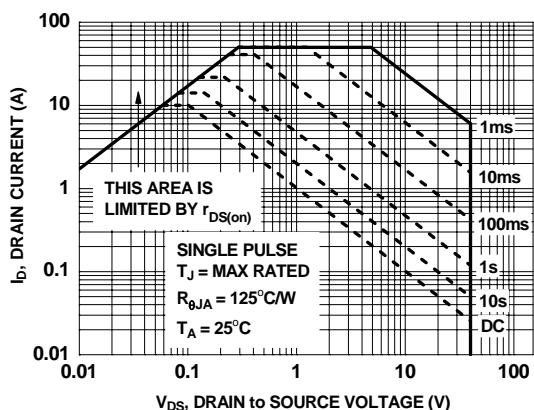


Figure 11. Forward Bias Safe Operating Area

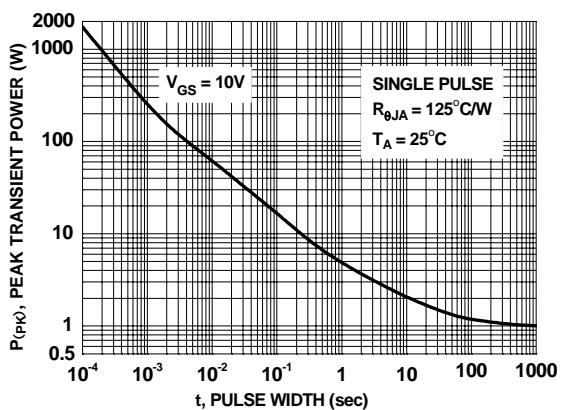


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics  $T_J = 25^\circ\text{C}$  unless otherwise noted

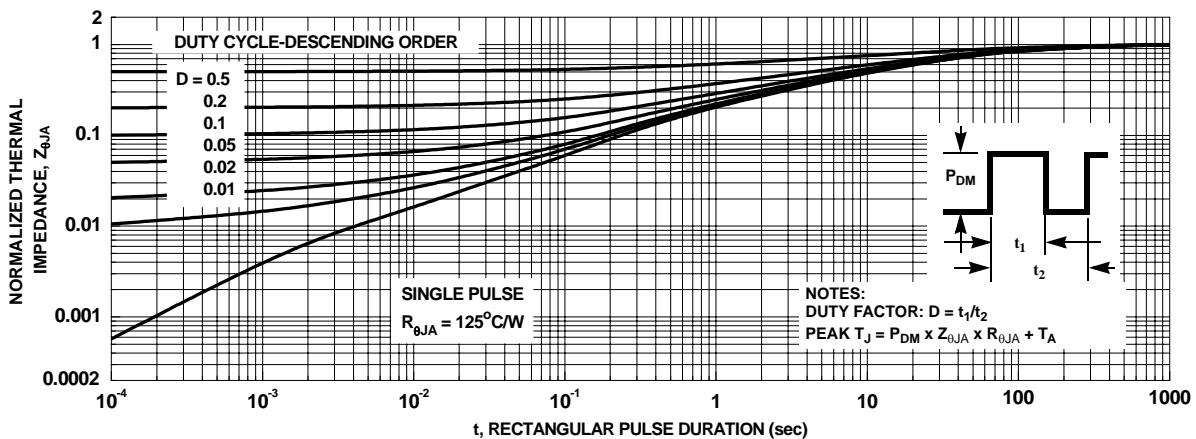
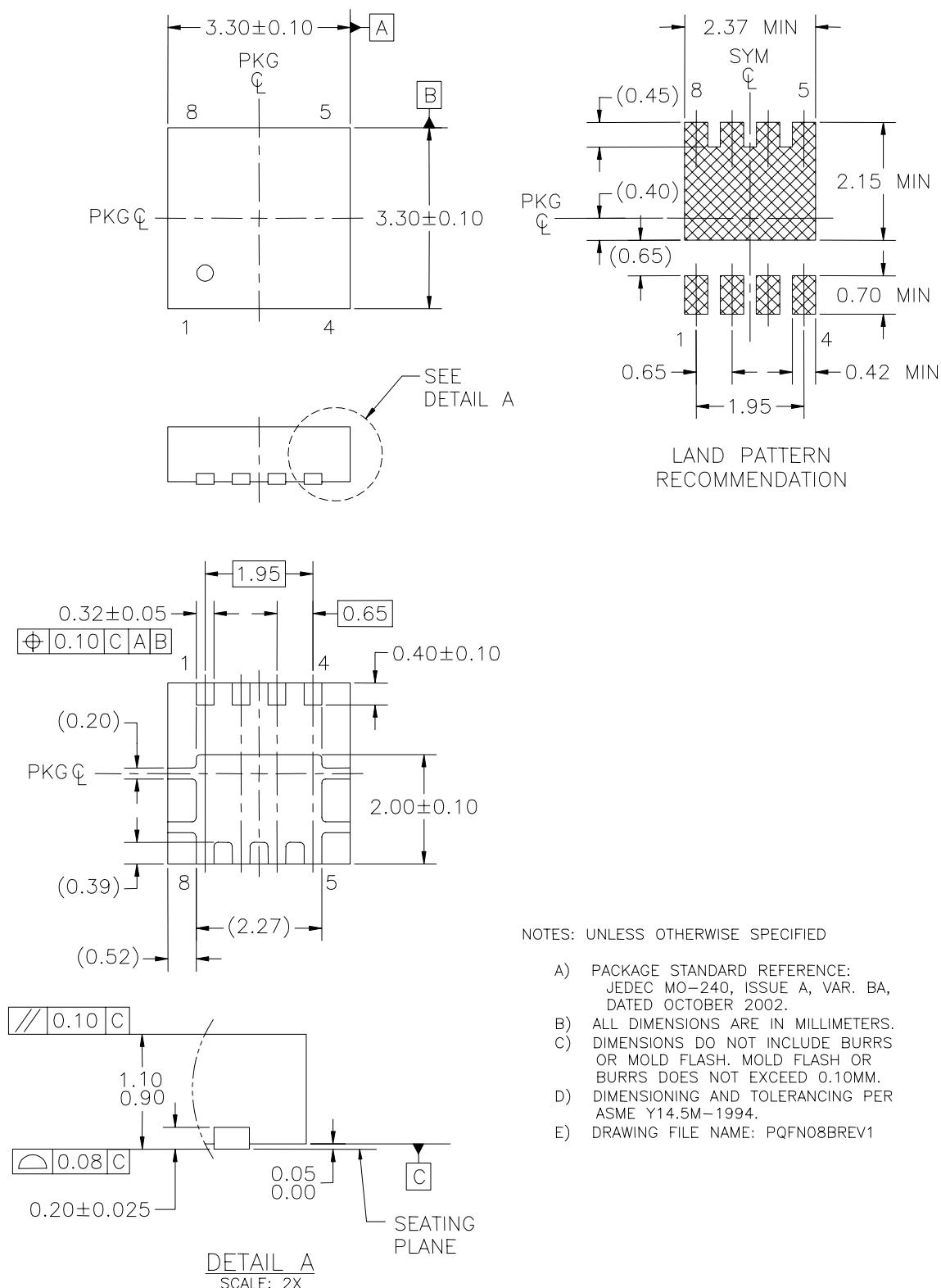


Figure 13. Transient Thermal Response Curve

Dimensional Outline and Pad Layout





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