

High Isolation SP3T SWITCH

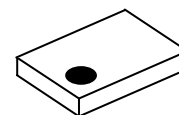
■ GENERAL DESCRIPTION

The NJG1698K84 is a two bit control GaAs high isolation SP3T switch. It features very high isolation and low control voltage. It has integrated DC blocking capacitor at PC port.

It has integrated ESD protection circuits to achieve high ESD tolerance.

The small and thin 10-pin QFN10-84 package is adopted.

■ PACKAGE OUTLINE



NJG1698K84

■ APPLICATIONS

Multi-mode 2G/3G and LTE application receive system

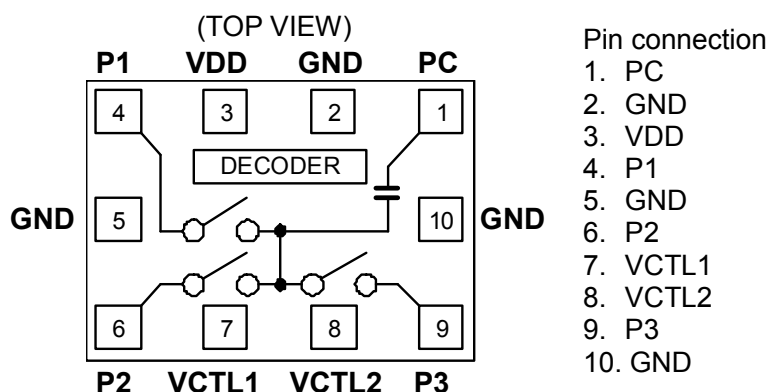
Pre PA switching, reception bands switching applications

General purpose switching applications

■ FEATURES

- Low voltage logic control $V_{CTL(H)}=1.8V$ typ.
- Low voltage operation $V_{DD}=2.7V$ typ.
- High isolation
 - 51dB typ. @f=1.0GHz, $P_{IN}=0dBm$
 - 50dB typ. @f=2.0GHz, $P_{IN}=0dBm$
 - 43dB typ. @f=2.7GHz, $P_{IN}=0dBm$
- Low insertion loss
 - 0.50dB typ. @f=1.0GHz, $P_{IN}=0dBm$
 - 0.55dB typ. @f=2.0GHz, $P_{IN}=0dBm$
 - 0.60dB typ. @f=2.7GHz, $P_{IN}=0dBm$
- Small & thin package QFN10-84 Package (Package size: 1.55 x 1.15 x 0.37mm typ.)
- RoHS compliant and Halogen Free, MSL1

■ PIN CONFIGURATION



■ TRUTH TABLE

"H"= $V_{CTL(H)}$, "L"= $V_{CTL(L)}$

VCTL1	VCTL2	PATH
H	L	PC-P1
L	H	PC-P2
H	H	PC-P3

NOTE: Please note that any information on this datasheet will be subject to change.

■ ABSOLUTE MAXIMUM RATINGS

($T_a=+25^{\circ}\text{C}$, $Z_s=Z_i=50\Omega$)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	P_{IN}	$V_{DD}=2.7\text{V}$	28	dBm
Supply Voltage	V_{DD}	VDD terminal	5.0	V
Control Voltage	V_{CTL}	VCTL terminal	5.0	V
Power Dissipation	P_D	Four-layer FR4 PCB without through-hole (114.3×76.2mm), $T_j=150^{\circ}\text{C}$	270	mW
Operating Temperature	T_{opr}		-40 to +90	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		-55 to +150	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS1 (DC CHARACTERISTICS)

(General conditions: $T_a=+25^{\circ}\text{C}$, $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	VDD terminal	1.5	2.7	4.5	V
Operating Current	I_{DD}		-	20	40	μA
Control Voltage (LOW)	$V_{CTL(L)}$	VCTL terminal	0	0	0.45	V
Control Voltage (HIGH)	$V_{CTL(H)}$	VCTL terminal	1.35	1.8	4.5	V
Control Current	I_{CTL}	$V_{CTL(H)} = 1.8\text{V}$	-	5	10	μA

■ ELECTRICAL CHARACTERISTICS2 (RF CHARACTERISTICS)

(General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$, $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss 1	LOSS1	$f=0.5\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.55	0.85	dB
Insertion Loss 2	LOSS2	$f=1.0\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.50	0.75	dB
Insertion Loss 3	LOSS3	$f=2.0\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.55	0.80	dB
Insertion Loss 4	LOSS4	$f=2.7\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.60	0.85	dB
Isolation 1	ISL1	PC-P1, P2, P3 $f=0.5\text{GHz}$, $P_{IN}=0\text{dBm}$	53	56	-	dB
Isolation 2	ISL2	PC-P1, P2, P3 $f=1.0\text{GHz}$, $P_{IN}=0\text{dBm}$	48	51	-	dB
Isolation 3	ISL3	PC-P1, P2, P3 $f=2.0\text{GHz}$, $P_{IN}=0\text{dBm}$	47	50	-	dB
Isolation 4	ISL4	PC-P1, P2, P3 $f=2.7\text{GHz}$, $P_{IN}=0\text{dBm}$	40	43	-	dB
Input power at 0.2dB Compression Point	$P_{-0.2\text{dB}}$	$f=2.0\text{GHz}$	19	23	-	dBm
VSWR	VSWR	$f=2.0\text{GHz}$, On port	-	1.3	1.5	-
Switching time	T_{SW}	50% V_{CTL} to 10/90% RF	-	2	5	μs

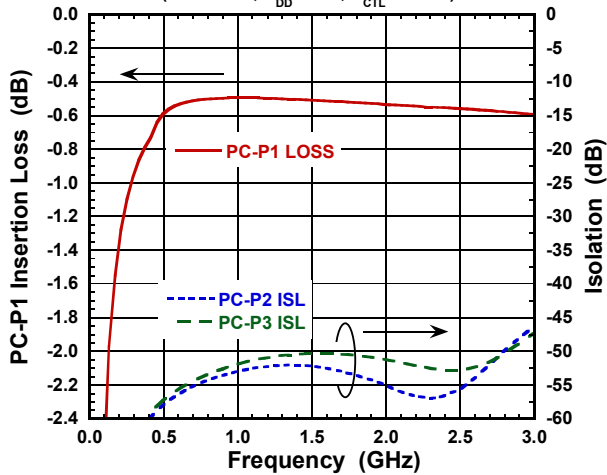
■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	PC	RF input/output port. No DC blocking capacitor is required for this port because of internal capacitor.
2	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
3	VDD	Positive voltage supply terminal. The positive voltage (+1.5 to +4.5V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.
4	P1	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
5	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
6	P2	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
7	VCTL1	Control signal input terminal. This terminal is set to High-Level (+1.35 to +4.5V) or Low-Level (0 to +0.45V). Please connect a bypass capacitor with GND terminal for excellent RF performance.
8	VCTL2	Control signal input terminal. This terminal is set to High-Level (+1.35 to +4.5V) or Low-Level (0 to +0.45V). Please connect a bypass capacitor with GND terminal for excellent RF performance.
9	P3	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
10	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.

■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

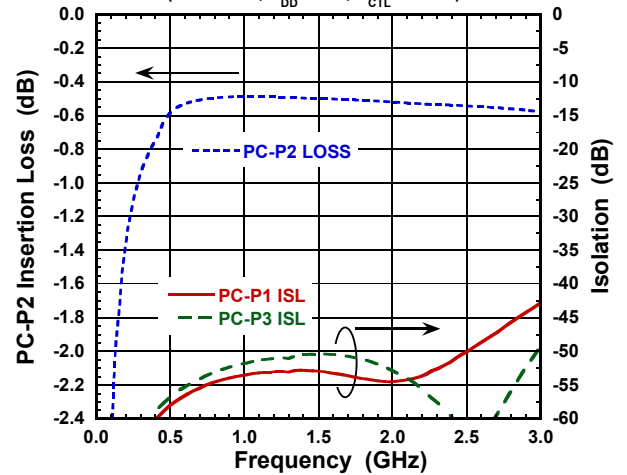
LOSS, ISL vs Frequency

(PC-P1 ON, $V_{DD}=2.7V$, $V_{CTL}=1.8/0V$)



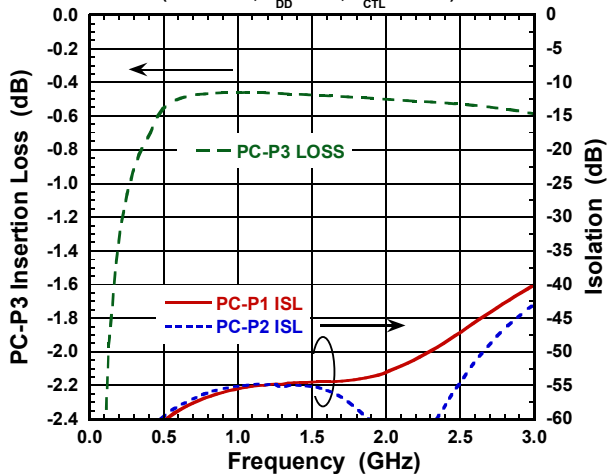
LOSS, ISL vs Frequency

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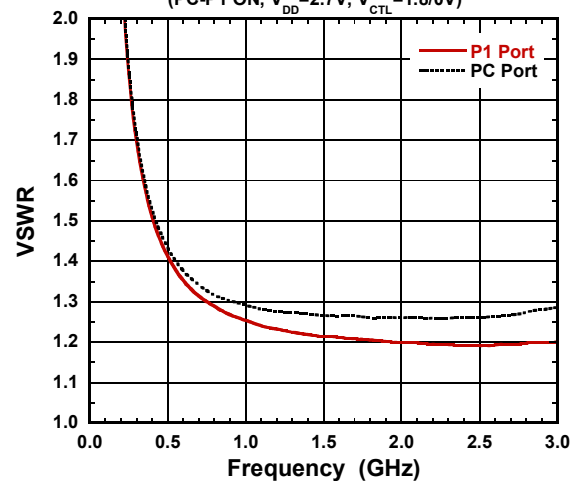
LOSS, ISL vs Frequency

(PC-P3 ON, $V_{DD}=2.7V$, $V_{CTL}=1.8/0V$)



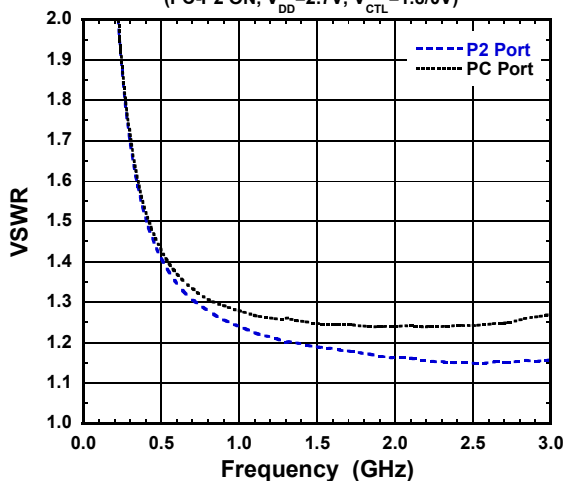
VSWR vs Frequency

(PC-P1 ON, $V_{DD}=2.7V$, $V_{CTL}=1.8/0V$)



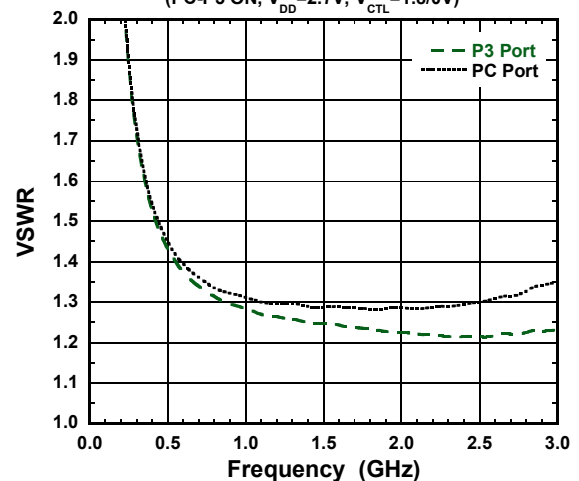
VSWR vs Frequency

(PC-P2 ON, $V_{DD}=2.7V$, $V_{CTL}=1.8/0V$)



VSWR vs Frequency

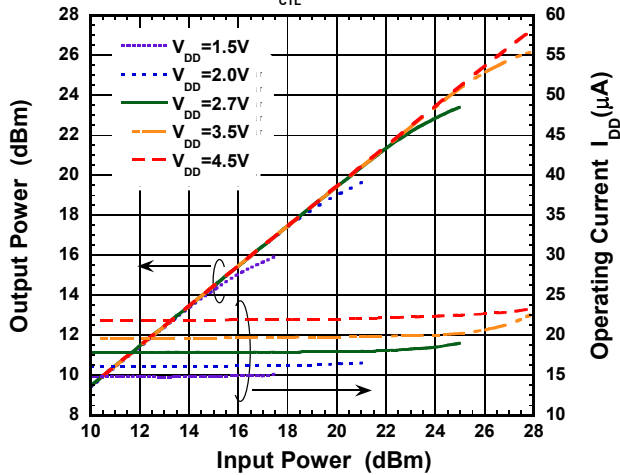
(PC-P3 ON, $V_{DD}=2.7V$, $V_{CTL}=1.8/0V$)



■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

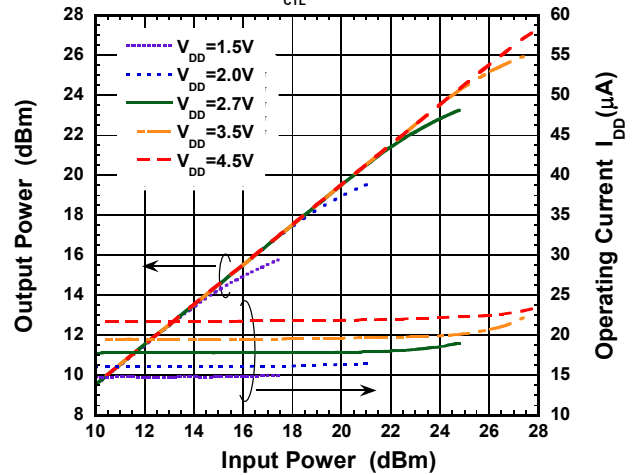
Output Power, I_{DD} vs Input Power

(PC-P1 ON, $V_{CTL}=1.8/0V$, $f=0.5GHz$)



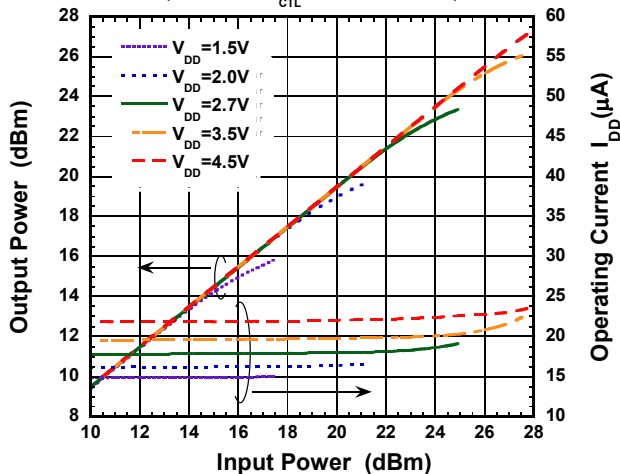
Output Power, I_{DD} vs Input Power

(PC-P1 ON, $V_{CTL}=1.8/0V$, $f=1.0GHz$)



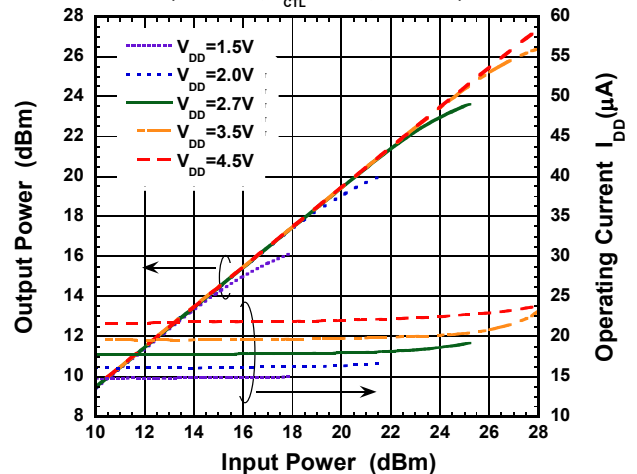
Output Power, I_{DD} vs Input Power

(PC-P1 ON, $V_{CTL}=1.8/0V$, $f=2.0GHz$)



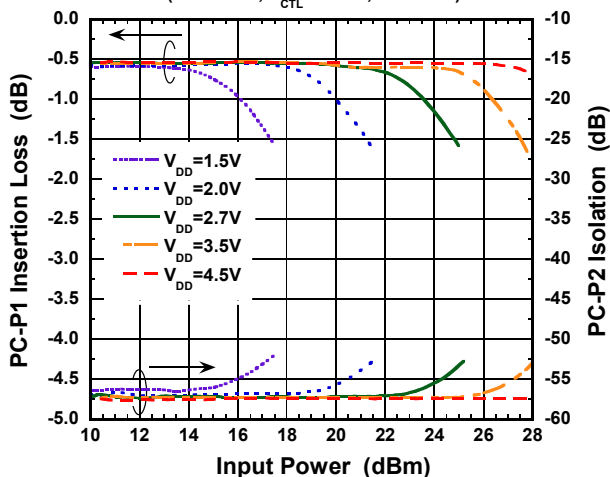
Output Power, I_{DD} vs Input Power

(PC-P1 ON, $V_{CTL}=1.8/0V$, $f=2.7GHz$)



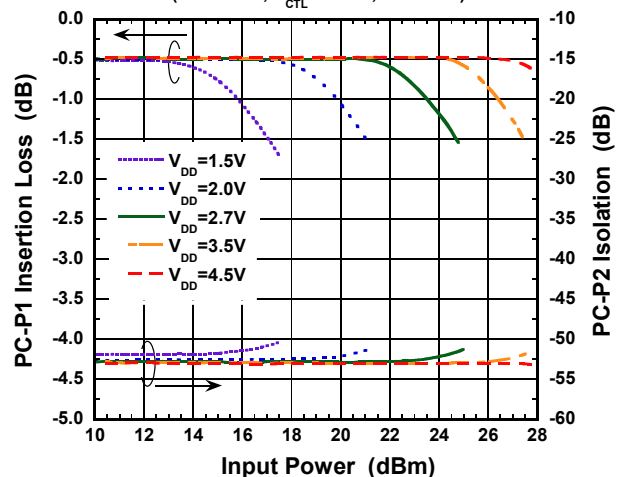
Loss, ISL vs Input Power

(PC-P1 ON, $V_{CTL}=1.8/0V$, $f=0.5GHz$)



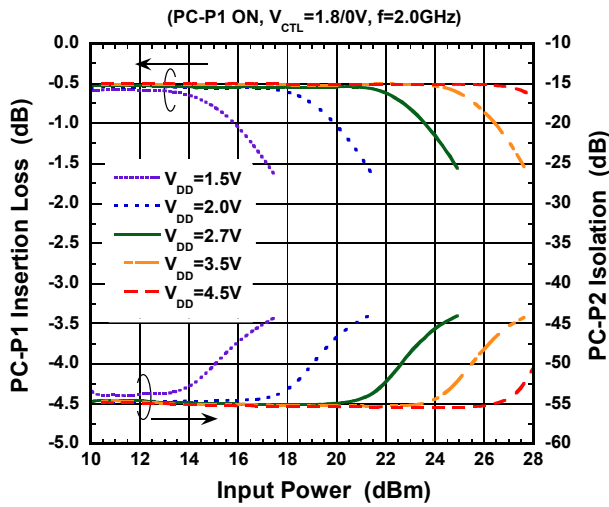
Loss, ISL vs Input Power

(PC-P1 ON, $V_{CTL}=1.8/0V$, $f=1.0GHz$)

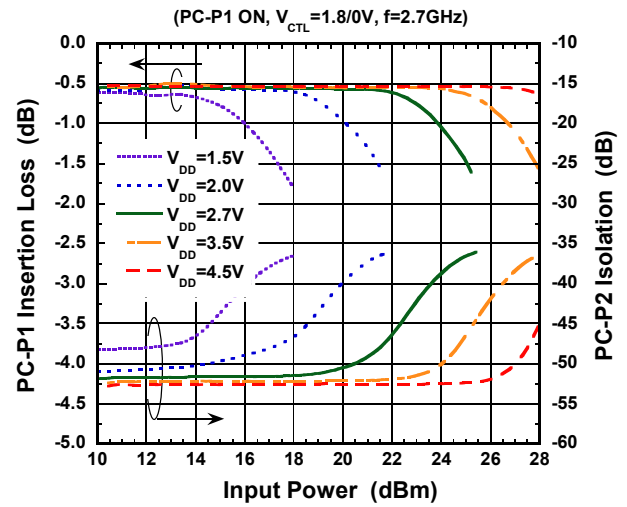


■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

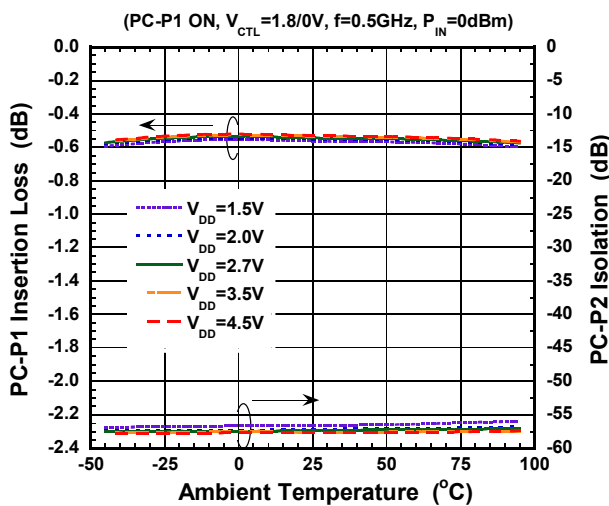
Loss, ISL vs Input Power



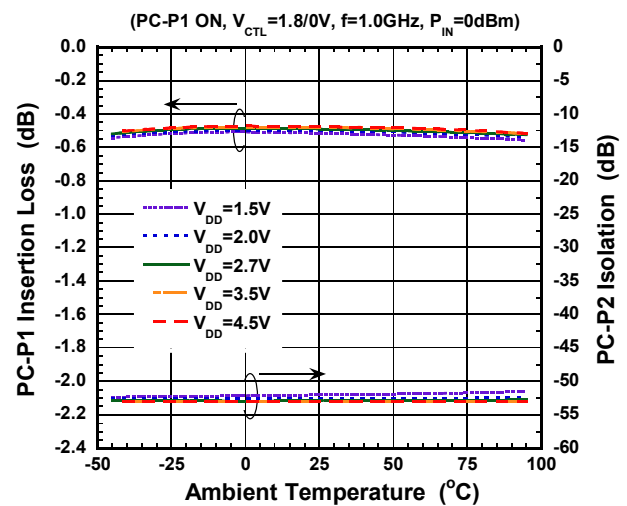
Loss, ISL vs Input Power



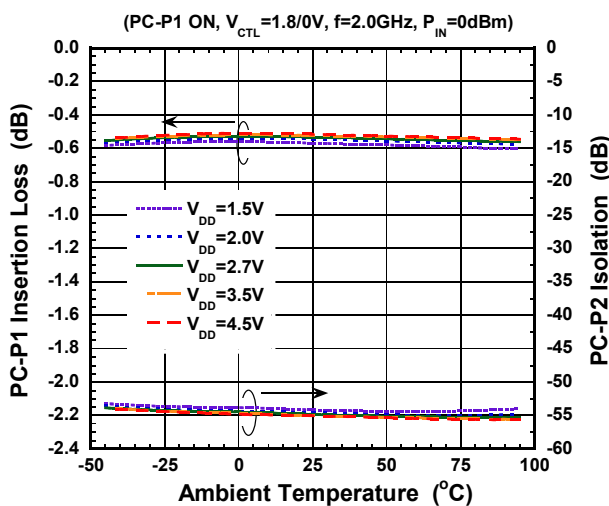
Loss, ISL vs Temperature



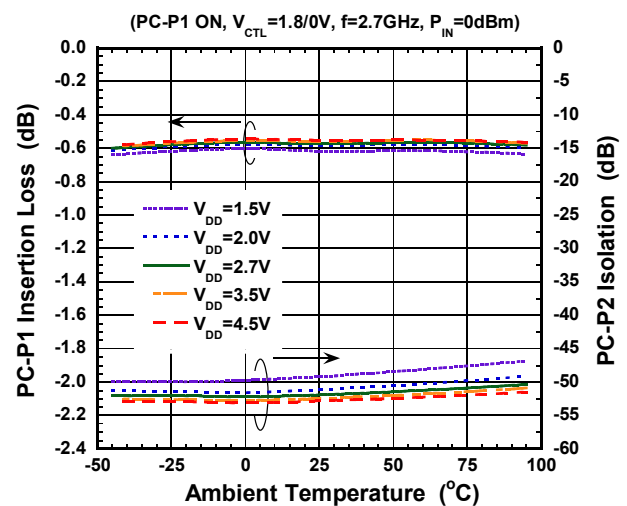
Loss, ISL vs Temperature



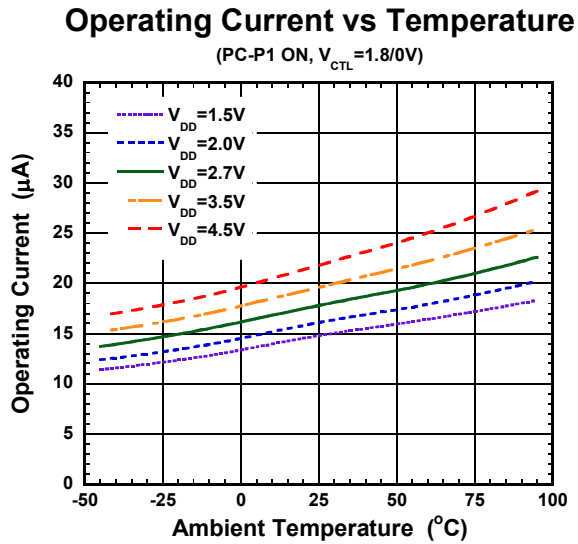
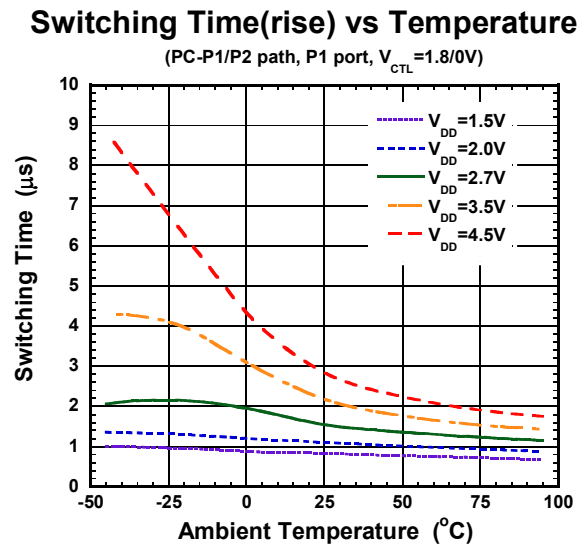
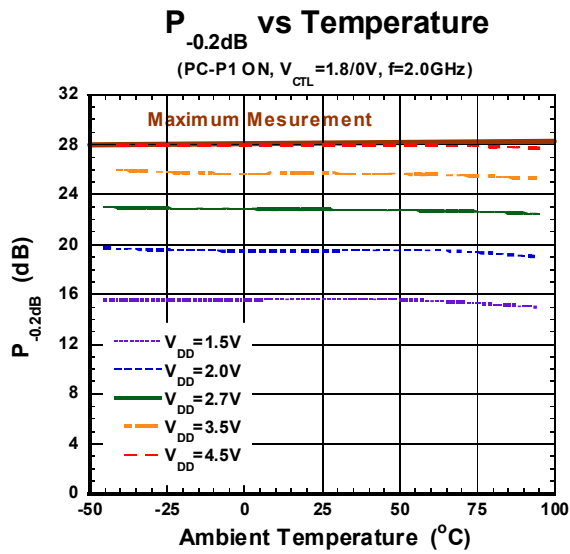
Loss, ISL vs Temperature



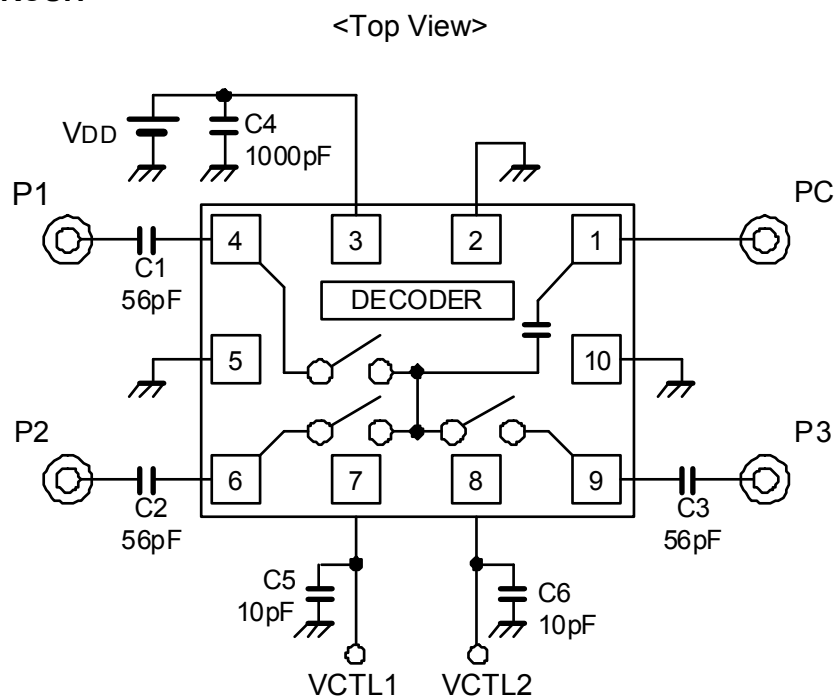
Loss, ISL vs Temperature



■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)



APPLICATION CIRCUIT



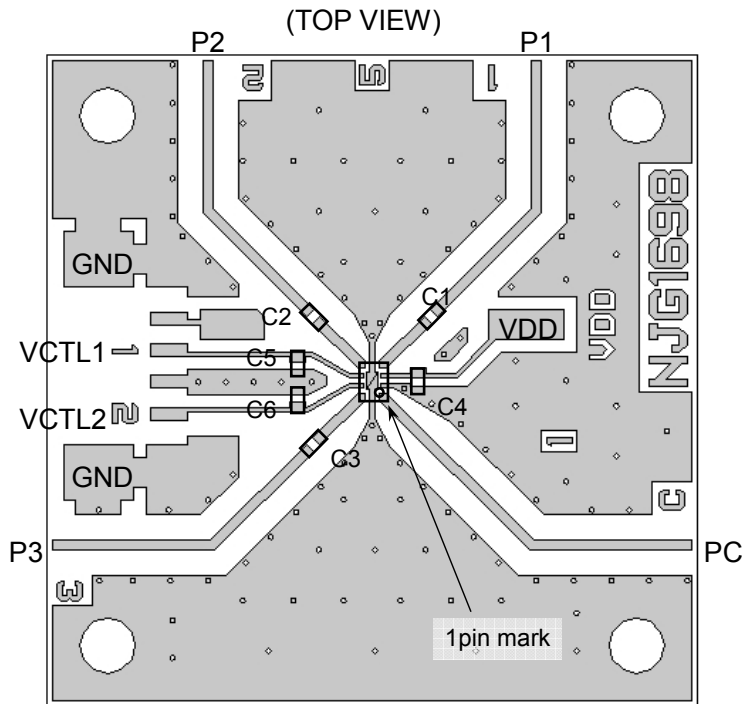
Note:

The DC blocking capacitor is not necessary at PC Port because of the integrated DC blocking capacitor.

PARTS LIST

Part ID	Value	Notes
C1 to C3	56pF	MURATA (GRM15)
C4	1000pF	MURATA (GRM15)
C5, C6	10pF	MURATA (GRM15)

■ APPLIED CIRCUIT BOARD EXAMPLES

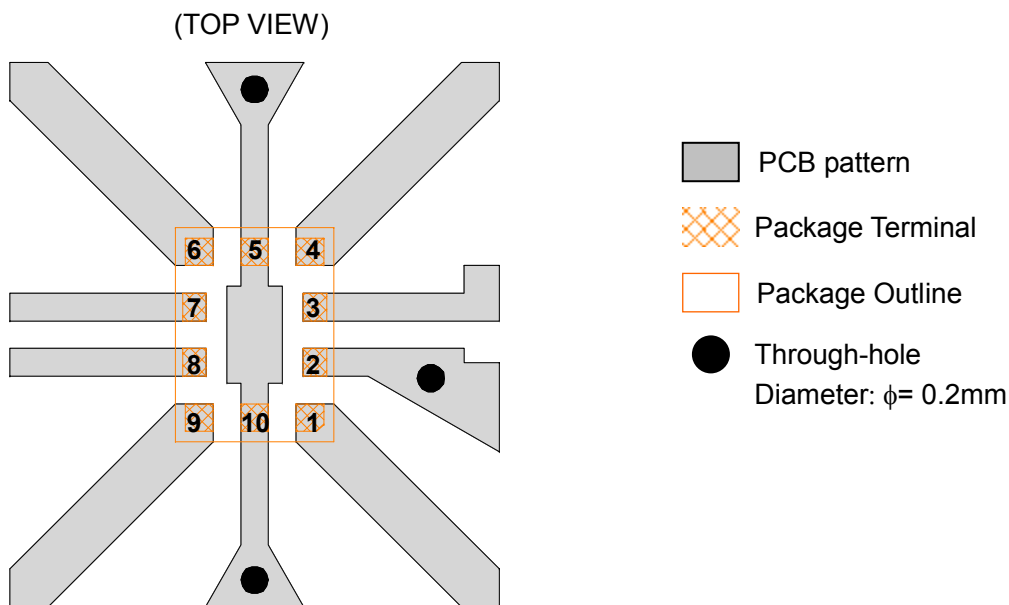


PCB: FR-4, $t=0.2\text{mm}$
 Capacitor Size: 1005 (1.0 x 0.5 mm)
 Strip Line Width: 0.4mm
 PCB Size: 25.8 x 25.8mm
 Through Hole Diameter: 0.2mm

Loss of PCB, capacitors and connectors

Frequency (GHz)	Loss (dB)
0.5	0.17
1.0	0.26
2.0	0.41
2.7	0.53

<PCB LAYOUT GUIDELINE>



To achieve the isolation specified in the datasheet, it is needed that the ground plane as shown above figure.

PRECAUTIONS

- [1] The DC current at RF ports must be equal to zero, which can be achieved with DC blocking capacitors (C1, C2, and C3). (However, in case there is no possibility that DC current flows, the DC blocking capacitors are unnecessary, i.e. the RF signals are fed by SAW filters that block DC current by nature, etc.)
- [2] To reduce stripline influence on RF characteristics, please locate the bypass capacitor C4, C5, and C6 close to VDD and VCTL terminal.
- [3] For good isolation, the GND terminals must be connected to the PCB ground plane of substrate, and the through-holes connecting the backside ground plane should be placed near by the pin connection.

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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А