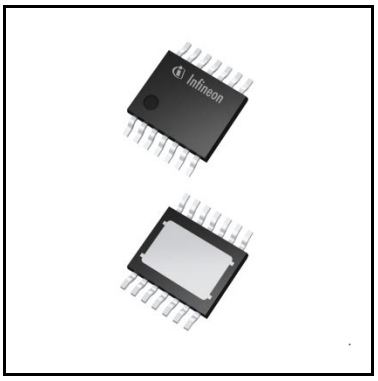
TLD1114-1EP

LITIX™ Basic+

AEC Qualified RoHS



Features

- Single channel device with integrated and protected output stage (current source), optimized to drive LEDs as additional low cost current source
- Easy direct control without external component from other LITIX Basic+ LED Drivers
- High output current (up to 360 mA)
- Possibility to off-load power consumption to allow maximum current driving capability via low cost external components (Power Shift)
- Very low current consumption in sleep mode
- Very low output leakage when channel is “off”
- Low current consumption during fault
- Output currents’ control via external low power resistor
- Easy delivery of additional current/power demand via other LITIX™ Basic+ family members with direct drive
- Reverse polarity protection allows reduction of external components and improves system performance at low battery/input voltages
- Overload protection
- Wide temperature range: -40°C < T_J < 150°C
- Output current control via external low power resistor
- Green product (RoHS compliant)

Potential applications

- Cost effective “stop”/ “tail” function implementation with shared and separated LEDs per function
- Turn indicators
- Position, fog, rear lights and side markers
- Animated light functions like wiping indicators and “welcome/goodbye” functions
- Day Running Light
- Interior lighting functions like ambient lighting (including RGB color control), illumination and dash board lighting
- LED indicators for industrial applications and instrumentation

Product validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100/101.

Description

The LITIX™ Basic+ TLD1114-1EP is a single channel high-side driver IC with integrated output stage. It is designed to control LEDs with a current up to 360 mA. In typical automotive applications the device is capable of driving 3 red LEDs with a current up to 180 mA and even above, if not limited by the overall system thermal properties. Practically, the output current is controlled by an external resistor or reference source, independently from load and supply voltage changes.

Table 1 Product summary

Parameter	Symbol	Values
Operating voltage	$V_{S(nom)}$	5.5 V … 40 V
Maximum voltage	$V_{S(max)}$ $V_{OUT(max)}$	40 V
Nominal output (load) current	$I_{OUT(nom)}$	180 mA (nominal) when using the automotive supply voltage range 8 V - 18 V. Currents up to $I_{OUT(max)}$ are possible with low thermal resistance R_{thJA}
Maximum output (load) current	$I_{OUT(max)}$	360 mA depending on R_{thJA}
Current accuracy at R_{SET} = 10 kΩ	K_{RT}	900±3.33%
Current consumption in sleep mode	$I_{S(sleep, typ)}$	0.1 µA
Maximum current consumption during fault	$I_{S(fault, ERRN)}$	850 µA or less when fault is detected from another device (disabled via ERRN)

Type	Package	Marking
TLD1114-1EP	PG-TSDSO-14	TLD1114

Table of Contents

1 Block diagram

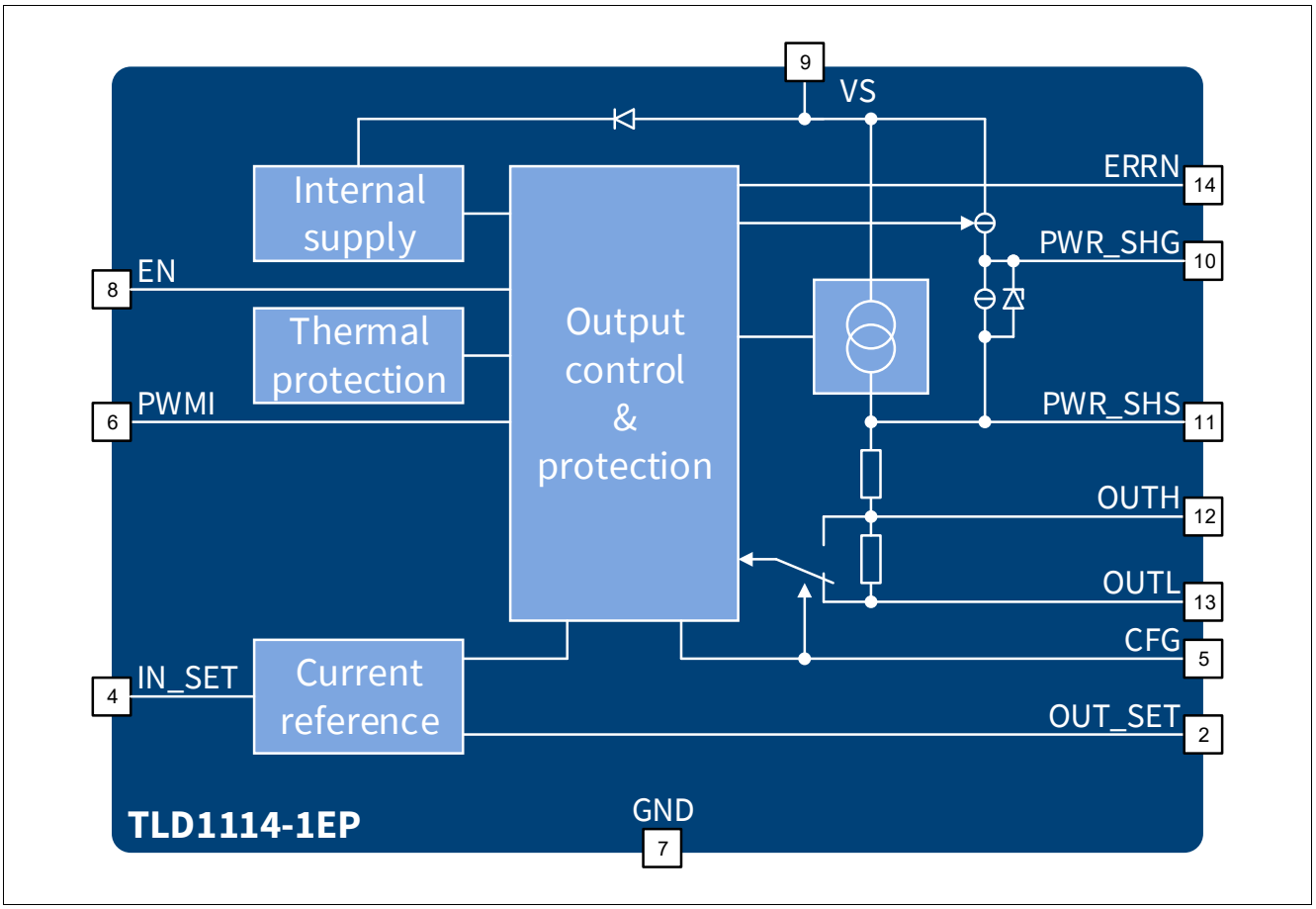


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

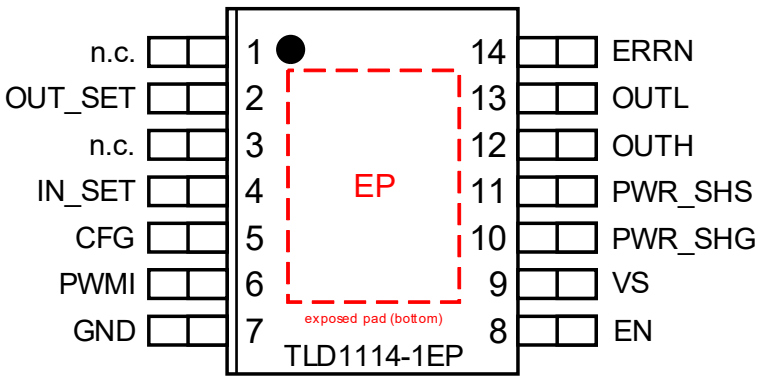


Figure 2 Pin configuration

2.2 Pin definitions and functions

Pin	Symbol	Function
9	VS	**Supply voltage;** Connected to battery or supply control switch, with EMC filter
7	GND	**Ground;** Signal ground
4	IN_SET	**Control input for OUT channel;** Connect to a low power resistor to adjust OUT output current. Alternatively, a different current reference (i.e. the OUT_SET of another LITIX™ Basic+ LED Driver) may be connected
2	OUT_SET	**Control output for additional current source;** If an additional channel or output current with same input control is needed, connect this pin to the IN_SET pin of the additional LED driver. If not used, leave the pin open
5	CFG	**Configuration input for OUT current accuracy;** If higher current accuracy is required to drive the target load, leave this pin open, else connect it to GND (see **Chapter 5** for further details)
6	PWMI	**PWM input;** Connect to an external PWM controller. If not used, connect to GND
14	ERRN	**ERROR flag I/O;** Open drain, active low. Connect to a pull-up resistor
8	EN	**Output enable control input;** Connect to a control input or VS via a resistor divider or Zener diode
12	OUTH	**Channel output;** Connect to the target load when low V_{PS} drop at higher output current is required, otherwise leave the pin open
13	OUTL	**Channel output;** Connect to the target load when high resolution at lower output current is required, otherwise leave the pin open

Pin configuration

Pin	Symbol	Function
11	PWR_SHS	**Power shift source control output;** Connect to a power resistor or to the source of an external NMOS to allow power shift control. If not used, leave the pin open
10	PWR_SHG	**Power shift gate control output;** Connect to the gate of an external NMOS to allow power shift control. If not used, leave the pin open
1, 3	n.c.	**Not connected;** Leave these pins open
Exposed Pad	EP	**Exposed Pad;** Connected to GND-pin in application

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings[1)]

T_J = -40°C to +150°C; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage							
Supply voltage	V_S	-18	–	40	V	–	P_4.1.1
EN voltage	V_{EN}	-18	–	40	V	–	P_4.1.3
EN voltage related to V_S: V_{EN} - V_S	$V_{EN(VS)}$	-40	–	18	V	–	P_4.1.4
EN voltage related to V_{OUT}: V_{EN} - V_{OUT}	$V_{EN(VOUT)}$	-18	–	40	V	–	P_4.1.5
PWR_SHG voltage	V_{PWR_SHG}	-1	–	40	V	–	P_4.1.6
PWR_SHS voltage related to V_{OUTH}: V_{PWR_SHIFTS} - V_{OUTH}	$V_{PWR\_SHS(OUTH)}$	-0.4	–	0.4	V	–	P_4.1.7
PWR_SHS voltage related to V_{OUTL}: V_{PWR_SHIFTS} - V_{OUTL}	$V_{PWR\_SHG(OUTL)}$	-0.8	–	0.8	V	–	P_4.1.46
PWR_SHS voltage	V_{PWR_SHIFTS}	-1	–	40	V	–	P_4.1.8
PWR_SHG voltage related to PWR_SHS: V_{PWR_SHIFTG} - V_{PWR_SHS}	$V_{PWR\_SHIFT(GS)}$	-0.3	–	6	V	–	P_4.1.9
Output voltage	$V_{OUTL/H}$	-1	–	40	V	–	P_4.1.10
Output voltage related to V_S: V_S - V_{OUT}	$V_{OUT(VS)}$	-18	–	40	V	–	P_4.1.11
IN_SET voltage	V_{IN_SET}	-0.3	–	6	V	–	P_4.1.12
OUT_SET voltage	V_{OUT_SET}	-0.3	–	6	V	–	P_4.1.13
CFG voltage	V_{CFG}	-0.3	–	6	V	–	P_4.1.20
PWMI voltage	V_{PWMI}	-0.3	–	6	V	–	P_4.1.14
ERRN voltage	V_{ERRN}	-0.3	–	40	V	–	P_4.1.18
Current							
Output current	I_{OUTH}	0	–	370	mA	–	P_4.1.22
Output current	I_{OUTL}	0	–	200	mA	–	P_4.1.41
PWMI current	I_{PWMI}	-0.5	–	0.5	mA	–	P_4.1.26
IN_SET current	I_{IN_SET}	0	–	800	µA	–	P_4.1.48
OUT_SET current	I_{OUT_SET}	0	–	0.5	mA	–	P_4.1.32
Temperature							
Junction temperature	T_J	-40	–	150	°C	–	P_4.1.33

Table 2 Absolute maximum ratings[1)] (cont'd)

T_J = -40°C to +150°C; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.34
ESD susceptibility							
ESD susceptibility all pins to GND	V_{ESD}	-2	–	2	kV	HBM[2)]	P_4.1.36
ESD susceptibility all pins to GND	V_{ESD}	-500	–	500	V	CDM[3)]	P_4.1.37
ESD susceptibility Pin 1, 7, 8, 14 (corner pins) to GND	$V_{ESD1,7,8,14}$	-750	–	750	V	CDM[3)]	P_4.1.38

1) Not subject to production test, specified by design
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5k Ω, 100 pF)
3) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage range for normal operation	$V_{S(nom)}$	5.5	–	18	V	–	P_4.2.1
Extended supply voltage for functional range	$V_{S(ext)}$	$V_{SUV(ON)}$	–	40	V	–	P_4.2.2
Junction temperature	T_J	-40	–	150	°C	–	P_4.2.4

Note: Within the Normal Operation range, the IC operates as described in the circuit description. Within the Extended Operation range, parameters deviations are possible. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

3.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	–	10	K/W	1)2)	P_4.3.1
Junction to Ambient 1s0p board	R_{thJA1}	– –	61 56	– –	K/W	1)3) T_A = 85°C T_A = 135°C	P_4.3.3
Junction to Ambient 2s2p board	R_{thJA2}	– –	45 43	– –	K/W	1)4) T_A = 85°C T_A = 135°C	P_4.3.4

1) Not subject to production test, specified by design.

2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and exposed pad are fixed to ambient temperature). T_A = 85°C. Total power dissipation = 1.5 W

3) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board. The product (chip+package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 70 µm Cu, 300 mm^2 cooling area. Total power dissipation 1.5W distributed statically and homogenously over all power stages

4) Specified R_{thJA} value is according to Jedec JESD51-5,-7 at natural convection on FR4 2s2p board; The product (chip+package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Total power dissipation 1.5W distributed statically and homogenously over all power stages

4 Internal supply

This chapter describes the internal supply in its main parameters and functionality.

4.1 Description

The internal supply principle is highlighted in the concept diagram of **Figure 3**.

If the voltage applied at the EN pin is below $V_{EN(th)}$ the device enters sleep mode. In this state all internal functions are switched off and the current consumption is reduced to $I_{S(sleep)}$.

As soon as the voltage applied at the supply pin V_S is above $V_{SUV(ON)}$ and the voltage applied at the EN pin is above $V_{EN(th)}$, after the power-on reset time t_{POR}, the device is ready to deliver output current from the output stage. The power on reset time t_{POR} has to be taken into account also in relevant application conditions, i. e. with PWM control from *VS* or EN lines.

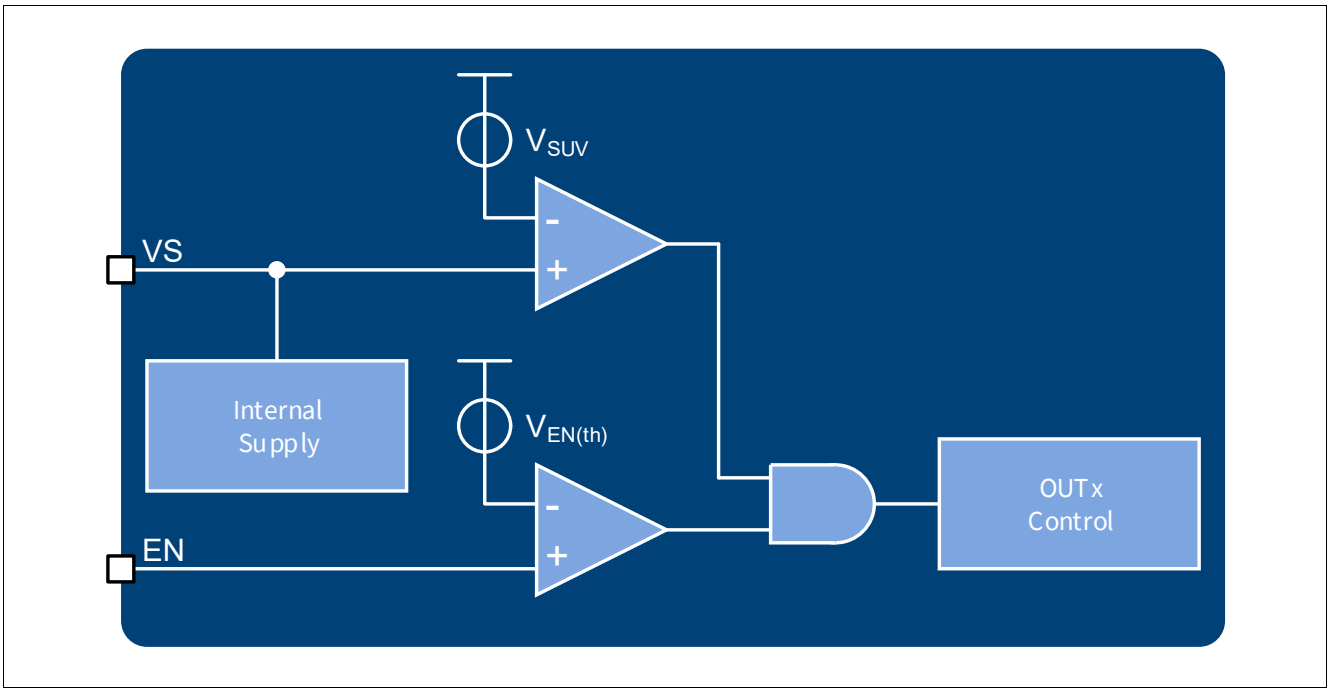


Figure 3 Internal supply

Furthermore, as soon as the voltage applied at the supply pin *VS* is above $V_{SUV(ON)}$ and the voltage applied to the EN pin V_{EN} is above $V_{EN(th)}$, the device is ready to detect and report overtemperature condition via ERRN (error network pin) as described in **Chapter 6**.

To program output enable via EN pin there are several possibilities, like a resistor divider from VS to GND, a Zener diode from EN to VS and also a logic control pin (e.g. from a microcontroller output).

4.2 Electrical characteristics internal supply and EN pin

Table 5 Electrical characteristics: Internal supply and EN pin

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption, sleep mode	$I_{S(sleep)}$	–	0.1	2	µA	1) V_{EN} = 0 V T_J < 85°C V_S = 18 V V_{OUT} = 3.6 V	P_5.2.1
Current consumption, active mode (no fault)	$I_{S(active)}$	–	1.5	3	mA	V_{EN} = 5.5 V I_{IN_SET} = 0 µA T_J < 105°C V_S = 18 V V_{OUT} = 3.6 V	P_5.2.3
Current consumption during fault condition triggered from another device sharing ERRN bus	$I_{S(fault, ERRN)}$	–	–	850	µA	V_{EN} = 5.5 V T_J < 105°C V_S = 18 V V_{ERRN} = 0 V V_{OUT} = 3.6 V	P_5.2.4
Supply thresholds							
Required supply voltage for output activation	$V_{SUV(ON)}$	–	–	5.5	V	V_{EN} = V_S V_{OUT} = 3 V R_{IN_SET} = 6.8 kΩ I_{OUT} > 50% $I_{OUT(nom)}$	P_5.2.5
Required supply voltage for output deactivation	$V_{SUV(OFF)}$	4.5	–	–	V	V_{EN} = V_S V_{OUT} = 3 V R_{IN_SET} = 6.8 kΩ I_{OUT} < 50% $I_{OUT(nom)}$	P_5.2.6
Supply voltage activation hysteresis: $V_{SUV(ON)}$ - $V_{SUV(OFF)}$	$V_{SUV(hys)}$	–	200	–	mV	1) V_{EN} > $V_{EN(th)}$	P_5.2.8
EN output enable threshold	$V_{EN(th)}$	1.4	1.65	1.8	V	V_S = 5.5 V V_{PS} = 2 V R_{IN_SET} = 6.8 kΩ I_{OUT} = 50% $I_{OUT(nom)}$	P_5.2.9
EN pull-down current	$I_{EN(PD)}$	–	–	60	µA	1) V_S > 8 V V_{EN} = 2.8 V	P_5.2.17
EN pull-down current	$I_{EN(PD)}$	–	–	110	µA	1) V_S > 8 V V_{EN} = 5.5 V	P_5.2.14
EN pull-down current	$I_{EN(PD)}$	–	–	350	µA	1) V_S > 8 V V_{EN} = V_S	P_5.2.15

Table 5 Electrical characteristics: Internal supply and EN pin (cont'd)

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Timing							
Power on reset delay time	t_{POR}	–	–	25	µs	[1] V_S rising from 0 V to 13.5 V V_{OUT} = 3.6 V R_{IN_SET} = 6.8 kΩ I_{OUT} = 80% $I_{OUT(nom)}$	P_5.2.13

1) Not subjected to production test: specified by design.

5 Power stage

The output stage is realized as high-side current source with an output current up to 360mA. During off state the leakage current at the output stage is minimized in order to prevent a slightly glowing LED.
The maximum output current is limited by the power dissipation and used PCB cooling areas.
For an operating output current control loop, the supply and output voltage have to be considered according to the following parameters:

- Required supply voltage for current control $V_{S(CC)}$
- Voltage drop over through the output stage during current control $V_{PS(CC)}$
- Required output voltage for current control $V_{OUT(CC)}$

5.1 Programmable output current accuracy

In many rear light functions, a significant cost reduction is achieved increasing the number of LEDs per OUT (typically in series of three): this system implementation implies the need for low output voltage drop at low battery operative range, together with very high output current accuracy. As high output current accuracy needs an internal shunt voltage drop measurement in series to the output stage (the highest drop on the internal implies the highest accuracy), these two system requirements often result in a trade-off where, within a certain maximum output voltage drop, only a reduced range of output current can achieve the desired accuracy.

To provide high accuracy at low output currents and low output voltage drop ($V_{PSH/L}$) at high currents, the TLD1114-1EP offers the capability to select alternative output accuracy settings via the CFG output configuration pin. In this way, choosing the proper connection of the output load between OUTH and OUTL, the highest current accuracy with low drop $V_{PSH/L}$ can be achieved. When CFG is connected to GND, the device provides low V_{PSH} drop and high accuracy for the highest current ranges, provided that OUTH pin is used as output. When CFG pin is left open and the load is connected to OUTL pin, the highest current accuracy is also provided in the lowest current range.

Table 6 shows the configuration options to achieve the best system targets. Further implementation details are shown in **Chapter 7**.

Table 6 Output current accuracy configuration overview[1)]

CFG	OUTL	OUTH	Output current accuracy	Output voltage drop
Connected to GND	Open	Connected to load	4% or better for 160 mA < $I_{OUTH(typ)}$ < 360 mA[2)]	V_{PSH} < 650 mV for 360 mA > I_{OUTH} > 88% $I_{OUTH(typ)}$[3)]
Open	Connected to load	Open	4% or better for 30 mA < $I_{OUTL(typ)}$ < 180 mA[2)]	V_{PSL} < 650 mV for 180 mA > I_{OUTL} > 88% $I_{OUTL(typ)}$[3)]

1) The table shows the recommended application configuration. For detailed test conditions refer to electrical characteristics (**Table 7**)
2) T_J = 25°C, refer to parameters P_6.5.3 and P_6.5.8.
3) T_J = -40°C, refer to parameters P_6.5.49 and P_6.5.50.

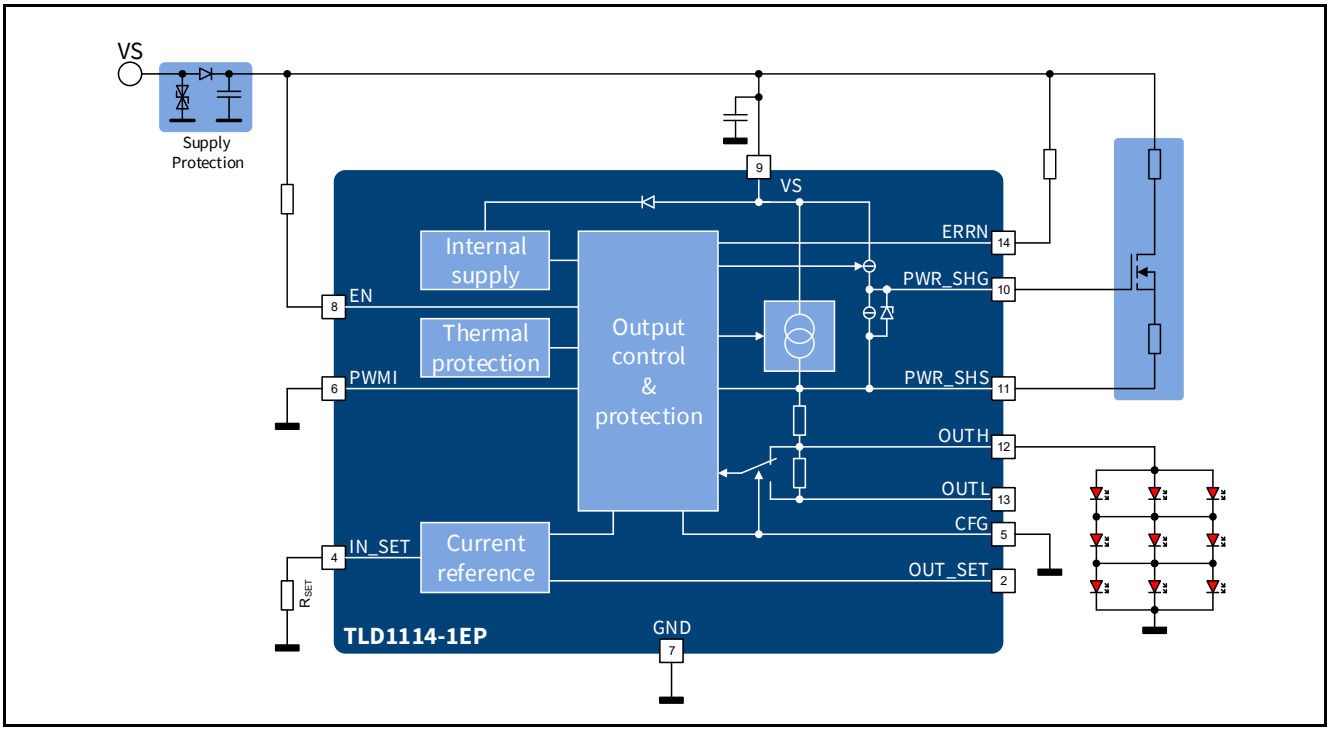


Figure 4 Configuration example with low V_{PS} drop at high current accuracy (CFG connected to GND)

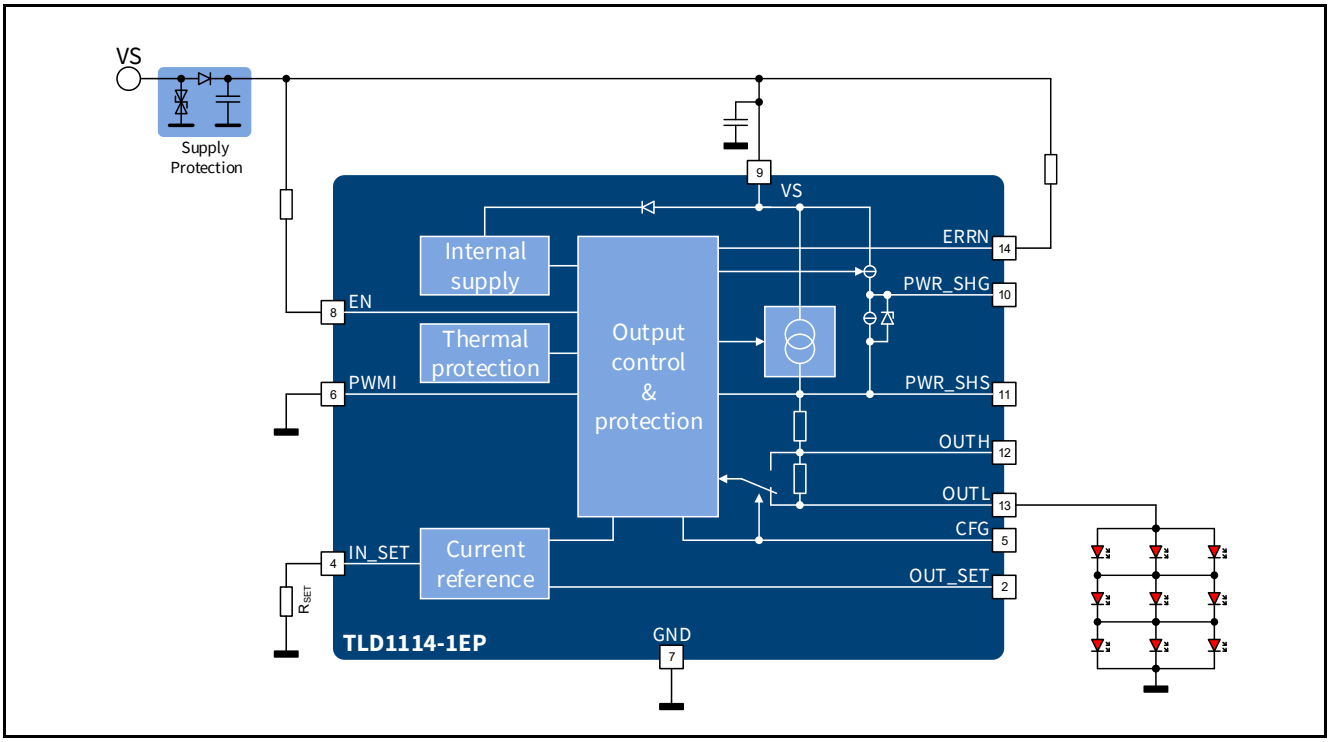


Figure 5 Configuration example with high accuracy at low current range (CFG open)

5.2 Power shift feature

Furthermore, the device provides the possibility of managing high power dissipation (higher than allowed by the thermal impedance R_{thJA} of the application) by controlling the current flow on a few external, low cost, discrete components.

5.2.1 Power shift via external MOSFET control and power resistors

The control of power dissipation can be done via usage of PWR_SHG and PWR_SHS control pins: when V_{PS} output voltage drop exceeds the activation voltage threshold of an external switch, the voltage between PWR_SHG and PWR_SHS allows to turn it on (usually a low power external NMOS) and, in conjunction with the usage of limiting power resistors, routes most of the configured output current (in a percentage depending on external components values) outside the TLD1114-1EP. **Figure 6** shows an embodiment example of the power shift feature.

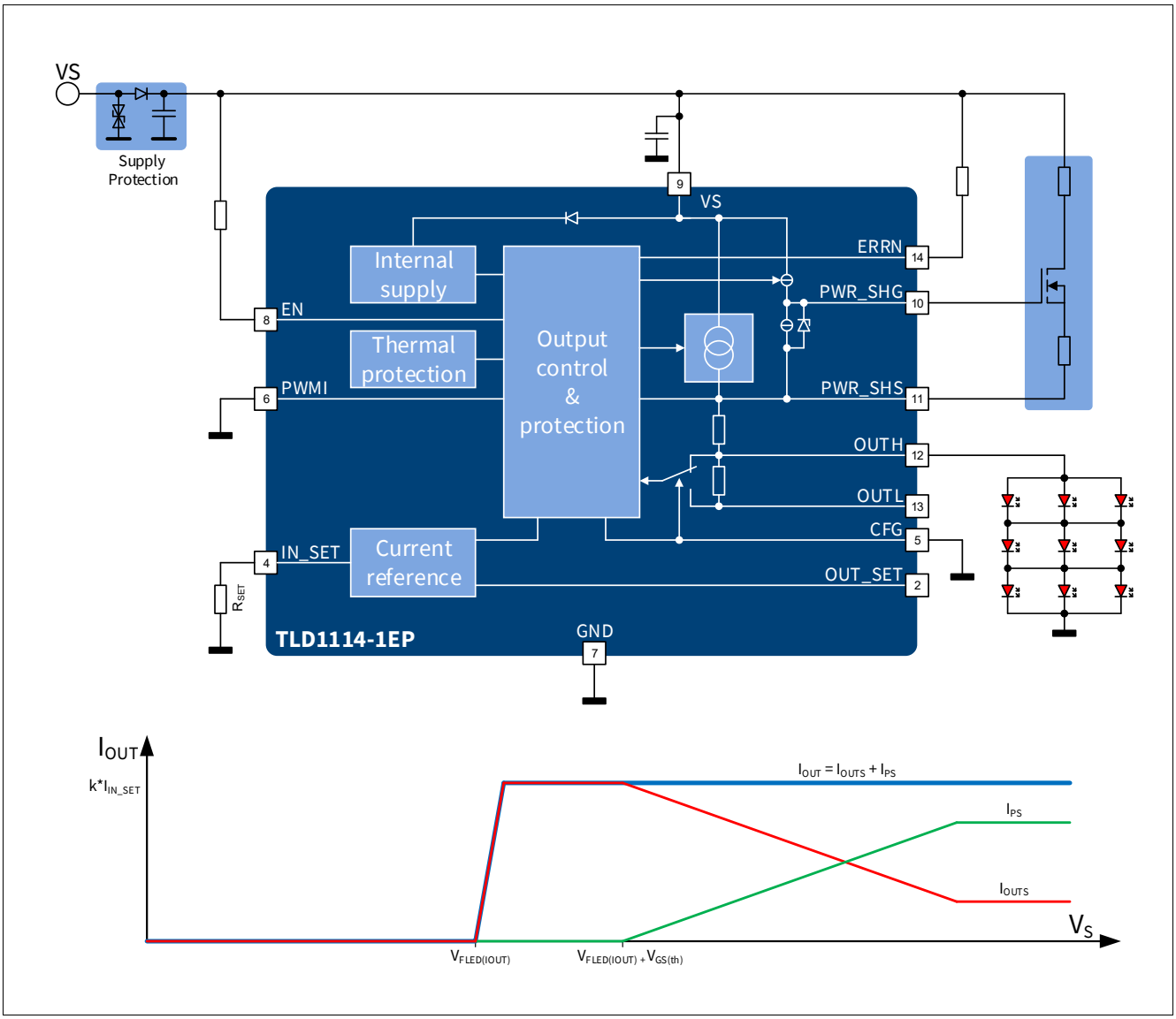


Figure 6 External MOSFET control concept

5.2.2 Power shift components calculation

Referring to the diagram example of **Figure 6**, in order to properly dimension the resistors values, the following parameters have to be considered:

- Minimum current $I_{OUT(int,\,min)}$ intended to flow through the TLD1114-1EP output stage at maximum operative supply voltage $V_{S(OP,max)}$
- Maximum current from power shift path $I_{OUT(int,\,max)}$ (e.g. through external NMOS and dissipation resistors) at maximum overvoltage battery stress $V_{S(OV,max)}$ in the application

- External NMOS voltage threshold V_{GS}
- Forward voltage $V_{F(LED)}$ of the output LED load and forward voltage $V_{F(D)}$ of the reverse polarity diode D (when used).

For a safe drive of the external NMOS switch, when the OUT voltage drop V_{PS} reaches a voltage greater than $V_{GS(CL)}$, the PWR_SHG voltage is automatically limited (see P_6.6.16).

5.3 Protection

The device provides embedded protective functions, which are designed to prevent IC damage under fault conditions described in this datasheet. Fault conditions are considered as “outside” normal operating range. Protective functions are not designed for continuous nor for repetitive operations.

5.3.1 Thermal protection

A thermal protection circuitry is integrated in the device. It is realized by a temperature monitoring of the output stages.

As soon as the junction temperature exceeds the overtemperature threshold T_{JSD} the output current is disabled and the IN_SET pin goes in a weak pull-down state with a current consumption $I_{IN\_SET(fault)}$. If the junction temperature cools down below T_{JSD} - $T_{J(hys)}$, the IN_SET pin rise again to $V_{IN\_SET(ref)}$ (within an additional time $t_{IN\_SET(del)}$) and consequently, the output current rise again (see **Chapter 6** for a detailed description of fault management).

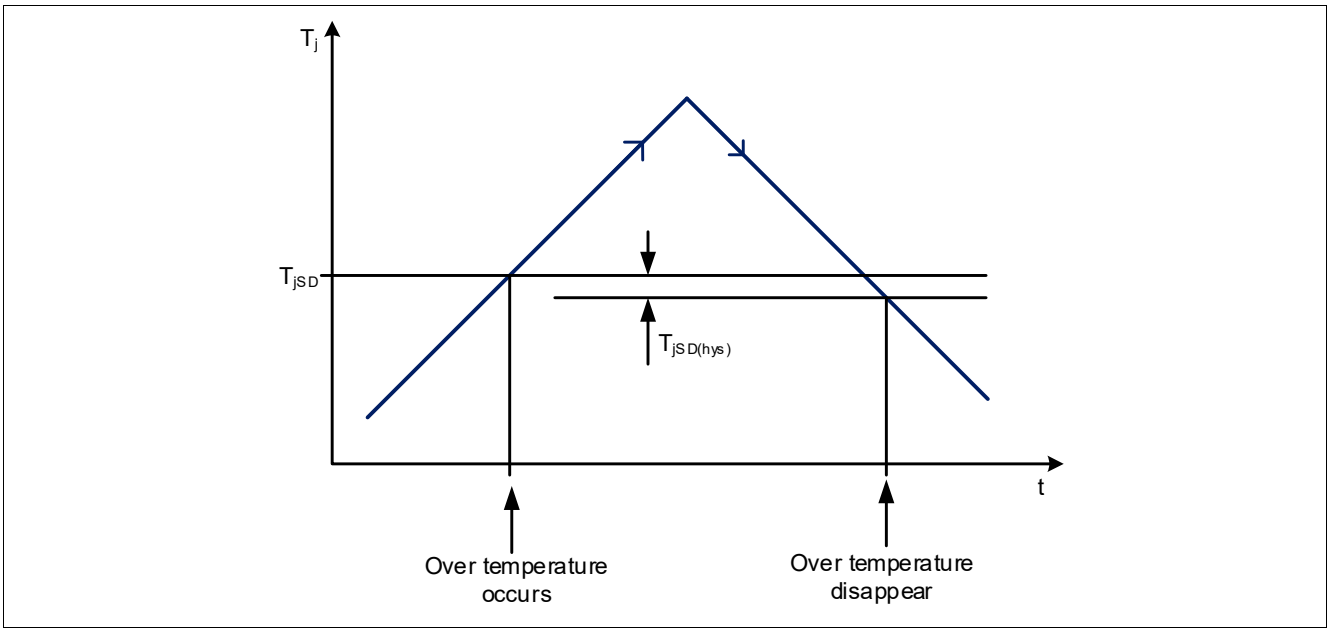


Figure 7 Overtemperature shut down auto-restart thresholds

As long as the device remains into overtemperature condition, ERRN pin remains low.

5.3.2 Reverse battery protection

The device has an integrated reverse battery protection feature. This feature protects the driver IC itself and, potentially, also connected LEDs. The output reverse current is limited to $I_{OUT(REV)}$ by the reverse battery protection.

5.4 Output configuration via IN_SET, OUT_SET and PWMI pins

Outputs current can be defined via IN_SET and OUT_SET (to drive additional devices without further external components) pin.

5.4.1 IN_SET pin

The IN_SET pin is a multiple function pin for the output current definition and input control.

Output current definition and analog dimming control can be done defining accordingly the IN_SET current.

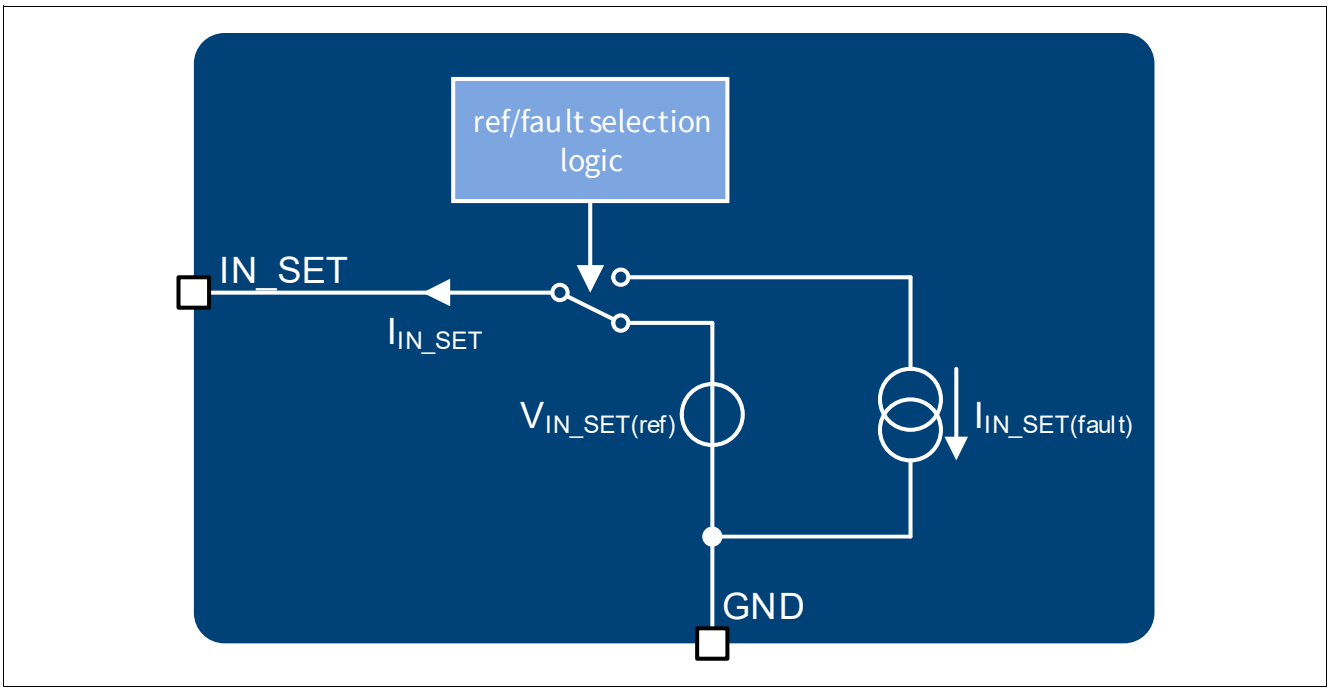


Figure 8 IN_SET pin block diagram

5.4.2 Output current adjustment via R_{SET}

The output current for the channel can be defined connecting a low power resistor (R_{SET}) between the IN_SET pin and GND. The dimensioning of the resistor can be done using the formula:

$$I_{OUT} = k \cdot I_{IN\_SET} = k \cdot V_{IN\_SET(ref)} / R_{SET} \tag{5.1}$$

The gain factor k (defined as the ratio I_{OUT}/I_{IN_SET}) is graphically described in **Figure 9**.

The current through the R_{SET} is defined by the resistor itself and the reference voltage $V_{IN\_SET(ref)}$, which is applied to the IN_SET pin when the device is supplied and the channel enabled.

5.4.3 Output control via IN_SET

The IN_SET pin can be connected via R_{SET} to the open-drain output of a microcontroller or to an external NMOS transistor as described in **Figure 11**. This signal can be used to turn off the relative output stages of the IC.

A minimum IN_SET current of $I_{IN\_SET(ACT)}$ is required to turn on the output stages. This feature is implemented to prevent glowing of LEDs caused by leakage currents on the IN_SET pin, see again **Figure 9** for details.

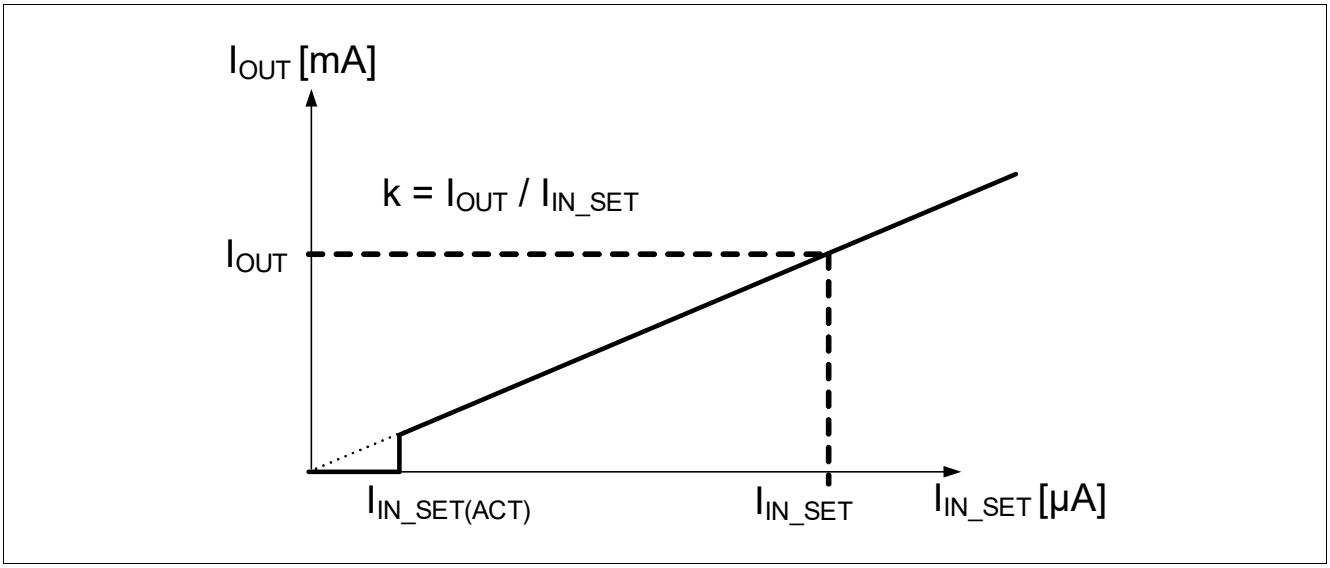


Figure 9 I_{OUT} **vs** I_{IN_SET}

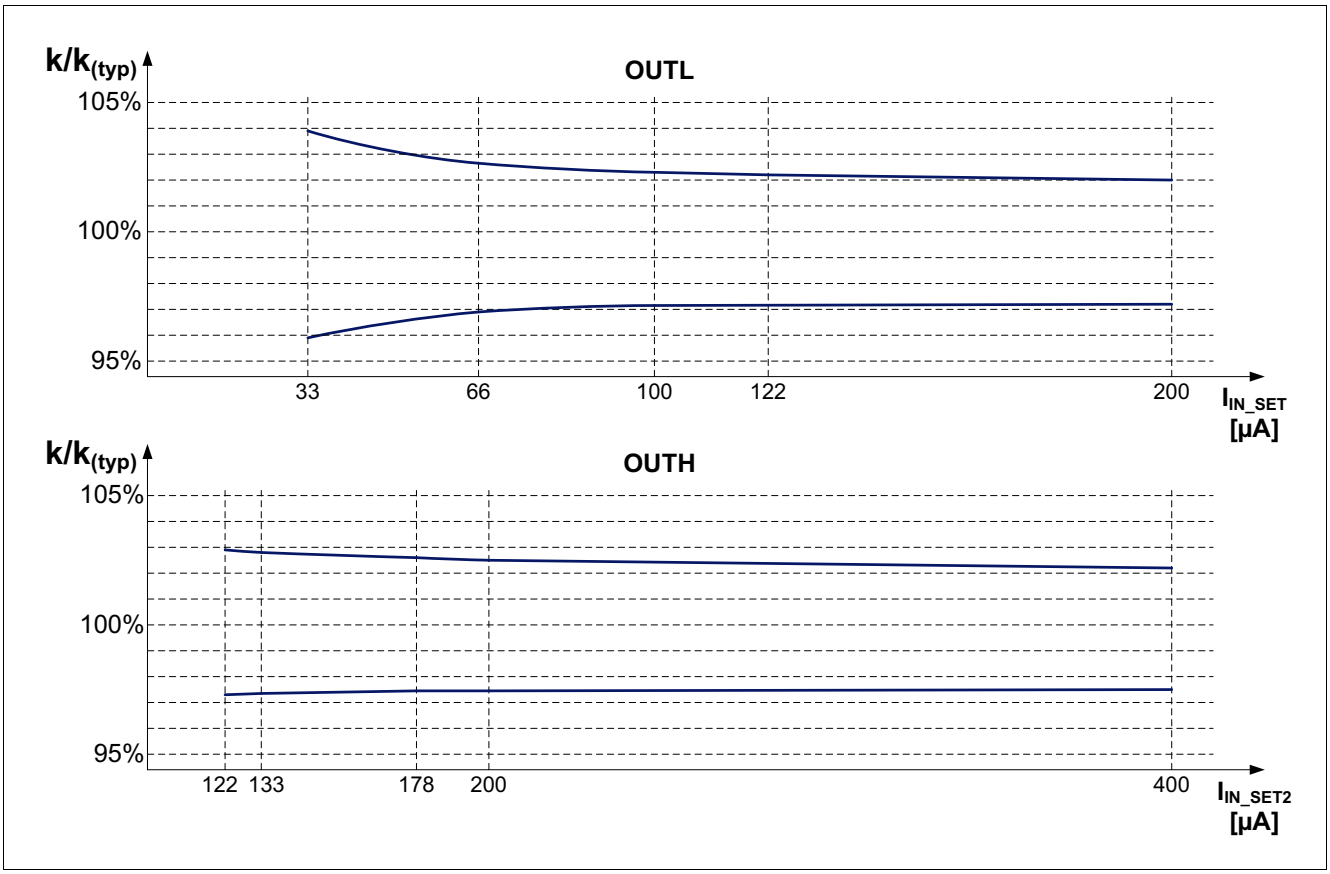


Figure 10 **Typical output current accuracy** I_{OUT} / I_{IN_SET} **at** T_J **= 25°C**

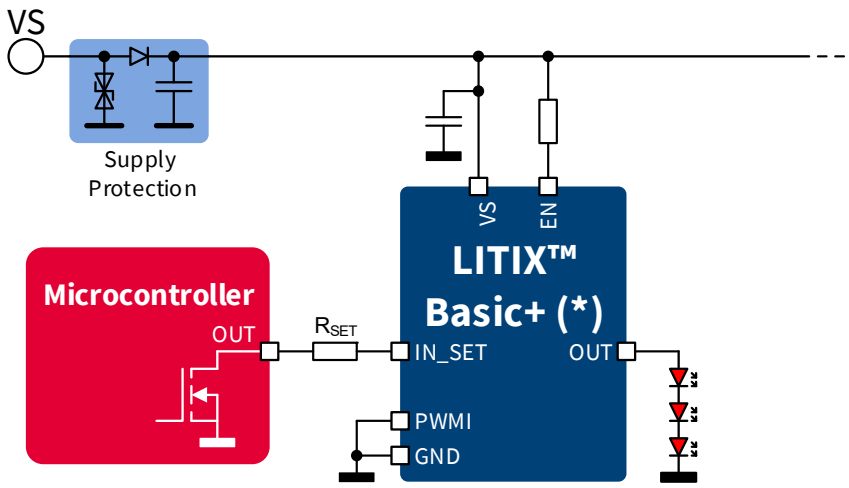


Figure 11 Output control via IN_SET pin and open-drain microcontroller out (simplified diagram)

5.4.4 IN_SET pin behavior during device overload management

If a fault condition arises on the channel controlled by the IN_SET pin, the IN_SET pin is reduced to $I_{IN\_SET(fault)}$, in order to minimise the current consumption of the whole device under fault condition.

5.4.5 OUT_SET pin

The OUT_SET pin, mirroring the IN_SET current defined by the external resistor R_{SET}, can be used to define the IN_SET current of an additional companion device.

If minimum IN_SET activation current $I_{IN\_SET(act)}$ is not reached the OUT_SET current is reduced to $I_{OUT\_SET(OFF)}$. This allows to drive other devices via OUT_SET, even when digital dimming is required, without external components (see application drawing example in **Chapter 7**).

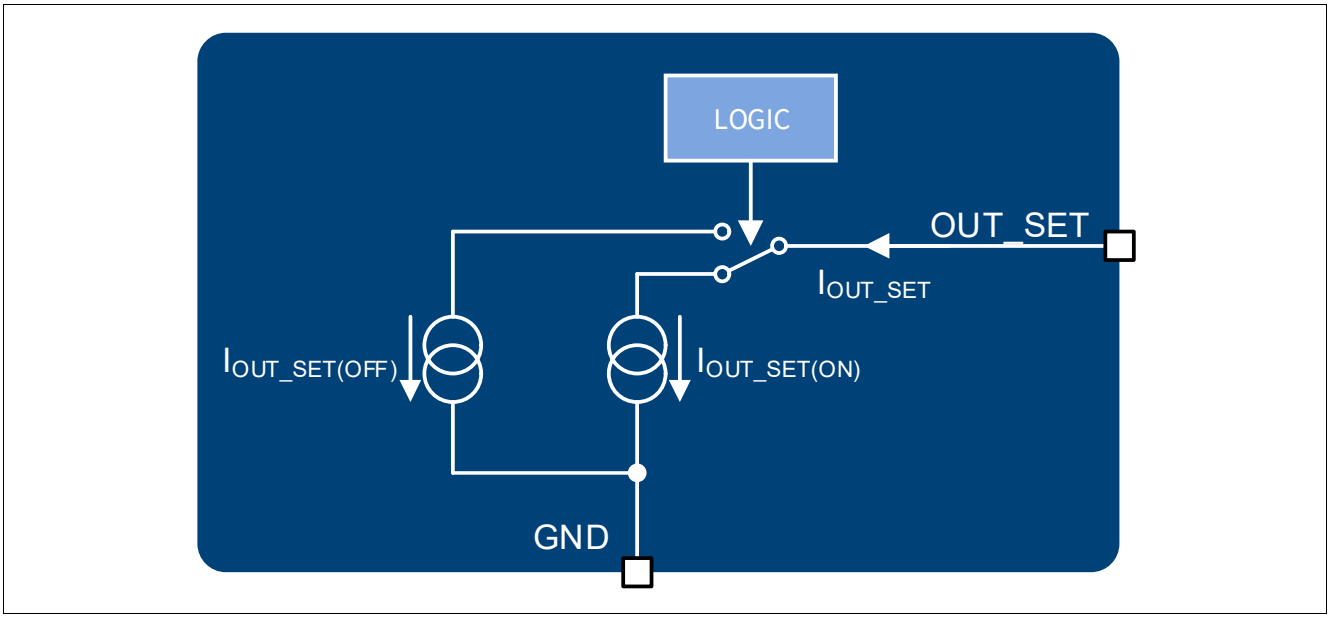


Figure 12 OUT_SET pin block diagram

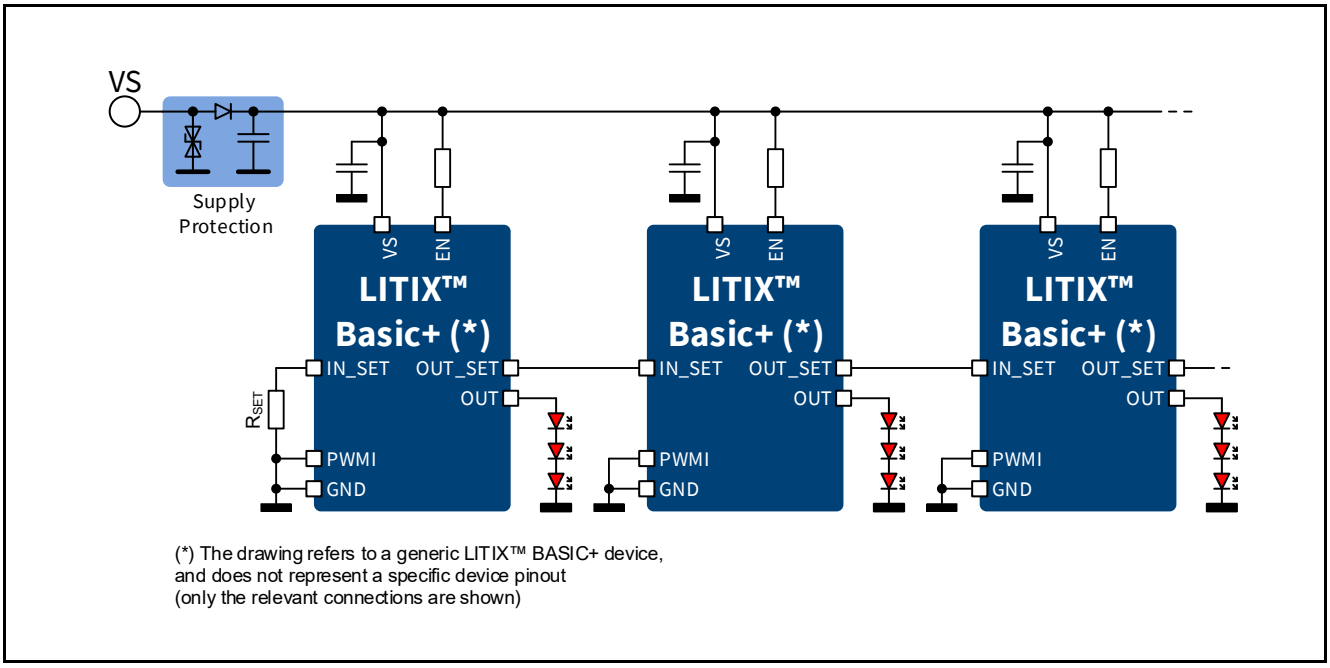


Figure 13 IN_SET to OUT_SET serial connection example

5.4.6 Direct control of PWMI

PWMI input can be controlled by the PWMO output of another device of LITIX™ Basic+ family or, alternatively, a push-pull output stage of a microcontroller: the host device decides the digital dimming characteristics by applying the proper control cycle in order to set the “on”/“off” timing, according to the chosen dimming function.

5.4.7 Timing diagrams

In the following diagram (**Figure 14**, **Figure 16**) the influences of inputs on output activation delays are shown.

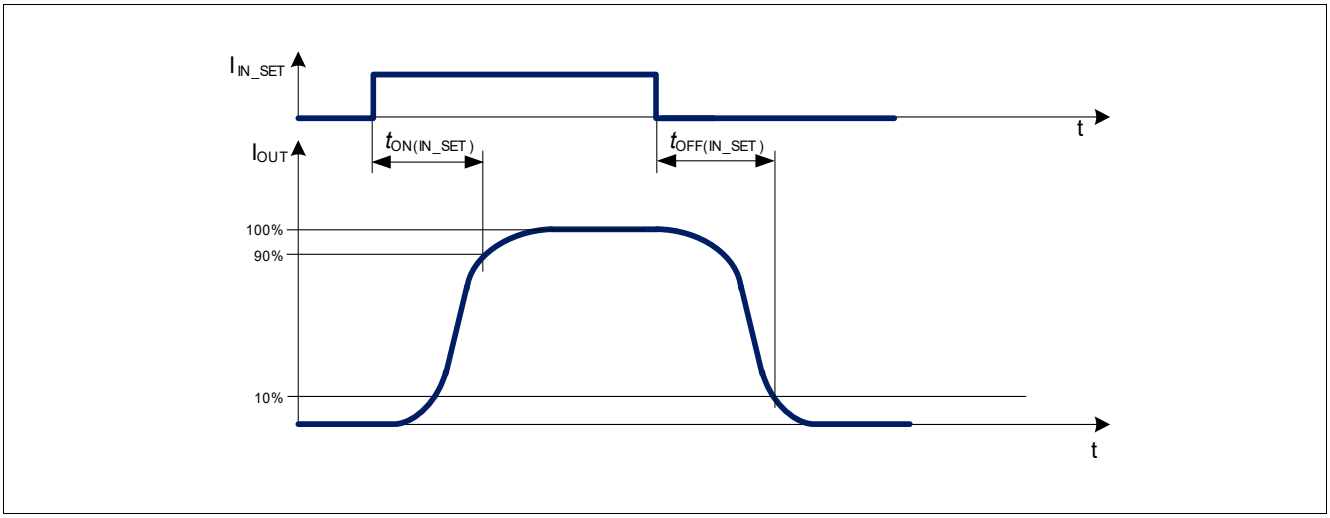


Figure 14 IN_SET turn on and turn off delay timing diagram

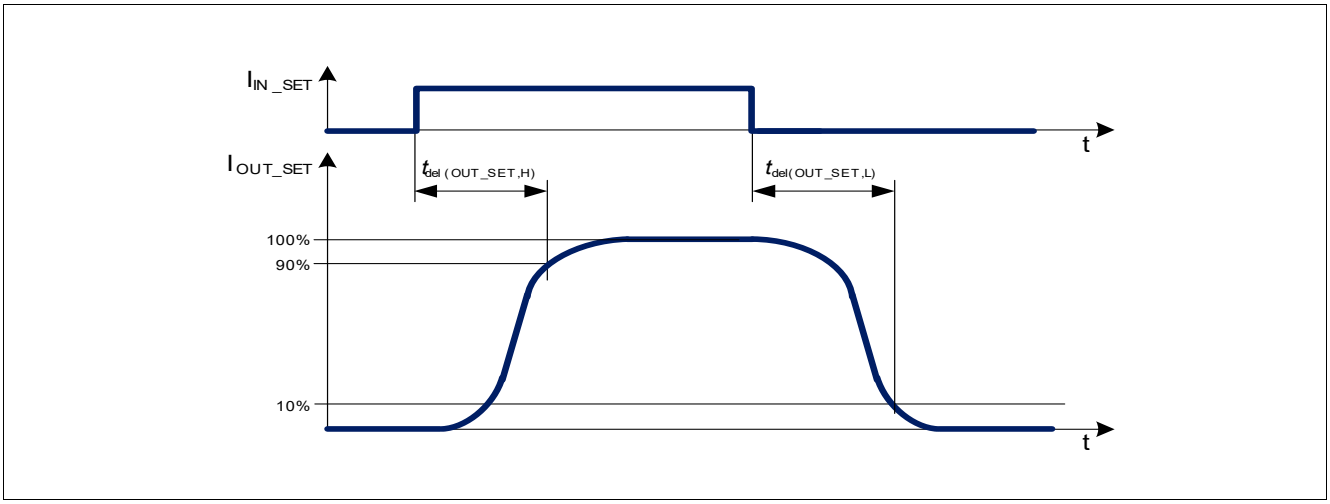


Figure 15 IN_SET to OUT_SET activation and deactivation delay timing diagram

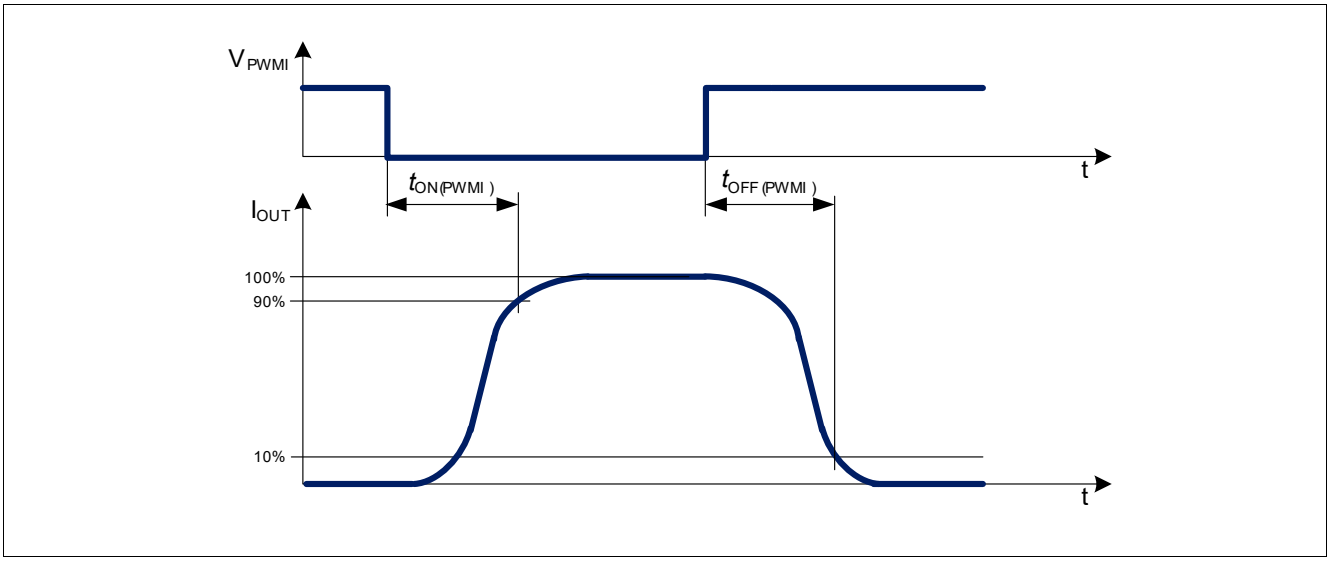


Figure 16 PWMI turn on and turn off timing diagram

5.5 Electrical characteristics power stage

Table 7 Electrical characteristics: Power stage and CGF pin

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output leakage current	$I_{OUT(leak)}$	–	–	9	µA	[1] V_{EN} = 5.5 V I_{IN_SET} = 0 µA V_{OUT} = 2.5 V T_J = 85°C	P_6.5.51
Output leakage current	$I_{OUT(leak)}$	–	–	21	µA	[1] V_{EN} = 5.5 V I_{IN_SET} = 0 µA V_{OUT} = 2.5 V T_J = 150°C	P_6.5.60
Reverse output current	$I_{OUT(rev)}$	–	–	3	µA	[1] V_{EN} = V_s V_S = -18 V Output load: LED with break down voltage < - 0.6 V	P_6.5.2
Output current accuracy							
Output current accuracy I_{OUTL}/I_{IN_SET}	K_{RT}	870	900	930	–	[1] T_J = 25°C V_S = 12.8 V V_{PSL} = 2 V CFG open OUTH open I_{IN_SET} = 66 µA	P_6.5.3
Output current accuracy I_{OUTL}/I_{IN_SET}	K_{LT}	846	900	954	–	[1] T_J = 25... 150°C V_S = 8... 18 V V_{PSL} = 2 V CFG open OUTH open I_{IN_SET} = 66 µA	P_6.5.4
Output current accuracy I_{OUTL}/I_{IN_SET}	K_{ALL}	837	900	963	–	[1] T_J = -40... 150°C V_S = 8... 18 V V_{PSL} = 2 V CFG open OUTH open I_{IN_SET} = 66 µA	P_6.5.5
Output current accuracy I_{OUTL}/I_{IN_SET}	K_{LT}	855	900	945	–	[1] T_J = 25... 150°C V_S = 8... 18 V V_{PSL} = 2 V CFG open OUTH open I_{IN_SET} = 100 ... 200 µA	P_6.5.6

Table 7 Electrical characteristics: Power stage and CGF pin (cont'd)

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output current accuracy I_{OUTL}/I_{IN_SET}	K_{ALL}	842	900	958	–	[1] T_J = -40... 150°C V_S = 8... 18 V V_{PSL} = 2 V CFG open OUTH open I_{IN_SET} = 100... 200 µA	P_6.5.7
Output current accuracy I_{OUTH}/I_{IN_SET}	K_{RT}	861	890	919	–	[1] T_J = 25°C V_S = 12.8 V V_{PSH} = 2 V V_{CFG} = 0 V OUTL open I_{IN_SET} = 133 µA	P_6.5.8
Output current accuracy I_{OUTH}/I_{IN_SET}	K_{LT}	837	890	943	–	[1] T_J = 25... 150°C V_S = 8... 18 V V_{PSH} = 2 V V_{CFG} = 0 V OUTL open I_{IN_SET} = 133 µA	P_6.5.9
Output current accuracy I_{OUTH}/I_{IN_SET}	K_{ALL}	828	890	952	–	[1] T_J = -40... 150°C V_S = 8... 18 V V_{PS} = 2 V V_{CFG} = 0 V OUTL open I_{IN_SET} = 133 µA	P_6.5.10
Output current accuracy I_{OUTH}/I_{IN_SET}	K_{LT}	855	890	925	–	[1] T_J = 25... 150°C V_S = 8... 18 V V_{PSH} = 2 V V_{CFG} = 0 V OUTL open I_{IN_SET} = 200... 400 µA	P_6.5.11
Output current accuracy I_{OUTH}/I_{IN_SET}	K_{ALL}	846	890	934	–	[1] T_J = -40... 150°C V_S = 8... 18 V V_{PSH} = 2 V V_{CFG} = 0 V OUTL open I_{IN_SET} = 200... 400 µA	P_6.5.12
Required voltage drop during current control $V_{PS(CC)} = V_S - V_{OUT}$	$V_{PS(CC)}$	1.0	–	–	V	[2] V_S = 8... 18 V I_{OUT} > 90% of $K_{(typ)} * I_{IN\_SET}$	P_6.5.36

Table 7 Electrical characteristics: Power stage and CGF pin (cont'd)

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Required voltage drop during high current control $V_{PSH(CC)} = V_S - V_{OUTH}$	$V_{PSH(CC)}$	0.65	–	–	V	V_S = 8... 18 V V_{CFG} = 0 V OUTL open I_{IN_SET} = 400 µA I_{OUTH} > 90% of $K_{(typ)}$*I_{IN_SET} T_J = -40°C	P_6.5.49
Required voltage drop during high current control $V_{PSH(CC)} = V_S - V_{OUTH}$	$V_{PSH(CC)}$	0.75	–	–	V	V_S = 8... 18 V V_{CFG} = 0 V OUTL open I_{IN_SET} = 400 µA I_{OUTH} > 90% of $K_{(typ)}$*I_{IN_SET} T_J = 25°C	P_6.5.61
Required voltage drop during high current control $V_{PSH(CC)} = V_S - V_{OUTH}$	$V_{PSH(CC)}$	0.85	–	–	V	V_S = 8... 18 V V_{CFG} = 0 V OUTL open I_{IN_SET} = 400 µA I_{OUTH} > 90% of $K_{(typ)}$*I_{IN_SET} T_J = 150°C	P_6.5.62
Required voltage drop during low current control $V_{PSL(CC)} = V_S - V_{OUTL}$	$V_{PSL(CC)}$	0.65	–	–	V	V_S = 8... 18 V CFG open OUTH open I_{IN_SET} = 200 µA I_{OUTL} > 90% of $K_{(typ)}$*I_{IN_SET} T_J = -40°C	P_6.5.50
Required voltage drop during low current control $V_{PSL(CC)} = V_S - V_{OUTL}$	$V_{PSL(CC)}$	0.75	–	–	V	V_S = 8... 18 V CFG open OUTH open I_{IN_SET} = 200 µA I_{OUTL} > 90% of $K_{(typ)}$*I_{IN_SET} T_J = 25°C	P_6.5.63
Required voltage drop during low current control $V_{PSL(CC)} = V_S - V_{OUTL}$	$V_{PSL(CC)}$	0.85	–	–	V	V_S = 8... 18 V CFG open OUTH open I_{IN_SET} = 200 µA I_{OUTL} > 90% of $K_{(typ)}$*I_{IN_SET} T_J = 150°C	P_6.5.64

Table 7 Electrical characteristics: Power stage and CGF pin (cont'd)

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Required supply voltage for current control	$V_{S(CC)}$	5.5	–	–	V	V_{EN} = 5.5 V V_{OUT} = 3 V R_{IN_SET} = 6.8 kΩ I_{OUT} > 90% of $K^*I_{IN\_SET}$	P_6.5.40
Required output voltage for current control	$V_{OUT(CC)}$	1.4	–	–	V	V_S = 8... 18 V I_{OUT} > 90% of $K^*I_{IN\_SET}$	P_6.5.41
CFG required voltage for low drop at high current	$V_{CFG(L)}$	–	–	1.35	V	V_S = 8 V to 18 V V_{EN} = 5.5 V	P_6.5.46
CFG required voltage for high accuracy at low output current range	$V_{CFG(H)}$	2	–	–	V	V_S = 8 V to 18 V V_{EN} = 5.5 V	P_6.5.47
CFG pull-up current	$I_{CFG(PU)}$	20	35	50	µA	V_S = 8 V to 18 V V_{EN} = 5.5 V	P_6.5.48
Overtemperature shutdown threshold	T_{JSD}	150	175	190	°C	1)	P_6.5.42
Overtemperature hysteresis	$T_{J(hys)}$	–	10	–	°C	1)	P_6.5.43

1) Not subjected to production test: specified by design.

2) In these test conditions, the parameter $K_{(typ)}$ represents the typical value of output current accuracy.

5.6 Electrical characteristics IN_SET, OUT_SET, PWR_SHS, PWM_SHG and PWMI pins for output settings

Table 8 Electrical characteristics: IN_SET, OUT_SET, PWR_SHS, PWM_SHG and PWMI pins

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IN_SET reference voltage	$V_{IN\_SET(ref)}$	1.195	1.22	1.245	V	[1] V_{EN} = 5.5 V T_J = 25°C	P_6.6.1
IN_SET reference voltage	$V_{IN\_SET(ref)}$	1.184	1.22	1.256	V	[1] V_{EN} = 5.5 V	P_6.6.17
IN_SET output activation current	$I_{IN\_SET(ACT)}$	–	–	15	µA	V_{EN} = 5.5 V V_{PS} = 3 V I_{OUT} > 50% of $K_{(typ)}$*I_{IN_SET}	P_6.6.2
OUT_SET output current matching	$\Delta I_{OUT\_SET(ON)}/I_{IN\_SET}$	-4	–	4	%	V_S = 8 V to 18 V V_{OUT_SET} = 1.2V I_{IN_SET} = 267 µA	P_6.6.3
PWR_SHG pull up current	$I_{PWR\_SHG(PU)}$	100	180	260	µA	V_S = 8 V to 18 V V_{EN} = 5.5 V V_{PWMI} = 1.5 V V_{PS} = 3 V V_{PWR_SHG} - V_{PWR_SHS} = 2 V	P_6.6.14
PWR_SHG pull-down current	$I_{PWR\_SHG(PD)}$	1.5	2.1	3	mA	V_S = 8 V to 18 V V_{EN} = 5.5 V V_{PWMI} = 3 V V_{PS} = 3 V V_{PWR_SHG} - V_{PWR_SHS} = 0.8 V	P_6.6.15
PWR_SHG clamping voltage V_{PWR_SHG} - V_{PWR_SHS}	$V_{GS(PWR\_SH)}$	4.5	–	6	V	V_S = 12 V to 18 V V_{EN} = 5.5 V $V_{PSL/H}$ > 7 V	P_6.6.16
PWMI low threshold	$V_{PWMI(L)}$	1.5	1.7	2	V	V_S = 8 V to 18 V V_{EN} = 5.5 V	P_6.6.6
PWMI high threshold	$V_{PWMI(H)}$	2.5	2.7	3	V	V_S = 8 V to 18 V V_{EN} = 5.5 V	P_6.6.7
Timing							
IN_SET turn on time	$t_{ON(IN\_SET)}$	–	–	20	µs	[1][2] V_S = 13.5 V V_{PS} = 4 V I_{IN_SET} rising from 0 to 180 µA I_{OUT} = 90% of K*I_{IN_SET}	P_6.6.8

Table 8 Electrical characteristics: IN_SET, OUT_SET, PWR_SHS, PWM_SHG and PWMI pins (cont'd)

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IN_SET turn off time	$t_{OFF(IN\_SET)}$	–	–	10	µs	[1)2)] V_S = 13.5 V V_{PS} = 4 V I_{IN_SET} falling from 180 to 0 µA I_{OUT} = 10% of $K^*I_{IN\_SET}$	P_6.6.9
OUT_SET activation time	$t_{del(OUT\_SET,H)}$	–	–	5	µs	[1)3)] V_S = 13.5 V I_{IN_SET} rising from 0 to 180 µA I_{OUT_SET} = 90% of I_{IN_SET}	P_6.6.10
OUT_SET deactivation time	$t_{del(OUT\_SET,L)}$	–	–	5	µs	[1)3)] V_S = 13.5 V I_{IN_SET} falling from 180 to 0 µA I_{OUT_SET} = 10% of I_{IN_SET}	P_6.6.11
PWMI turn on time	$t_{ON(PWMI)}$	–	–	15	µs	[1)4)] V_S = 8 V to 18 V V_{EN} = 5.5 V V_{PWMI} falling from 5 V to 0 V I_{OUT} = 90% of $K^*I_{IN\_SET}$	P_6.6.12
PWMI turn off time	$t_{OFF(PWMI)}$	–	–	10	µs	[1)4)] V_S = 8 V to 18 V V_{EN} = 5.5 V V_{PWMI} = 0 rising from 0 V to 5 V I_{OUT} = 10% of $K^*I_{IN\_SET}$	P_6.6.13

1) Not subjected to production test: specified by design.
2) Refer to **Figure 14**.
3) Refer to **Figure 15**.
4) Refer to **Figure 16**.

6 Overload diagnosis

6.1 Error management via ERRN

6.1.1 ERRN pin

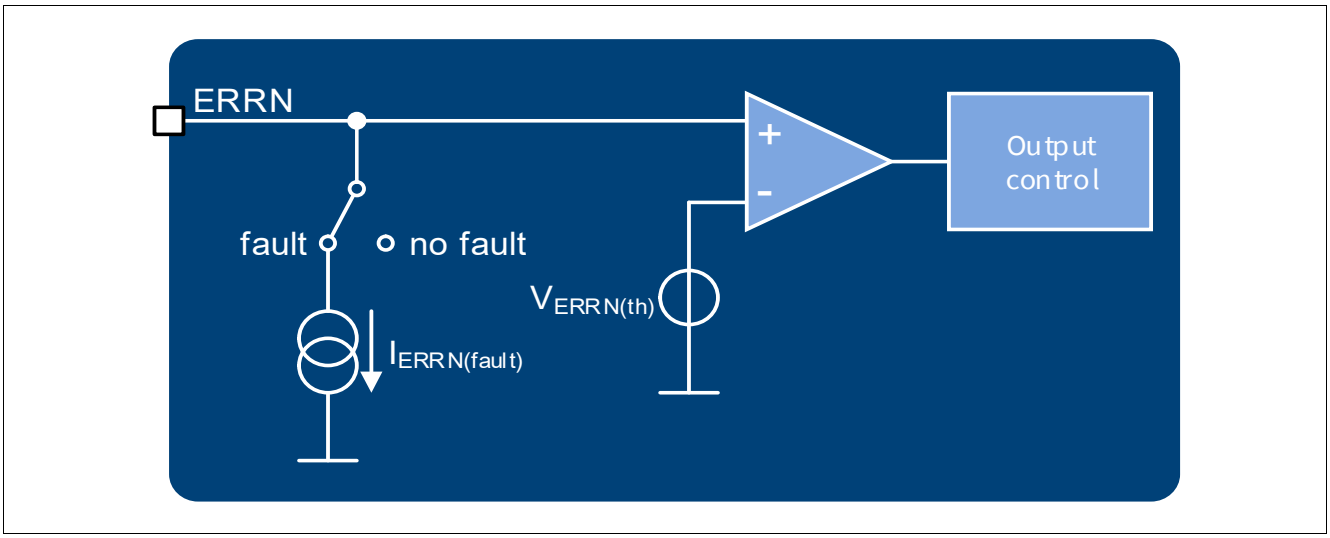


Figure 17 ERRN pin (block diagram)

The device is able to report an overtemperature failure in its driven load and react to a fault detected by another LED driver in the system if a shared error network is implemented (i. e. driving LED chains of the same light function). This is possible with the usage of an external pull-up resistor, allowing multiple devices to share the open drain diagnosis output pin ERRN. All devices sharing the common error network are capable to detect the fault from any of the channels driven by the LITIX™ Basic+ LED drivers and, if desired, to switch multiple loads off.

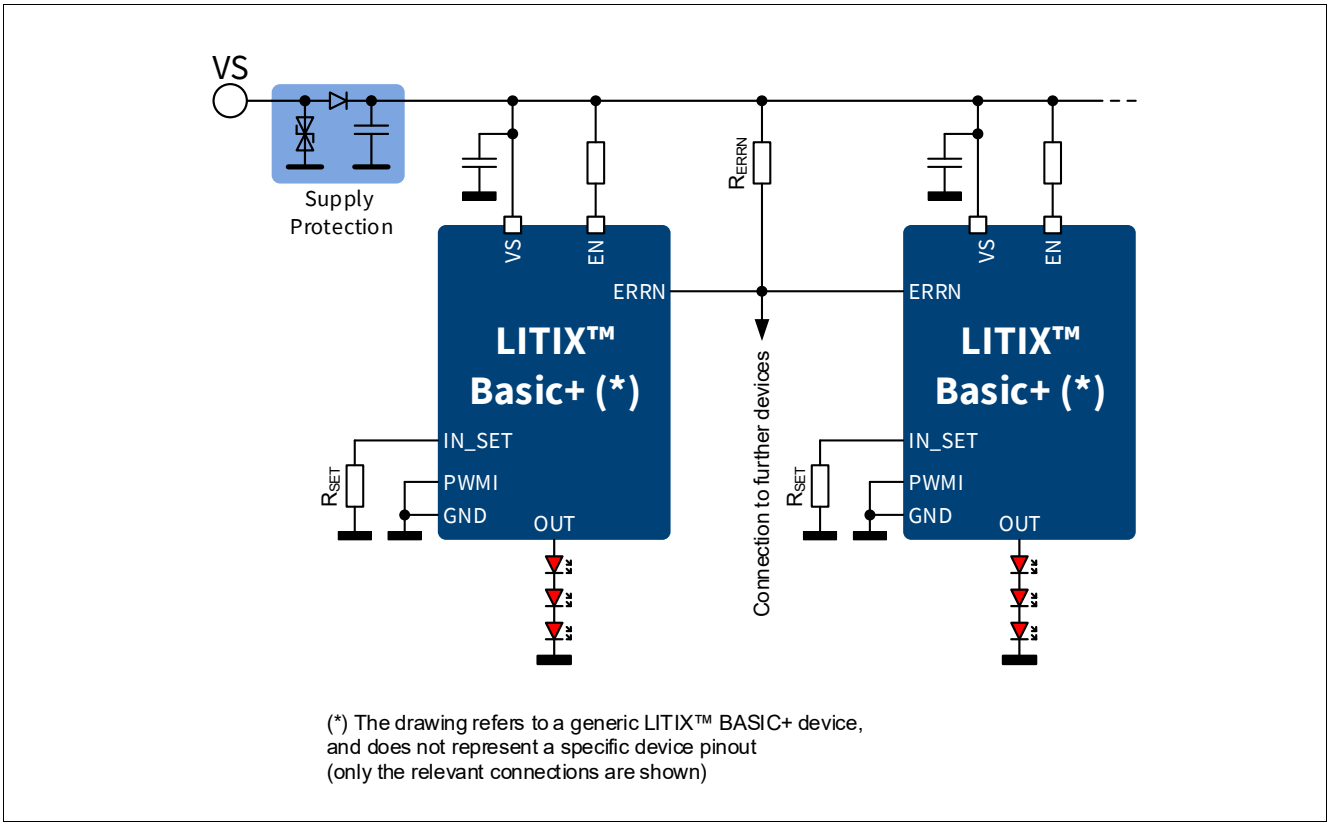


Figure 18 Shared error network principle between LITIX™ Basic+ family devices

When the channel is detected to be under fault conditions (for, at least, a filter time t_{fault}), the open-drain ERRN pin sinks a pull-down current $I_{ERRN(fault)}$ toward GND. Therefore an active low state can be detected at ERRN pin when $V_{ERRN} < V_{ERRN(fault)}$ and if this condition is reached, the channel is switched off. Similarly, when the fault is removed, ERRN pin is put back in high impedance state, and the channels reactivation procedure can be completed as illustrated in the timing diagrams in this chapter.

6.2 Fault management

Under overtemperature condition the ERRN pin starts sinking a current, $I_{ERRN(PD)}$ to ground and the voltage level on this pin will drop below $V_{ERRN(fault)}$ if the external pull-up resistor is properly dimensioned. The ERRN low voltage can also be used as input signal for a µC to perform the desired diagnosis policy. The IN_SET pin goes in a weak pull-down state with a current consumption $I_{N\_SET(fault)}$ after an additional latency time $t_{IN\_SET(del)}$.

The fault status is not latched: as soon as the overtemperature condition is no longer present (at least for a filter time t_{fault}), ERRN goes back to high impedance and, when its voltage is above $V_{ERRN(fault)}$, the IN_SET voltage goes up to $V_{SET(ref)}$, again after a time $t_{IN\_SET(del)}$. Finally the output stage will be activated again after a time $t_{ERR(reset)}$, which takes into account also the additional latency which depends on the external ERRN circuitry.

An example of error diagnosis conditions is shown in the timing diagram of **Figure 19**.

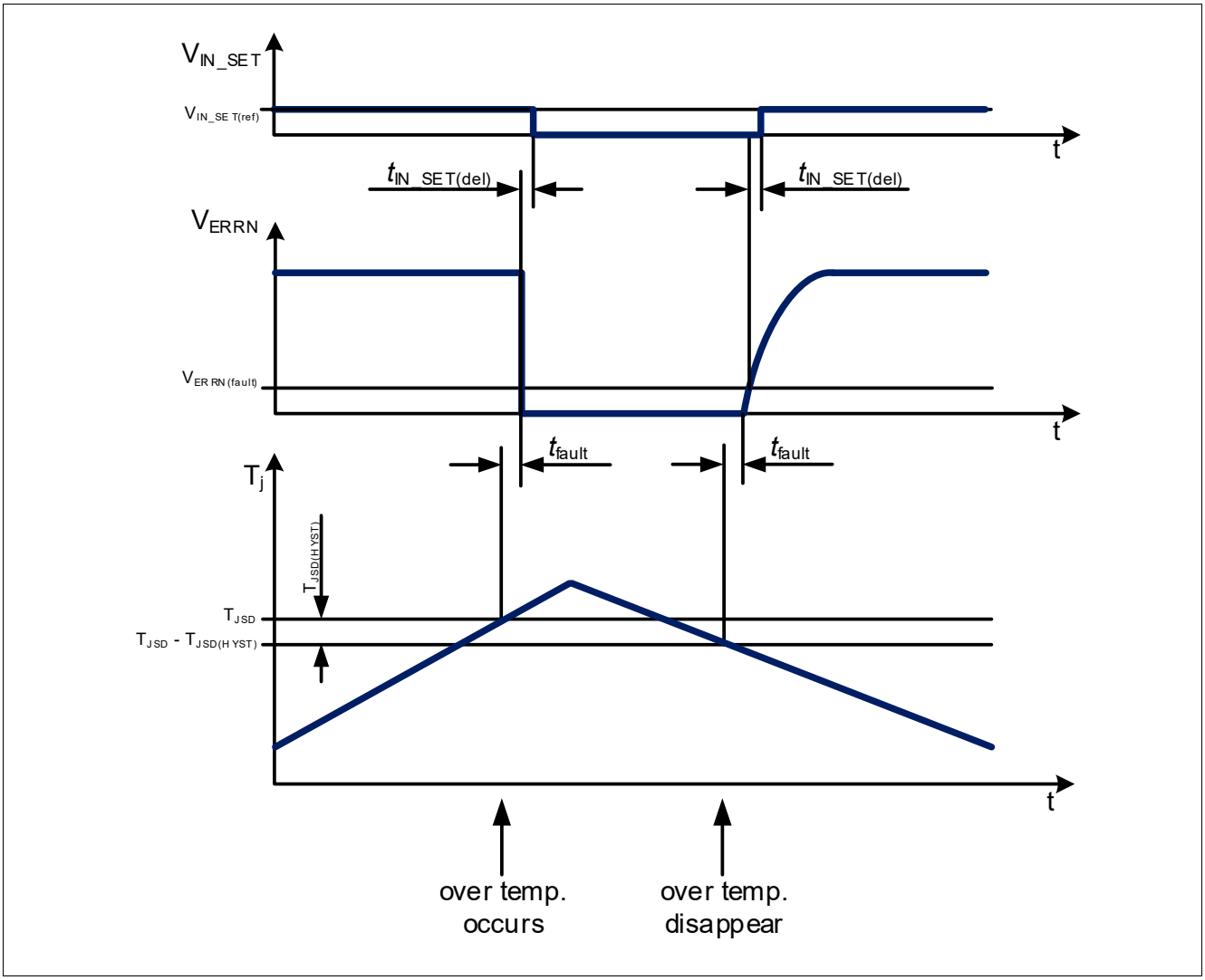


Figure 19 Overtemperature condition timing diagram example

6.3 Electrical characteristics: Overload management

Table 9 Electrical Characteristics: Fault management

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IN_SET fault current	$I_{IN\_SET(fault)}$	–	–	10	µA	[1] V_S > 8 V V_{OUT} = 3.6 V V_{ERRN} = 0 V V_{IN_SET} = 1 V V_{EN} > $V_{EN(th,max)}$	P_7.5.1
ERRN fault current	$I_{ERRN(fault)}$	2	–	–	mA	[1] V_S > 8 V V_{ERRN} = 0.8 V Overtemperature condition V_{EN} > $V_{EN(th,max)}$	P_7.5.2

Table 9 Electrical Characteristics: Fault management (cont'd)

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ERRN input threshold	$V_{ERRN(th)}$	0.8	–	2.0	V	1) V_S > 8 V	P_7.5.3
Timing							
Fault deactivation delay	t_{fault}	40	–	150	µs	1) V_S > 8 V 2) V_{OUT} falling from 5 V to 0 V or overtemperature condition $V_{EN} > V_{EN(th, max)}$	P_7.5.19
Fault appearance/removal to IN_SET deactivation/activation delay	$t_{IN\_SET(del)}$	–	–	10	µs	1) V_S > 8 V ERRN falling from 5 V to 0 V $V_{EN} > V_{EN(th, max)}$	P_7.5.4

1) Not subjected to production test: specified by design.

2) ERRN status only changed during overtemperature condition

7 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

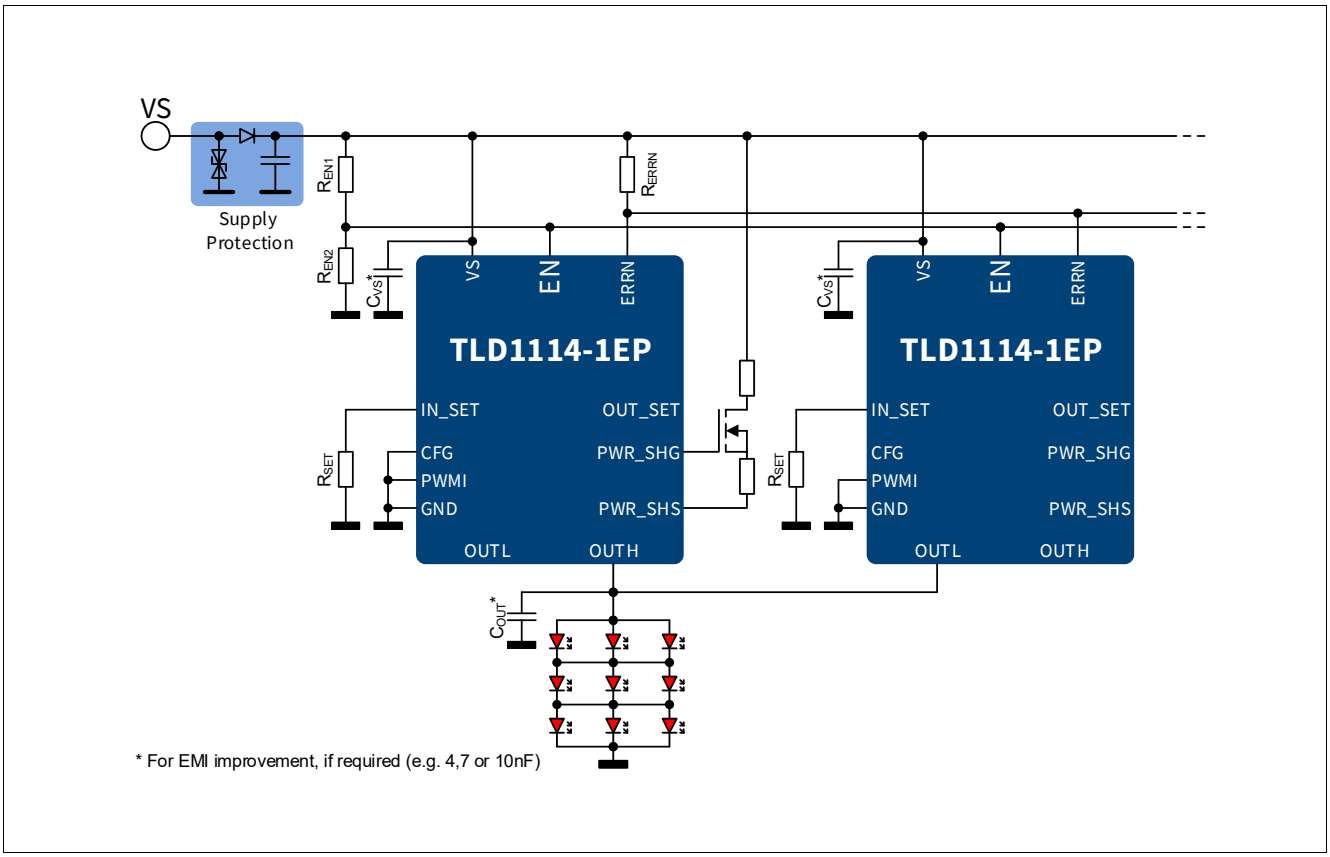


Figure 20 Application diagram example

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

8 Package outline

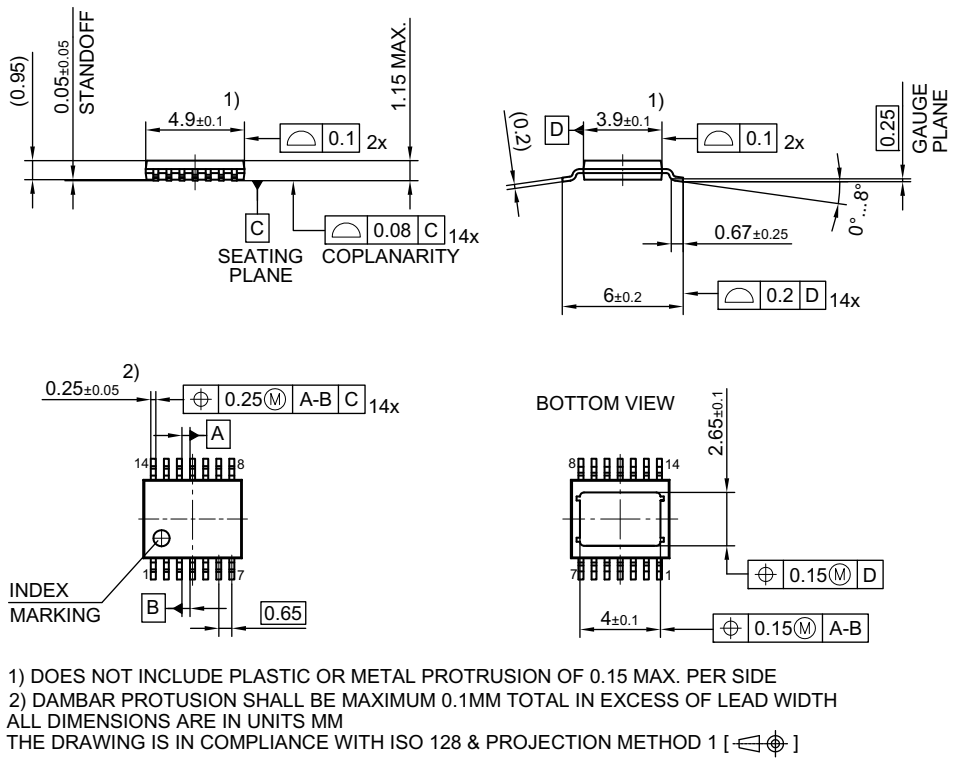


Figure 21 PG-TSDSO-14

Green product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

9 Revision History

Revision	Date	Changes
1.00	2018-10-09	Initial datasheet created

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2018-10-09
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about any aspect of this document?
Email: erratum@infineon.com

Document reference
LITIX™ Basic+ **TLD1114-1EP**

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Infineon:
TLD11141EPXUMA1

OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «**JONHON**», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «**FORSTAR**».

AVIC JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

FORSTAR®

Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А