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## FDMA6676PZ

### Single P-Channel PowerTrench® MOSFET

-30 V, -11 A, 13.5 mΩ

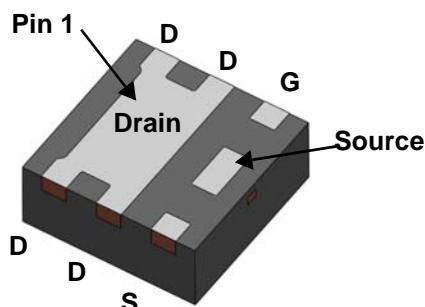
#### Features

- Max  $r_{DS(on)} = 13.5 \text{ m}\Omega$  @  $V_{GS} = -10 \text{ V}$
- 25V  $V_{GS}$  Extended Operating Rating
- 30V  $V_{DS}$  Blocking
- 2x2mm Form Factor
- Low Profile - 0.8 mm maximum
- Integrated Protection Diode
- RoHS Compliant
- Halogen Free

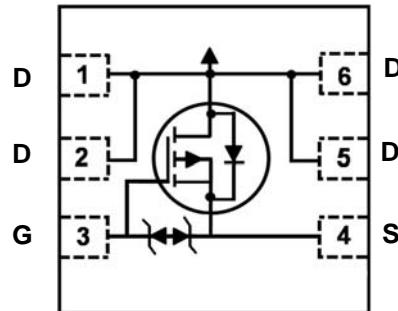


#### General Description

This device is an ultra low resistance P-Channel FET. It is designed for power line load switching applications and reverse polarity protection. It is especially optimized for voltage rails that can climb as high as 25V. Typical end systems include laptop computers, tablets and mobile phone. Applications include battery protection, input power line protection and charge path protection, including USB and other charge paths. The FDMA6676PZ has an enhanced  $V_{GS}$  rating of 25V specifically designed to simplify installation. When used as reverse polarity protection, with gate tied to ground and drain tied to V input, it is designed to support operating input voltages that can raise as high as 25V without the need for external Zener protection on the gate. Its small 2x2x0.8 form factor make it an ideal part for mobile and space constrained applications.



MicroFET 2X2 (Bottom View)



#### MOSFET Maximum Ratings $T_A = 25 \text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-30	V
$V_{GS}$	Gate to Source Voltage	$\pm 25$	V
$I_D$	Drain Current -Continuous $T_A = 25 \text{ }^\circ\text{C}$ (Note 1a)	-11	A
	-Pulsed (Note 3)	-165	
$P_D$	Power Dissipation $T_A = 25 \text{ }^\circ\text{C}$ (Note 1a)	2.4	W
	Power Dissipation $T_A = 25 \text{ }^\circ\text{C}$ (Note 1b)	0.9	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

#### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
676	FDMA6676PZ	MicroFET 2X2	7 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$\text{BV}_{\text{DSS}}$	Drain to Source Breakdown Voltage	$I_D = -250 \mu\text{A}, V_{GS} = 0 \text{ V}$	-30			V
$\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		-19		$\text{mV}/^\circ\text{C}$
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$			-1	$\mu\text{A}$
$I_{\text{GSS}}$	Gate to Source Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$			$\pm 10$	$\mu\text{A}$

## On Characteristics

$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250 \mu\text{A}$	-1.2	-2	-2.6	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		5.9		$\text{mV}/^\circ\text{C}$
$r_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = -10 \text{ V}, I_D = -11 \text{ A}$		11	13.5	$\text{m}\Omega$
		$V_{GS} = -4.5 \text{ V}, I_D = -8 \text{ A}$		19	27	
		$V_{GS} = -10 \text{ V}, I_D = -11 \text{ A}, T_J = 125^\circ\text{C}$		14.5	21	
$g_{\text{FS}}$	Forward Transconductance	$V_{DD} = -5 \text{ V}, I_D = -11 \text{ A}$		38		S

## Dynamic Characteristics

$C_{\text{iss}}$	Input Capacitance	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		1440	2160	pF
$C_{\text{oss}}$	Output Capacitance			477	720	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance			458	690	pF
$R_g$	Gate Resistance			12		$\Omega$

## Switching Characteristics

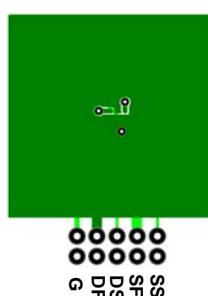
$t_{\text{d(on)}}$	Turn-On Delay Time	$V_{DD} = -15 \text{ V}, I_D = -11 \text{ A}, V_{GS} = -10 \text{ V}, R_{\text{GEN}} = 6 \Omega$		8.8	18	ns	
$t_r$	Rise Time			19	34	ns	
$t_{\text{d(off)}}$	Turn-Off Delay Time			87	139	ns	
$t_f$	Fall Time			72	115	ns	
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ V to } -10 \text{ V}$		33	46	nC	
$Q_g$	Total Gate Charge		$V_{GS} = 0 \text{ V to } -4.5 \text{ V}$	$V_{DD} = -15 \text{ V}, I_D = -11 \text{ A}$	20	28	nC
$Q_{gs}$	Gate to Source Charge				4.5	nC	
$Q_{gd}$	Gate to Drain "Miller" Charge				13	nC	

## Drain-Source Diode Characteristics

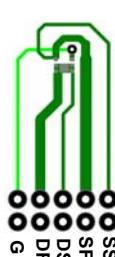
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = -2 \text{ A}$ (Note 2)		-0.7	-1.2	V
		$V_{GS} = 0 \text{ V}, I_S = -11 \text{ A}$ (Note 2)		-0.9	-1.4	V
$t_{\text{rr}}$	Reverse Recovery Time	$I_F = -11 \text{ A}, \text{di/dt} = 100 \text{ A}/\mu\text{s}$		31	50	ns
				9	18	nC

### NOTES:

1.  $R_{\text{thJA}}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\text{thCA}}$  is determined by the user's board design.



a. 52 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 145 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3. Pulse Id refers to Forward Bias Safe Operation Area.

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

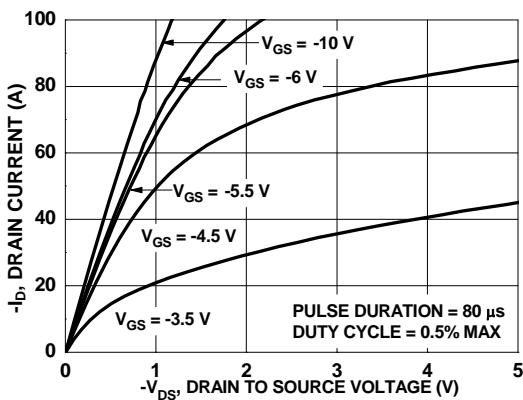


Figure 1. On-Region Characteristics

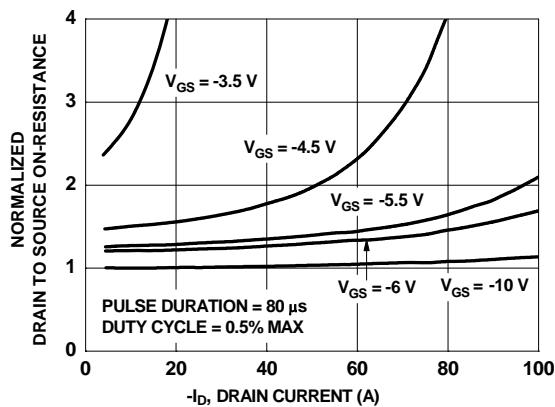


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

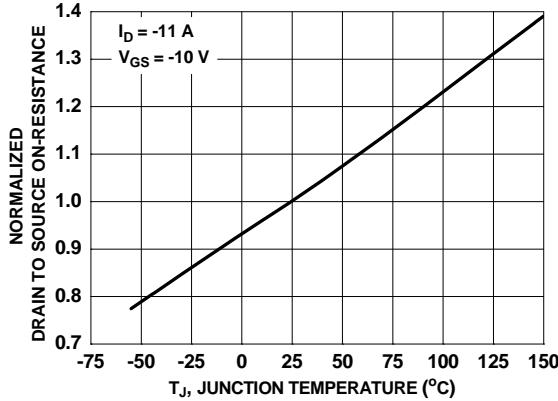


Figure 3. Normalized On-Resistance vs Junction Temperature

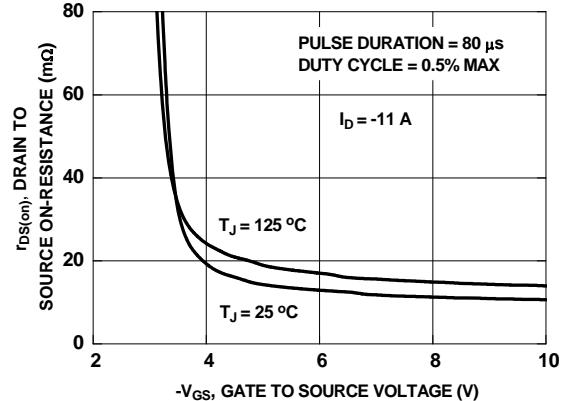


Figure 4. On-Resistance vs Gate to Source Voltage

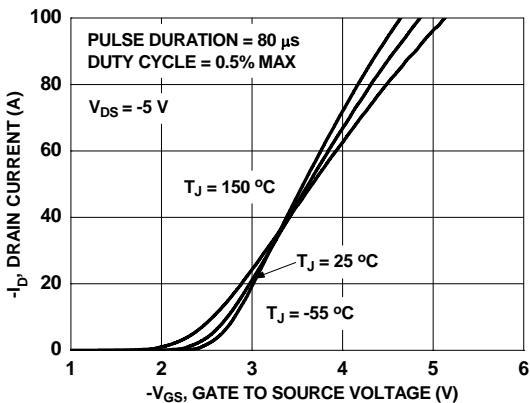


Figure 5. Transfer Characteristics

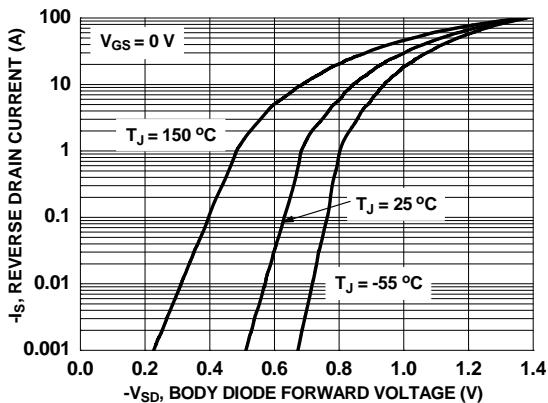


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

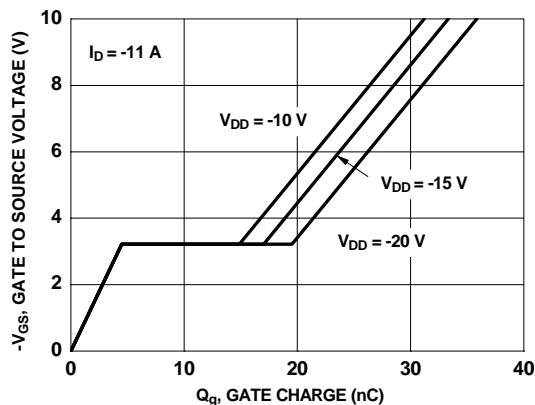


Figure 7. Gate Charge Characteristics

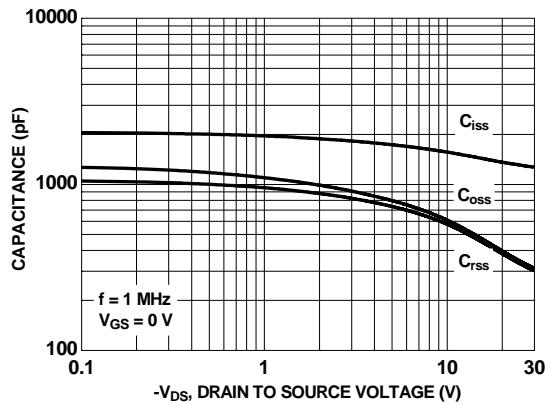


Figure 8. Capacitance vs Drain to Source Voltage

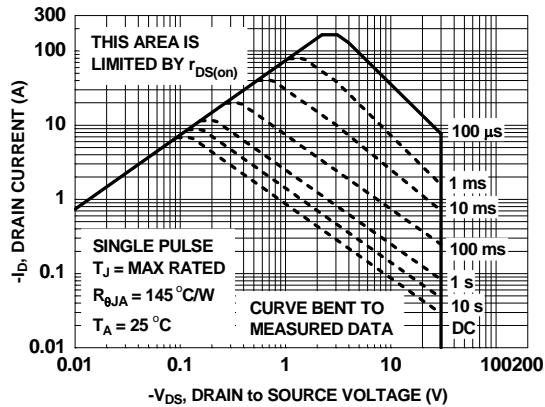


Figure 9. Forward Bias Safe Operating Area

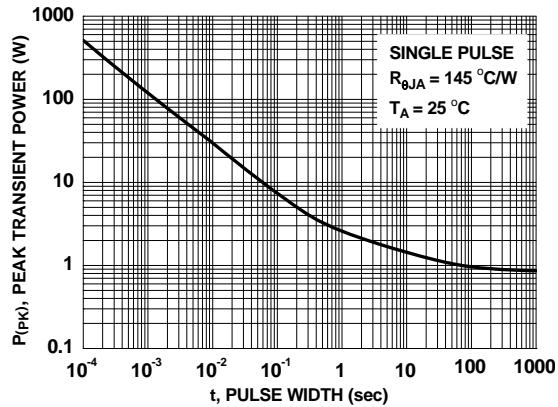


Figure 10. Single Pulse Maximum Power Dissipation

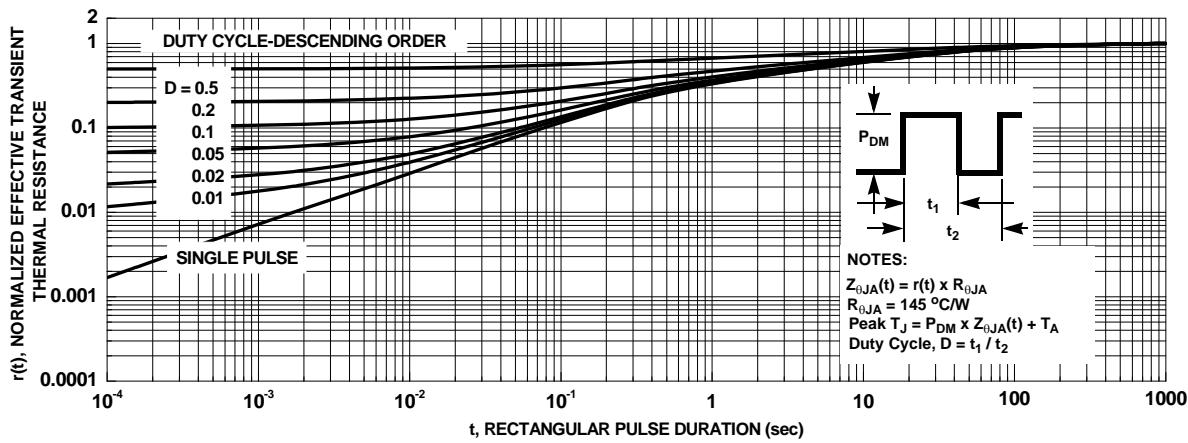
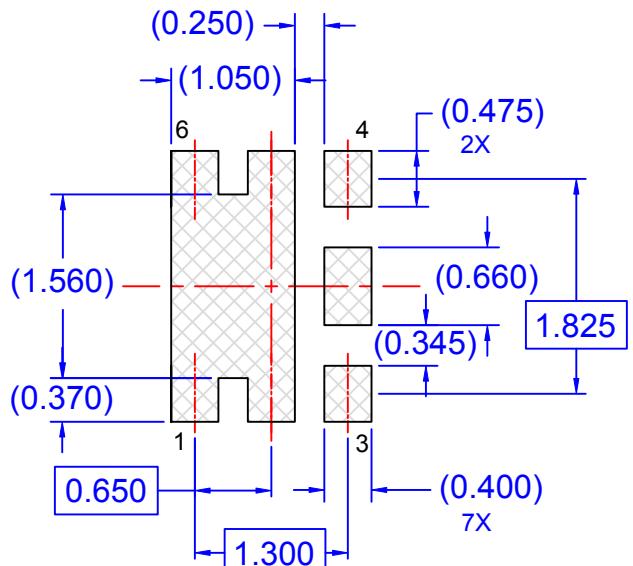
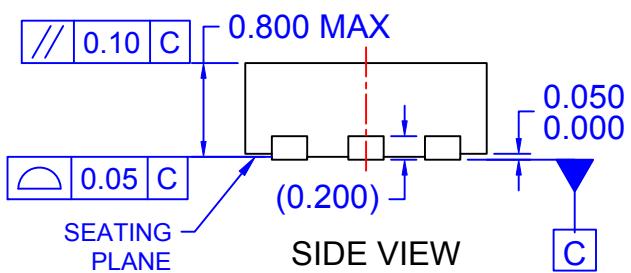
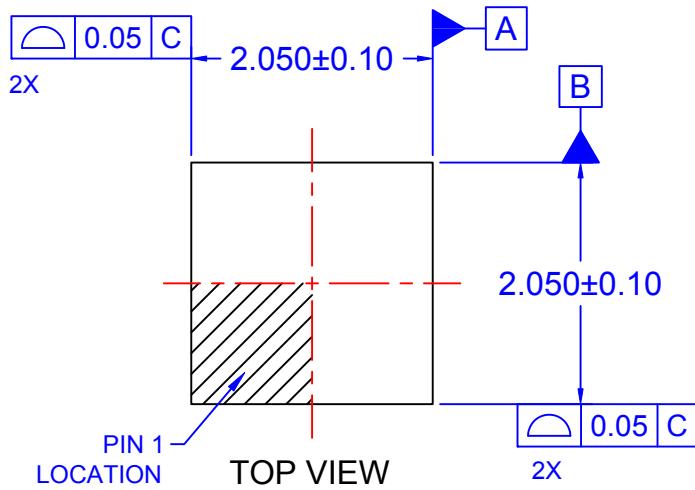
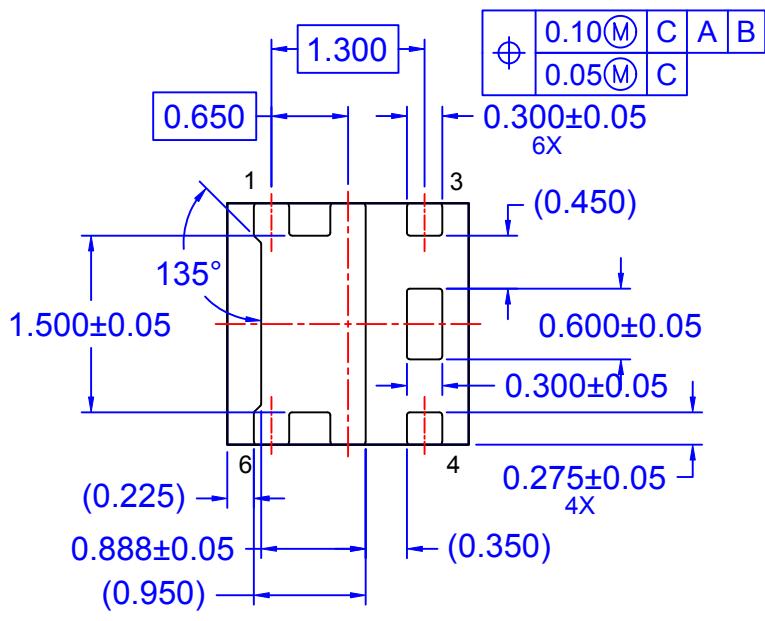


Figure 11. Junction-to-Ambient Transient Thermal Response Curve



## LAND PATTERN RECOMMENDATION



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