

# NB6L14S

## 2.5 V 1:4 AnyLevel™ Differential Input to LVDS Fanout Buffer/Translator

The NB6L14S is a differential 1:4 Clock or Data Receiver and will accept AnyLevel differential input signals: LVPECL, CML, LVDS, or HSCL. These signals will be translated to LVDS and four identical copies of Clock or Data will be distributed, operating up to 2.0 GHz or 2.5 Gb/s, respectively. As such, the NB6L14S is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock or Data distribution applications.

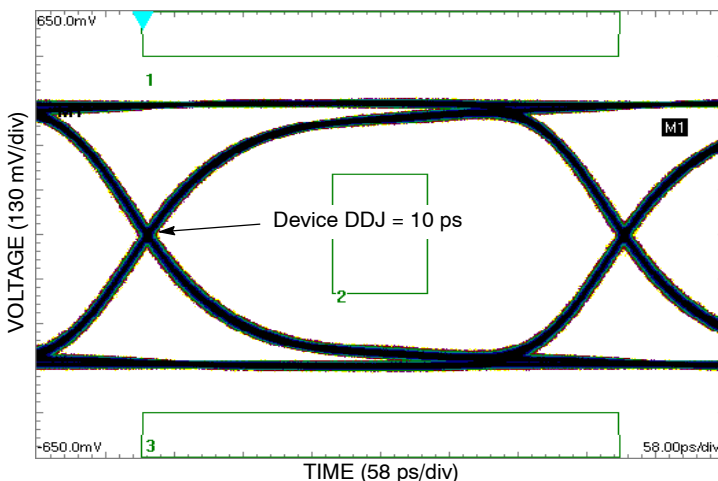
The NB6L14S has a wide input common mode range from  $GND + 50\text{ mV}$  to  $V_{CC} - 50\text{ mV}$ . Combined with the  $50\ \Omega$  internal termination resistors at the inputs, the NB6L14S is ideal for translating a variety of differential or single-ended Clock or Data signals to 350 mV typical LVDS output levels.

The NB6L14S is the 2.5 V version of the NB6N14S and is offered in a small 3 mm x 3 mm 16-QFN package. Application notes, models, and support documentation are available at [www.onsemi.com](http://www.onsemi.com).

The NB6L14S is a member of the ECLinPS MAX™ family of high performance products.

### Features

- Maximum Input Clock Frequency > 2.0 GHz
- Maximum Input Data Rate > 2.5 Gb/s
- 1 ps Maximum of RMS Clock Jitter
- Typically 10 ps of Data Dependent Jitter
- 380 ps Typical Propagation Delay
- 120 ps Typical Rise and Fall Times
- Single Power Supply;  $V_{CC} = 2.5 \pm 5\%$
- $V_{REF\_AC}$  Reference Output
- These are Pb-Free Devices



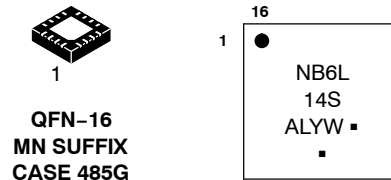
**Figure 2. Typical Output Waveform at 2.488 Gb/s with PRBS 2<sup>23</sup>-1 ( $V_{INPP} = 400\text{ mV}$ ; Input Signal DDJ = 14 ps)**



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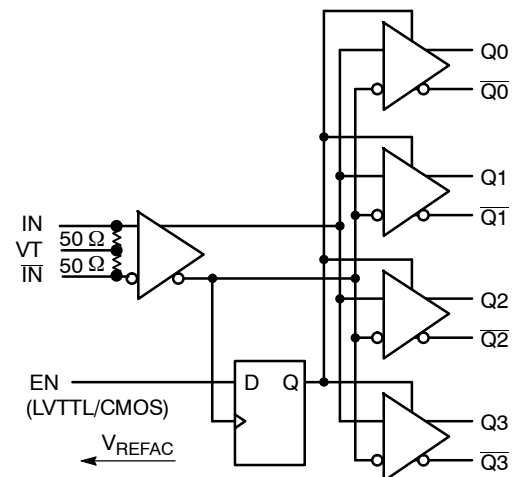
### MARKING DIAGRAM\*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.



**Figure 1. Logic Diagram**

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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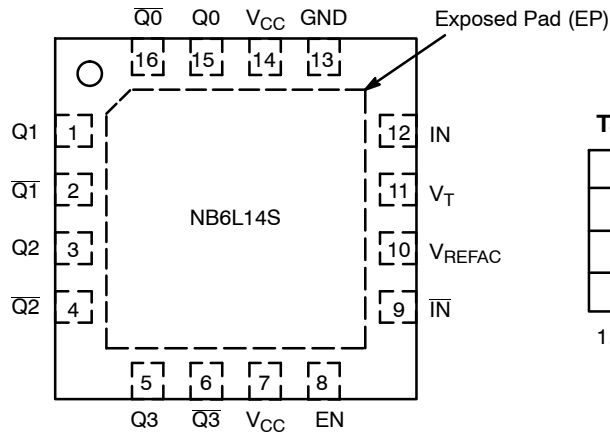


Figure 3. NB6L14S Pinout, 16-pin QFN (Top View)

Table 1. TRUTH TABLE

| IN | $\overline{\text{IN}}$ | EN | Q          | $\overline{\text{Q}}$ |
|----|------------------------|----|------------|-----------------------|
| 0  | 1                      | 1  | 0          | 1                     |
| 1  | 0                      | 1  | 1          | 0                     |
| x  | x                      | 0  | 0 (Note 1) | 1 (Note 1)            |

1. On next transition of the input signal (IN).

Table 2. PIN DESCRIPTION

| Pin | Name                      | I/O                   | Description  |
|-----|---------------------------|-----------------------|--|
| 1   | Q1                        | LVDS Output           | Non-inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.   |
| 2   | $\overline{\text{Q1}}$    | LVDS Output           | Inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.   |
| 3   | Q2                        | LVDS Output           | Non-inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.   |
| 4   | $\overline{\text{Q2}}$    | LVDS Output           | Inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.   |
| 5   | Q3                        | LVDS Output           | Non-inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.   |
| 6   | $\overline{\text{Q3}}$    | LVDS Output           | Inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.   |
| 7   | $\text{V}_{\text{CC}}$    | -                     | Positive Supply Voltage.   |
| 8   | EN                        | LVTTTL / LVCMOS Input | Synchronous Output Enable. When LOW, Q outputs will go LOW and Qb outputs will go HIGH on the next negative transition of IN input. The internal DFF register is clocked on the falling edge of IN input; see Figure 26. The EN pin has an internal pullup resistor and defaults HIGH when left open.                              |
| 9   | $\overline{\text{IN}}$    | LVPECL, CML, LVDS     | Inverted Differential Input  |
| 10  | $\text{V}_{\text{REFAC}}$ | LVPECL Output         | The $\text{V}_{\text{REFAC}}$ reference output can only be used to rebias capacitor-coupled differential or single-ended input signals. For the capacitor-coupled IN and/or INb inputs, $\text{V}_{\text{REFAC}}$ should be connected to the VT pin and bypassed to ground with a 0.01 $\mu\text{F}$ capacitor.                    |
| 11  | $\text{V}_{\text{T}}$     | LVPECL Output         | Internal 100 $\Omega$ Center-tapped Termination Pin for IN and $\overline{\text{IN}}$  |
| 12  | IN                        | LVPECL, CML, LVDS     | Non-inverted Differential Input. (Note 2)  |
| 13  | GND                       | -                     | Negative Supply Voltage.   |
| 14  | $\text{V}_{\text{CC}}$    | -                     | Positive Supply Voltage.   |
| 15  | Q0                        | LVDS Output           | Non-inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.   |
| 16  | $\overline{\text{Q0}}$    | LVDS Output           | Inverted IN output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.   |
| -   | EP                        | -                     | The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to GND on the PC board. |

2. In the differential configuration, when the input termination pin (VT) is connected to a termination voltage or left open, and if no signal is applied on IN/ $\overline{\text{IN}}$  inputs, then the device will be susceptible to self-oscillation.

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**Table 3. ATTRIBUTES**

| Characteristics  | Value                |
|--|----------------------|
| Moisture Sensitivity (Note 3)                          | Level 1              |
| Flammability Rating<br>Oxygen Index: 28 to 34          | UL 94 V-0 @ 0.125 in |
| ESD Protection<br>Human Body Model<br>Machine Model    | > 2 kV<br>> 200 V    |
| Transistor Count                                       | 745                  |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test |                      |

3. For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

| Symbol              | Parameter   | Condition 1                             | Condition 2                       | Rating       | Unit         |
|---------------------|---|---|-----------------------------------|--------------|--------------|
| V <sub>CC</sub>     | Positive Power Supply   | GND = 0 V                               |                                   | 3.8          | V            |
| V <sub>IN</sub>     | Positive Input  | GND = 0 V                               | V <sub>IN</sub> ≤ V <sub>CC</sub> | 3.8          | V            |
| I <sub>IN</sub>     | Input Current Through R <sub>T</sub> (50 Ω Resistor)  | Static<br>Surge                         |                                   | 35<br>70     | mA<br>mA     |
| I <sub>OSC</sub>    | Output Short Circuit Current<br>Line-to-Line (Q to $\bar{Q}$ )<br>Line-to-End (Q or $\bar{Q}$ to GND) | Q or $\bar{Q}$<br>Q to $\bar{Q}$ to GND | Continuous<br>Continuous          | 12<br>24     | mA           |
| I <sub>REF_AC</sub> | V <sub>REF_AC</sub> Sink/Source Current   |   |                                   | ±0.5         | mA           |
| T <sub>A</sub>      | Operating Temperature Range   | QFN-16                                  |                                   | -40 to +85   | °C           |
| T <sub>stg</sub>    | Storage Temperature Range   |   |                                   | -65 to +150  | °C           |
| θ <sub>JA</sub>     | Thermal Resistance (Junction-to-Ambient) (Note 4)   | 0 lfpm<br>500 lfpm                      | QFN-16<br>QFN-16                  | 41.6<br>35.2 | °C/W<br>°C/W |
| θ <sub>JC</sub>     | Thermal Resistance (Junction-to-Case)   | 1S2P (Note 4)                           | QFN-16                            | 4.0          | °C/W         |
| T <sub>sol</sub>    | Wave Solder<br>Pb-Free  |   |                                   | 265          | °C           |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board – 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

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**Table 5. DC CHARACTERISTICS**  $V_{CC} = 2.375\text{ V to }2.625\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

| Symbol   | Characteristic                | Min | Typ | Max | Unit |
|----------|-------------------------------|-----|-----|-----|------|
| $I_{CC}$ | Power Supply Current (Note 9) |     | 65  | 100 | mA   |

**DIFFERENTIAL INPUTS DRIVEN SINGLE-ENDED** (Figures 17, 18, 22, and 24)

|             |  |                  |                  |                  |    |
|-------------|--|------------------|------------------|------------------|----|
| $V_{th}$    | Input Threshold Reference Voltage Range (Note 8) | GND +100         |                  | $V_{CC} - 100$   | mV |
| $V_{IH}$    | Single-ended Input HIGH Voltage                  | $V_{th} + 100$   |                  | $V_{CC}$         | mV |
| $V_{IL}$    | Single-ended Input LOW Voltage                   | GND              |                  | $V_{th} - 100$   | mV |
| $V_{REFAC}$ | Reference Output Voltage (Note 11)               | $V_{CC} - 1.600$ | $V_{CC} - 1.425$ | $V_{CC} - 1.300$ | V  |

**DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY** (Figures 10, 12, NO TAG, NO TAG, 23, and 25)

|           |  |          |    |                 |          |
|-----------|--|----------|----|-----------------|----------|
| $V_{IHD}$ | Differential Input HIGH Voltage                      | 100      |    | $V_{CC}$        | mV       |
| $V_{ILD}$ | Differential Input LOW Voltage                       | GND      |    | $V_{IHD} - 100$ | mV       |
| $V_{CMR}$ | Input Common Mode Range (Differential Configuration) | GND + 50 |    | $V_{CC} - 50$   | mV       |
| $V_{ID}$  | Differential Input Voltage ( $V_{IHD} - V_{ILD}$ )   | 100      |    | $V_{CC}$        | mV       |
| $R_{TIN}$ | Internal Input Termination Resistor                  | 40       | 50 | 60              | $\Omega$ |

**LVDS OUTPUTS** (Note 5)

|                 |   |      |      |      |    |
|-----------------|---|------|------|------|----|
| $V_{OD}$        | Differential Output Voltage   | 250  |      | 450  | mV |
| $\Delta V_{OD}$ | Change in Magnitude of $V_{OD}$ for Complementary Output States (Note 10) | 0    | 1    | 25   | mV |
| $V_{OS}$        | Offset Voltage (Figure 21)  | 1125 |      | 1375 | mV |
| $\Delta V_{OS}$ | Change in Magnitude of $V_{OS}$ for Complementary Output States (Note 10) | 0    | 1    | 25   | mV |
| $V_{OH}$        | Output HIGH Voltage (Note 6)  |      | 1425 | 1600 | mV |
| $V_{OL}$        | Output LOW Voltage (Note 7)   | 900  | 1075 |      | mV |

**LVTTL/LVCMOS INPUT, EN**

|          |                    |      |  |          |               |
|----------|--------------------|------|--|----------|---------------|
| $V_{IH}$ | Input HIGH Voltage | 2.0  |  | $V_{CC}$ | V             |
| $V_{IL}$ | Input LOW Voltage  | GND  |  | 0.8      | V             |
| $I_{IH}$ | Input HIGH Current | -150 |  | 150      | $\mu\text{A}$ |
| $I_{IL}$ | Input LOW Current  | -150 |  | 150      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. LVDS outputs require 100  $\Omega$  receiver termination resistor between differential pair. See Figure 20.
6.  $V_{OHmax} = V_{OSmax} + \frac{1}{2} V_{ODmax}$ .
7.  $V_{OLmax} = V_{OSmin} - \frac{1}{2} V_{ODmax}$ .
8.  $V_{th}$  is applied to the complementary input when operating in single-ended mode.
9. Input termination pins open at the DC level within  $V_{CMR}$  and output pins loaded with  $R_L = 100\ \Omega$  across differential.
10. Parameter guaranteed by design verification not tested in production.
11.  $V_{REFAC}$  used to rebias capacitor-coupled inputs only (see Figures 17 and 18).

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**Table 6. AC CHARACTERISTICS**  $V_{CC} = 2.375\text{ V to }2.625\text{ V}$ ,  $GND = 0\text{ V}$ ; (Note 12)

| Symbol                   | Characteristic  | -40°C to +85°C  |  |                | Unit |
|--------------------------|---|---|--|----------------|------|
|                          |   | Min   | Typ  | Max            |      |
| $f_{inMax}$              | Maximum Input Clock Frequency   | 2.0   |  |                | GHz  |
| $V_{OUTPP}$              | Output Voltage Amplitude (@ $V_{INPPmin}$ )<br>(Figure 4)                         | $f_{in} \leq 1.0\text{ GHz}$<br>220<br>$f_{in} = 1.5\text{ GHz}$<br>200<br>$f_{in} = 2.0\text{ GHz}$<br>170 | 350<br>300<br>270  |                | mV   |
| $f_{DATA}$               | Maximum Operating Data Rate   | 2.5   |  |                | Gb/s |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Differential Input to Differential Output, IN to Q<br>Propagation Delay @ 100 MHz | 300   | 450  | 600            | ps   |
| $t_s$<br>$t_h$           | Setup Time<br>Hold Time   | 300<br>500  | 20<br>20   |                |      |
| $t_{SKEW}$               | Within Device Skew (Note 17)<br>Device-to-Device Skew (Note 16)                   |   | 5<br>30  | 20<br>200      | ps   |
| $t_{JITTER}$             | RMS Random Clock Jitter (Note 14)<br>Deterministic Jitter (Note 15)               |   | $f_{in} = 2.0\text{ GHz}$<br>0.5<br>5.0<br>$f_{DATA} \leq 2.488\text{ Gb/s}$ | 0.8<br>20      | ps   |
| $V_{INPP}$               | Input Voltage Swing/Sensitivity<br>(Differential Configuration) (Note 13)         | 100   |  | $V_{CC} - GND$ | mV   |
| $t_r$<br>$t_f$           | Output Rise/Fall Times @ 250 MHz<br>(20% – 80%)                                   | 70  | 150  | 225            | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

12. Measured by forcing  $V_{INPPmin}$  with 50% duty cycle clock source and  $V_{CC} - 1400\text{ mV}$  offset. All loading with an external  $R_L = 100\ \Omega$ . Input edge rates 150 ps (20%–80%). See Figure 20.

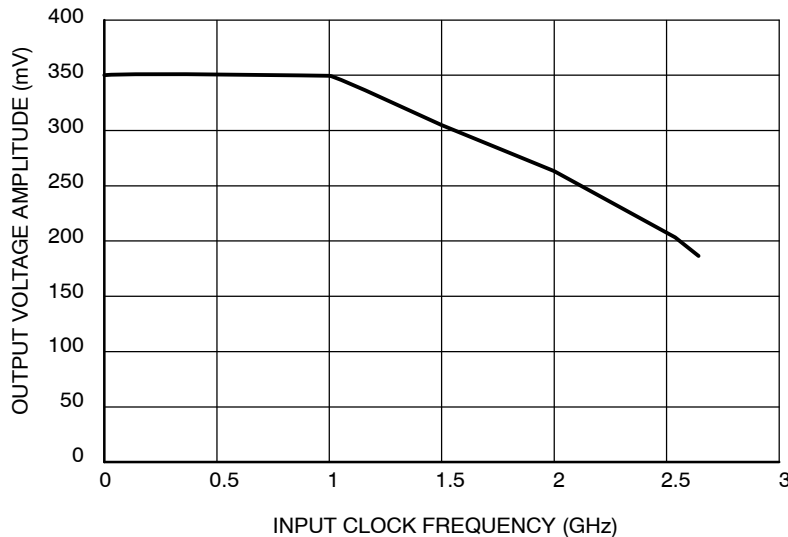
13. Input voltage swing is a single-ended measurement operating in differential mode.

14. RMS jitter with 50% Duty Cycle clock signal at 750 MHz.

15. Deterministic jitter with input NRZ data at PRBS  $2^{23}-1$  and K28.5.

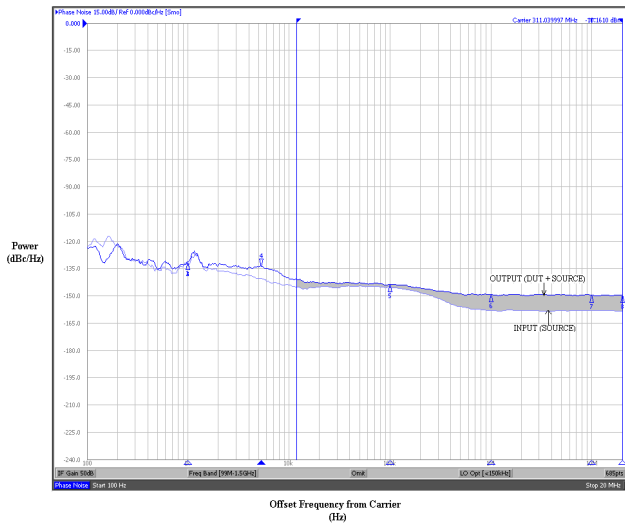
16. Skew is measured between outputs under identical transition @ 250 MHz.

17. The worst case condition between  $Q0/\bar{Q}0$  and  $Q1/\bar{Q}1$  from either  $D0/\bar{D}0$  or  $D1/\bar{D}1$ , when both outputs have the same transition.

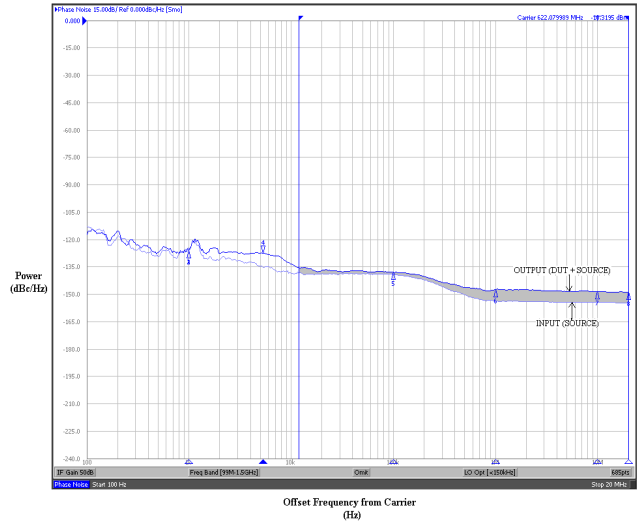


**Figure 4. Output Voltage Amplitude ( $V_{OUTPP}$ ) versus Input Clock Frequency ( $f_{in}$ ) and Temperature (@  $V_{CC} = 2.5\text{ V}$ )**

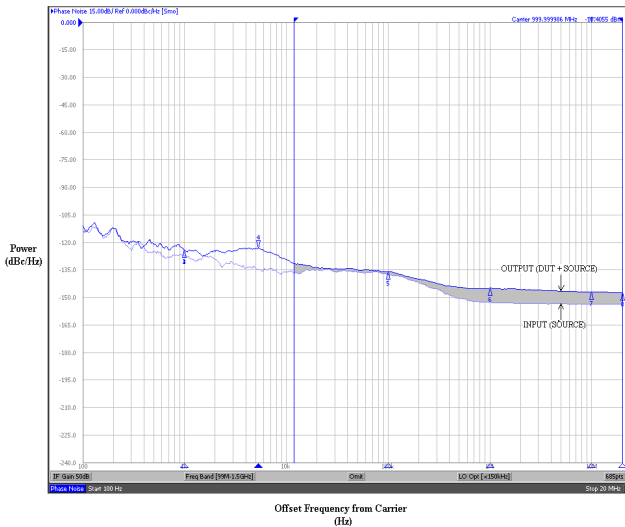
# NB6L14S



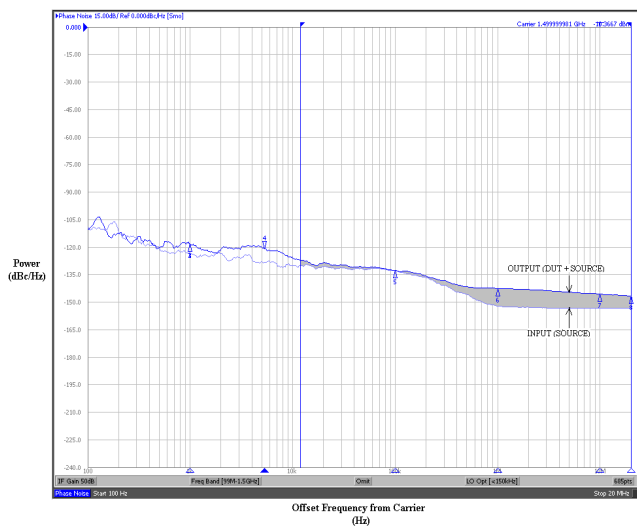
**Figure 5. Typical Phase Noise Plot at  $f_{\text{carrier}} = 311.04 \text{ MHz}$**



**Figure 6. Typical Phase Noise Plot at  $f_{\text{carrier}} = 622.08 \text{ MHz}$**



**Figure 7. Typical Phase Noise Plot at  $f_{\text{carrier}} = 1 \text{ GHz}$**

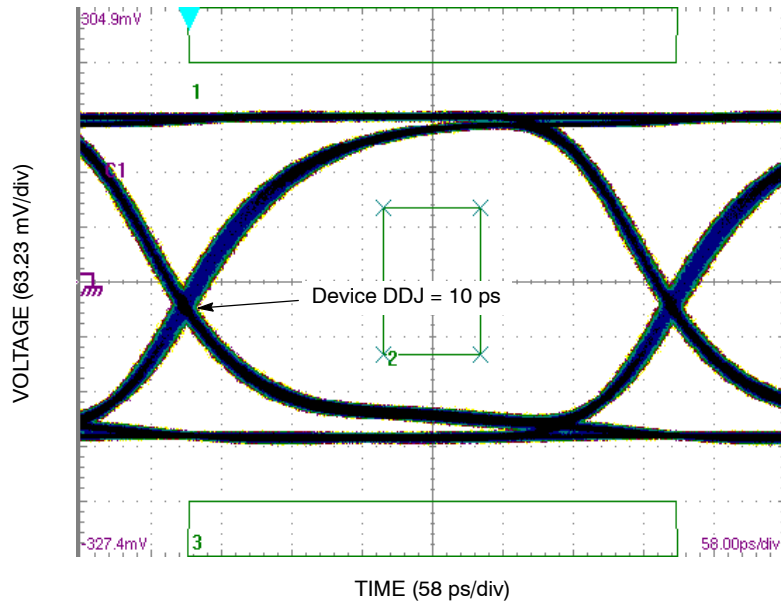


**Figure 8. Typical Phase Noise Plot at  $f_{\text{carrier}} = 1.5 \text{ GHz}$**

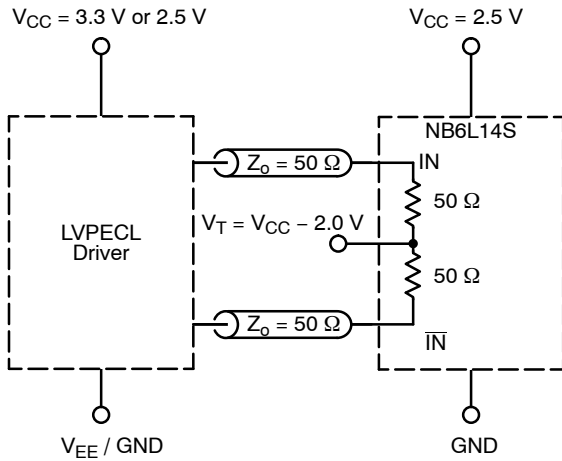
The above phase noise plots captured using Agilent E5052A show additive phase noise of the NB6L14S device at frequencies 311.04 MHz, 622.08 MHz, 1 GHz and 1.5 GHz respectively at an operating voltage of 2.5 V in room temperature. The RMS Phase Jitter contributed by the

device (integrated between 12 kHz and 20 MHz; as shown in the shaded region of the plot) at each of the frequencies is 65 fs, 29 fs, 24 fs and 20 fs respectively. The input source used for the phase noise measurements is Agilent E8663B.

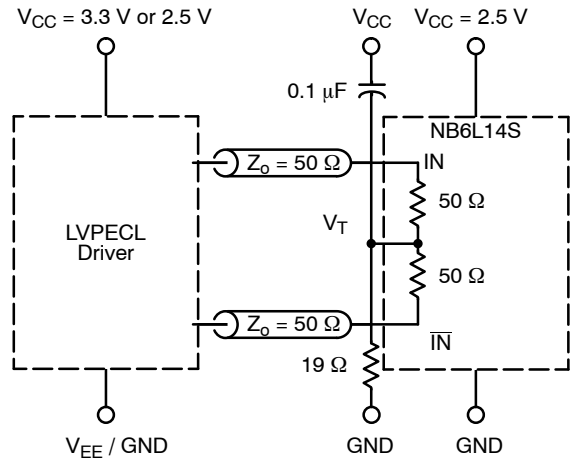
# NB6L14S



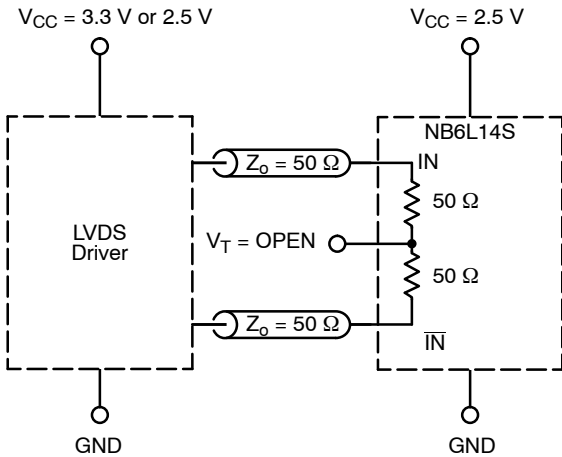
**Figure 9. Typical Output Waveform at 2.488 Gb/s with PRBS  $2^{23-1}$  and OC48 mask ( $V_{INPP} = 100$  mV; Input Signal DDJ = 14 ps)**



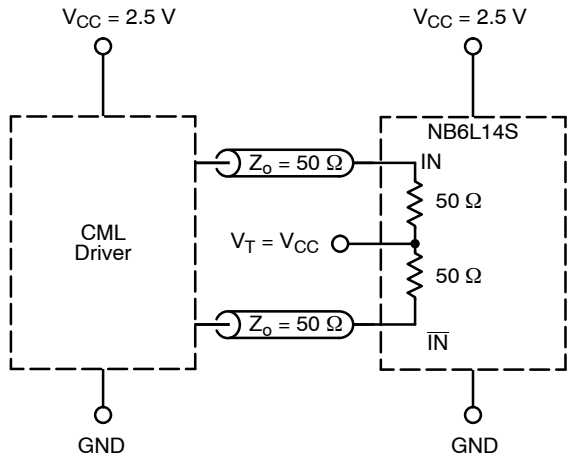
**Figure 10. LVPECL Interface**



**Figure 11. LVPECL Y-Termination Interface**



**Figure 12. LVDS Interface**



**Figure 13. CML Interface**

# NB6L14S

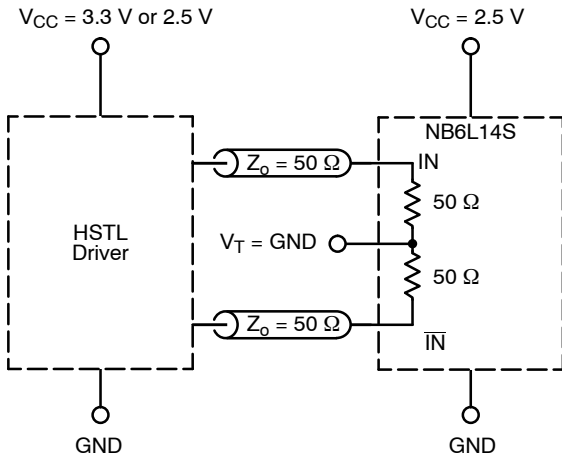


Figure 14. HSTL Interface

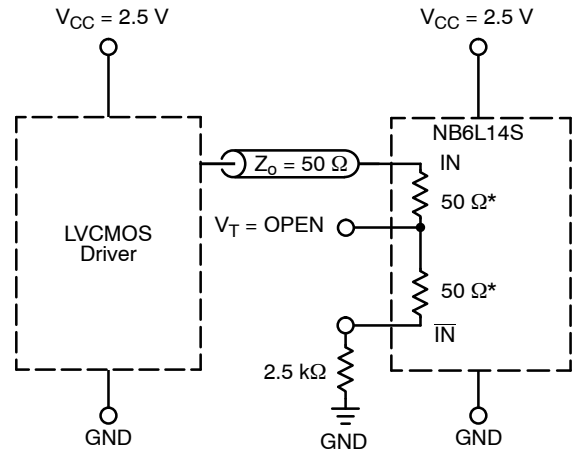


Figure 15. LVCMOS Interface

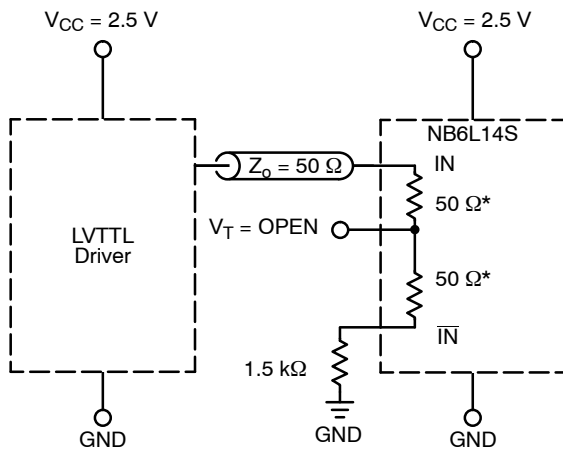


Figure 16. LVTTTL Interface

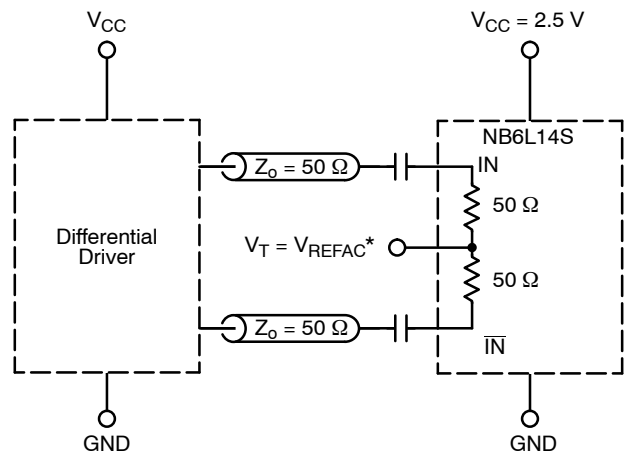


Figure 17. Capacitor-Coupled Differential Interface ( $V_T$  Connected to  $V_{REF\_AC}$ )

\* $V_{REFAC}$  bypassed to ground with a 0.1  $\mu$ F capacitor.

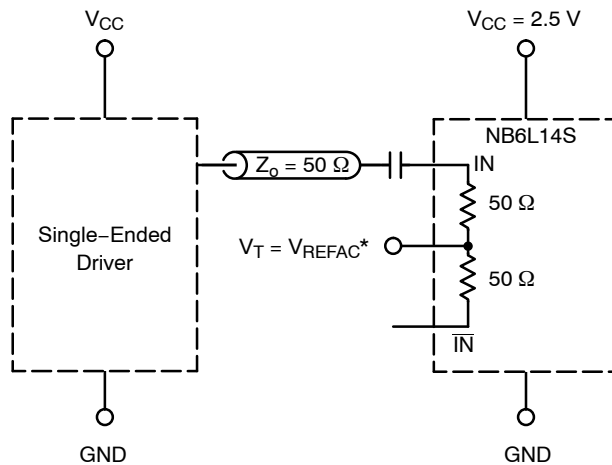


Figure 18. Capacitor-Coupled Single-Ended Interface ( $V_T$  Connected to  $V_{REFAC}$ )

\* $V_{REFAC}$  bypassed to ground with a 0.1  $\mu$ F capacitor.



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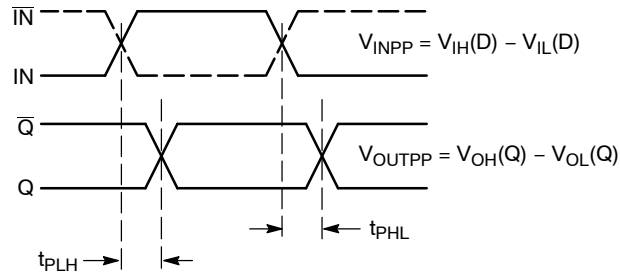


Figure 19. AC Reference Measurement

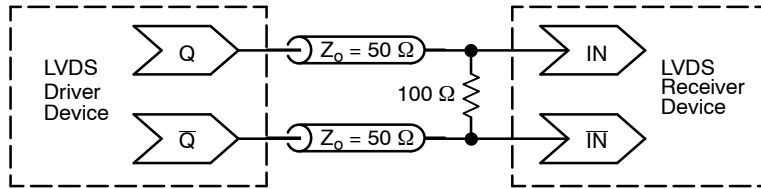


Figure 20. Typical LVDS Termination for Output Driver and Device Evaluation

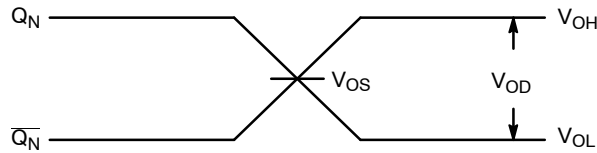


Figure 21. LVDS Output

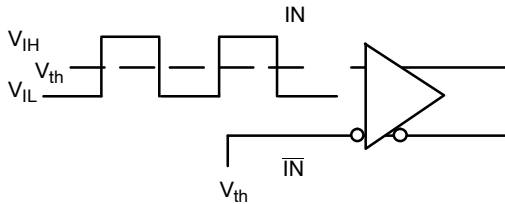


Figure 22. Differential Input Driven Single-Ended

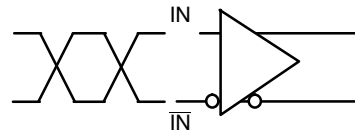


Figure 23. Differential Inputs Driven Differentially

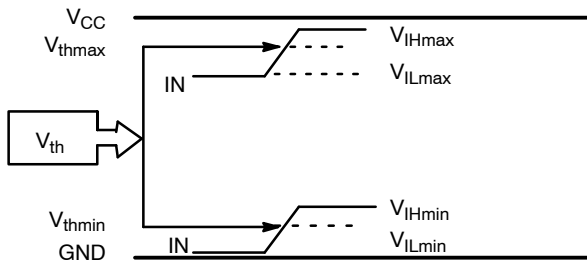


Figure 24.  $V_{th}$  Diagram

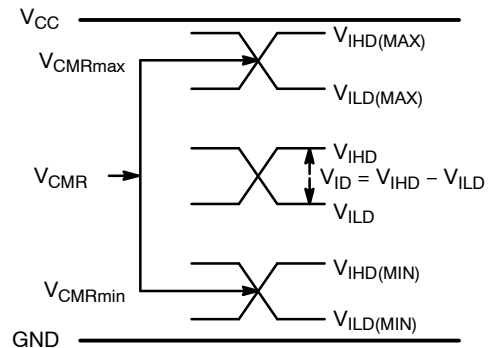


Figure 25.  $V_{CMR}$  Diagram

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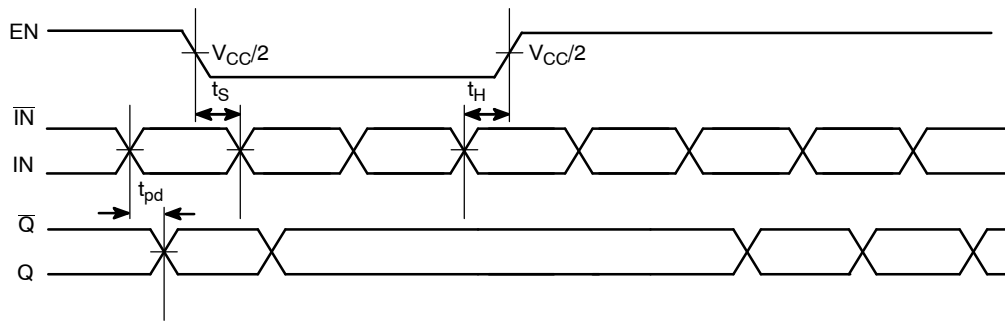


Figure 26. EN Timing Diagram

## ORDERING INFORMATION

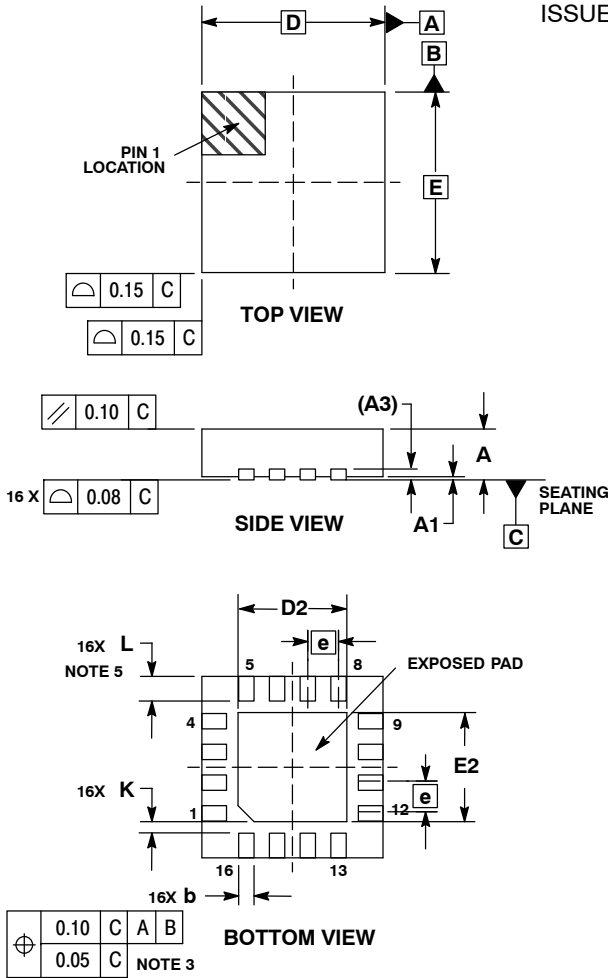
| Device       | Package                       | Shipping <sup>†</sup> |
|--------------|-------------------------------|-----------------------|
| NB6L14SMNG   | QFN-16, 3 X 3 mm<br>(Pb-Free) | 123 Units / Rail      |
| NB6L14SMNTXG | QFN-16, 3 X 3 mm<br>(Pb-Free) | 3000 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## PACKAGE DIMENSIONS

### 16 PIN QFN CASE 485G-01 ISSUE C

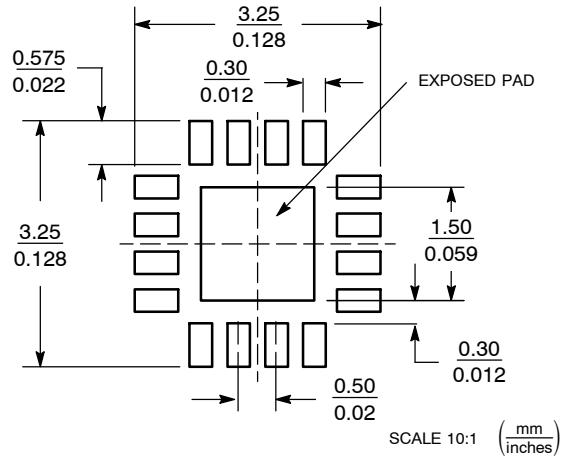


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L<sub>max</sub> CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 0.80        | 1.00 |
| A1  | 0.00        | 0.05 |
| A3  | 0.20        | REF  |
| b   | 0.18        | 0.30 |
| D   | 3.00        | BSC  |
| D2  | 1.65        | 1.85 |
| E   | 3.00        | BSC  |
| E2  | 1.65        | 1.85 |
| e   | 0.50        | BSC  |
| K   | 0.18        | TYP  |
| L   | 0.30        | 0.50 |

#### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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