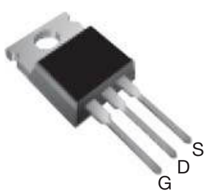
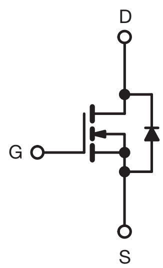
E Series Power MOSFET with Fast Body Diode and Low Gate Charge

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ typ. (Ω) at 25 °C	V_{GS} = 10 V	0.127
Q_g (Max.) (nC)	75	
Q_{gs} (nC)	17	
Q_{gd} (nC)	19	
Configuration	Single	

TO-220AB





N-Channel MOSFET

FEATURES

- Reduced figure-of-merit (FOM): R_{on} x Q_g
- Fast body diode MOSFET using E series technology
- Reduced t_{rr}, Q_{rr}, and I_{RRM}
- Increased robustness due to low Q_{rr}
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Telecommunications
  - Server and telecom power supplies
- Computing
  - ATX power supplies
- Industrial
  - Welding
  - Induction heating
  - Battery chargers
  - Uninterruptible power supplies (UPS)
- Renewable energy
  - String PV inverters

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free and Halogen-free	SiHP25N60EFL-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

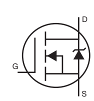
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	600	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	25	A
		T_C = 100 °C		16	
Pulsed Drain Current [a]			I_{DM}	61	
Linear Derating Factor				2	W/°C
Single Pulse Avalanche Energy [b]			E_{AS}	353	mJ
Maximum Power Dissipation			P_D	250	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	V_{DS} = 0 V to 80 % V_{DS}		dV/dt	70	V/ns
Reverse Diode dV/dt [d]				15	
Soldering Recommendations (Peak temperature) [c]	for 10 s			300	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. V_{DD} = 140 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω, I_{AS} = 5 A.
c. 1.6 mm from case.
d. $I_{SD} \le I_D$, dI/dt = 100 A/μs, starting T_J = 25 °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.5	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA		600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 10 mA		-	0.69	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 100	nA
		V_{GS} = ± 30 V		-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 480 V, V_{GS} = 0 V		-	-	1	μA
		V_{DS} = 480 V, V_{GS} = 0 V, T_J = 125 °C		-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 12.5 A	-	0.127	0.146	Ω
Forward Transconductance	g_{fs}	V_{DS} = 30 V, I_D = 12.5 A		-	11.3	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz		-	2274	-	pF
Output Capacitance	C_{oss}			-	137	-	
Reverse Transfer Capacitance	C_{rss}			-	4	-	
Effective Output Capacitance, Energy Related [a]	$C_{o(er)}$	V_{DS} = 0 V to 480 V, V_{GS} = 0 V		-	79	-	
Effective Output Capacitance, Time Related [b]	$C_{o(tr)}$			-	330	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 12.5 A, V_{DS} = 480 V	-	50	75	nC
Gate-Source Charge	Q_{gs}			-	17	-	
Gate-Drain Charge	Q_{gd}			-	19	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 480 V, I_D = 12.5 A, R_g = 9.1 Ω, V_{GS} = 10 V		-	25	50	ns
Rise Time	t_r			-	39	68	
Turn-Off Delay Time	$t_{d(off)}$			-	47	94	
Fall Time	t_f			-	21	42	
Gate Input Resistance	R_g	f = 1 MHz, open drain		0.4	0.7	1.4	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	25	A
Pulsed Diode Forward Current	I_{SM}			-	-	61	
Diode Forward Voltage	V_{SD}	T_J = 25 °C, I_S = 12.5 A, V_{GS} = 0 V		-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S =12.5 A, dI/dt = 100 A/μs, V_R = 25 V		-	138	276	ns
Reverse Recovery Charge	Q_{rr}			-	0.8	1.6	μC
Reverse Recovery Current	I_{RRM}			-	11	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

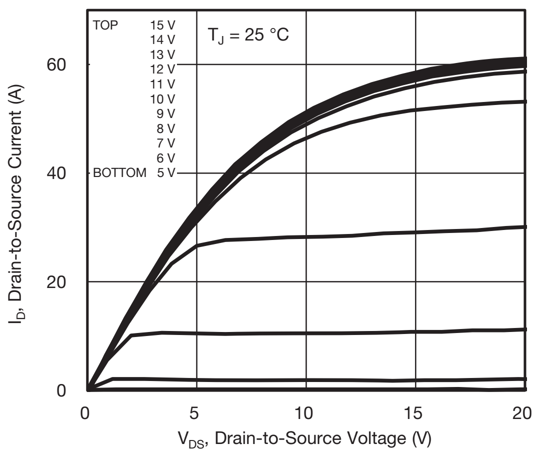


Fig. 1 - Typical Output Characteristics

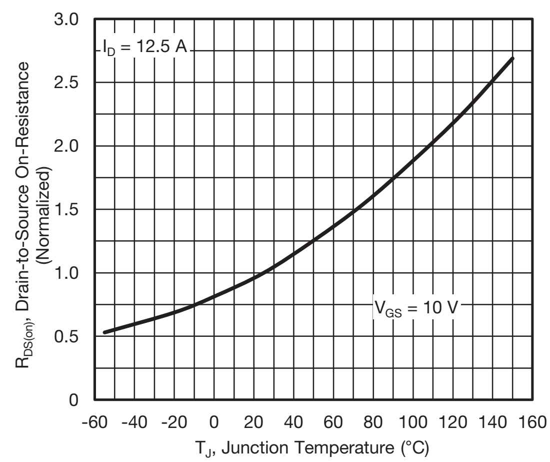


Fig. 4 - Normalized On-Resistance vs. Temperature

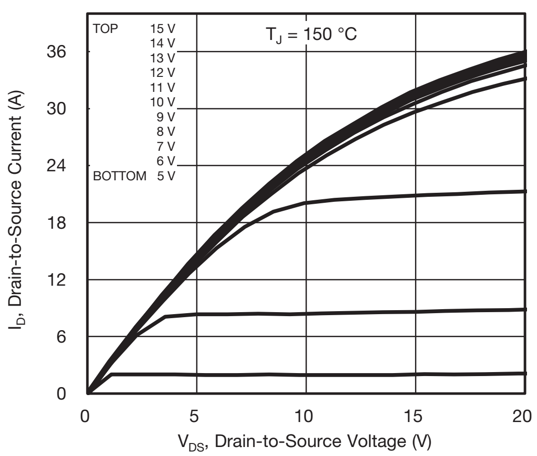


Fig. 2 - Typical Output Characteristics

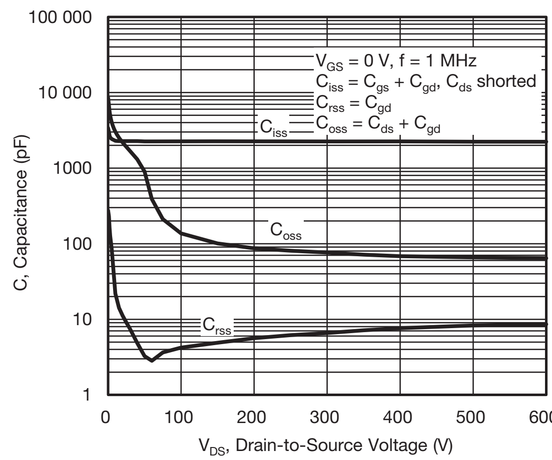


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

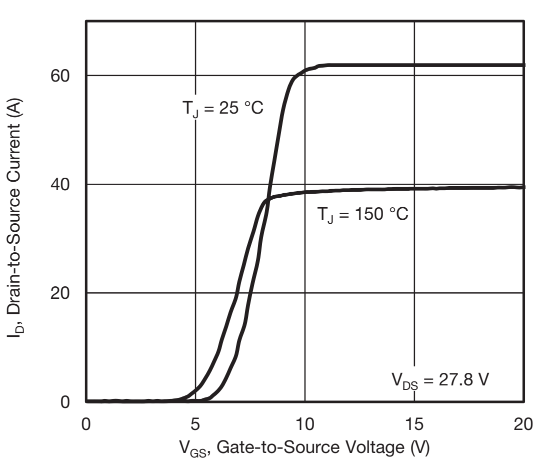


Fig. 3 - Typical Transfer Characteristics

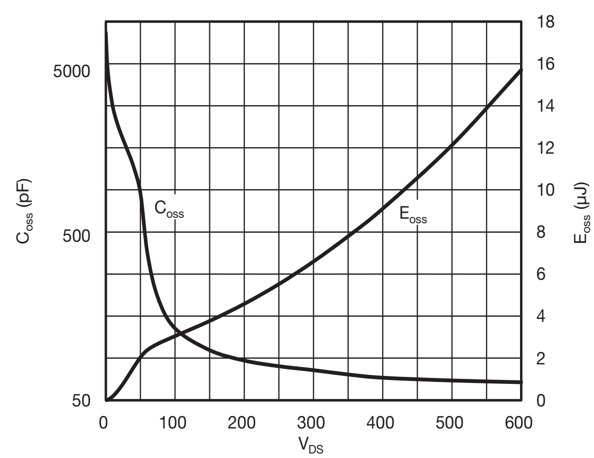


Fig. 6 - C_{OSS} and E_{OSS} vs. V_{DS}

For technical questions, contact: hvm@vishay.com

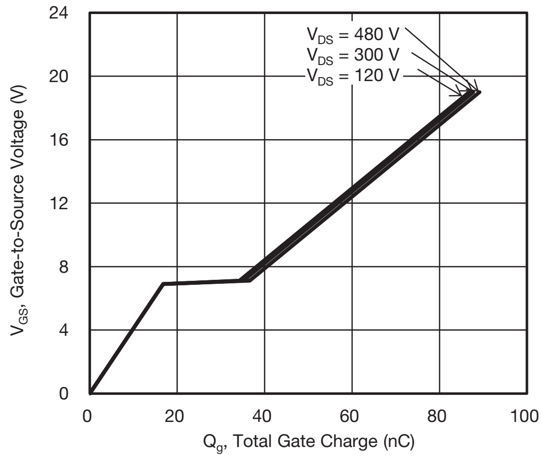


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

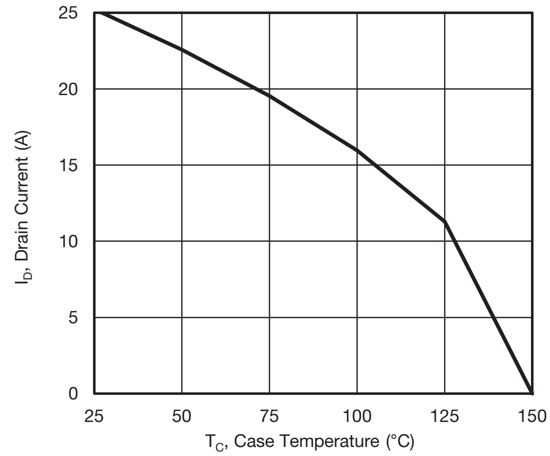


Fig. 10 - Maximum Drain Current vs. Case Temperature

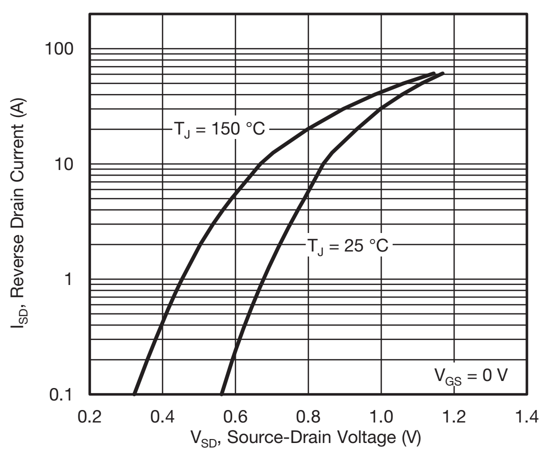


Fig. 8 - Typical Source-Drain Diode Forward Voltage

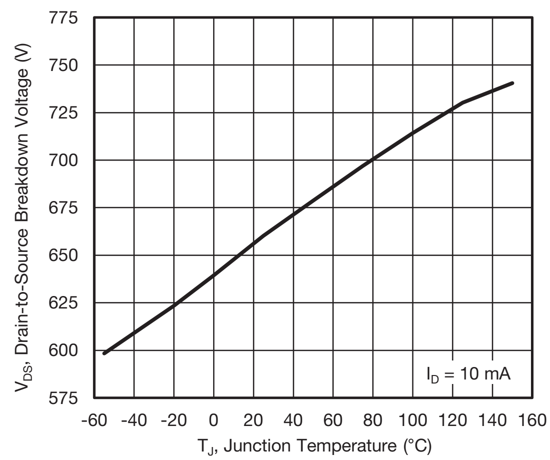
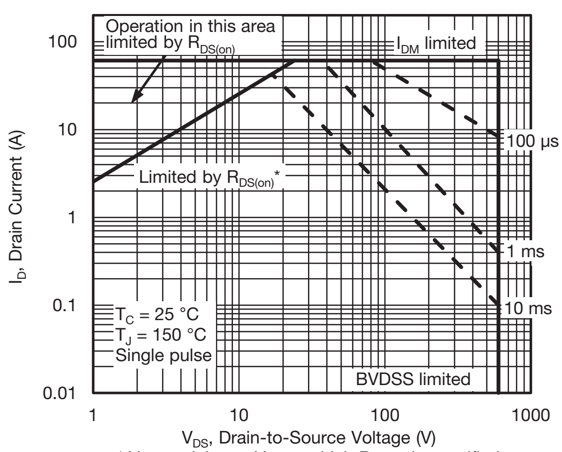


Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Fig. 9 - Maximum Safe Operating Area

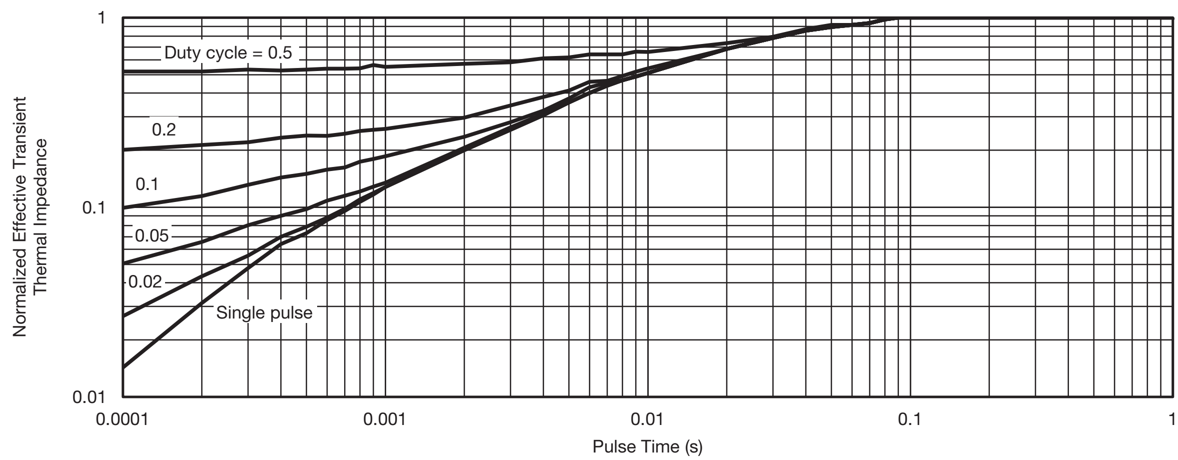


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

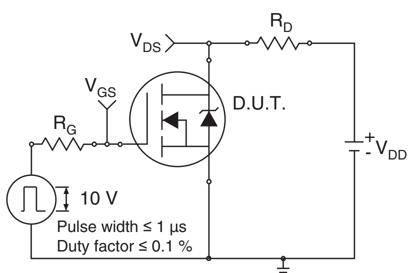


Fig. 13 - Switching Time Test Circuit

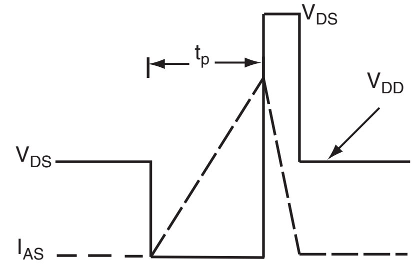


Fig. 16 - Unclamped Inductive Waveforms

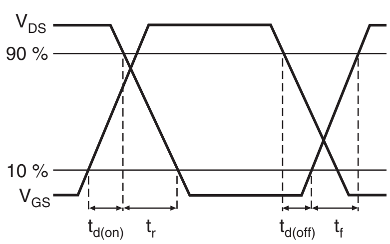


Fig. 14 - Switching Time Waveforms

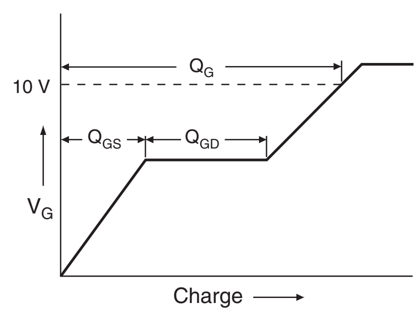


Fig. 17 - Basic Gate Charge Waveform

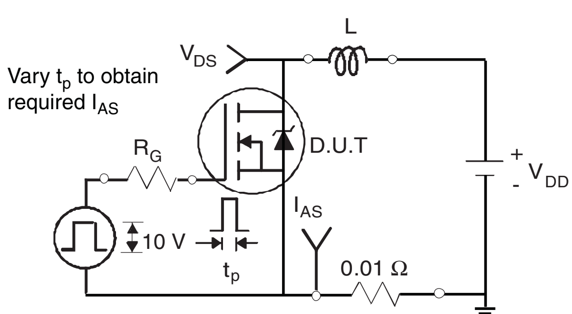


Fig. 15 - Unclamped Inductive Test Circuit

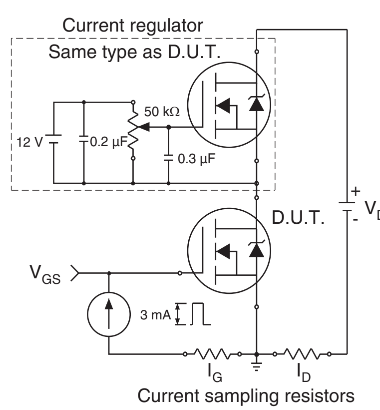
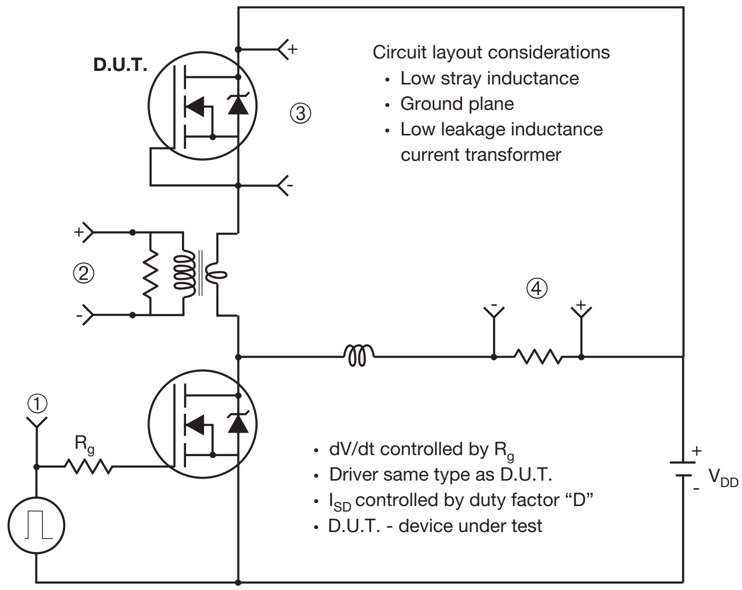
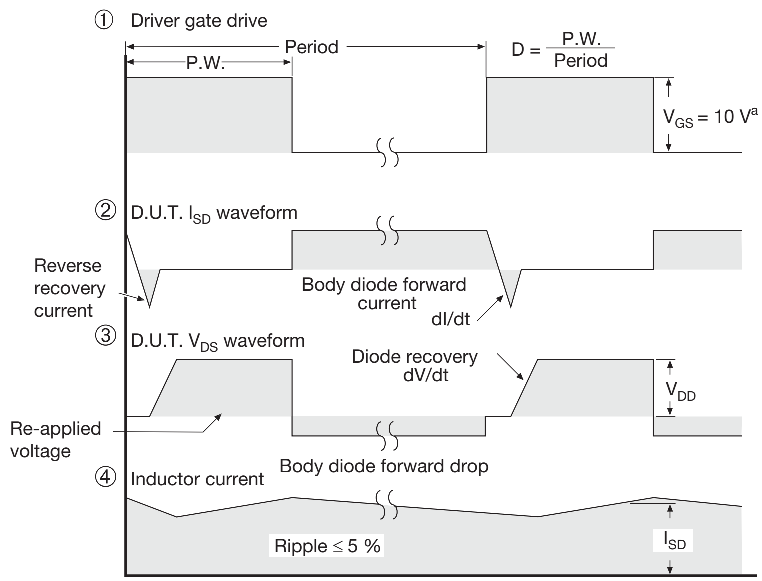


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 19 - For N-Channel

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