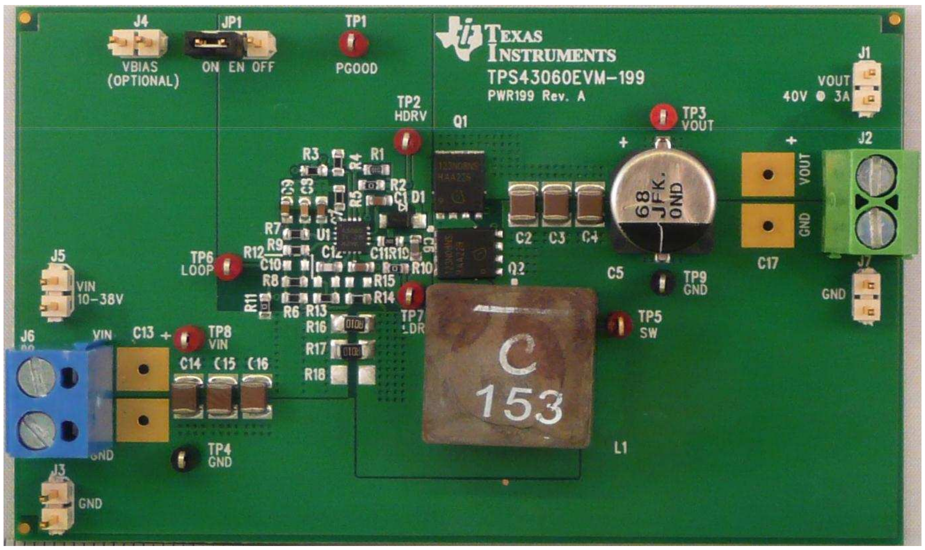
Using the TPS43060 Boost Evaluation Module (EVM)



This user's guide contains information for the TPS43060EVM-199 evaluation module (PWR199) including the performance specifications, schematic, and the bill of materials.

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1 Introduction

This user's guide contains background information for the TPS43060 as well as support documentation for the TPS43060EVM-199 evaluation module (PWR199). Also included are the performance specifications, schematic, and the bill of materials for the EVM.

1.1 Background

The TPS43060 is a DC-DC synchronous boost controller designed for a maximum output voltage of 58 V from an input voltage source of 4.5 V to 38 V. It has a 7.5-V gate-drive supply optimized for use with standard threshold MOSFETs. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the high efficiency and high power possible when designing with the TPS43060 controller. The switching frequency is externally set at a nominal 300 kHz. The gate-drive circuitry for the external high-side and low-side FET is incorporated inside the TPS43060 package. PWR199 uses the Infineon BSC123N08NS3G for both the high-side and low-side MOSFETs. External inductor DCR or resistor current sensing allows for an adjustable cycle-by-cycle current limit. The compensation components are external to the integrated circuit (IC), and an external resistor divider allows for an adjustable output voltage. Additionally, the TPS43060 provides an adjustable undervoltage lockout with hysteresis through an external resistor divider, adjustable slow-start time with an external capacitor and a power good output voltage indicator. The absolute maximum input voltage for the PWR199 is 38 V.

Table 1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS43060EVM-199	V_{IN} = 10 V to 38 V	I_{OUT} = 0 A to 3 A

1.2 Performance Specification Summary

A summary of the EVM performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 24 V and an output voltage of 40 V, unless otherwise specified. This EVM is designed and tested for V_{IN} = 10 V to 38 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS43060EVM-199 Performance Specification Summary

Specification	Test Conditions		MIN	TYP	MAX	Unit
V_{IN} voltage range			10	24	38	V
Output voltage set point				40		V
Output current range	V_{IN} = 15 V to 38 V		0		3	A
Output current range	V_{IN} = 10 V		0		2	A
Line regulation	V_{IN} = 10 V to 35 V, I_{OUT} = 2 A			±0.1%		
Load regulation	I_{OUT} = 0.001 A to 3 A			±0.1%		
Load transient response	I_{OUT} = 0.75 A to 2.25 A	Voltage change		–700		mV
		Recovery time		1		ms
	I_{OUT} = 2.25 A to 0.75 A	Voltage change		600		mV
		Recovery time		1		ms
Loop bandwidth	I_{OUT} = 3 A			4.7		kHz
Phase margin	I_{OUT} = 3 A			64		°
Input voltage ripple	I_{OUT} = 3 A			100		mVpp
Output voltage ripple	I_{OUT} = 3 A			350		mVpp
Output rise time				25		ms
Operating frequency				300		kHz
Peak efficiency	I_{OUT} = 3 A			97.7%		
DCM threshold				660		mA
Pulse skipping threshold				3.5		mA
No load input current				1.3		mA
UVLO start threshold				9.66		V
UVLO stop threshold				7.92		V

1.3 Schematic

Figure 1 is the schematic for the EVM.

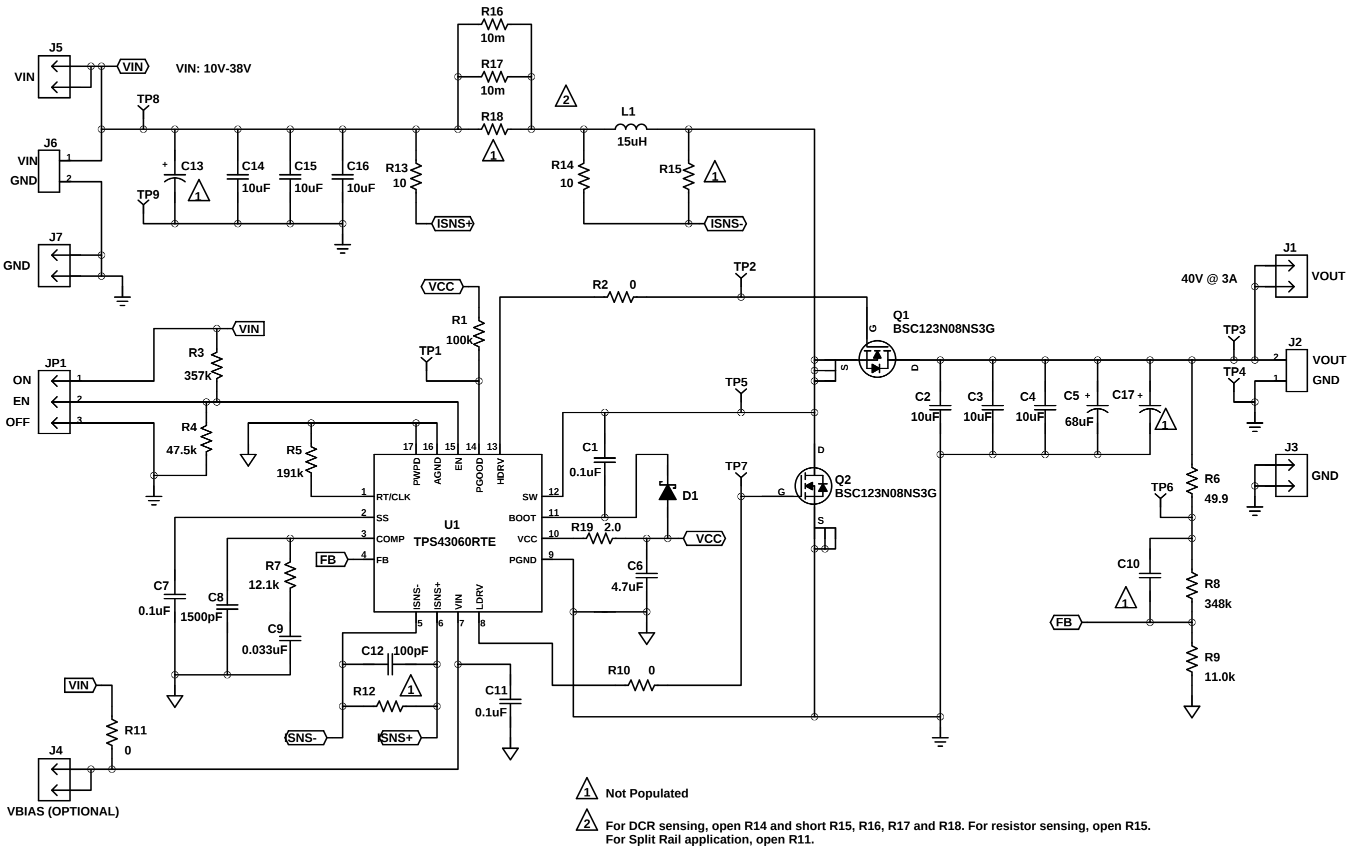


Figure 1. TPS43060EVM-199 Schematic

1.4 Modifications

The EVM is designed to provide access to the features of the TPS43060. Some modifications can be made to this module. For further details please see the product data sheet.

1.4.1 Output Voltage Set Point

To change the output voltage of the EVM, it is necessary to change the value of resistor R8. The value of R8 for a specific output voltage can be calculated using Equation 1, where R_{HS} is R8, R_{LS} is R9 and V_{FB} is 1.22 V. It is recommended to use a value of R9 near 10 kΩ.

$$R_{HS} = R_{LS} \times \frac{V_{OUT} - V_{FB}}{V_{FB}} \tag{1}$$

Note: V_{IN} must be in a range so the minimum on-time is greater than the typical 100 ns and the minimum off-time is greater than the largest of typical 250 ns and 5% of the switching period.

1.4.2 Current Sensing

The default configuration of the EVM is for resistor current sensing. R13 and R14 are populated with R15 open. When adjusting the input voltage, output voltage or desired maximum output voltage, the current sense resistors R16 and R17 may need to be adjusted. The peak inductor current should first be calculated with Equation 2. Equation 3 is then used to calculate the required current sense resistor where $V_{CS}typ$ is the current sense threshold. $V_{CS}typ$ should be determined from the TPS43060 data sheet with the maximum duty cycle in the application. Ensure the current sense resistor is rated for the expected power dissipation. For inductor DCR current sensing, R14 should be left open while R15, R16, R17 and R18 are shorted.

$$I_L peak = \frac{I_{OUT}}{1 - \frac{V_{OUT} - V_{IN} min}{V_{OUT}}} + \frac{V_{IN} min \times \frac{V_{OUT} - V_{IN} min}{V_{OUT}}}{2 \times L \times f_{SW}} \quad (2)$$

$$R_{CS} = \frac{V_{CS} typ}{1.2 \times I_L peak} \quad (3)$$

1.4.3 Slow-Start Time

Adjust the slow-start time by changing the value of C7. Equation 4 can be used to calculate the required capacitance based on a desired slow-start time, t_{SS}. I_{SS} is the charging current of 5-µA typical and V_{REF} is the internal reference voltage of 1.22 V. The EVM is set for a slow-start time of 25 ms using C7 = 0.1 µF.

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{REF}} \quad (4)$$

1.4.4 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R3 and R4. The EVM is set for a start voltage of 9.66 V and stop voltage of 7.92 V, using R3 = 357 kΩ and R4 = 47.5 kΩ. Use Equation 5 and Equation 6 to calculate the required resistor values for R3 and R4, respectively, for different start and stop voltages. The typical values of the constants in the two equations are as follows: V_{EN_DIS} = 1.14 V, V_{EN_ON} = 1.21 V, I_{EN_pup} = 1.8 µA, and I_{EN_hys} = 3.2 µA.

$$R_{UVLO\_H} = \frac{V_{START} \times \left(\frac{V_{EN\_DIS}}{V_{EN\_ON}}\right) - V_{STOP}}{I_{EN\_pup} \times \left(1 - \frac{V_{EN\_DIS}}{V_{EN\_ON}}\right) + I_{EN\_hys}} \quad (5)$$

$$R_{UVLO\_L} = \frac{R_{UVLO\_H} \times V_{EN\_DIS}}{V_{STOP} - V_{EN\_DIS} + R_{UVLO\_H} \times \left(I_{EN\_pup} + I_{EN\_hys}\right)} \quad (6)$$

1.4.5 Input Voltage Rails

The EVM is designed to accommodate different input voltage levels for the power stage and control logic. In the default configuration, the VIN inputs connected with R11 populated with a 0-Ω resistor. The input voltage is supplied to J6. If desired, the two input voltage rails may be separated by unpopulating R11. The control logic input voltage can be supplied to J4 and the power stage input voltage to J6.

1.4.6 Further Modification

Changing the input and output of conditions of the EVM will impact the design. It may also be necessary to modify the inductor, output capacitor and compensation components for the desired performance in the application. Please see the data sheet or the excel design spreadsheet located in the product folder for details.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the EVM. The section also includes test results typical for the EVM covering efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, start up and shutdown.

2.1 Input/Output Connections

This EVM includes I/O connectors and test points as shown in Table 3. A power supply capable of supplying at least 12 A must be connected to J6 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load-current capability must be 3 A. Wire lengths must be minimized to reduce losses in the wires. If any modification is done to the EVM design, an input supply and load rated for the new design are required. Test point TP8 provides a connection to monitor the V_{IN} input voltages with TP9 providing a convenient ground reference. TP3 is used to monitor the output voltage with TP4 as the ground reference.

Table 3. EVM Connectors and Test points

Reference Designator	Function
J1	2-pin header for V_{OUT} voltage connections
J2	V_{OUT}, 40 V at 3-A maximum
J3	2-pin header for GND connections
J4	2-pin header for optional V_{BIAS} input voltage connections (see Section 1.4.5)
J5	2-pin header for V_{IN} input voltage connections
J6	V_{IN} (see Table 1 for V_{IN} range)
J7	2-pin header for GND connections
JP1	3-pin header for EN jumper. Install jumper from pins 1-2 to enable or pins 2-3 to disable.
TP1	PGOOD test point for power good output voltage indicator
TP2	HDRV test point for high-side gate-drive voltage
TP3	V_{OUT} test point at V_{OUT} connector
TP4	GND test point at V_{OUT} connector
TP5	SW test point for switch node voltage
TP6	Test point between voltage divider network and output used for loop response measurements
TP7	LDRV test point for low-side gate-drive voltage
TP8	V_{IN} test point at V_{IN} connector
TP9	GND test point at $V_{IN\ connector}$

2.2 Efficiency

With the nominal V_{IN} of 24 V, the efficiency of this EVM peaks at a load current of about 3 A, and then decreases as the load current increases towards maximum load. Figure 2 shows the efficiency for the EVM up to current limit with 1-V input and up to a 5-A load with 24-V and 38-V input. Figure 3 shows the light load efficiency using a semi-log scale. Measurements are taken at ambient temperature of 25°C. The efficiency may be lower at higher ambient temperatures due to temperature variation in the drain-to-source resistance of the selected external MOSFETs.

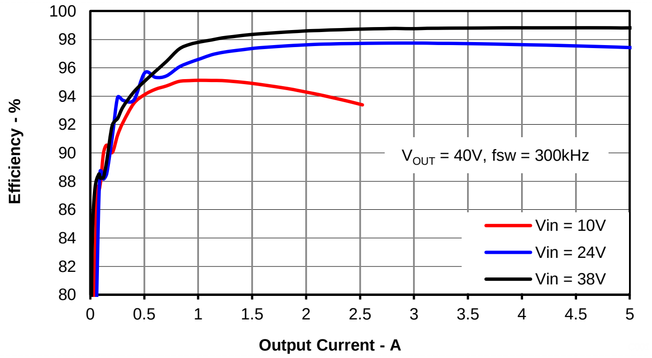


Figure 2. Efficiency Versus Load Current

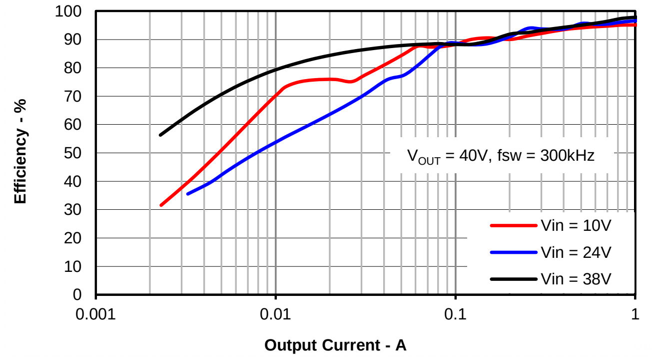


Figure 3. Light Load Efficiency Versus Load Current

2.3 Output Voltage Regulation

The load regulation for the EVM is shown in Figure 4. The line regulation for the EVM is shown in Figure 5. Measurements are given for an ambient temperature of 25°C.

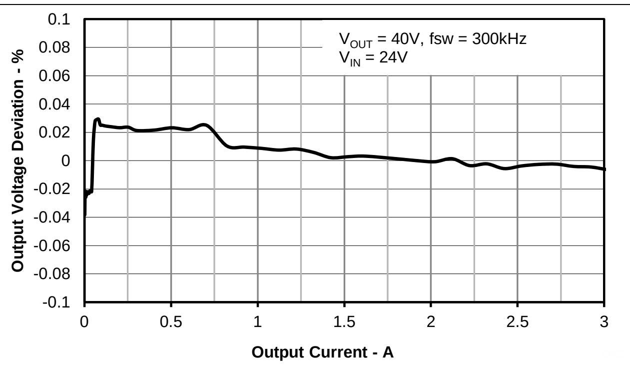


Figure 4. Regulation Versus Output Current

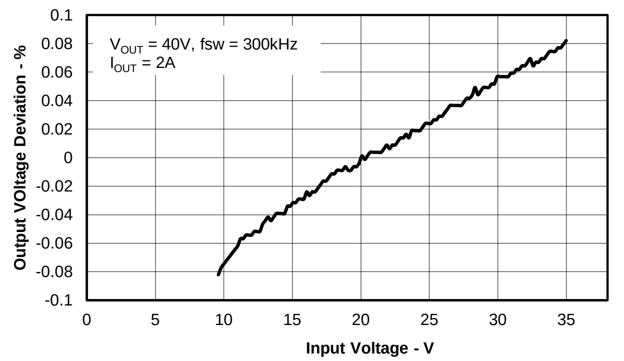
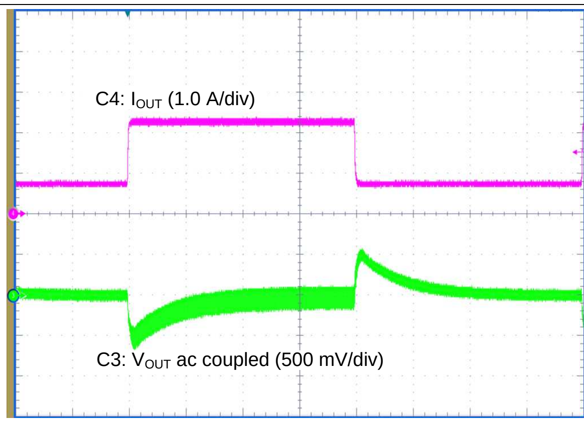


Figure 5. Regulation Versus Input Voltage

2.4 Load Transients and Loop Response

The EVM response to load transients is shown in Figure 6. The current step is from 25% to 75% of maximum rated load at nominal 24-V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output. The EVM loop-response characteristics are shown in Figure 7. Gain and phase plots are shown for nominal V_{IN} voltage of 24 V. Load current for the measurement is 3 A.



Time: 500 µs/div

Figure 6. Load Transient Response

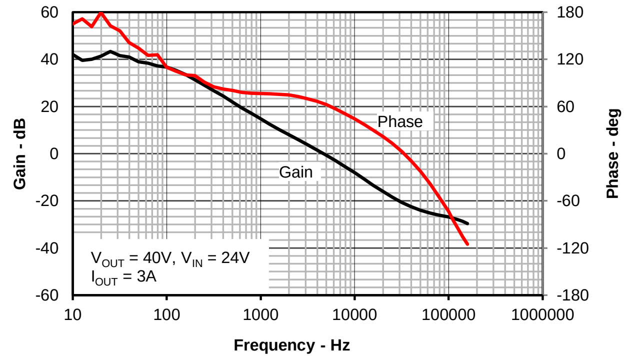
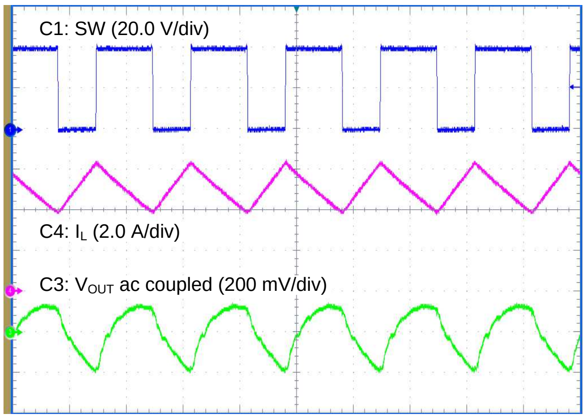


Figure 7. Loop Response

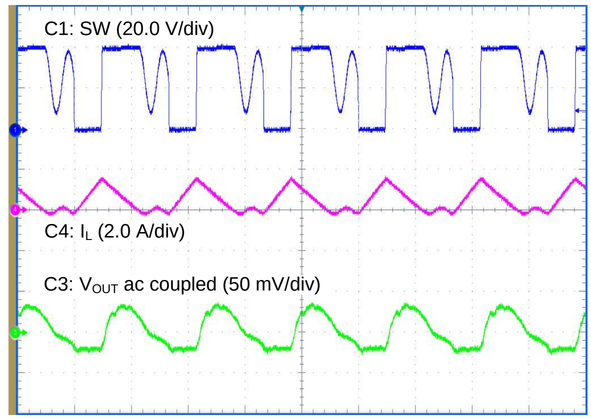
2.5 Output Voltage Ripple

The EVM continuous conduction mode (CCM) output voltage ripple is shown in Figure 8. The output current is the rated full load of 3 A and nominal V_{IN} of 24 V. The voltage ripple is measured directly across the output capacitors with a short ground lead. The discontinuous conduction mode (DCM) output voltage ripple is shown in Figure 9. The output current is 0.3 A and nominal V_{IN} of 24 V. The pulse skip mode output voltage ripple is shown in Figure 10. There is no external load on the output and nominal V_{IN} of 24 V.



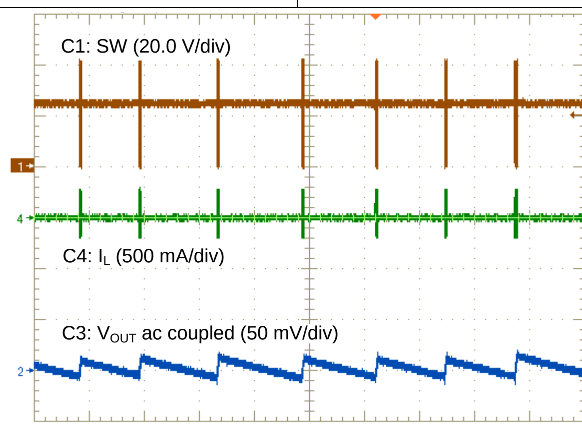
Time: 2.0 µs/div

Figure 8. Output Voltage Ripple CCM



Time: 2.0 µs/div

Figure 9. Output Voltage Ripple DCM



Time: 10.0 ms/div

Figure 10. Output Voltage Ripple Pulse Skip Mode

2.6 Input Voltage Ripple

The EVM CCM input voltage ripple is shown in Figure 11. The output current is the rated full load of 3 A and nominal V_{IN} of 24 V. The voltage ripple is measured directly across the input capacitors. The DCM input voltage ripple is shown in Figure 12. The output current is 0.3 A and nominal V_{IN} of 24 V.

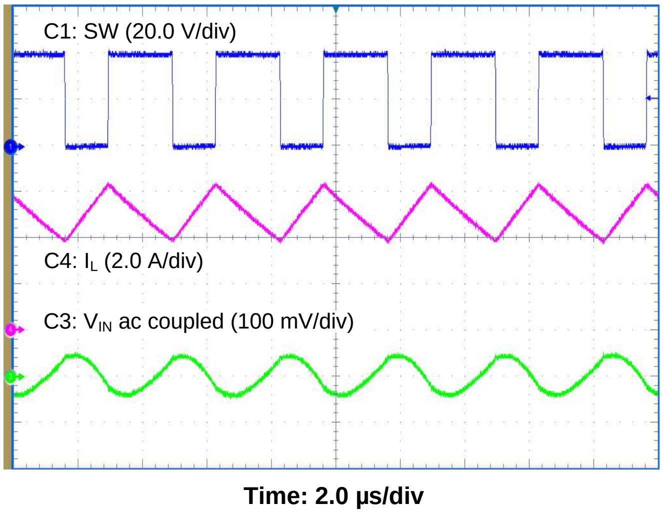


Figure 11. Input Voltage Ripple CCM

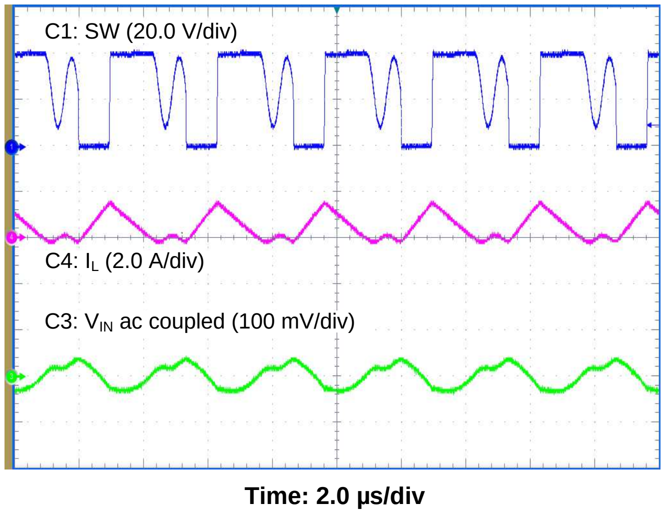


Figure 12. Input Voltage Ripple DCM

2.7 Start Up

The start up waveforms are shown in Figure 13 and Figure 14. The input voltage for these plots is the nominal 24 V and the output has a 2.5-A resistive load. In Figure 13 the input voltage supply is turned on and V_{IN} begins rising. Both the V_{CC} and V_{OUT} rail initially rise with V_{IN}. When the input reaches the undervoltage lockout threshold set by the external resistor divider, the device can begin switching and the output ramps up to the set value of 40 V with the slow-start voltage. PGOOD goes high when V_{OUT} is in regulation.

In Figure 14 the input voltage is applied with EN held low. The output voltage is a diode drop below the input voltage and V_{CC} is disabled. When EN is released, the start up sequence begins with V_{CC} coming into regulation and the output ramps up to the set value of 40 V. PGOOD goes high when V_{OUT} is in regulation.

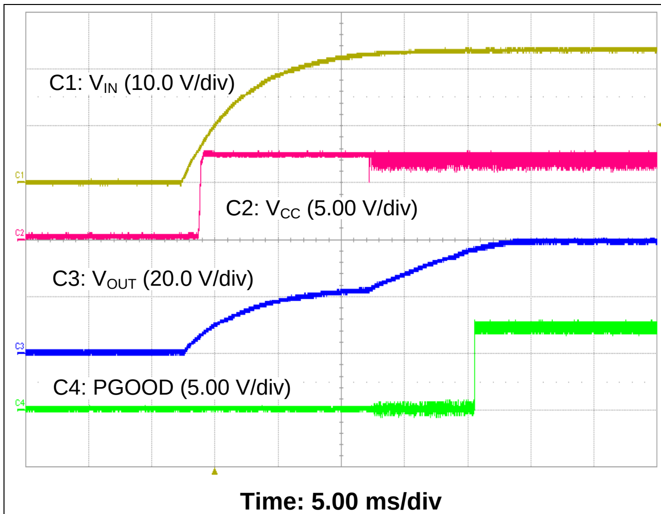


Figure 13. Start Up Relative to V_{IN}

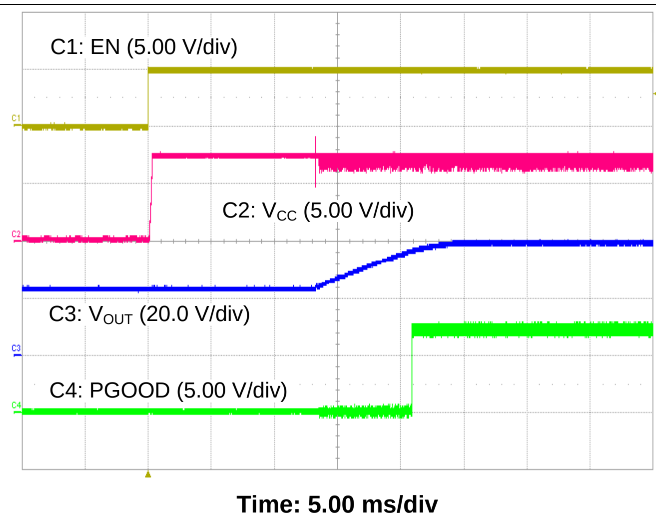


Figure 14. Start Up Relative to EN

2.8 Shutdown

The shutdown waveforms are shown in Figure 15 and Figure 16. In Figure 15 the input voltage is removed, and when the input falls below the undervoltage lockout threshold set by the EN resistor divider, the TPS43060 shuts down, PGOOD is pulled low and the output falls to ground. The output has a 2.5-A resistive load.

In Figure 16 the input voltage is held at 24 V with no load and EN is shorted to ground. When EN is grounded, the TPS43060 is disabled, PGOOD is pulled low and the output voltage discharges to V_{IN}.

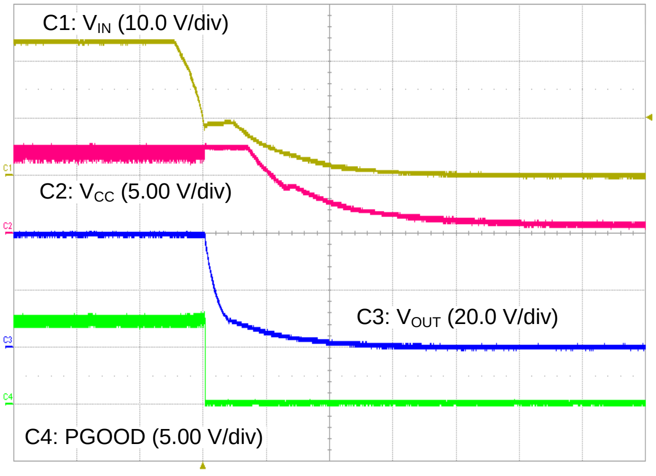


Figure 15. Shutdown Relative to V_{IN}

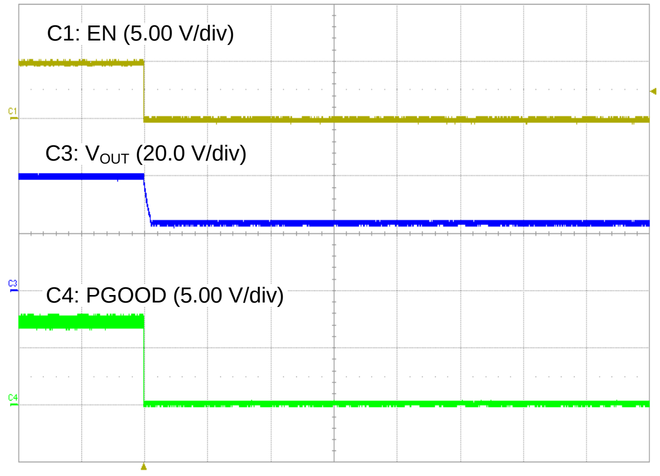


Figure 16. Shutdown Relative to EN

2.9 Gate-Drive Signals

In Figure 17 the gate-drive signals for the high-side and low-side FETs can be seen with the switching node are shown. The input voltage is 24 V and the output has a 3-A load.

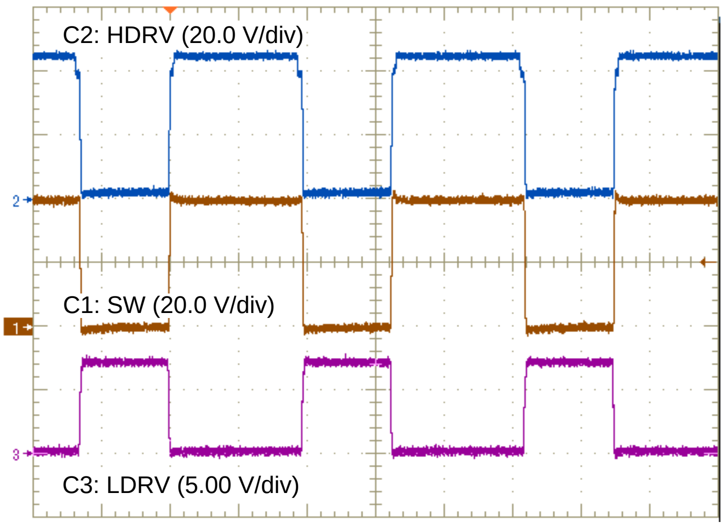


Figure 17. Gate-Drive Signals

3 Bill of Materials

Table 4 presents the bill of materials for the EVM.

Table 4. TPS43060EVM-199 Bill of Materials

COUNT	RefDes	Value	Description	Size	Part Number	MFR
1	C5	68µF	Capacitor, Aluminum, 63V, 20%	0.406 x 0.406 inch	EEVFK1J680P	Panasonic
1	C6	4.7µF	Capacitor, Ceramic, 16V, X5R, 10%	0603	STD	STD
1	C8	1200pF	Capacitor, Ceramic, 10V, X5R, 10%	0603	STD	STD
1	C9	0.022µF	Capacitor, Ceramic, 10V, X5R, 10%	0603	STD	STD
0	C10	Open	Capacitor, Ceramic, 10V, X7R, 10%	0603	STD	STD
1	C12	100pF	Capacitor, Ceramic, 50V, X7R, 20%	0603	STD	STD
3	C1 C7 C11	0.1µF	Capacitor, Ceramic, 50V, X7R, 10%	0603	STD	STD
5	C2-4 C14-16	10µF	Capacitor, Ceramic, 50V, X7R, 10%	1210	STD	STD
0	C13 C17	Open	Capacitor	Multi sizes	Engineering Only	STD
1	D1	MBR1H100SFT3G	Diode, Schottky Power Rectifier, 1A, 100V	SOD-123LF	MBR1H100SFT3G	On Semi
5	J1 J3-5 J7	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
2	J2 J6	ED120/2DS	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35 inch	ED120/2DS	OST
1	JP1	PEC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
1	L1	15µH	Inductor, Shielded Power, 14A, 9mΩ	15.2x16.2 mm	XAL1510-153 alt:74435571500	Coilcraft alt:WE
2	Q1 Q2	BSC123N08NS3G	MOSFET, Nch, 80V, 55A, 12.3mΩ	TDSON-8	BSC123N08NS3G	Infineon
1	R1	100k	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R3	357k	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R4	47.5k	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R5	191k	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R6	49.9	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R7	15.4k	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R8	348k	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R9	11.0k	Resistor, Chip, 1/16W, 1%	0603	STD	STD
0	R18	Open	Resistor, Chip, 1W, 1%	1206	STD	STD
0	R12 R15	Open	Resistor, Chip, 1/16W, 1%	0603	STD	STD
2	R13-14	10	Resistor, Chip, 1/16W, 1%	0603	STD	STD
2	R16-17	10m	Resistor, Chip, 1W, 1%	1206	STD	STD
3	R2 R10-11	0	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	SH1		Short jumper, 100mil	0.100 inch	929950-00	3M
2	TP4 TP9	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
7	TP1-3 TP5-8	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
1	U1	TPS43060RTE	IC, Wide VIN Current Mode Synchronous Boost Controller	VQFN	TPS43060RTE	TI
1	--		PCB, 3.5 in x 2.1 in x 0.062 in		PWR199	Any
Notes:	1. These assemblies are ESD sensitive, ESD precautions shall be observed.					
	2. These assemblies must be clean and free from flux and all contaminants.					
	Use of no clean flux is not acceptable.					
	3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.					
	4. Ref designators marked with an asterisk ('**') cannot be substituted.					
	All other components can be substituted with equivalent MFG's components.					

4 Board Layout

This section provides a description of the EVM, board layout, and layer illustrations.

4.1 Layout

The board layout for the EVM is shown in Figure 18 through Figure 22. This design has 4 layers of 2-oz copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and SW. Also on the top layer are all other components to allow the user to easily view, probe, and evaluate the TPS43060 control IC. The remaining area is filled with ground. The remaining three layers have additional copper for VIN, VOUT, AGND, and PGND connected with multiple vias. Additional copper is also connected to the sense resistor to aid with thermal dissipation. The second internal layer and bottom layer contain signal routes. Four vias directly under the TPS43060 device provide a thermal path from the top-side ground plane to the bottom-side and internal AGND plane. Lastly, the layout guidelines should be followed for Q1 and Q2. Vias are placed near both FETs to aid with thermal dissipation.

All noise-sensitive analog circuitry are placed as close as possible to the IC. The voltage divider network ties to the output voltage at the point of regulation on the bottom layer, near the output capacitors. Q1 and Q2 are placed as close as possible to the IC to keep the gate-drive traces as short as possible. The output capacitors are placed next to Q1 and Q2 to limit the length of the high frequency switching current path. The SW copper is kept as small as possible to limit radiated noise from the high-frequency switching voltage node. The power pad is connected to the AGND pin and all noise-sensitive circuitry must use this as the ground return path. The ground return for the power components are connected to the PGND pin. The AGND and PGND are connected at one point near the PGND pin. The bypass capacitors for VIN and VCC are placed next to their respective pins. The filter capacitor between ISNS+ and ISNS– is located next to the pins to help filter out switching noise. An additional input bulk capacitor may be required (C13) depending on the connection to the EVM from the input supply. See the product datasheet for all layout recommendations.

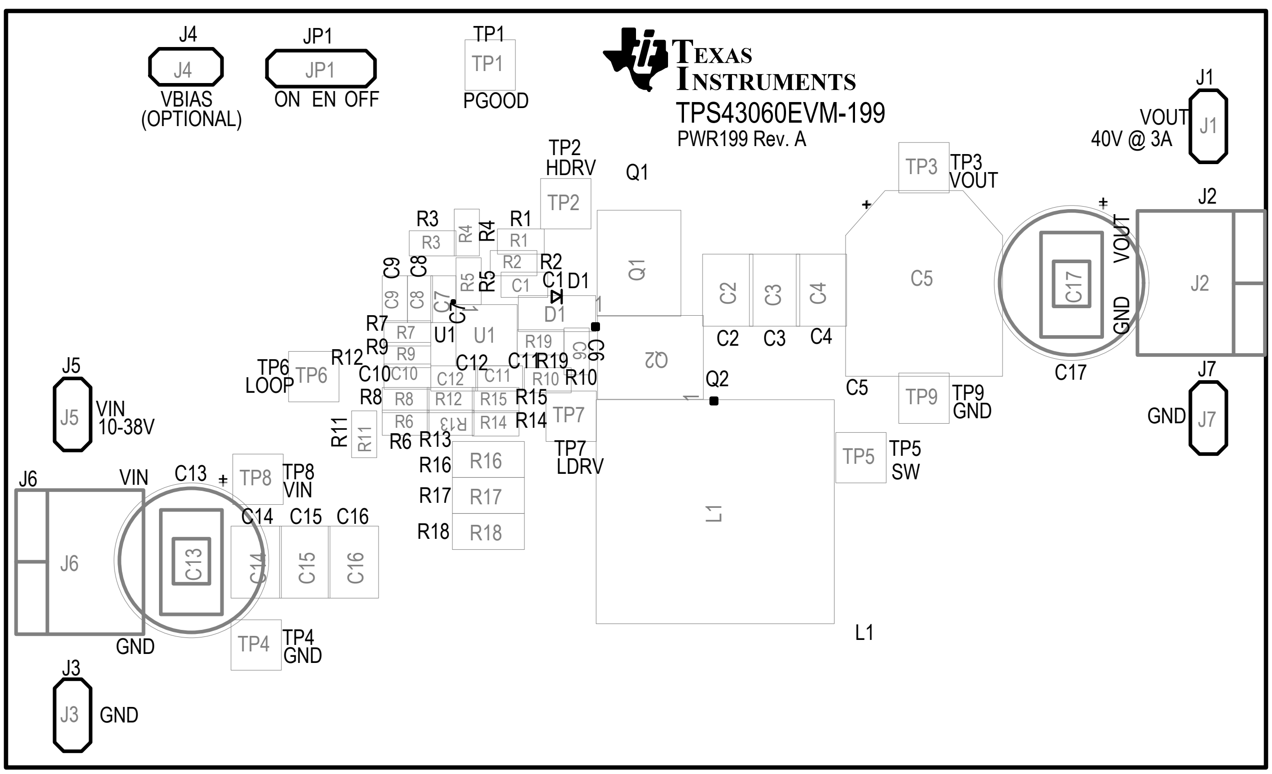


Figure 18. TPS43060EVM-199 Top Assembly and Silkscreen

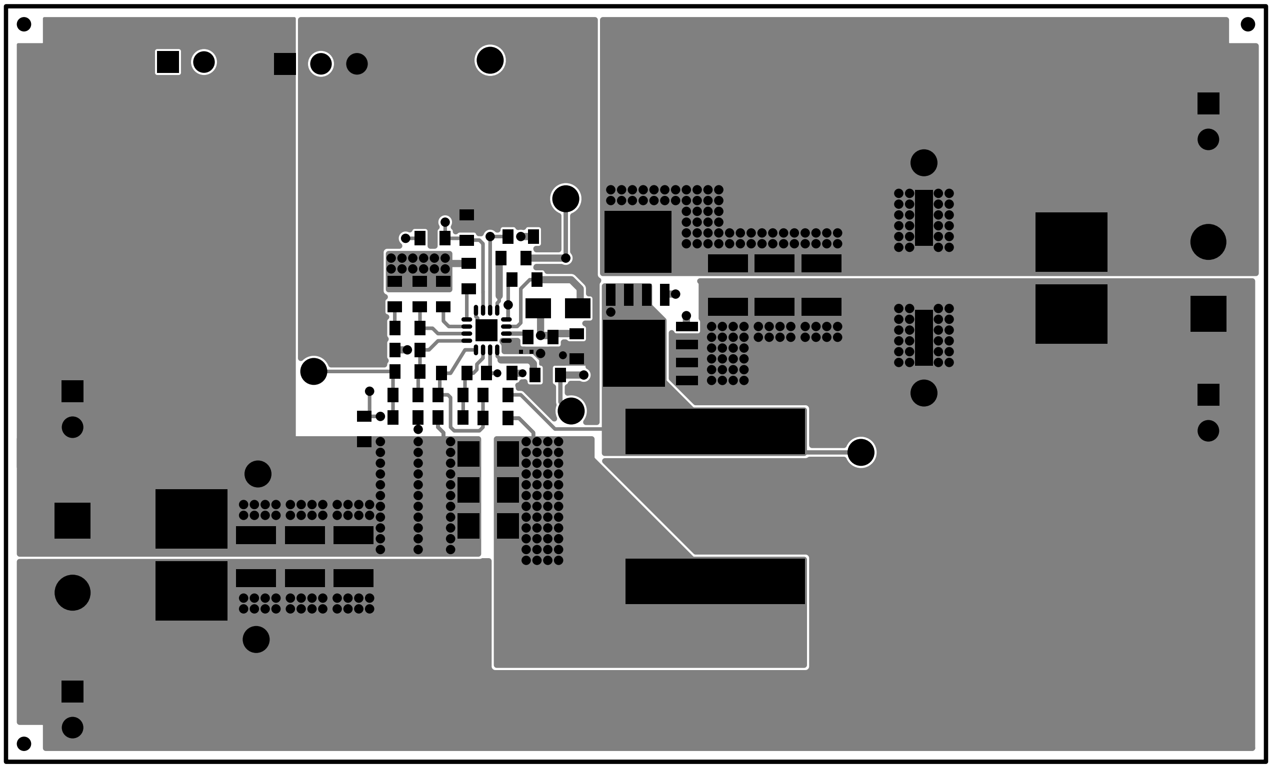


Figure 19. TPS43060EVM-199 Top-Side Layout

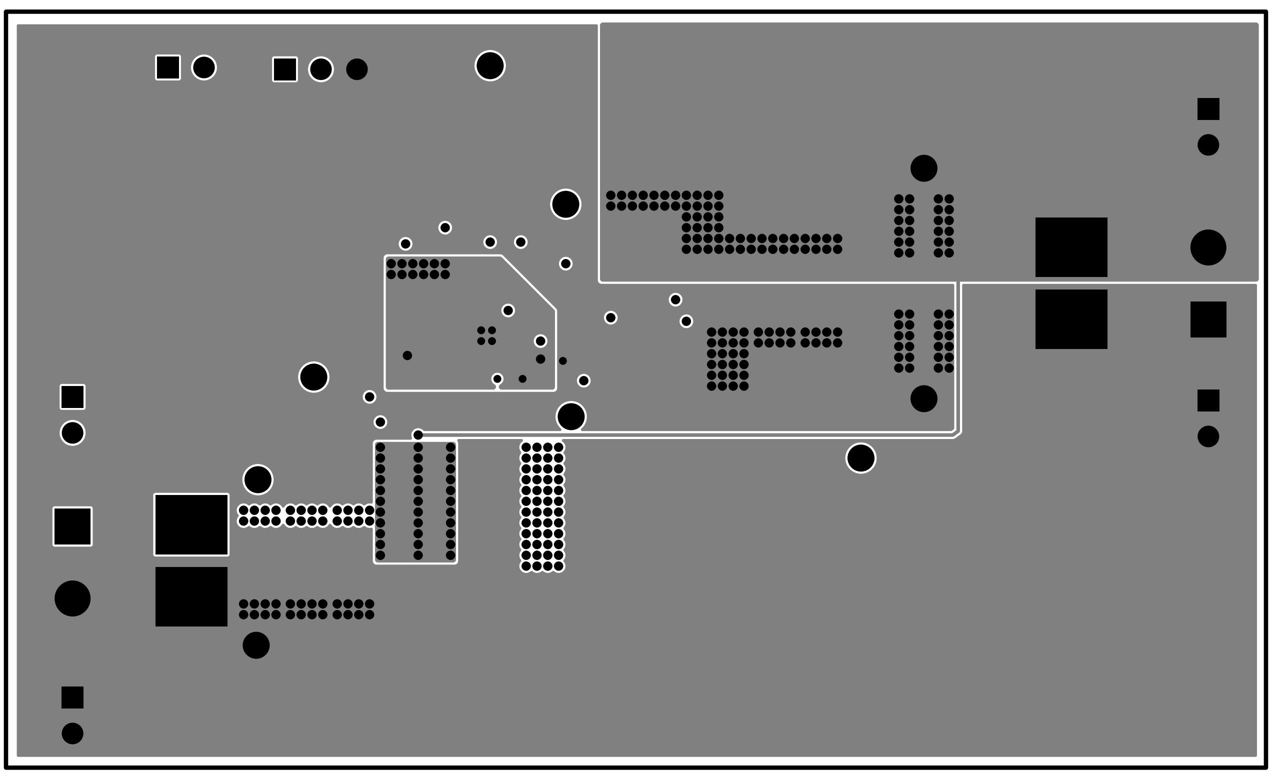


Figure 20. TPS43060EVM-199 Layer 2 Layout

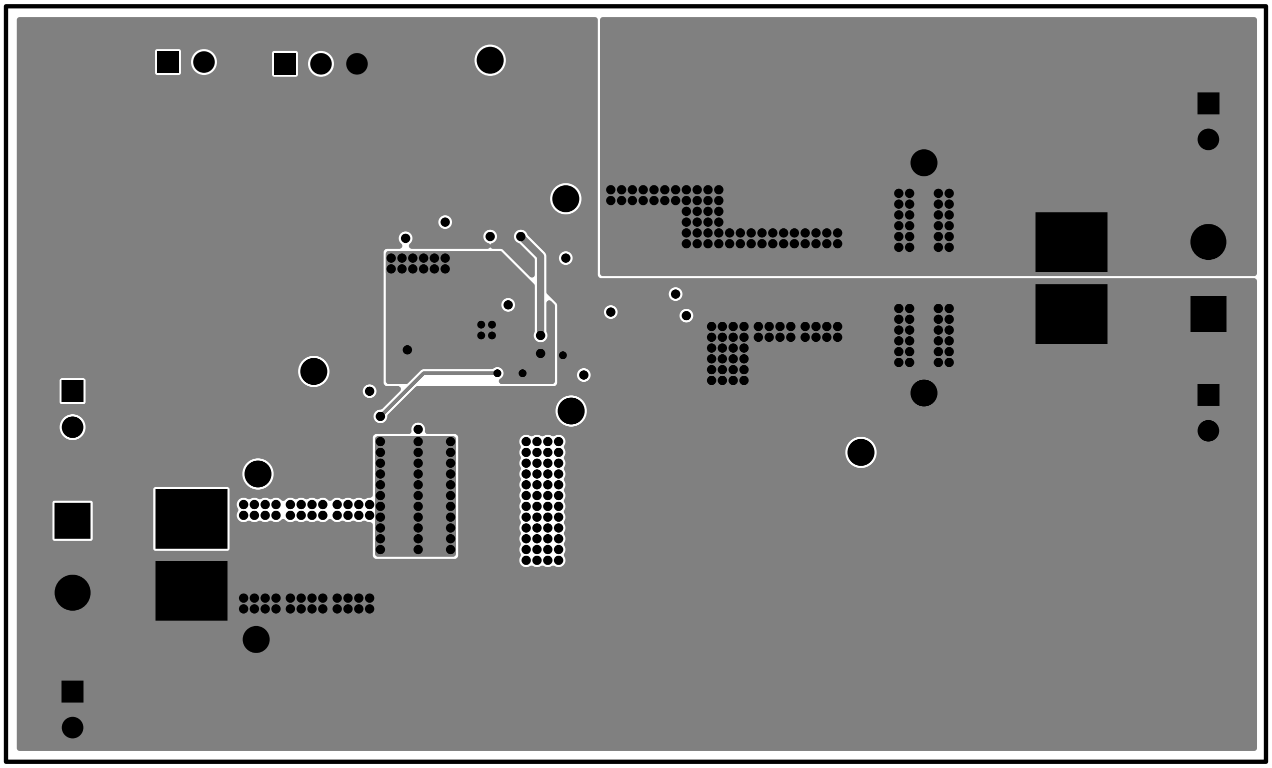


Figure 21. TPS43060EVM-199 Layer 3 Layout

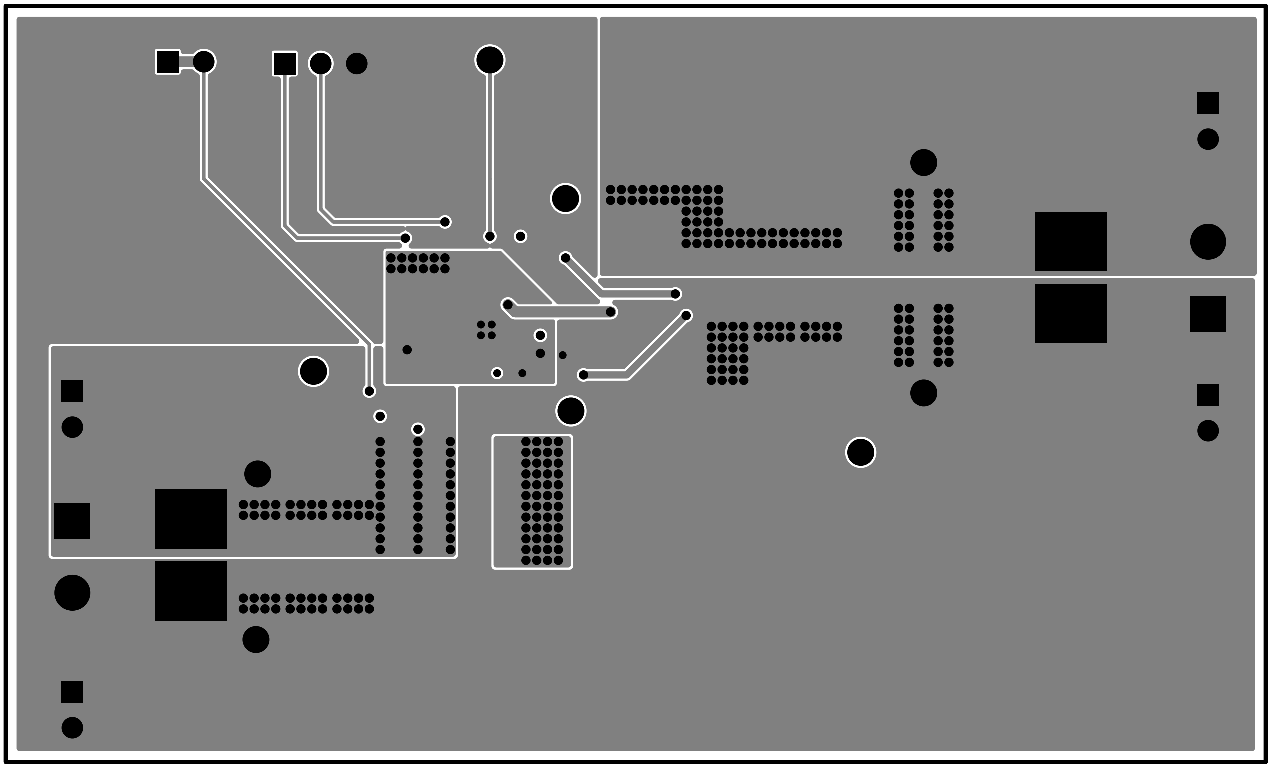


Figure 22. TPS43060EVM-199 Bottom-Side Layout

4.2 Estimated Circuit Area

The estimated printed-circuit-board area by outlining the components and the routing between them is 1.86 in^2 (1202 mm^2). This area does not include test points or connectors. Also note, this design uses 0603 components for easy modifications and places all components on one layer so the area can be reduced.

Revision History

Changes from Original (January 2013) to A Revision	Page
• Changed Table 4, L1 Part Number From: XAL1510-103 To: XAL1510-153	13

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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U.S. Federal Communications Commission Compliance

For EVMs Annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at its own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

For EVMs Annotated as IC – INDUSTRY CANADA Compliant:

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs Including Detachable Antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Canada Industry Canada Compliance (French)

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry’s Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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