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FDMA86108LZ

Single N-Channel PowerTrench® MOSFET

100 V, 2.2 A, 243 mΩ

Features

- Max $r_{DS(on)}$ = 243 mΩ at $V_{GS} = 10$ V, $I_D = 2.2$ A
- Max $r_{DS(on)}$ = 366 mΩ at $V_{GS} = 4.5$ V, $I_D = 1.8$ A
- Low Profile - 0.8 mm Maximum in the New Package MicroFET 2x2 mm
- Free from Halogenated Compounds and Antimony Oxides
- RoHS Compliant

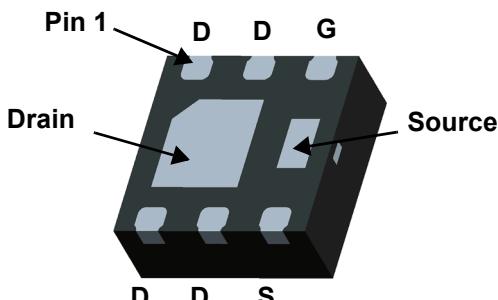


General Description

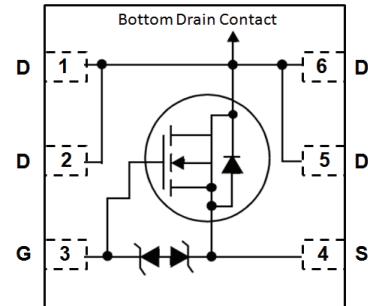
This device has been designed to provide maximum efficiency and thermal performance for synchronous buck converters. The low $r_{DS(on)}$ and gate charge provide excellent switching performance.

Application

- DC – DC Buck Converters



MicroFET 2X2 (Bottom View)



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous $T_A = 25$ °C	2.2	A
	-Pulsed	6	
P_D	Power Dissipation $T_A = 25$ °C	2.4	W
	Power Dissipation $T_A = 25$ °C	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	145	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
108	FDMA86108LZ	MicroFET 2X2	7 "	8 mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100			V
$\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		74		$\text{mV/}^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			± 10	μA

On Characteristics

$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	1.0	2.2	3.0	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		-5		$\text{mV/}^\circ\text{C}$
$r_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 2.2 \text{ A}$		188	243	$\text{m}\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 1.8 \text{ A}$		275	366	
		$V_{GS} = 10 \text{ V}, I_D = 2.2 \text{ A}, T_J = 125^\circ\text{C}$		345	446	
g_{FS}	Forward Transconductance	$V_{DD} = 5 \text{ V}, I_D = 2.2 \text{ A}$		3.7		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		116	163	pF
C_{oss}	Output Capacitance			23	35	pF
C_{rss}	Reverse Transfer Capacitance			1	5	pF
R_g	Gate Resistance		0.1	1.0	3.0	Ω

Switching Characteristics

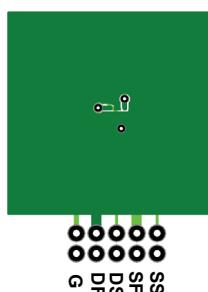
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, I_D = 2.2 \text{ A}, V_{GS} = 10 \text{ V}, R_{\text{GEN}} = 6 \Omega$		4.2	10	ns
t_r	Rise Time			1.7	10	ns
$t_{d(off)}$	Turn-Off Delay Time			7.6	15	ns
t_f	Fall Time			1.7	10	ns
$Q_{g(\text{TOT})}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}$		2.1	3.0	nC
$Q_{g(\text{TOT})}$	Total Gate Charge		$V_{GS} = 0 \text{ V to } 4.5 \text{ V}$	$V_{DD} = 50 \text{ V}, I_D = 2.2 \text{ A}$	1.1	nC
Q_{gs}	Gate to Source Charge			0.5		nC
Q_{gd}	Gate to Drain "Miller" Charge			0.5		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.2 \text{ A}$ (Note 2)		0.9	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 2.2 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		32	51	ns
Q_{rr}	Reverse Recovery Charge				20	32

NOTES:

1. R_{fJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{fJC} is guaranteed by design while R_{fJA} is determined by the user's board design.



a. 52 °C/W when mounted on a 1 in² pad of 2 oz copper.

b. 145 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. Pulse Id measured at 250 μs , refer to Fig 11 SOA graph for more details.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

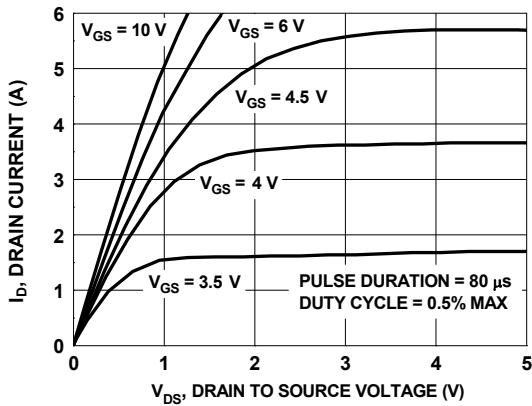


Figure 1. On Region Characteristics

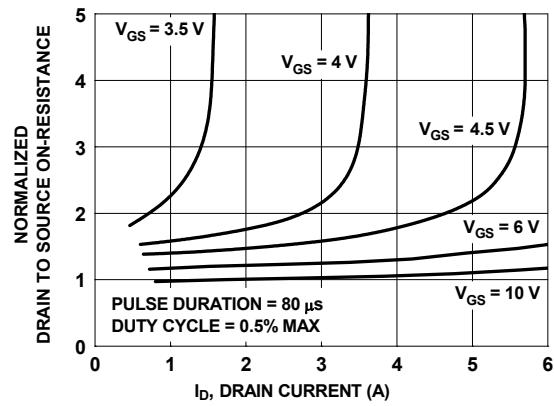


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

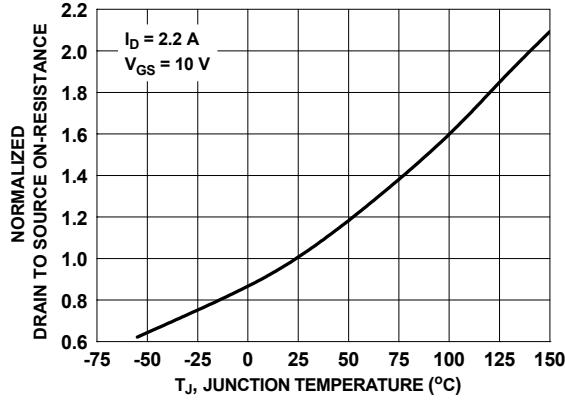


Figure 3. Normalized On Resistance vs. Junction Temperature

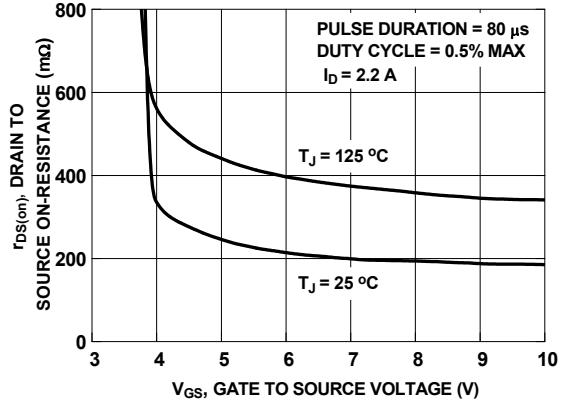


Figure 4. On-Resistance vs. Gate to Source Voltage

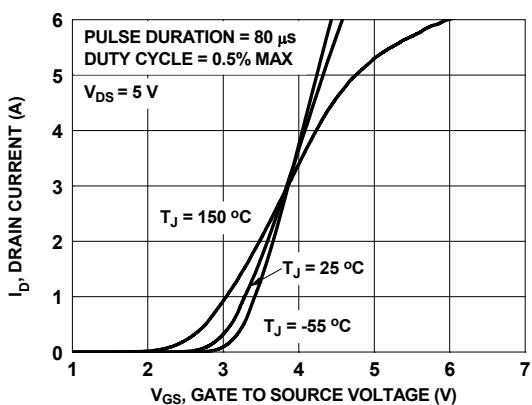


Figure 5. Transfer Characteristics

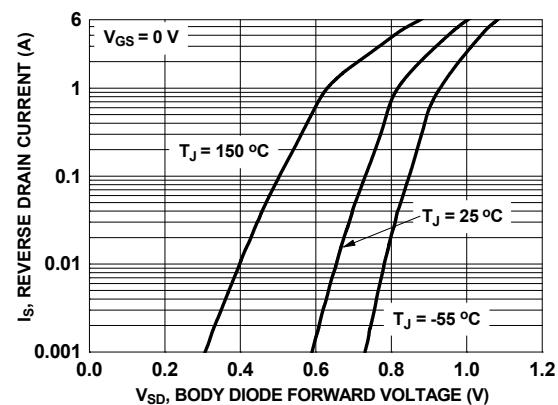


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

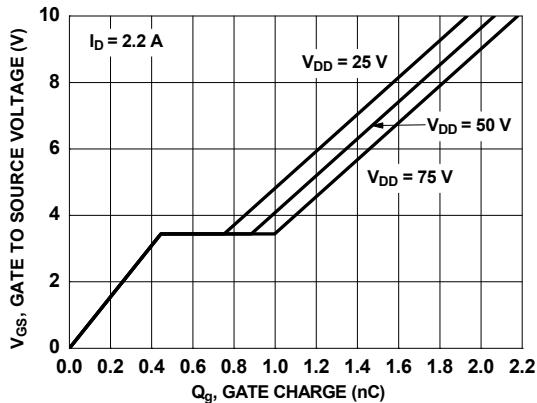


Figure 7. Gate Charge Characteristics

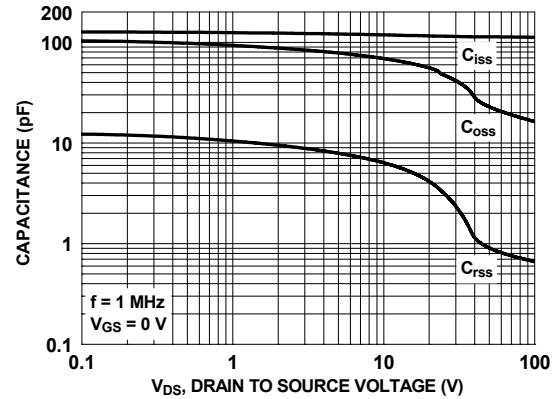


Figure 8. Capacitance vs. Drain to Source Voltage

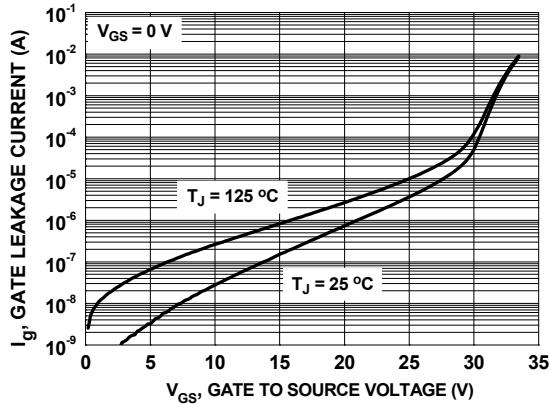


Figure 9. Gate Leakage Current vs. Gate to Source Voltage

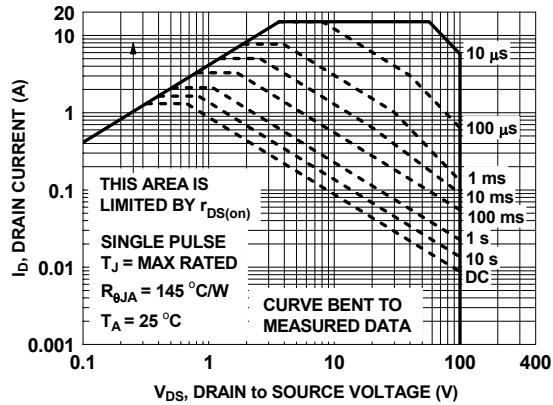


Figure 10. Forward Bias Safe Operating Area

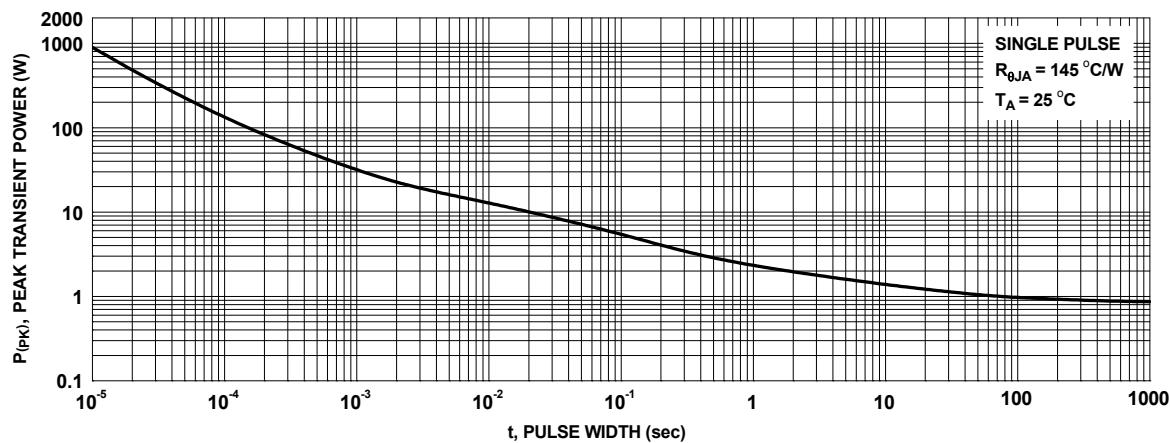


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

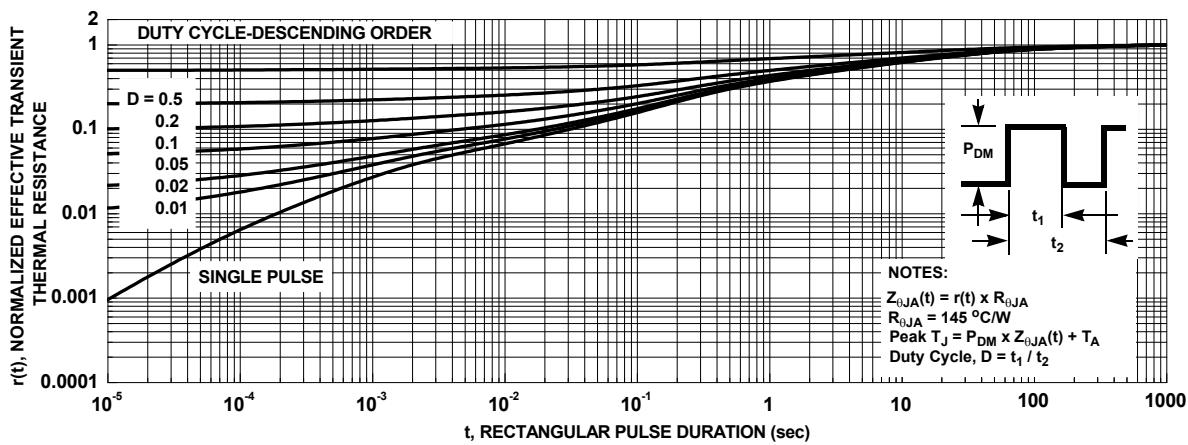
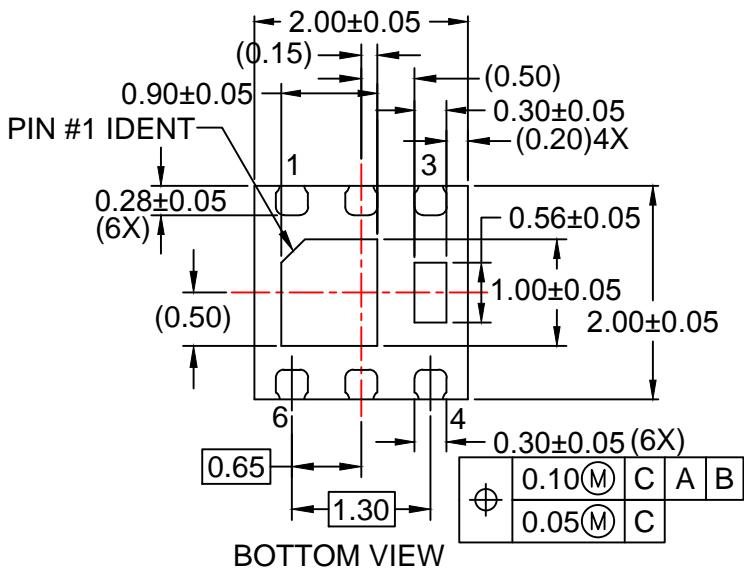
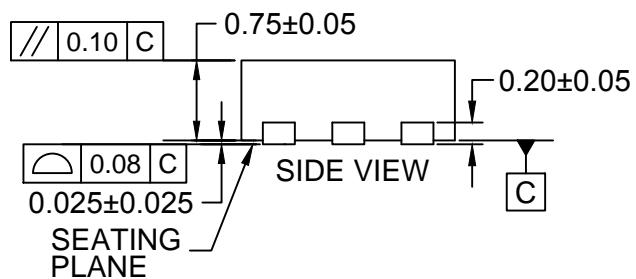
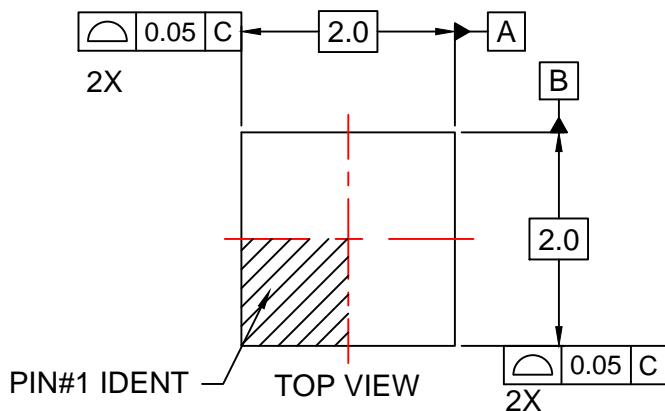
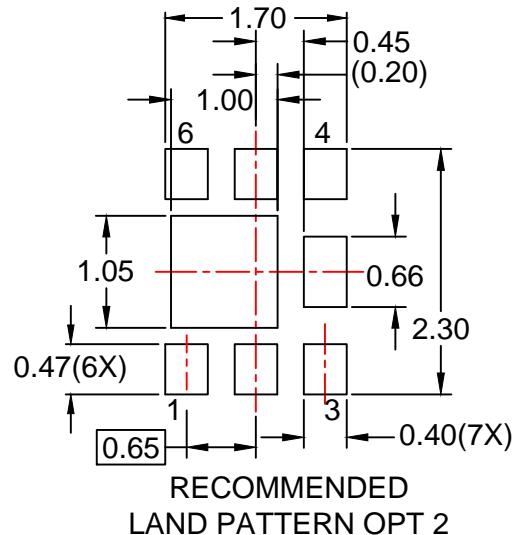
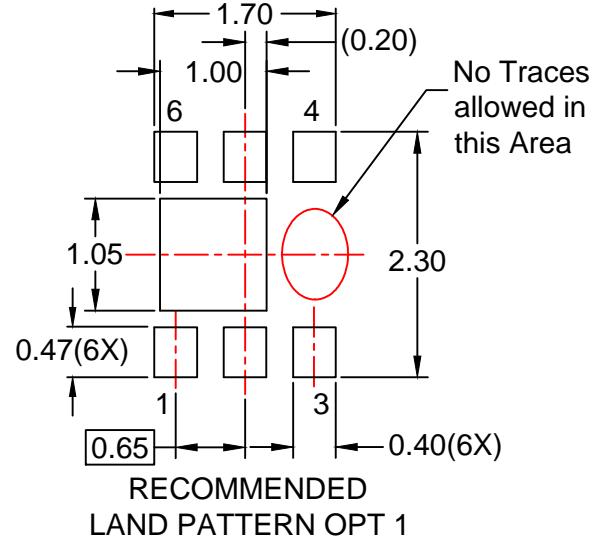


Figure 12. Junction-to-Ambient Transient Thermal Response Curve



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
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