EL8100, EL8101

200MHz Rail-to-Rail Amplifiers

FN7103
Rev 9.00
September 14, 2010

The EL8100 and EL8101 represent single rail-to-rail amplifiers with a -3dB bandwidth of 200MHz and slew rate of 200V/µs. Running off a very low 2mA supply current, the EL8100 and EL8101 also feature inputs that go to 0.15V below the V_S- rail.

The EL8100 includes a fast-acting disable/power-down circuit. With a 25ns disable and a 200ns enable, the EL8100 is ideal for multiplexing applications.

The EL8100 and EL8101 are designed for a number of general purpose video, communication, instrumentation, and industrial applications. The EL8100 is available in 8 Ld SO and 6 Ld SOT-23 packages and the EL8101 is available in a 5 Ld SOT-23 package. All are specified for operation over the -40°C to +85°C temperature range.

Ordering Information

PART NUMBER (Note 1)	PART MARKING	PACKAGE	PKG. DWG. #
EL8100ISZ	8100ISZ	8 Ld SOIC (Pb-Free)	M8.15E
EL8100ISZ-T7*	8100ISZ	8 Ld SOIC (Pb-Free)	M8.15E
EL8100ISZ-T13*	8100ISZ	8 Ld SOIC (Pb-Free)	M8.15E
EL8100IWZ-T7*	BASA (Note 2)	6 Ld SOT-23 (Pb-free)	P6.064A
EL8100IWZ-T7A*	BASA (Note 2)	6 Ld SOT-23 (Pb-free)	P6.064A
EL8101IWZ-T7*	BATA (Note 2)	5 Ld SOT-23 (Pb-Free)	P5.064A
EL8101IWZ-T7A*	BATA (Note 2)	5 Ld SOT-23 (Pb-Free)	P5.064A

*Please refer to TB347 for details on reel specifications.

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. The part marking is located on the bottom of the part.

Features

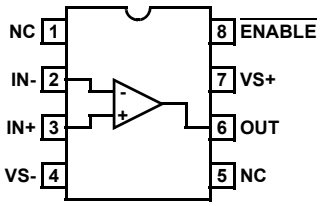
- 200MHz -3dB bandwidth
- 200V/µs slew rate
- Low supply current = 2mA
- Supplies from 3V to 5.0V
- Rail-to-rail output
- Input to 0.15V below V_S-
- Fast 25ns disable (EL8100 only)
- Low cost
- Pb-Free (RoHS compliant)

Applications

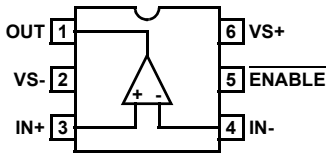
- Video amplifiers
- Portable/hand-held products
- Communications devices

Pinouts

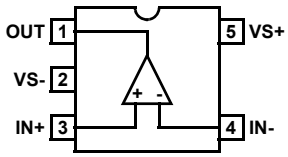
EL8100
(8 LD SOIC)
TOP VIEW



EL8100
(6 LD SOT-23)
TOP VIEW



EL8101
(5 LD SOT-23)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage from V_S+ to V_S- 5.5V
Input Voltage . . . . . V_S+ +0.3V to V_S- -0.3V
Differential Input Voltage 2V
Continuous Output Current 40mA
ESD Tolerance
Human Body Model 3kV
Machine Model 300V

Thermal Information

Power Dissipation . . . . . See Curves
Storage Temperature . . . . . .-65°C to +125°C
Ambient Operating Temperature . . . . . .-40°C to +85°C
Operating Junction Temperature . . . . . .+125°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = 5V, V_S- = GND, T_A = +25°C, V_{CM} = 2.5V, R_L to 2.5V, A_V = 1, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Offset Voltage		-6	-0.8	+6	mV
TCV_{OS}	Offset Voltage Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		3		µV/°C
IB	Input Bias Current	V_{IN} = 0V	-2.1	-1.5		µA
I_{OS}	Input Offset Current	V_{IN} = 0V		0.2	0.55	µA
TCI_{OS}	Input Bias Current Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		2		nA/°C
CMRR	Common Mode Rejection Ratio	V_{CM} = -0.15V to +3.5V	70	90		dB
CMIR	Common Mode Input Range		V_S- -0.15		V_S+ -1.5	V
R_{IN}	Input Resistance	Common Mode		16		MΩ
C_{IN}	Input Capacitance			0.5		pF
A_{VOL}	Open Loop Gain	V_{OUT} = +1.5V to +3.5V, R_L = 1kΩ to GND	75	90		dB
		V_{OUT} = +1.5V to +3.5V, R_L = 150Ω to GND		80		dB
OUTPUT CHARACTERISTICS						
R_{OUT}	Output Resistance	A_V = +1		30		mΩ
V_{OP}	Positive Output Voltage Swing	R_L = 1kΩ	4.85	4.9		V
		R_L = 150Ω	4.6	4.7		V
V_{ON}	Negative Output Voltage Swing	R_L = 150Ω		100	150	mV
		R_L = 1kΩ		35	50	mV
I_{OUT}	Linear Output Current			65		mA
I_{SC} (source)	Short Circuit Current	R_L = 10Ω	60	70		mA
I_{SC} (sink)	Short Circuit Current	R_L = 10Ω	120	140		mA
POWER SUPPLY						
PSRR	Power Supply Rejection Ratio	V_S+ = 4.5V to 5.5V	75	100		dB
I_{S-ON}	Supply Current - Enabled			2	2.4	mA
I_{S-OFF}	Supply Current - Disabled			30		µA
ENABLE (EL8100 ONLY)						
t_{EN}	Enable Time			200		ns
t_{DS}	Disable Time			25		ns

Electrical Specifications $V_S+ = 5V$, $V_S- = GND$, $T_A = +25°C$, $V_{CM} = 2.5V$, R_L to 2.5V, $A_V = 1$, Unless Otherwise Specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNIT
V_{IH-ENB}	$\overline{\text{ENABLE}}$ Pin Voltage for Power-up			0.8		V
V_{IL-ENB}	$\overline{\text{ENABLE}}$ Pin Voltage for Shut-down			2		V
I_{IH-ENB}	$\overline{\text{ENABLE}}$ Pin Input Current High			8.6		µA
I_{IL-ENB}	$\overline{\text{ENABLE}}$ Pin Input for Current Low			0.01		µA
AC PERFORMANCE						
BW	-3dB Bandwidth	$A_V = +1$, $R_F = 0\Omega$, $C_L = 5pF$		200		MHz
		$A_V = -1$, $R_F = 1k\Omega$, $C_L = 5pF$		90		MHz
		$A_V = +2$, $R_F = 1k\Omega$, $C_L = 5pF$		90		MHz
		$A_V = +10$, $R_F = 1k\Omega$, $C_L = 5pF$		10		MHz
BW	±0.1dB Bandwidth	$A_V = +1$, $R_F = 0\Omega$, $C_L = 5pF$		20		MHz
Peak	Peaking	$A_V = +1$, $R_F = 1k\Omega$, $C_L = 5pF$		1		dB
GBWP	Gain Bandwidth Product			100		MHz
PM	Phase Margin	$R_L = 1k\Omega$, $C_L = 5pF$		55		°
SR	Slew Rate	$A_V = 2$, $R_L = 100\Omega$, $V_{OUT} = 0.5V$ to 4.5V	160	200		V/µs
t_R	Rise Time	$2.5V_{STEP}$, 20% to 80%		8		ns
t_F	Fall Time	$2.5V_{STEP}$, 20% to 80%		7		ns
OS	Overshoot	200mV step		10		%
t_{PD}	Propagation Delay	200mV step		2		ns
t_S	0.1% Settling Time	200mV step		20		ns
dG	Differential Gain	$A_V = +2$, $R_F = 1k\Omega$, $R_L = 150\Omega$		0.035		%
dP	Differential Phase	$A_V = +2$, $R_F = 1k\Omega$, $R_L = 150\Omega$		0.05		°
e_N	Input Noise Voltage	f = 10kHz		10		nV/√Hz
i_N+	Positive Input Noise Current	f = 10kHz		1		pA/√Hz
i_N-	Negative Input Noise Current	f = 10kHz		0.8		pA/√Hz

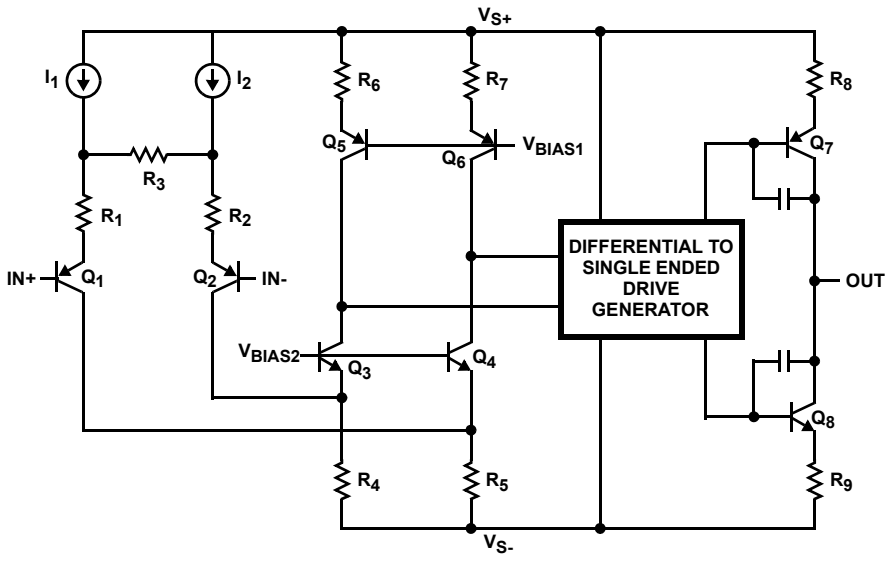
NOTE:

3. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Pin Descriptions

PIN NUMBER			PIN NAME	DESCRIPTION
EL8100IS (8 Ld SOIC)	EL8100IW (6 Ld SO- 23)	EL8101IW 5 Ld SOT-23)		
1, 5			NC	Not connected
2	4	4	IN-	Inverting input
3	3	3	IN+	Non-inverting input
4	2	2	VS-	Negative power supply
6	1	1	OUT	Amplifier output
7	6	5	VS+	Positive power supply
8	5		$\overline{\text{ENABLE}}$	Enable and disable input

Simplified Schematic Diagram



Typical Performance Curves

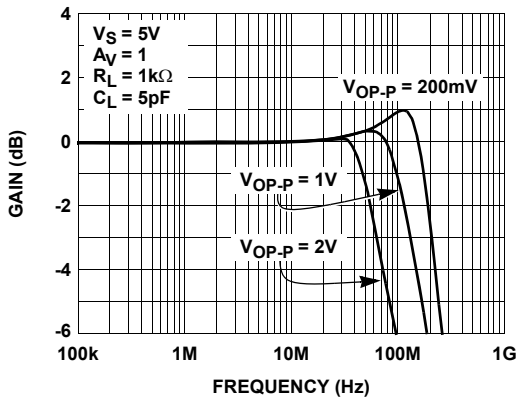


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGE LEVELS

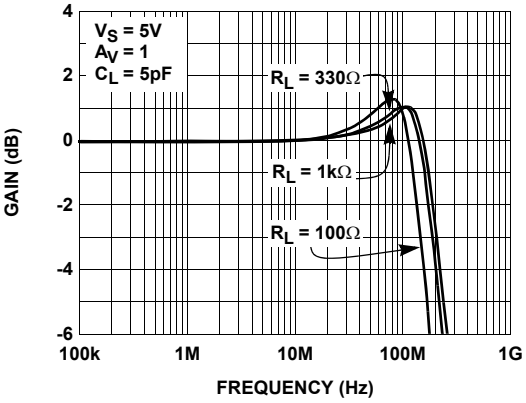


FIGURE 2. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS R_{LOAD}

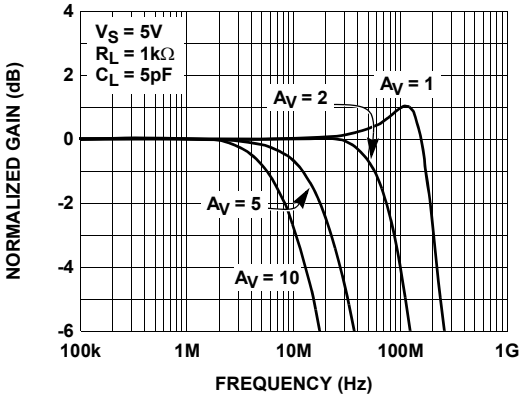


FIGURE 3. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS NON-INVERTING GAINS

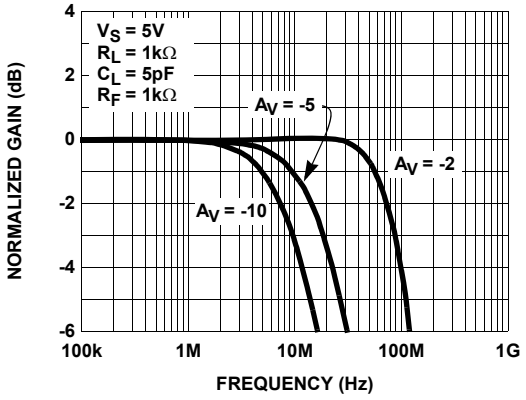


FIGURE 4. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS INVERTING GAINS

Typical Performance Curves (Continued)

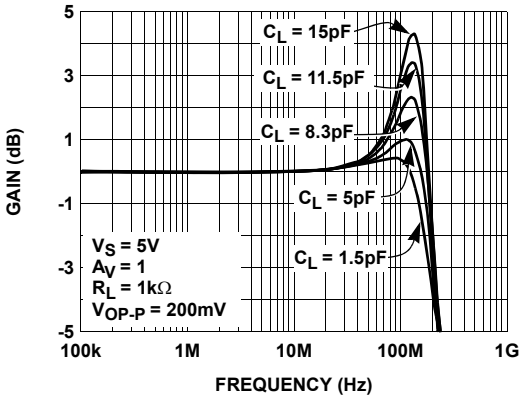


FIGURE 5. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS C_L

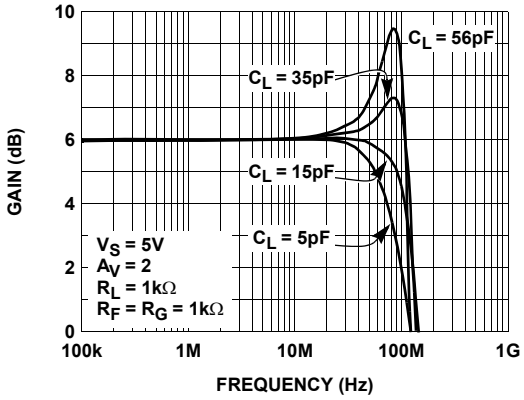


FIGURE 6. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS C_L

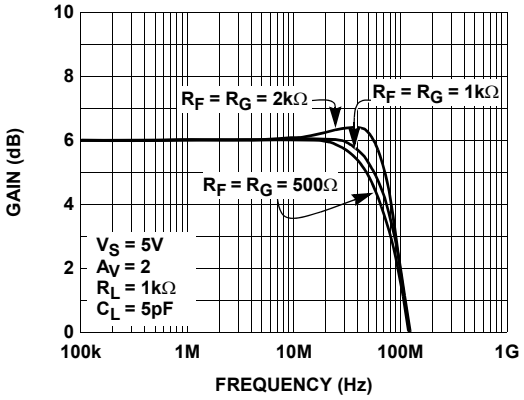


FIGURE 7. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS R_F AND R_G

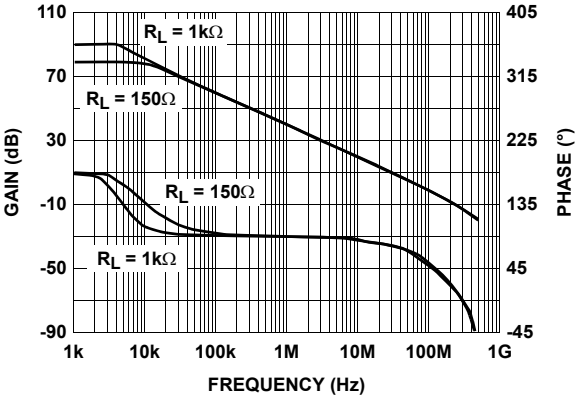


FIGURE 8. OPEN LOOP GAIN AND PHASE vs FREQUENCY

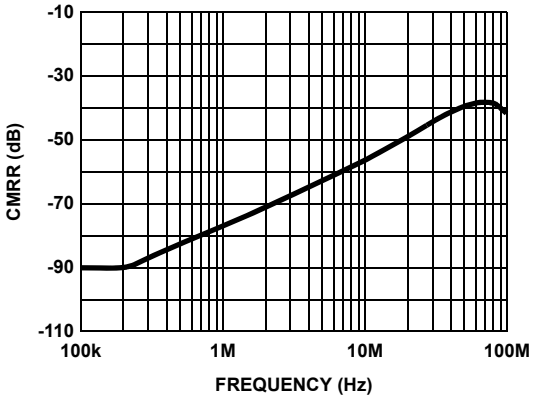


FIGURE 9. COMMON-MODE REJECTION RATIO vs FREQUENCY

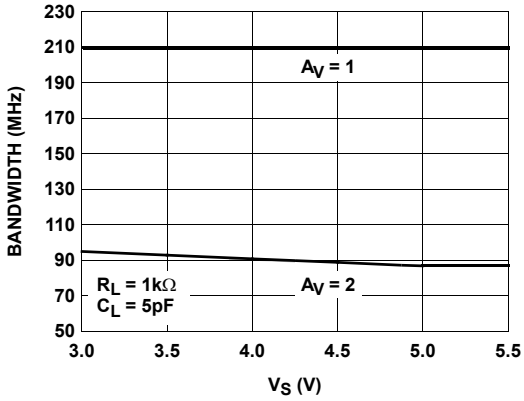


FIGURE 10. SMALL SIGNAL BANDWIDTH vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

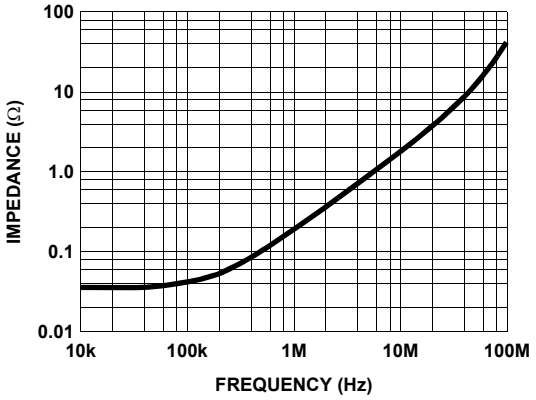


FIGURE 11. OUTPUT IMPEDANCE vs FREQUENCY

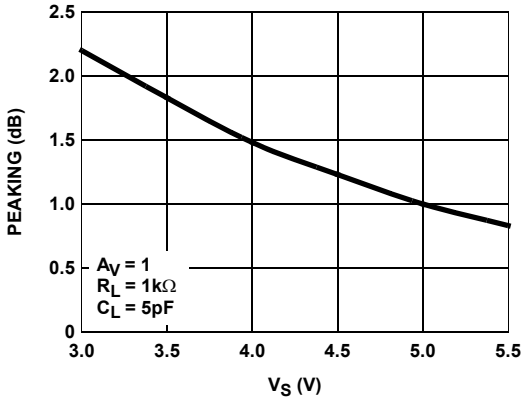


FIGURE 12. SMALL SIGNAL PEAKING vs SUPPLY VOLTAGE

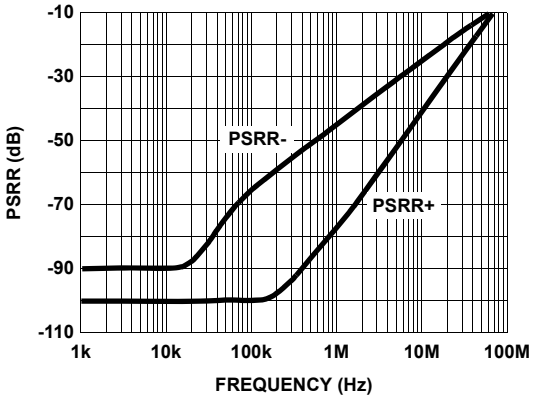


FIGURE 13. POWER SUPPLY REJECTION RATIO vs FREQUENCY

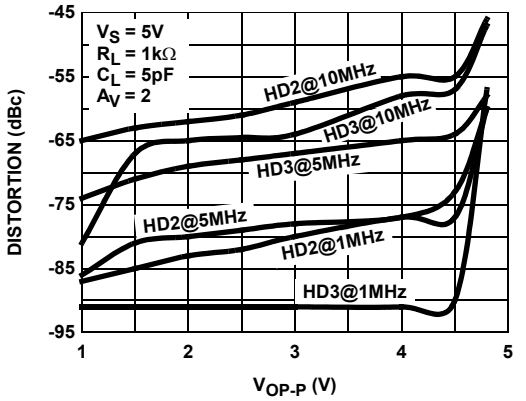


FIGURE 14. HARMONIC DISTORTION vs OUTPUT VOLTAGE

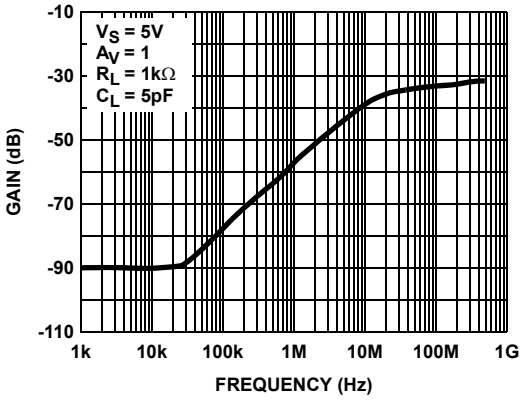


FIGURE 15. DISABLED OUTPUT ISOLATION FREQUENCY RESPONSE

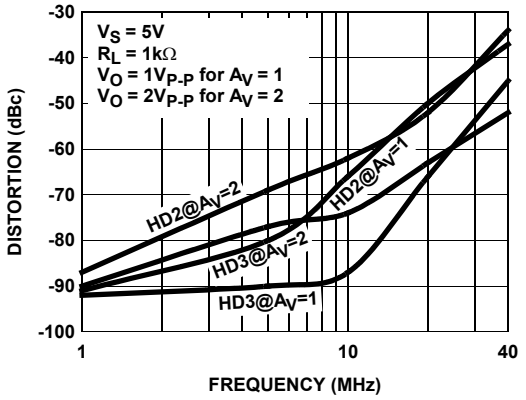


FIGURE 16. HARMONIC DISTORTION vs FREQUENCY

Typical Performance Curves (Continued)

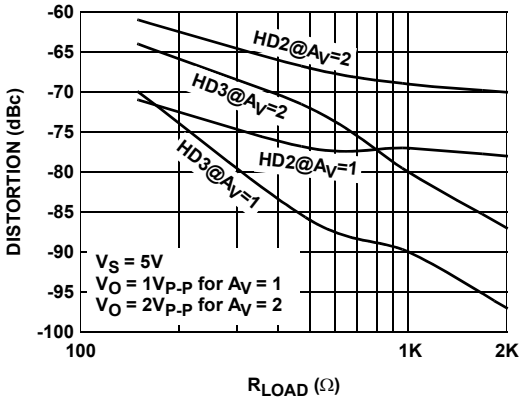


FIGURE 17. HARMONIC DISTORTION vs LOAD RESISTANCE

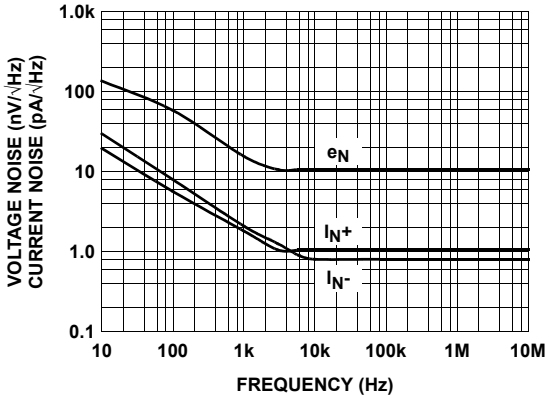


FIGURE 18. VOLTAGE AND CURRENT NOISE vs FREQUENCY

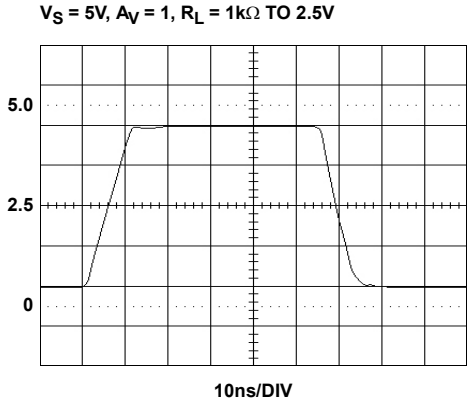


FIGURE 19. LARGE SIGNAL TRANSIENT RESPONSE

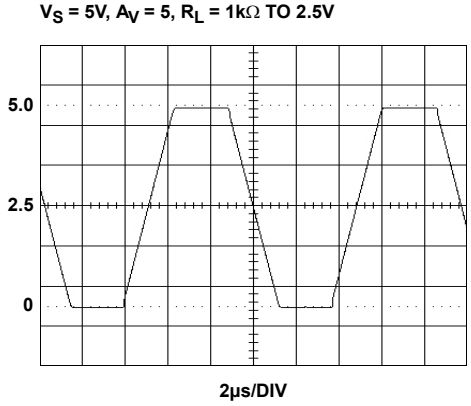


FIGURE 20. OUTPUT SWING

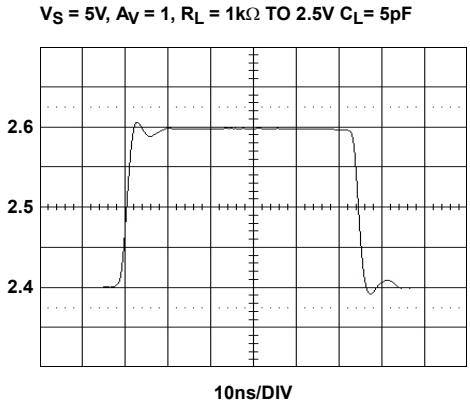


FIGURE 21. SMALL SIGNAL TRANSIENT RESPONSE

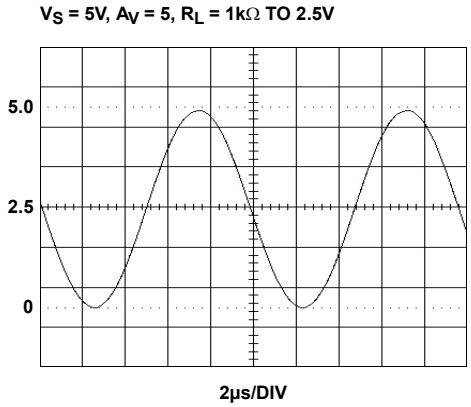


FIGURE 22. OUTPUT SWING

Typical Performance Curves (Continued)

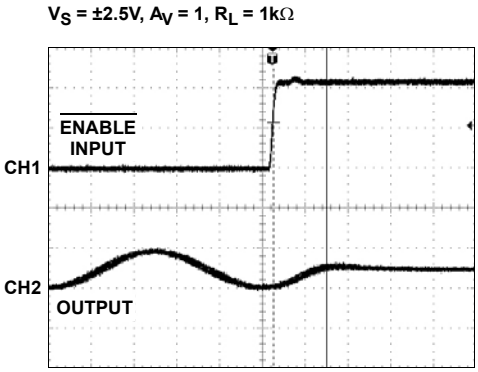


FIGURE 23. DISABLED RESPONSE

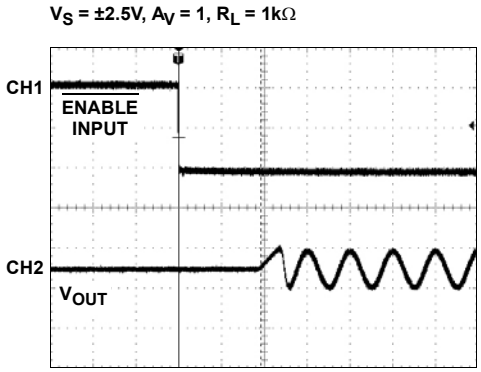


FIGURE 24. ENABLED RESPONSE

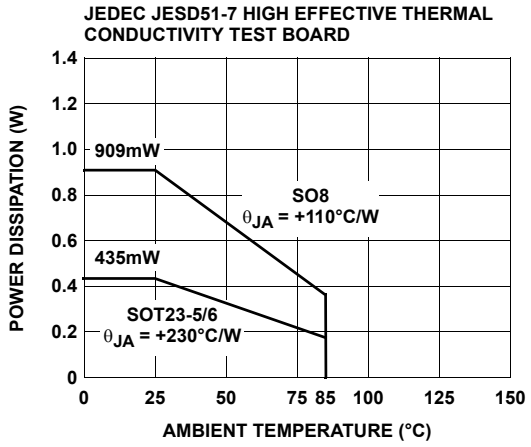


FIGURE 25. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

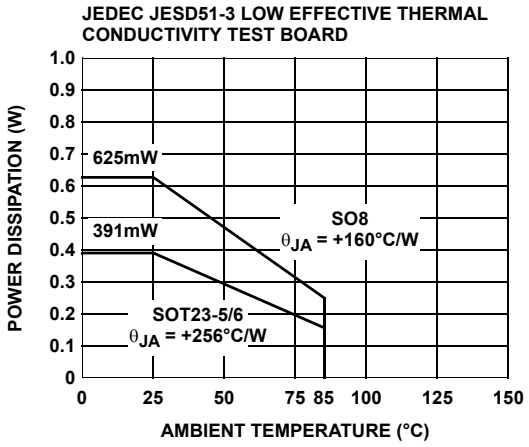


FIGURE 26. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Description of Operation and Application Information

Product Description

The EL8100, EL8101 are wide bandwidth, single supply, low power and rail-to-rail output voltage feedback operational amplifiers. Both amplifiers are internally compensated for closed loop gain of +1 of greater. Connected in voltage follower mode and driving a 1kΩ load, the EL8100, EL8101 have a -3dB bandwidth of 200MHz. Driving a 150Ω load, the bandwidth is about 130MHz while maintaining a 200V/µs slew rate. The EL8100 is available with a power-down pin to reduce power to 30µA typically while the amplifier is disabled.

Input, Output and Supply Voltage Range

The EL8100, EL8101 have been designed to operate with a single supply voltage from 3V to 5.0V. Split supplies can also be used as long as their total voltage is within 3V to 5.0V.

The amplifiers have an input common mode voltage range from 0.15V below the negative supply (VS- pin) to within 1.5V of the positive supply (VS+ pin). If the input signal is outside the above specified range, it will cause the output signal to be distorted.

The output of the EL8100, EL8101 can swing rail-to-rail. As the load resistance becomes lower, the ability to drive close to each rail is reduced. For the load resistor 1kΩ, the output swing is about 4.9V at a 5V supply. For the load resistor 150Ω, the output swing is about 4.6V.

Choice of Feedback Resistor and Gain Bandwidth Product

For applications that require a gain of +1, no feedback resistor is required. Just short the output pin to the inverting input pin. For gains greater than +1, the feedback resistor forms a pole with the parasitic capacitance at the inverting input. As this pole becomes smaller, the amplifier's phase margin is reduced. This causes ringing in the time domain

and peaking in the frequency domain. Therefore, R_F has some maximum value that should not be exceeded for optimum performance. If a large value of R_F must be used, a small capacitor in the few Pico farad range in parallel with R_F can help to reduce the ringing and peaking at the expense of reducing the bandwidth.

As far as the output stage of the amplifier is concerned, the output stage is also a gain stage with the load. R_F and R_G appear in parallel with R_L for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, R_F also has a minimum value that should not be exceeded for optimum performance. For gain of +1, R_F = 0 is optimum. For the gains other than +1, optimum response is obtained with R_F between 300Ω to 1kΩ.

The EL8100, EL8101 have a gain bandwidth product of 100MHz. For gains ≥5, its bandwidth can be predicted by Equation 1:

$$Gain \times BW = 100MHz \quad \text{(EQ. 1)}$$

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because the change in output current with DC level. Special circuitry has been incorporated in the EL8100, EL8101 to reduce the variation of the output impedance with the current output. This results in dG and dP specifications of 0.03% and 0.05°, while driving 150Ω at a gain of 2. Driving high impedance loads would give a similar or better dG and dP performance.

Driving Capacitive Loads and Cables

The EL8100, EL8101 can drive 15pF loads in parallel with 1kΩ with less than 5dB of peaking at gain of +1. If less peaking is desired in applications, a small series resistor (usually between 5Ω to 50Ω) can be placed in series with the output to eliminate most peaking. However, this will reduce the gain slightly. If the gain setting is greater than 1, the gain resistor R_G can then be chosen to make up for any gain loss which may be created by the additional series resistor at the output.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

Disable/Power-Down

The EL8100 can be disabled and placed its output in a high impedance state. The turn-off time is about 25ns and the turn-on time is about 200ns. When disabled, the amplifier's supply current is reduced to 30µA typically, thereby effectively eliminating the power consumption. The amplifier's power-down can be controlled by standard TTL or CMOS signal levels at the $\overline{ENABLE}$ pin. The applied logic signal is relative to V_S- pin. Letting the $\overline{ENABLE}$ pin float or applying a signal that is less than 0.8V above V_S- will enable the amplifier. The amplifier will be disabled when the signal at the $\overline{ENABLE}$ pin is 2V above V_S-.

Output Drive Capability

The EL8100, EL8101 do not have internal short circuit protection circuitry. They have a typical short circuit current of 70mA sourcing and 140mA sinking for the output is connected to half way between the rails with a 10Ω resistor. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±40mA. This limit is set by the design of the internal metal interconnections.

Power Dissipation

With the high output drive capability of the EL8100, EL8101, it is possible to exceed the +125°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if the load conditions or package types need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 2:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \quad \text{(EQ. 2)}$$

Where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

For sourcing, Equation 3:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_S - V_{OUT}) \times \frac{V_{OUT}}{R_L} \quad \text{(EQ. 3)}$$

For sinking, Equation 4:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_{OUT} - V_S\text{-}) \times I_{LOAD} \quad \text{(EQ. 4)}$$

Where:

V_S = Total supply voltage

I_{SMAX} = Maximum quiescent supply current

V_{OUT} = Maximum output voltage of the application

R_{LOAD} = Load resistance tied to ground

I_{LOAD} = Load current

By setting the two PD_{MAX} equations equal to each other, we can solve the output current and R_{LOAD} to avoid the device overheat.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as sort as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the VS- pin is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V_S+ to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the V_S- pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to a minimum. Use of wire-wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

Typical Applications

Video Sync Pulse Remover

Many CMOS analog to digital converters have a parasitic latch up problem when subjected to negative input voltage levels. Since the sync tip contains no useful video information and it is a negative going pulse, we can chop it off. Figure 27 shows a gain of 2 connections for EL8100, EL8101. Figure 28 shows the complete input video signal applied at the input, as well as the output signal with the negative going sync pulse removed.

Multiplexer

Besides the normal power-down usage, the $\overline{\text{ENABLE}}$ pin of the EL8100 can be used for multiplexing applications. Figure 29 shows two EL8100s with the outputs tied together, driving a back terminated 75Ω video load. A $2V_{P-P}$ 2MHz sine wave is applied to Amp A and a $1V_{P-P}$ 2MHz sine wave is applied to Amp B. Figure 30 shows the $\overline{\text{ENABLE}}$ signal and the resulting output waveform at V_{OUT}. Observe the break-before-make operation of the multiplexing. Amp A is on and V_{IN1} is passed through to the output when the $\overline{\text{ENABLE}}$ signal is low and turns off in about 25ns when the $\overline{\text{ENABLE}}$ signal is high. About 200ns later, Amp B turns on and V_{IN2} is passed through to the output. The break-before-make operation ensures that more than one amplifier isn't trying to drive the bus at the same time.

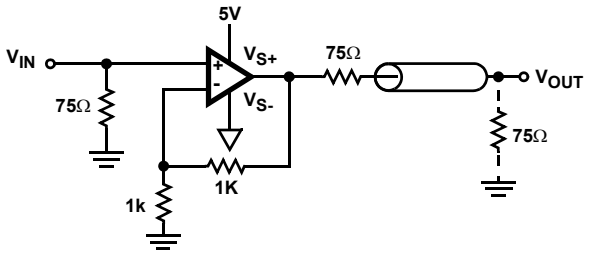


FIGURE 27. SYNC PULSE REMOVER

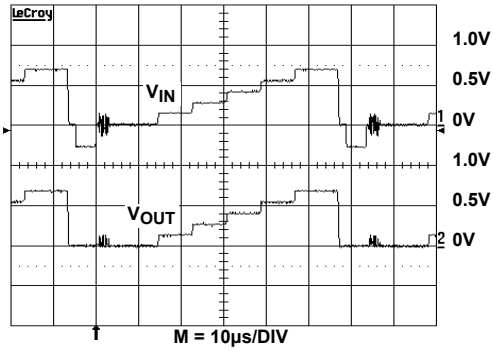


FIGURE 28. VIDEO SIGNAL

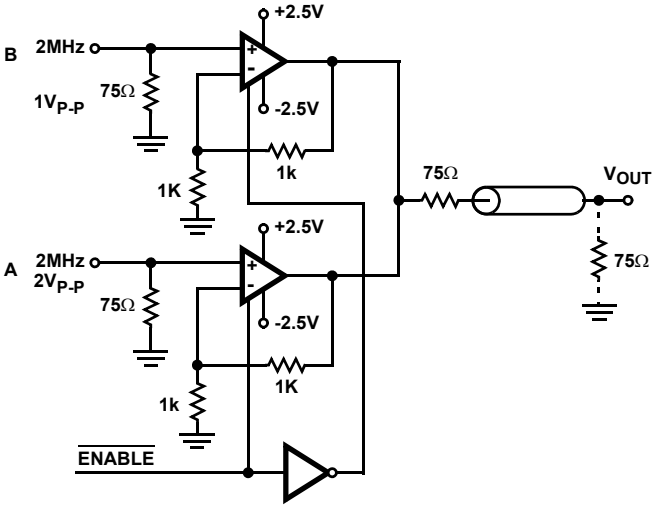


FIGURE 29. TWO TO ONE MULTIPLEXER

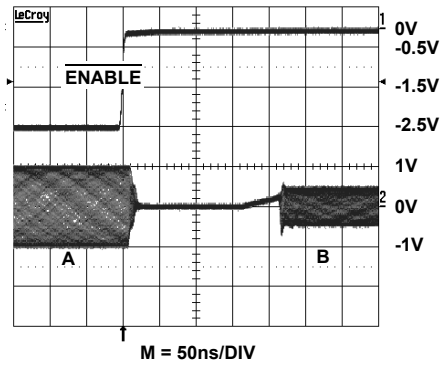


FIGURE 30. ENABLE SIGNAL

Single Supply Video Line Driver

The EL8100, EL8101 are wideband rail-to-rail output op amplifiers with large output current, excellent dG, dP, and low distortion that allow them to drive video signals in low supply applications. Figure 31 is the single supply non-inverting video line driver configuration and Figure 32 is the inverting video ling driver configuration. The signal is AC-coupled by C_1. R_1 and R_2 are used to level shift the input and output to provide the largest output swing. R_F and R_G set the AC gain. C_2 isolates the virtual ground potential. R_T and R_3 are the termination resistors for the line. C_1, C_2 and C_3 are selected big enough to minimize the droop of the luminance signal.

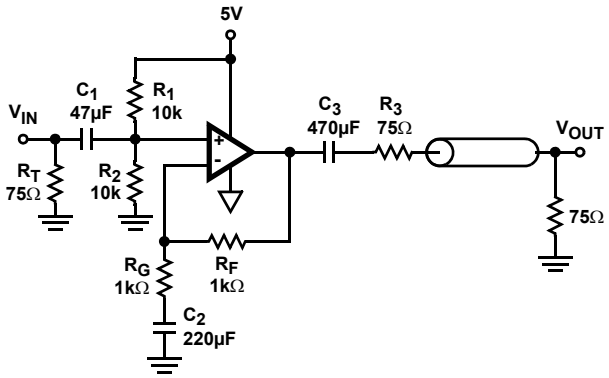


FIGURE 31. 5V SINGLE SUPPLY NON INVERTING VIDEO LINE DRIVER

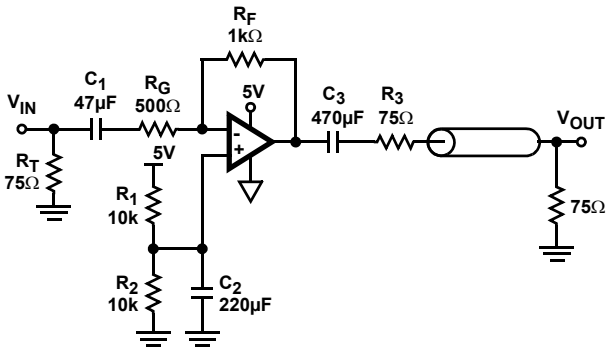


FIGURE 32. 5V SINGLE SUPPLY INVERTING VIDEO LINE DRIVER

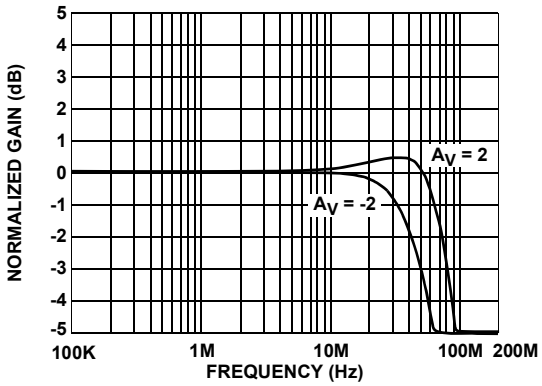
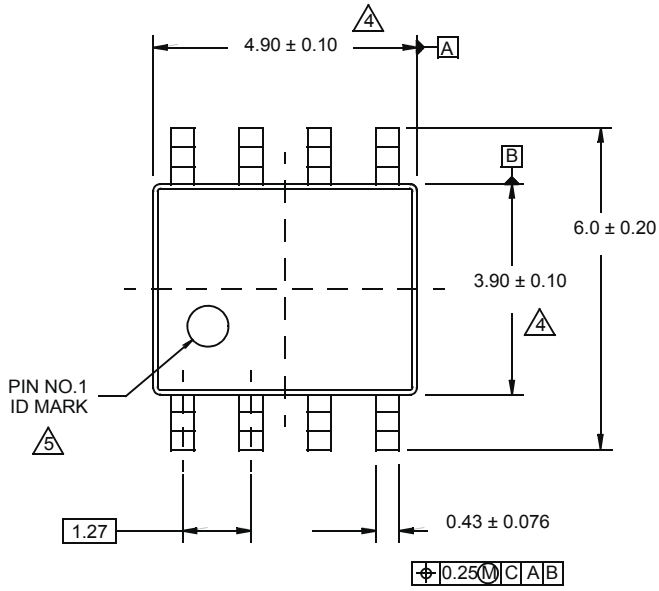


FIGURE 33. VIDEO LINE DRIVER FREQUENCY RESPONSE

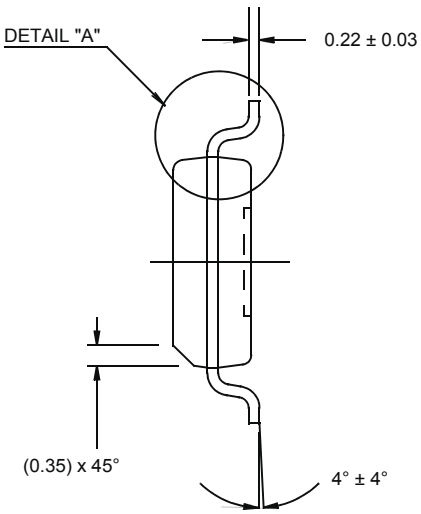
Package Outline Drawing

M8.15E

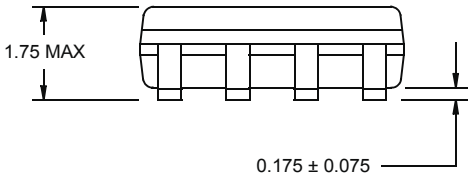
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



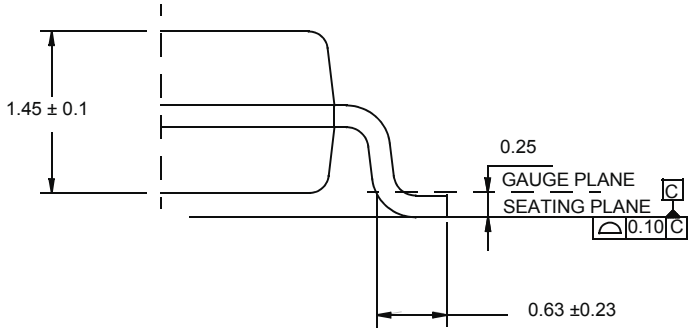
TOP VIEW



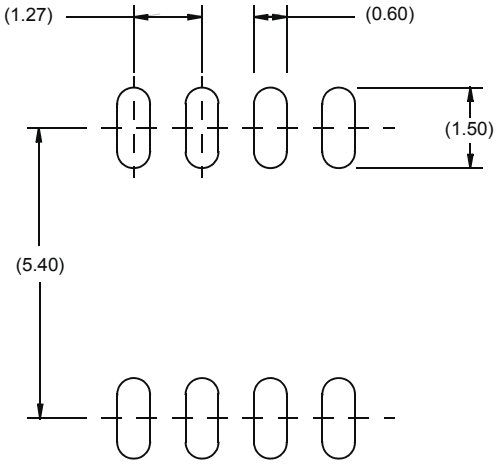
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

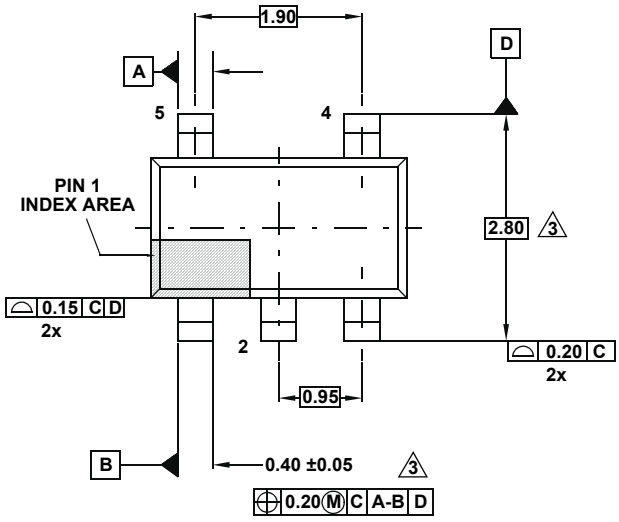
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

Package Outline Drawing

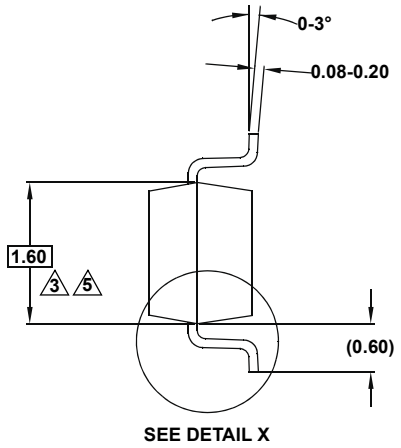
P5.064A

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

Rev 0, 2/10

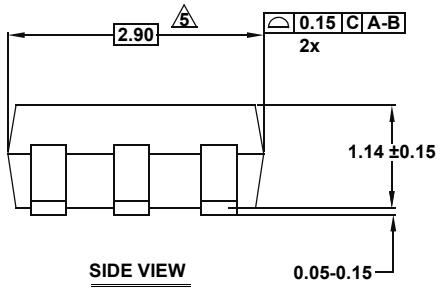


TOP VIEW

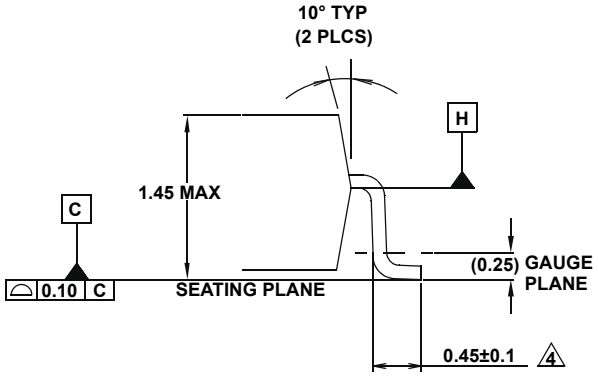


SEE DETAIL X

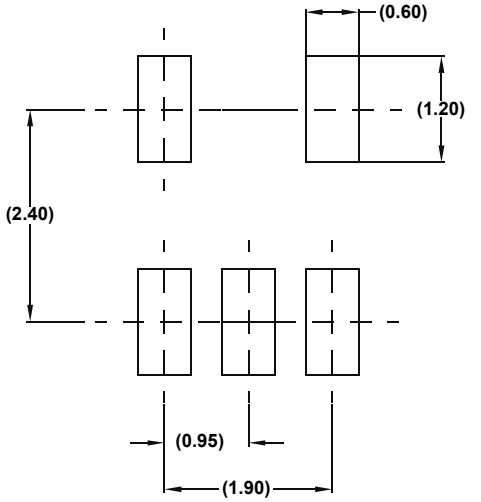
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

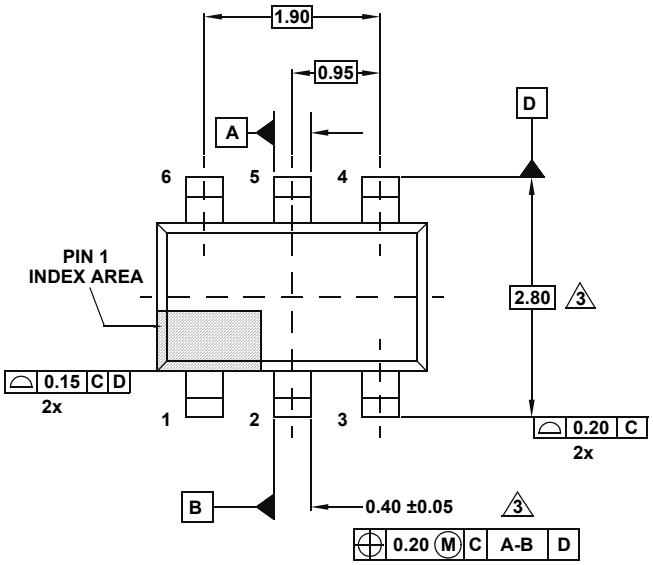
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.

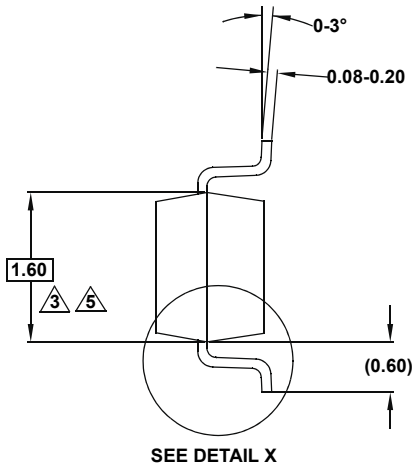
Package Outline Drawing

P6.064A

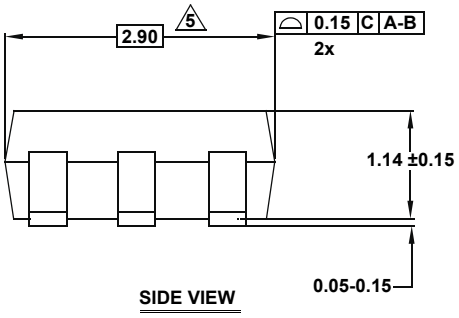
6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
Rev 0, 2/10



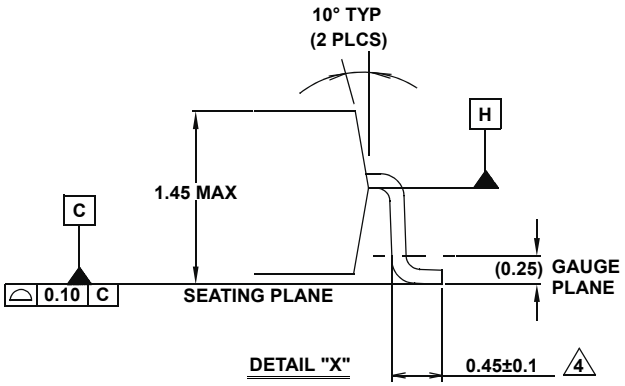
TOP VIEW

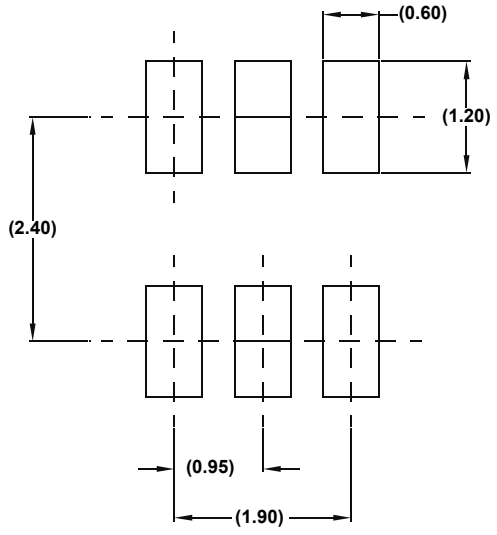


END VIEW



SIDE VIEW





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NOTES:

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2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.

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