1-/2-/4-Channel Digital Potentiometers

AD8400/AD8402/AD8403

FEATURES

256-position variable resistance device
Replaces 1, 2, or 4 potentiometers
1 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
Power shutdown—less than 5 µA
3-wire,SPI-compatible serial data input
10 MHz update data loading rate
2.7 V to 5.5 V single-supply operation
Qualified for automotive applications

APPLICATIONS

Mechanical potentiometer replacement
Programmable filters, delays, time constants
Volume control, panning
Line impedance matching
Power supply adjustment

GENERAL DESCRIPTION

The AD8400/AD8402/AD8403 provide a single-, dual-, or quad-channel, 256-position, digitally controlled variable resistor (VR) device.[1] These devices perform the same electronic adjustment function as a mechanical potentiometer or variable resistor. The AD8400 contains a single variable resistor in the compact SOIC-8 package. The AD8402 contains two independent variable resistors in space-saving SOIC-14 surface-mount packages. The AD8403 contains four independent variable resistors in 24-lead PDIP, SOIC, and TSSOP packages. Each part contains a fixed resistor with a wiper contact that taps the fixed resistor value at a point determined by the digital code loaded into the controlling serial input register. The resistance between the wiper and either endpoint of the fixed resistor varies linearly with respect to the digital code transferred into the VR latch. Each variable resistor offers a completely programmable value of resistance between the A terminal and the wiper or the B terminal and the wiper. The fixed A-to-B terminal resistance of 1 kΩ, 10 kΩ, 50 kΩ, or 100 kΩ has a ±1% channel-to-channel matching tolerance with a nominal temperature coefficient of 500 ppm/°C. A unique switching circuit minimizes the high glitch inherent in traditional switched resistor designs, avoiding any make-before-break or break-before-make operation.

(continued on Page 3)

[1] The terms digital potentiometer, VR, and RDAC are used interchangeably.

FUNCTIONAL BLOCK DIAGRAM

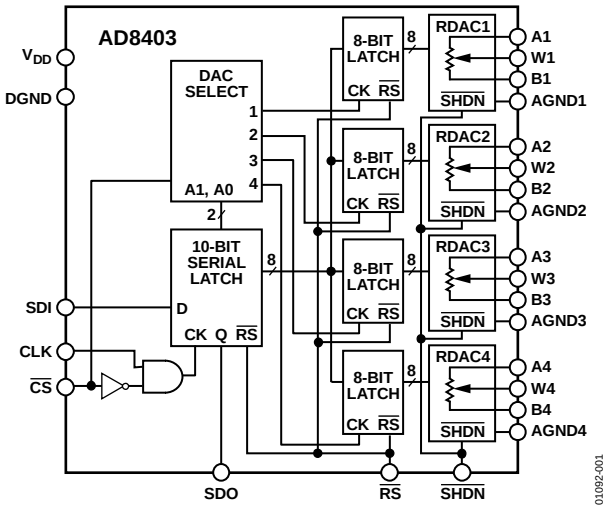

Figure 1.

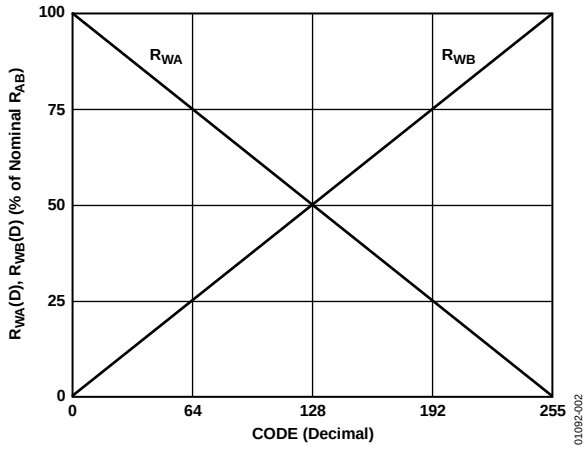

Figure 2. R_{WA} and R_{WB} vs. Code

Rev. E
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GENERAL DESCRIPTION

(continued from Page 1)

Each VR has its own VR latch that holds its programmed resistance value. These VR latches are updated from an SPI-compatible, serial-to-parallel shift register that is loaded from a standard 3-wire, serial-input digital interface. Ten data bits make up the data-word clocked into the serial input register.

The data-word is decoded where the first two bits determine the address of the VR latch to be loaded, and the last eight bits are the data. A serial data output pin at the opposite end of the serial register allows simple daisy chaining in multiple VR applications without additional external decoding logic.

The reset ($\overline{RS}$) pin forces the wiper to midscale by loading 80_H into the VR latch. The $\overline{SHDN}$ pin forces the resistor to an end-to-end open-circuit condition on the A terminal and shorts the wiper to the B terminal, achieving a microwatt power shutdown state. When $\overline{SHDN}$ is returned to logic high, the previous latch settings put the wiper in the same resistance setting prior to shutdown. The digital interface is still active in shutdown so that code changes can be made that will produce new wiper positions when the device is taken out of shutdown.

The AD8400 is available in the SOIC-8 surface mount. The AD8402 is available in both surface-mount (SOIC-14) and 14-lead PDIP packages, while the AD8403 is available in a narrow-body, 24-lead PDIP and a 24-lead, surface-mount package. The AD8402/AD8403 are also offered in the 1.1 mm thin TSSOP-14/TSSOP-24 packages for PCMCIA applications. All parts are guaranteed to operate over the extended industrial temperature range of −40°C to +125°C.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—10 KΩ VERSION

V_{DD} = 3 V ± 10% or 5 V ± 10%, $V_A = V_{DD}$, V_B = 0 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE (Specifications Apply to All VRs)						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = no connect	−1	±1/4	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−2	±1/2	+2	LSB
Nominal Resistance[3]	R_{AB}	T_A = 25°C, model: AD840XYY10	8	10	12	kΩ
Resistance Tempco	$\Delta R_{AB}/\Delta T$	$V_{AB} = V_{DD}$, wiper = no connect		500		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5V, $I_W = V_{DD}/R_{AB}$		50	100	Ω
	R_W	V_{DD} = 3V, $I_W = V_{DD}/R_{AB}$		200		Ω
Nominal Resistance Match	$\Delta R/R_{AB}$	CH 1 to CH 2, CH 3, or CH 4, $V_{AB} = V_{DD}$, T_A = 25°C		0.2	1	%
DC CHARACTERISTICS POTENTIOMETER DIVIDER (Specifications Apply to All VRs)						
Resolution	N		8			Bits
Integral Nonlinearity[4]	INL		−2	±1/2	+2	LSB
Differential Nonlinearity[4]	DNL	V_{DD} = 5 V	−1	±1/4	+1	LSB
	DNL	V_{DD} = 3 V, T_A = 25°C	−1	±1/4	+1	LSB
	DNL	V_{DD} = 3 V, T_A = −40°C to +85°C	−1.5	±1/2	+1.5	LSB
Voltage Divider Tempco	$\Delta V_W/\Delta T$	Code = 80_H		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = FF_H	−4	−2.8	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	1.3	2	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A, B, W}$		0		V_{DD}	V
Capacitance[6] Ax, Capacitance Bx	$C_{A, B}$	f = 1 MHz, measured to GND, code = 80_H		75		pF
Capacitance[6] Wx	C_W	f = 1 MHz, measured to GND, code = 80_H		120		pF
Shutdown Current[7]	I_{A_SD}	$V_A = V_{DD}$, V_B = 0 V, $\overline{SHDN}$ = 0		0.01	5	µA
Shutdown Wiper Resistance	R_{W_SD}	$V_A = V_{DD}$, V_B = 0 V, $\overline{SHDN}$ = 0, V_{DD} = 5 V		100	200	Ω
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Output Logic High	V_{OH}	R_L = 2.2 kΩ to V_{DD}	V_{DD} − 0.1			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{DD} = 5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V, V_{DD} = 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD} range		2.7		5.5	V
Supply Current (CMOS)	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = 0 V		0.01	5	µA
Supply Current (TTL)[8]	I_{DD}	V_{IH} = 2.4 V or 0.8 V, V_{DD} = 5.5 V		0.9	4	mA
Power Dissipation (CMOS)[9]	P_{DISS}	$V_{IH} = V_{DD}$ or V_{IL} = 0 V, V_{DD} = 5.5 V			27.5	µW
Power Supply Sensitivity	PSS	V_{DD} = 5 V ± 10%		0.0002	0.001	%/%
	PSS	V_{DD} = 3 V ± 10%		0.006	0.03	%/%

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[6, 10]						
Bandwidth −3 dB	BW_10 K	R = 10 kΩ		600		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms + 2 V dc, V_B = 2 V dc, f = 1 kHz		0.003		%
V_W Settling Time	t_S	$V_A = V_{DD}$, V_B = 0 V, ±1% error band		2		µs
Resistor Noise Voltage	e_{NWB}	R_{WB} = 5 kΩ, f = 1 kHz, $\overline{RS}$ = 0		9		nV/√Hz
Crosstalk[11]	C_T	$V_A = V_{DD}$, V_B = 0 V		−65		dB

[1] Typical represents average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See the test circuit in Figure 38. I_W = 50 µA for V_{DD} = 3 V and I_W = 400 µA for V_{DD} = 5 V for the 10 kΩ versions.
[3] $V_{AB} = V_{DD}$, wiper (V_W) = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions. See the test circuit in Figure 37.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test. Resistor-terminal capacitance tests are measured with 2.5 V bias on the measured terminal. The remaining resistor terminals are left open circuit.
[7] Measured at the Ax terminals. All Ax terminals are open-circuited in shutdown mode.
[8] Worst-case supply current is consumed when the input logic level is at 2.4 V, a standard characteristic of CMOS logic. See Figure 28 for a plot of I_{DD} vs. logic voltage.
[9] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[10] All dynamic characteristics use V_{DD} = 5 V.
[11] Measured at a V_W pin where an adjacent V_W pin is making a full-scale voltage change.

ELECTRICAL CHARACTERISTICS—50 KΩ AND 100 KΩ VERSIONS

V_{DD} = 3 V ± 10% or 5 V ± 10%, $V_A = V_{DD}$, V_B = 0 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE (Specifications Apply to All VRs)						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = No Connect	−1	±1/4	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = No Connect	−2	±1/2	+2	LSB
Nominal Resistance[3]	R_{AB}	T_A = 25°C, Model: AD840XYY50	35	50	65	kΩ
	R_{AB}	T_A = 25°C, Model: AD840XYY100	70	100	130	kΩ
Resistance Tempco	$\Delta R_{AB}/\Delta T$	$V_{AB} = V_{DD}$, Wiper = No Connect		500		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5V, $I_W = V_{DD}/R_{AB}$		50	100	Ω
	R_W	V_{DD} = 3V, $I_W = V_{DD}/R_{AB}$		200		Ω
Nominal Resistance Match	$\Delta R/R_{AB}$	CH 1 to CH 2, CH 3, or CH 4, $V_{AB} = V_{DD}$, T_A = 25°C		0.2	1	%
DC CHARACTERISTICS POTENTIOMETER DIVIDER (Specifications Apply to All VRs)						
Resolution	N		8			Bits
Integral Nonlinearity[4]	INL		−4	±1	+4	LSB
Differential Nonlinearity[4]	DNL	V_{DD} = 5 V	−1	±1/4	+1	LSB
	DNL	V_{DD} = 3 V, T_A = 25°C	−1	±1/4	+1	LSB
	DNL	V_{DD} = 3 V, T_A = −40°C to +85°C	−1.5	±1/2	+1.5	LSB
Voltage Divider Tempco	$\Delta V_W/\Delta T$	Code = 80_H		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = FF_H	−1	−0.25	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	+0.1	+1	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A, V_B, V_W		0		V_{DD}	V
Capacitance[6] Ax, Bx	C_A, C_B	f = 1 MHz, measured to GND, code = 80_H		15		pF
Capacitance[6] Wx	C_W	f = 1 MHz, measured to GND, code = 80_H		80		pF
Shutdown Current[7]	I_{A_SD}	$V_A = V_{DD}$, V_B = 0 V, $\overline{SHDN}$ = 0		0.01	5	µA
Shutdown Wiper Resistance	R_{W_SD}	$V_A = V_{DD}$, V_B = 0 V, $\overline{SHDN}$ = 0, V_{DD} = 5 V		100	200	Ω
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Output Logic High	V_{OH}	R_L = 2.2 kΩ to V_{DD}	V_{DD} − 0.1			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{DD} = 5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V, V_{DD} = 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD} range		2.7		5.5	V
Supply Current (CMOS)	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = 0 V		0.01	5	µA
Supply Current (TTL)[8]	I_{DD}	V_{IH} = 2.4 V or 0.8 V, V_{DD} = 5.5 V		0.9	4	mA
Power Dissipation (CMOS)[9]	P_{DISS}	$V_{IH} = V_{DD}$ or V_{IL} = 0 V, V_{DD} = 5.5 V			27.5	µW
Power Supply Sensitivity	PSS	V_{DD} = 5 V ± 10%		0.0002	0.001	%/%
	PSS	V_{DD} = 3 V ± 10%		0.006	0.03	%/%

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[6, 10]						
Bandwidth –3 dB	BW_50 K	R = 50 kΩ		125		kHz
	BW_100 K	R = 100 kΩ		71		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms + 2 V dc, V_B = 2 V dc, f = 1 kHz		0.003		%
V_W Settling Time	t_S_50 K	$V_A = V_{DD}$, V_B = 0 V, ±1% error band		9		µs
	t_S_100 K	$V_A = V_{DD}$, V_B = 0 V, ±1% error band		18		µs
Resistor Noise Voltage	e_{NWB}_50 K	R_{WB} = 25 kΩ, f = 1 kHz, $\overline{RS}$ = 0		20		nV/√Hz
	e_{NWB}_100 K	R_{WB} = 50 kΩ, f = 1 kHz, $\overline{RS}$ = 0		29		nV/√Hz
Crosstalk[11]	C_T	$V_A = V_{DD}$, V_B = 0 V		–65		dB

[1] Typicals represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See the test circuit in Figure 38. $I_W = V_{DD}/R$ for V_{DD} = 3 V or 5 V for the 50 kΩ and 100 kΩ versions.
[3] $V_{AB} = V_{DD}$, wiper (V_W) = no connect.
[4] INL and DNL are measured at VW with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions. See the test circuit in Figure 37.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test. Resistor-terminal capacitance tests are measured with 2.5 V bias on the measured terminal. The remaining resistor terminals are left open circuit.
[7] Measured at the Ax terminals. All Ax terminals are open-circuited in shutdown mode.
[8] Worst-case supply current consumed when input logic level at 2.4 V, standard characteristic of CMOS logic. See Figure 28 for a plot of I_{DD} vs. logic voltage.
[9] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[10] All dynamic characteristics use V_{DD} = 5 V.
[11] Measured at a V_W pin where an adjacent V_W pin is making a full-scale voltage change.

ELECTRICAL CHARACTERISTICS—1 KΩ VERSION

V_{DD} = 3 V ± 10% or 5 V ± 10%, $V_A = V_{DD}$, V_B = 0 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE (Specifications Apply to All VRs)						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = no connect	−5	−1	+3	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−4	±1.5	+4	LSB
Nominal Resistance[3]	R_{AB}	T_A = 25°C, model: AD840XYY1	0.8	1.2	1.6	kΩ
Resistance Tempco	$\Delta R_{AB}/\Delta T$	$V_{AB} = V_{DD}$, wiper = no connect		700		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5V, $I_W = V_{DD}/R_{AB}$		53	100	Ω
	R_W	V_{DD} = 3V, $I_W = V_{DD}/R_{AB}$		200		Ω
Nominal Resistance Match	$\Delta R/R_{AB}$	CH 1 to CH 2, $V_{AB} = V_{DD}$, T_A = 25°C		0.75	2	%
DC CHARACTERISTICS POTENTIOMETER DIVIDER (Specifications Apply to All VRs)						
Resolution	N		8			Bits
Integral Nonlinearity[4]	INL		−6	±2	+6	LSB
Differential Nonlinearity[4]	DNL	V_{DD} = 5 V	−4	−1.5	+2	LSB
	DNL	V_{DD} = 3 V, T_A = 25°C	−5	−2	+5	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 80H		25		ppm/°C
Full-Scale Error	V_{WFSE}	Code = FF_H	−20	−12	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	6	10	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A, V_B, V_W		0		V_{DD}	V
Capacitance[6] Ax, Bx	C_A, C_B	f = 1 MHz, measured to GND, code = 80_H		75		pF
Capacitance[6] Wx	C_W	f = 1 MHz, measured to GND, code = 80_H		120		pF
Shutdown Supply Current[7]	I_{A_SD}	$V_A = V_{DD}$, V_B = 0 V, $\overline{SHDN} = 0$		0.01	5	µA
Shutdown Wiper Resistance	R_{W_SD}	$V_A = V_{DD}$, V_B = 0 V, $\overline{SHDN} = 0$, V_{DD} = 5 V		50	100	Ω
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Output Logic High	V_{OH}	R_L = 2.2 kΩ to V_{DD}	V_{DD} − 0.1			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{DD} = 5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V, V_{DD} = 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD} range		2.7		5.5	V
Supply Current (CMOS)	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = 0 V		0.01	5	µA
Supply Current (TTL)[8]	I_{DD}	V_{IH} = 2.4 V or 0.8 V, V_{DD} = 5.5 V		0.9	4	mA
Power Dissipation (CMOS)[9]	P_{DISS}	$V_{IH} = V_{DD}$ or V_{IL} = 0 V, V_{DD} = 5.5 V			27.5	µW
Power Supply Sensitivity	PSS	ΔV_{DD} = 5 V ± 10%		0.0035	0.008	%/%
	PSS	ΔV_{DD} = 3 V ± 10%		0.05	0.13	%/%

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[6, 10]						
Bandwidth −3 dB	BW_1 K	R = 1 kΩ		5,000		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms + 2 V dc, V_B = 2 V dc, f = 1 kHz		0.015		%
V_W Settling Time	t_S	$V_A = V_{DD}$, V_B = 0 V, ±1% error band		0.5		µs
Resistor Noise Voltage	e_{NWB}	R_{WB} = 500 Ω, f = 1 kHz, $\overline{RS}$ = 0		3		nV/√Hz
Crosstalk[11]	C_T	$V_A = V_{DD}$, V_B = 0 V		−65		dB

[1] Typicals represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. See the test circuit in Figure 38. I_W = 500 µA for V_{DD} = 3 V and I_W = 2.5 mA for V_{DD} = 5 V for 1 kΩ version.
[3] $V_{AB} = V_{DD}$, wiper (V_W) = no connect.
[4] INL and DNL are measured at VW with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions. See the test circuit in Figure 37.
[5] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test. Resistor-terminal capacitance tests are measured with 2.5 V bias on the measured terminal. The remaining resistor terminals are left open circuit.
[7] Measured at the Ax terminals. All Ax terminals are open-circuited in shutdown mode.
[8] Worst-case supply current is consumed when the input logic level is at 2.4 V, a standard characteristic of CMOS logic. See Figure 28 for a plot of I_{DD} vs. logic voltage.
[9] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[10] All dynamic characteristics use V_{DD} = 5 V.
[11] Measured at a V_W pin where an adjacent V_W pin is making a full-scale voltage change.

ELECTRICAL CHARACTERISTICS—ALL VERSIONS

V_{DD} = 3 V ± 10% or 5 V ± 10%, $V_A = V_{DD}$, V_B = 0 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
SWITCHING CHARACTERISTICS[2, 3]						
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock level high or low	10			ns
Data Setup Time	t_{DS}		5			ns
Data Hold Time	t_{DH}		5			ns
CLK to SDO Propagation Delay[4]	t_{PD}	R_L = 1 kΩ to 5 V, C_L ≤ 20 pF	1		25	ns
$\overline{CS}$ Setup Time	t_{CSS}		10			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		10			ns
Reset Pulse Width	t_{RS}		50			ns
CLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		10			ns

[1] Typicals represent average readings at 25°C and V_{DD} = 5 V.
[2] Guaranteed by design and not subject to production test. Resistor-terminal capacitance tests are measured with 2.5 V bias on the measured terminal. The remaining resistor terminals are left open circuit.
[3] See the timing diagram in Figure 3 for location of measured values. All input control voltages are specified with $t_R = t_F$ = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. Switching characteristics are measured using V_{DD} = 3 V or 5 V. To avoid false clocking, a minimum input logic slew rate of 1 V/µs should be maintained.
[4] Propagation delay depends on the value of V_{DD}, R_L, and C_L (see the Applications section).

TIMING DIAGRAMS

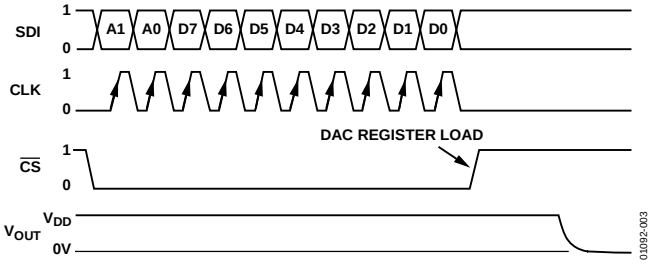


Figure 3. Timing Diagram

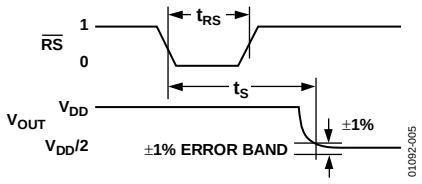


Figure 5. Reset Timing Diagram

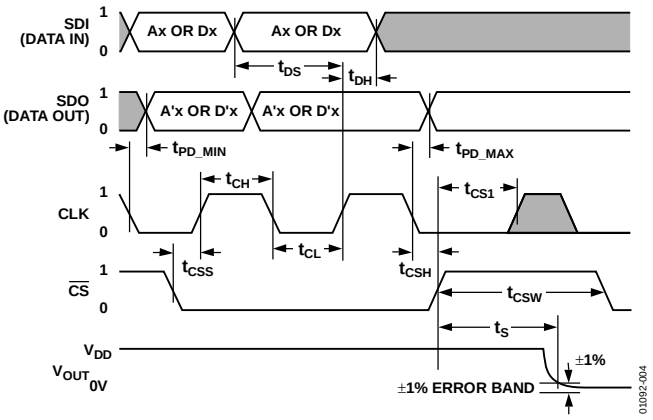


Figure 4. Detailed Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V, +8 V
V_A, V_B, V_W to GND	0 V, V_{DD}
Maximum Current	
I_{WB}, I_{WA} Pulsed	±20 mA
I_{WB} Continuous (R_{WB} ≤ 1 kΩ, A Open)[1]	±5 mA
I_{WA} Continuous (R_{WA} ≤ 1 kΩ, B Open)[1]	±5 mA
I_{AB} Continuous (R_{AB} = 1 kΩ/10 kΩ/ 50 kΩ/100 kΩ)[1]	±2.1 mA/±2.1 mA/ ±540 µA/±540 µA
Digital Input and Output Voltage to GND	0 V, 7 V
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature (T_J Maximum)	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Package Power Dissipation	(T_J max − T_A)/θ_{JA}
Thermal Resistance (θ_{JA})	
SOIC (R-8)	158°C/W
PDIP (N-14)	83°C/W
PDIP (N-24)	63°C/W
SOIC (R-14)	120°C/W
SOIC (R-24)	70°C/W
TSSOP-14 (RU-14)	180°C/W
TSSOP-24 (RU-24)	143°C/W

[1] Maximum terminal current is bounded by the maximum applied voltage across any two of the A, B, and W terminals at a given resistance, the maximum current handling of the switches, and the maximum power dissipation of the package; VDD = 5 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SERIAL DATA-WORD FORMAT

Table 6.

ADDR		DATA							
B9	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
MSB	LSB	MSB							LSB
2^9	2^8	2^7							2^0

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

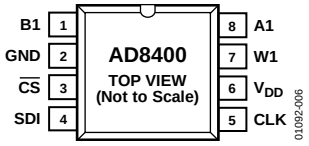


Figure 6. AD8400 Pin Configuration

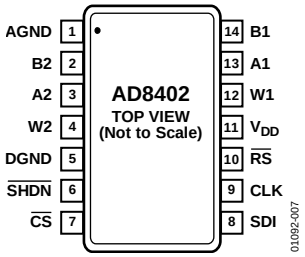


Figure 7. AD8402 Pin Configuration

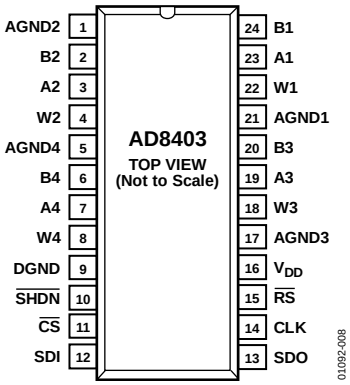


Figure 8. AD8403 Pin Configuration

Table 7. AD8400 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	B1	Terminal B RDAC.
2	GND	Ground.
3	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data in the serial input register is decoded, based on the address bits, and loaded into the target DAC register.
4	SDI	Serial Data Input.
5	CLK	Serial Clock Input, Positive Edge Triggered.
6	V_{DD}	Positive Power Supply. Specified for operation at both 3 V and 5 V.
7	W1	Wiper RDAC, Addr = 00_2.
8	A1	Terminal A RDAC.

Table 8. AD8402 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AGND	Analog Ground.[1]
2	B2	Terminal B RDAC 2.
3	A2	Terminal A RDAC 2.
4	W2	Wiper RDAC 2, Addr = 01_2.
5	DGND	Digital Ground.[1]
6	$\overline{SHDN}$	Terminal A Open Circuit. Shutdown controls Variable Resistor 1 and Variable Resistor 2.
7	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data in the serial input register is decoded, based on the address bits, and loaded into the target DAC register.
8	SDI	Serial Data Input.
9	CLK	Serial Clock Input, Positive Edge Triggered.
10	$\overline{RS}$	Active Low Reset to Midscale. Sets RDAC registers to 80_H.
11	V_{DD}	Positive Power Supply. Specified for operation at both 3 V and 5 V
12	W1	Wiper RDAC 1, Addr = 00_2.
13	A1	Terminal A RDAC 1.
14	B1	Terminal B RDAC 1.

[1] All AGND pins must be connected to DGND.

Table 9. AD8403 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AGND2	Analog Ground 2.[1]
2	B2	Terminal B RDAC 2.
3	A2	Terminal A RDAC 2.
4	W2	Wiper RDAC 2, Addr = 01_2.
5	AGND4	Analog Ground 4.[1]
6	B4	Terminal B RDAC 4.
7	A4	Terminal A RDAC 4.
8	W4	Wiper RDAC 4, Addr = 11_2.
9	DGND	Digital Ground.[1]
10	$\overline{SHDN}$	Active Low Input. Terminal A open circuit. Shutdown controls Variable Resistor 1 through Variable Resistor 4.
11	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data in the serial input register is decoded, based on the address bits, and loaded into the target DAC register.
12	SDI	Serial Data Input.
13	SDO	Serial Data Output. Open drain transistor requires a pull-up resistor.
14	CLK	Serial Clock Input, Positive Edge Triggered.
15	$\overline{RS}$	Active Low Reset to Midscale. Sets RDAC registers to 80_H.
16	V_{DD}	Positive Power Supply. Specified for operation at both 3 V and 5 V.
17	AGND3	Analog Ground 3.[1]
18	W3	Wiper RDAC 3, Addr = 10_2.
19	A3	Terminal A RDAC 3.
20	B3	Terminal B RDAC 3.
21	AGND1	Analog Ground 1.[1]
22	W1	Wiper RDAC 1, Addr = 00_2.
23	A1	Terminal A RDAC 1.
24	B1	Terminal B RDAC 1.

[1] All AGND pins must be connected to DGND.

TYPICAL PERFORMANCE CHARACTERISTICS

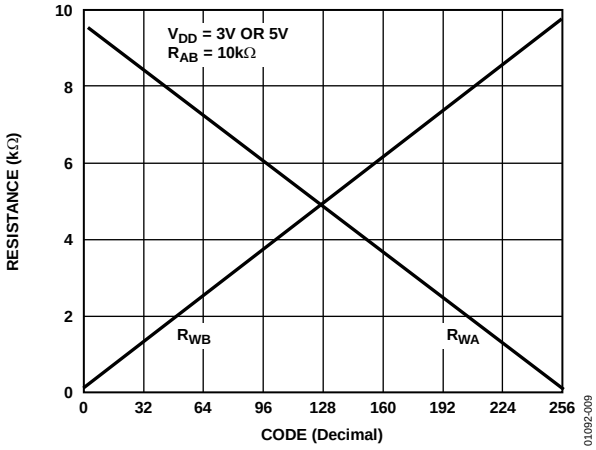


Figure 9. Wiper to End Terminal Resistance vs. Code

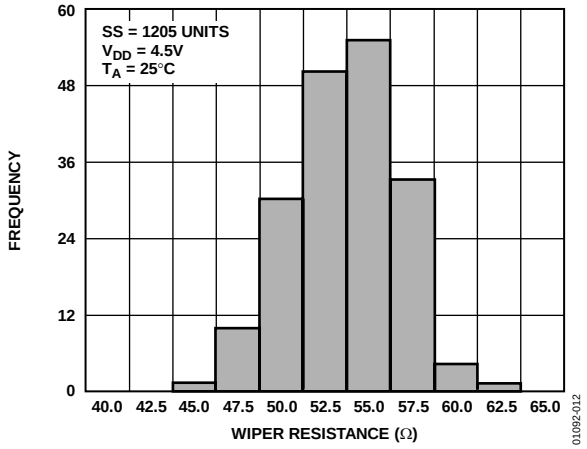


Figure 12. 10 kΩ Wiper-Contact-Resistance Histogram

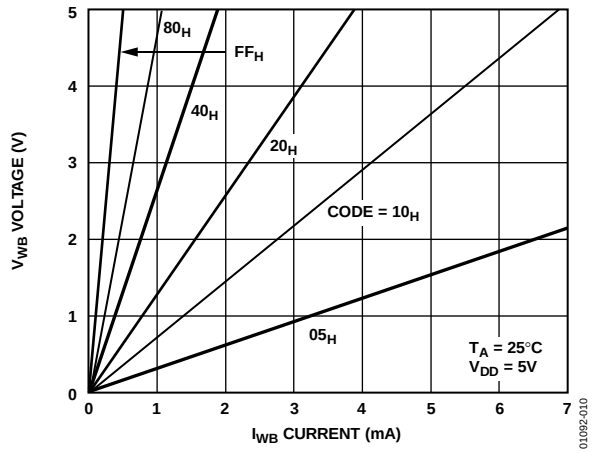


Figure 10. Resistance Linearity vs. Conduction Current

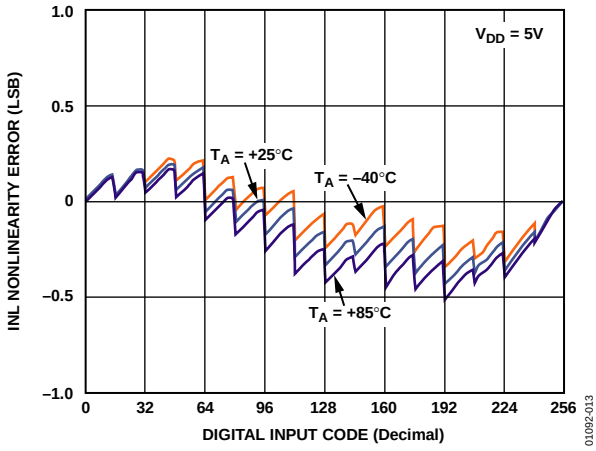


Figure 13. Potentiometer Divider Nonlinearity Error vs. Code

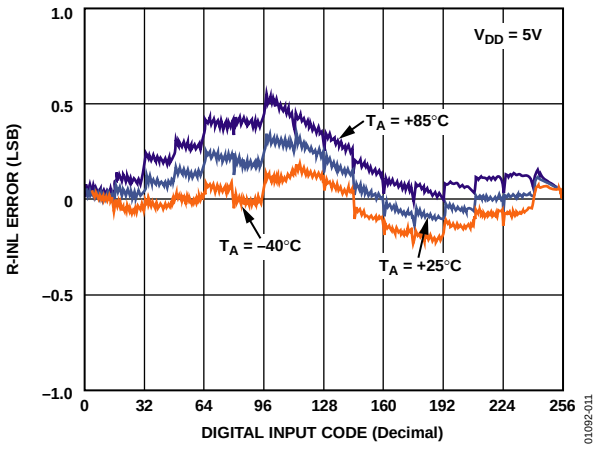


Figure 11. Resistance Step Position Nonlinearity Error vs. Code

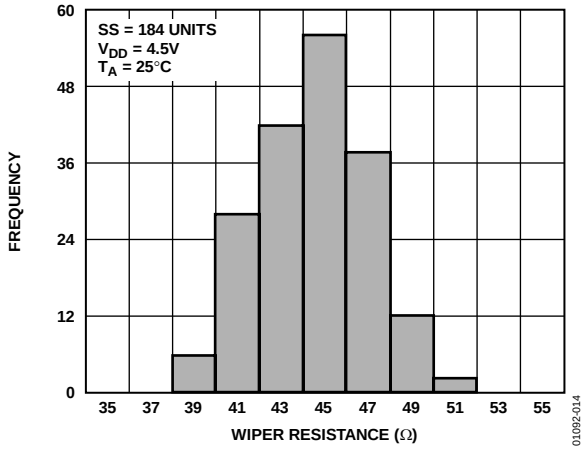


Figure 14. 50 kΩ Wiper-Contact-Resistance Histogram

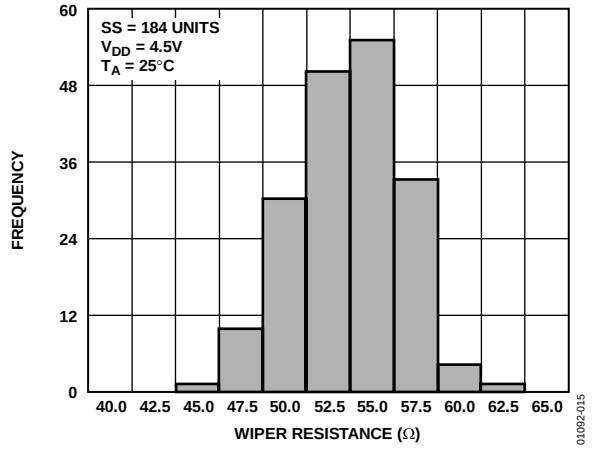


Figure 15. 100 kΩ Wiper-Contact-Resistance Histogram

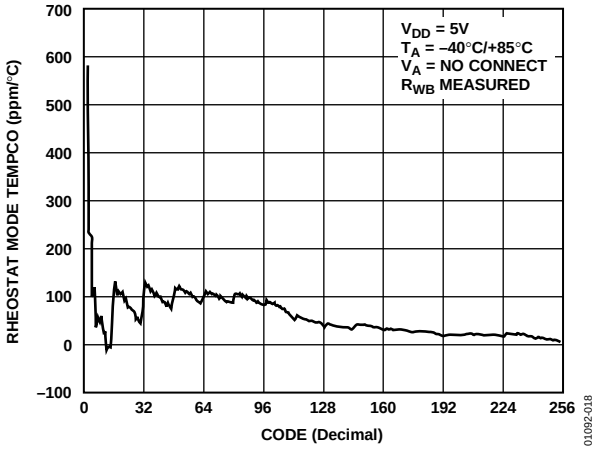


Figure 18. $\Delta R_{WB}/\Delta T$ Rheostat Mode Tempco

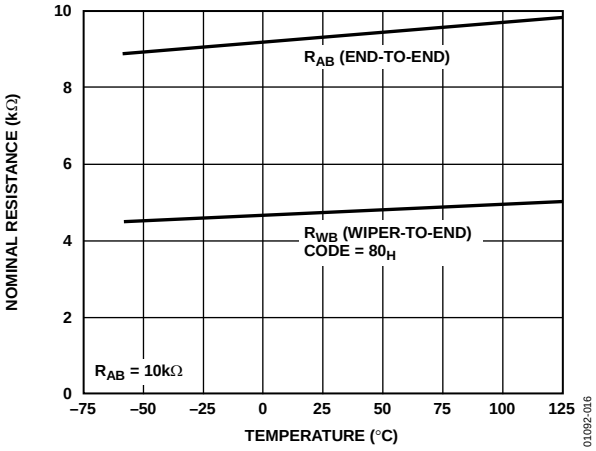


Figure 16. Nominal Resistance vs. Temperature

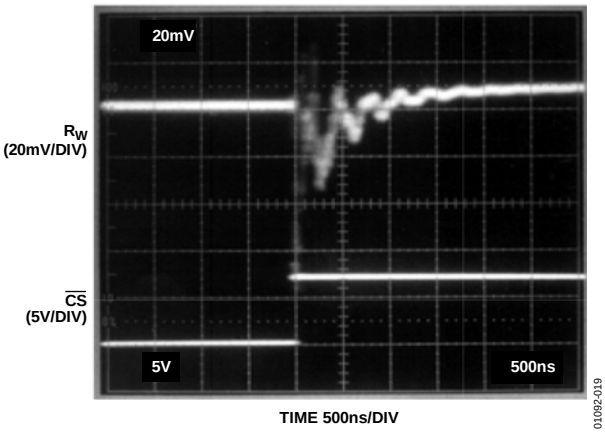


Figure 19. One Position Step Change at Half-Scale (Code $7F_H$ to 80_H)

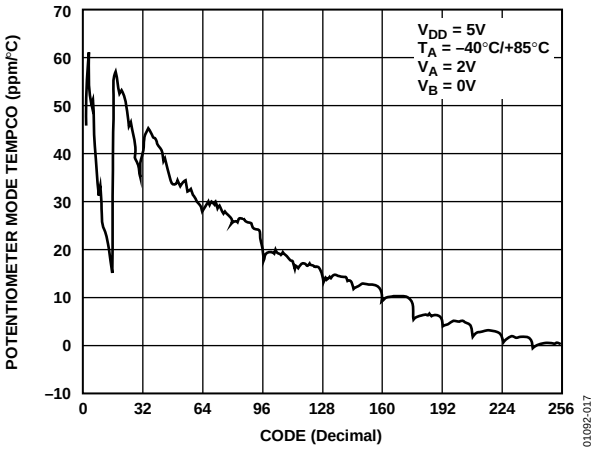


Figure 17. $\Delta V_{WB}/\Delta T$ Potentiometer Mode Tempco

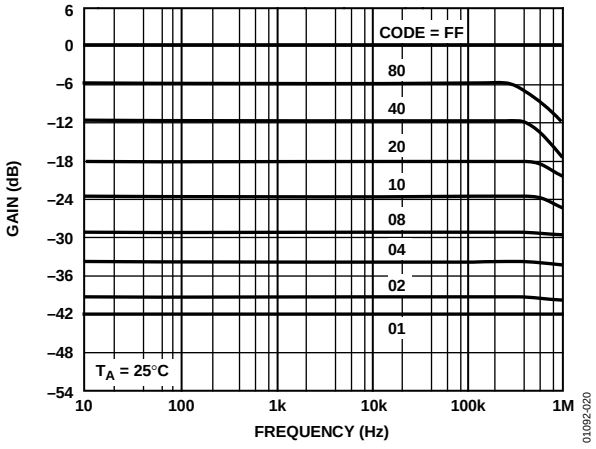


Figure 20. 10 kΩ Gain vs. Frequency vs. Code (See Figure 43)

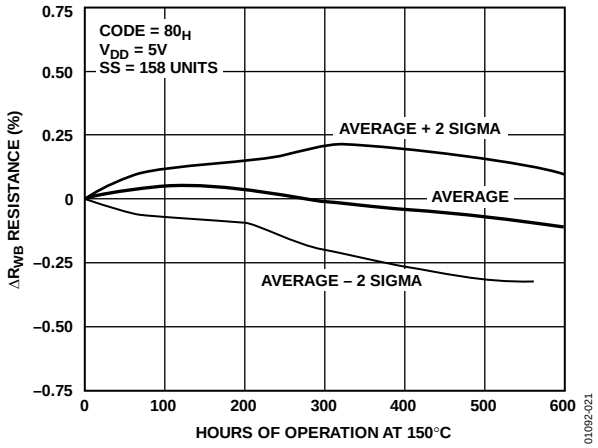


Figure 21. Long-Term Drift Accelerated by Burn-In

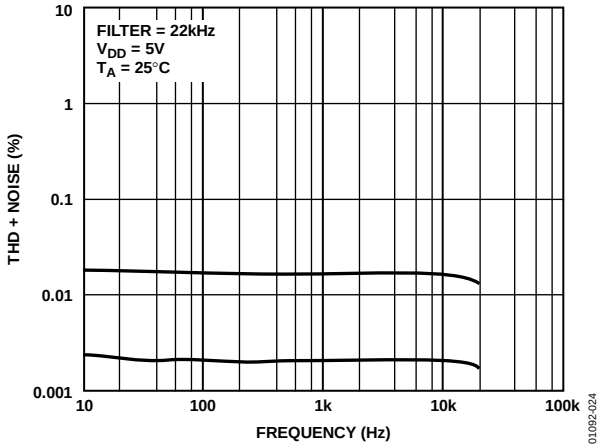


Figure 24. Total Harmonic Distortion Plus Noise vs. Frequency (See Figure 41 and Figure 42)

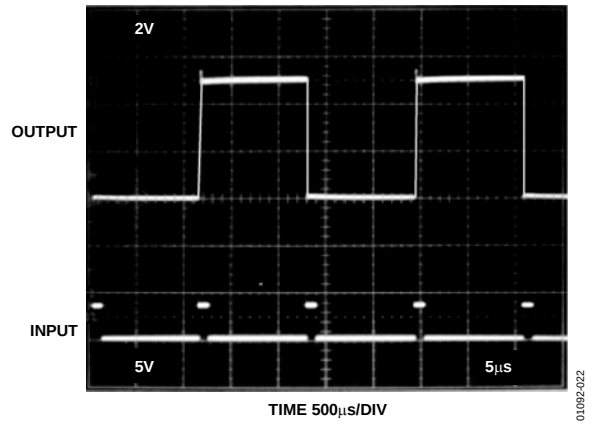


Figure 22. Large Signal Settling Time

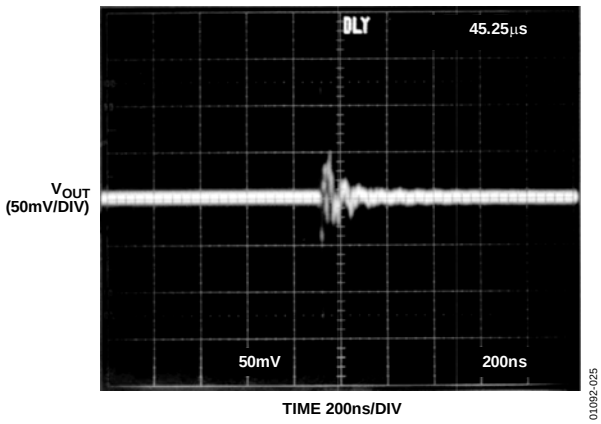


Figure 25. Digital Feedthrough vs. Time

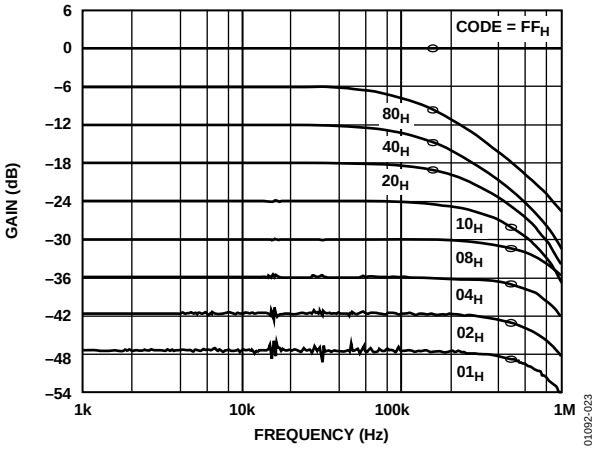


Figure 23. 50 kΩ Gain vs. Frequency vs. Code

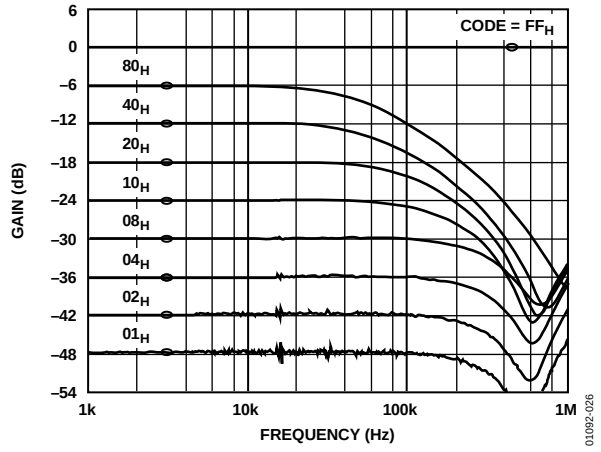


Figure 26. 100 kΩ Gain vs. Frequency vs. Code

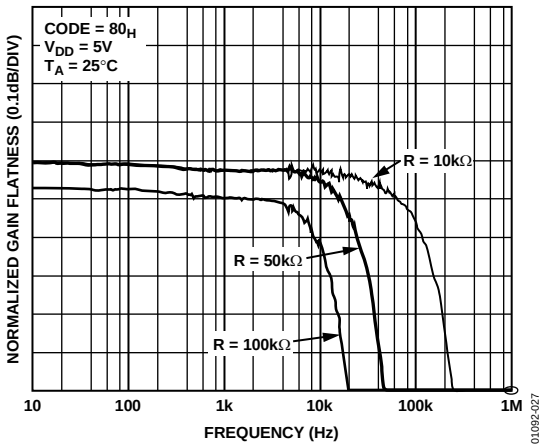


Figure 27. Normalized Gain Flatness vs. Frequency (See Figure 43)

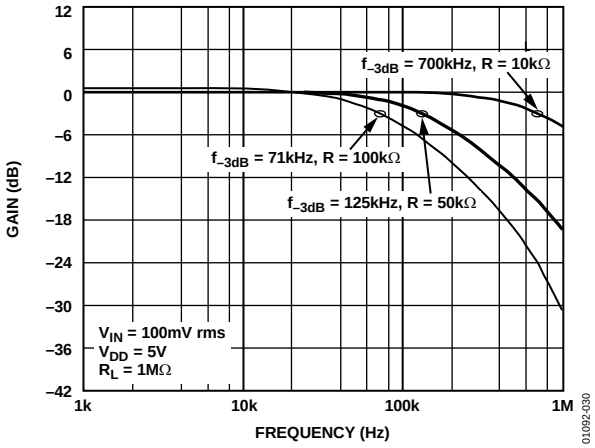


Figure 30. –3 dB Bandwidths

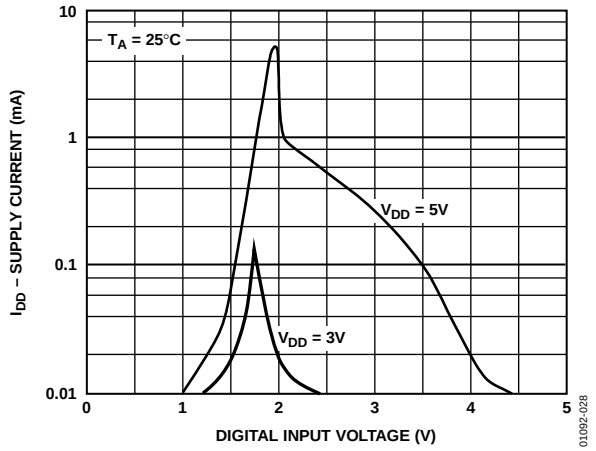


Figure 28. Supply Current vs. Digital Input Voltage

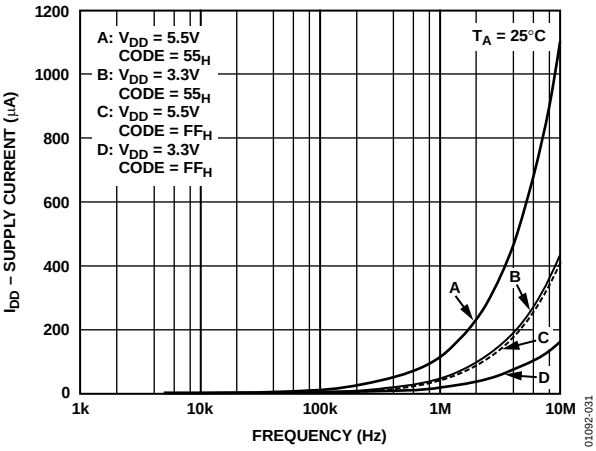


Figure 31. Supply Current vs. Clock Frequency

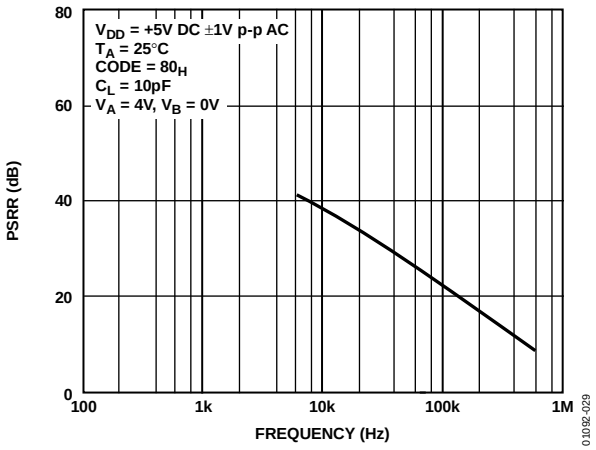


Figure 29. Power Supply Rejection Ratio vs. Frequency (See Figure 40)

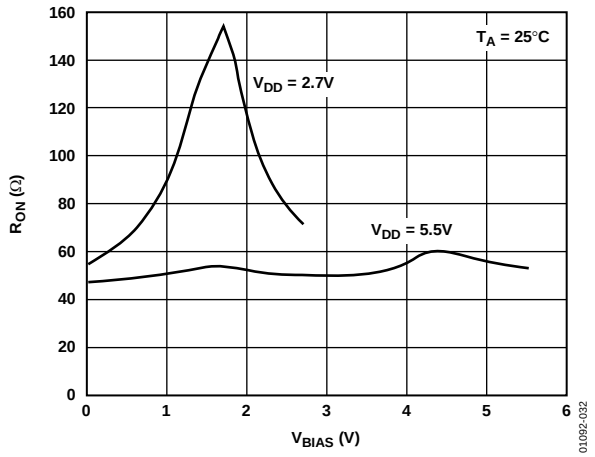


Figure 32. AD8403 Incremental Wiper On Resistance vs. V_{DD} (See Figure 39)

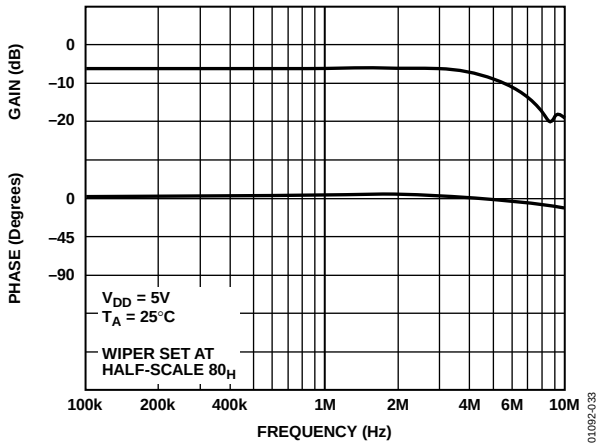


Figure 33. 1 kΩ Gain and Phase vs. Frequency

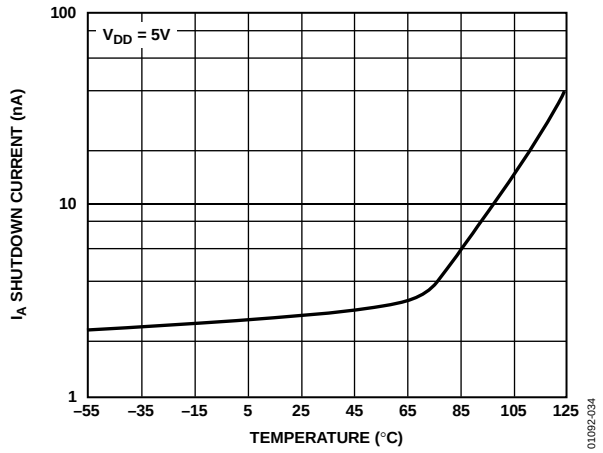


Figure 34. Shutdown Current vs. Temperature

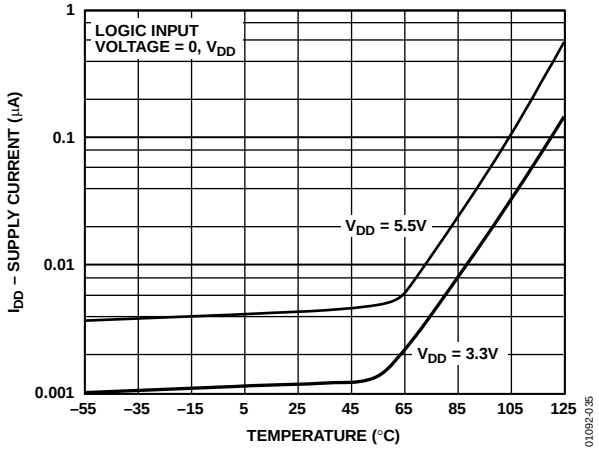


Figure 35. Supply Current vs. Temperature

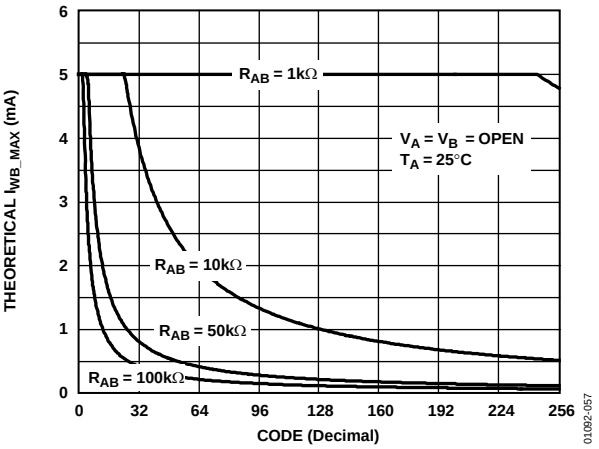


Figure 36. I_{WB_MAX} vs. Code

TEST CIRCUITS

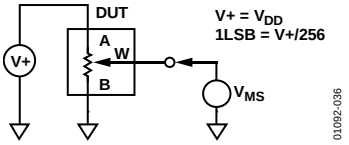


Figure 37. Potentiometer Divider Nonlinearity Error (INL, DNL)

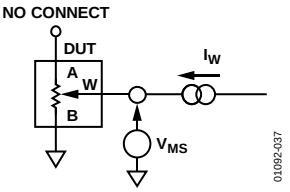


Figure 38. Resistor Position Nonlinearity Error (Rheostat Operations; R-INL, R-DNL)

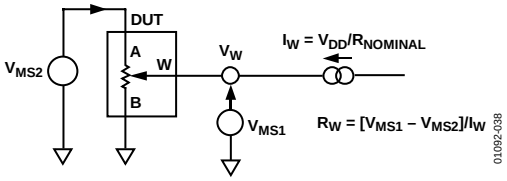


Figure 39. Wiper Resistance

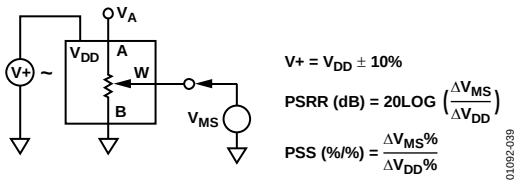


Figure 40. Power Supply Sensitivity (PSS, PSRR)

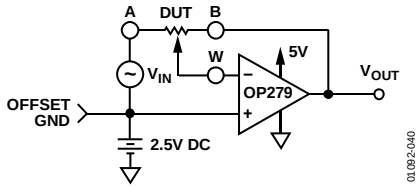


Figure 41. Inverting Programmable Gain

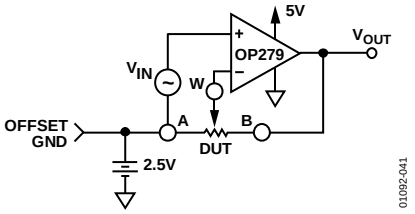


Figure 42. Noninverting Programmable Gain

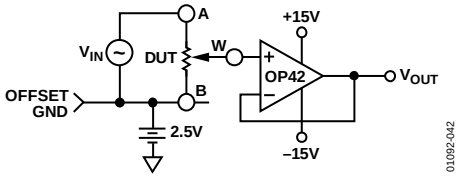


Figure 43. Gain vs. Frequency

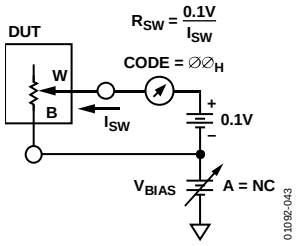


Figure 44. Incremental On Resistance

THEORY OF OPERATION

The AD8400/AD8402/AD8403 provide a single, dual, and quad channel, 256-position, digitally controlled variable resistor (VR) device. Changing the programmed VR setting is accomplished by clocking in a 10-bit serial data-word into the SDI (Serial Data Input) pin. The format of this data-word is two address bits, MSB first, followed by eight data bits, also MSB first. Table 6 provides the serial register data-word format. The AD8400/AD8402/AD8403 have the following address assignments for the ADDR decoder, which determines the location of the VR latch receiving the serial register data in Bit B7 to Bit B0:

$$VR\# = A1 \times 2 + A0 + 1 \quad (1)$$

The single-channel AD8400 requires A1 = A0 = 0. The dual-channel AD8402 requires A1 = 0. VR settings can be changed one at a time in random sequence. A serial clock running at 10 MHz makes it possible to load all four VRs under 4 µs (10 × 4 × 100 ns) for AD8403. The exact timing requirements are shown in Figure 3, Figure 4, and Figure 5.

The AD8400/AD8402/AD8403 do not have power-on midscale preset, so the wiper can be at any random position at power-up. However, the AD8402/AD8403 can be reset to midscale by asserting the $\overline{RS}$ pin, simplifying initial conditions at power-up. Both parts have a power shutdown $\overline{SHDN}$ pin that places the VR in a zero-power-consumption state where Terminal Ax is open-circuited and the Wiper Wx is connected to Terminal Bx, resulting in the consumption of only the leakage current in the VR. In shutdown mode, the VR latch settings are maintained so that upon returning to the operational mode, the VR settings return to the previous resistance values. The digital interface is still active in shutdown, except that SDO is deactivated. Code changes in the registers can be made during shutdown that will produce new wiper positions when the device is taken out of shutdown.

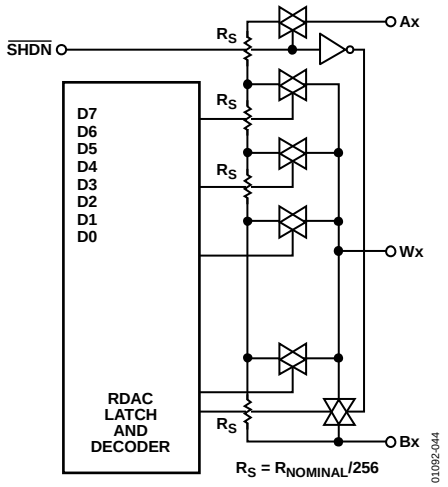


Figure 45. AD8402/AD8403 Equivalent VR (RDAC) Circuit

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the VR (RDAC) between Terminal A and Terminal B is available with values of 1 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The final digits of the part number determine the nominal resistance value; that is, 10 kΩ = 10; 100 kΩ = 100. The nominal resistance (R_{AB}) of the VR has 256 contact points accessible by the wiper terminal, and the resulting resistance can be measured either across the wiper and B terminals (R_{WB}) or across the wiper and A terminals (R_{WA}). The 8-bit data-word loaded into the RDAC latch is decoded to select one of the 256 possible settings. The wiper's first connection starts at the B terminal for data 00_H. This B terminal connection has a wiper contact resistance of 50 Ω. The second connection (for the 10 kΩ part) is the first tap point located at 89 Ω = [R_{AB} (nominal resistance) + R_W = 39 Ω + 50 Ω] for data 01_H. The third connection is the next tap point representing 78 Ω + 50 Ω = 128 Ω for data 02_H. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,011 Ω. Note that the wiper does not directly connect to the B terminal even for data 00_H. See Figure 45 for a simplified diagram of the equivalent RDAC circuit.

The AD8400 contains one RDAC, the AD8402 contains two independent RDACs, and the AD8403 contains four independent RDACs. The general transfer equation that determines the digitally programmed output resistance between Wx and Bx is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \quad (2)$$

where *D*, in decimal, is the data loaded into the 8-bit RDAC# latch, and R_{AB} is the nominal end-to-end resistance.

For example, when the A terminal is either open-circuited or tied to the Wiper W, the following RDAC latch codes result in the following R_{WB} (for the 10 kΩ version):

Table 10.

D (Dec)	R_{WB} (Ω)	Output State
255	10,011	Full scale
128	5,050	Midscale ($\overline{RS}$ = 0 condition)
1	89	1 LSB
0	50	Zero-scale (wiper contact resistance)

Note that in the zero-scale condition, a finite wiper resistance of 50 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum value of 5 mA to avoid degradation or possible destruction of the internal switch contact.

Like a mechanical potentiometer, RDAC is symmetrical. The resistance between the Wiper W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. When these terminals are used, the B terminal can be tied to the wiper or left floating. R_{WA} starts at the maximum and decreases as the data loaded into the RDAC latch increases. The general transfer equation for this R_{WA} is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \quad (3)$$

where D is the data loaded into the 8-bit RDAC# latch, and R_{AB} is the nominal end-to-end resistance.

For example, when the B terminal is either open-circuited or tied to the Wiper W, the following RDAC latch codes result in the following R_{WA} (for the 10 kΩ version):

Table 11.

D (Dec)	R_{WA} (Ω)	Output State
255	89	Full-Scale
128	5,050	Midscale ($\overline{RS}$ = 0 Condition)
1	10,011	1 LSB
0	10,050	Zero-Scale

The typical distribution of RAB from channel to channel matches within ±1%. However, device-to-device matching is process lot dependent and has a ±20% variation. The temperature coefficient, or the change in R_{AB} with temperature, is 500 ppm/°C.

The wiper-to-end-terminal resistance temperature coefficient has the best performance over the 10% to 100% of adjustment range where the internal wiper contact switches do not contribute any significant temperature related errors. The graph in Figure 18 shows the performance of R_{WB} tempco vs. code. Using the potentiometer with codes below 32 results in the larger temperature coefficients plotted.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates an output voltage proportional to the input voltage applied to a given terminal.

For example, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper starting at 0 V up to 1 LSB less than 5 V. Each LSB is equal to the voltage applied across the A to B terminals divided by the 256-position resolution of the potentiometer divider. The general equation defining the output voltage with respect to ground for any given input voltage applied to the A to B terminals is

$$V_W = \frac{D}{256} \times V_{AB} + V_B \quad (4)$$

Operation of the digital potentiometer in the voltage divider mode results in more accurate operation over temperature. Here the output voltage is dependent on the ratio of the internal resistors, not the absolute value; therefore, the temperature drift improves to 15 ppm/°C.

At the lower wiper position settings, the potentiometer divider temperature coefficient increases because the contribution of the CMOS switch wiper resistance becomes an appreciable portion of the total resistance from the B terminal to the Wiper W. See Figure 17 for a plot of potentiometer tempco performance vs. code setting.

DIGITAL INTERFACING

The AD8400/AD8402/AD8403 contain a standard SPI-compatible, 3-wire, serial input control interface. The three inputs are clock (CLK), chip select ($\overline{CS}$), and serial data input (SDI). The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. For the best result, use logic transitions faster than 1 V/µs. Standard logic families work well. If mechanical switches are used for product evaluation, they should be debounced by a flip-flop or other suitable means. The block diagrams in Figure 46, Figure 47, and Figure 48 show the internal digital circuitry in more detail. When $\overline{CS}$ is taken active low, the clock loads data into the 10-bit serial register on each positive clock edge (see Table 12).

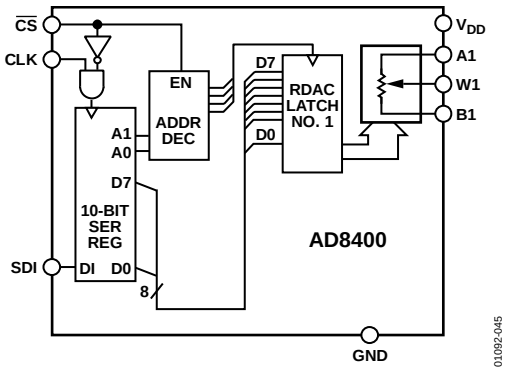


Figure 46. AD8400 Block Diagram

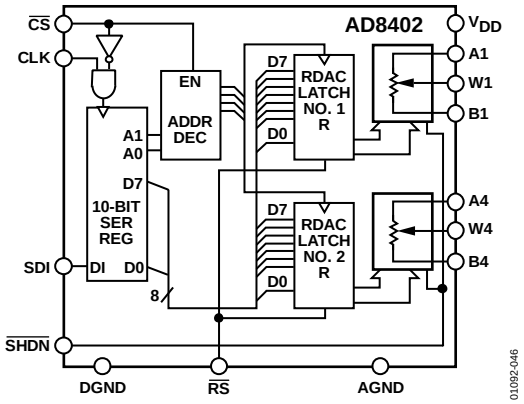


Figure 47. AD8402 Block Diagram

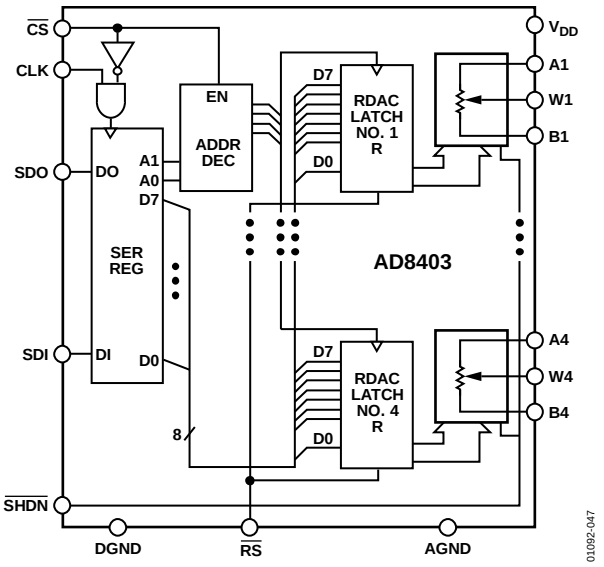


Figure 48. AD8403 Block Diagram

Table 12. Input Logic Control Truth Table[1]

CLK	$\overline{CS}$	$\overline{RS}$	$\overline{SHDN}$	Register Activity
L	L	H	H	No SR effect; enables SDO pin
P	L	H	H	Shift one bit in from the SDI pin. The 10th previously entered bit is shifted out of the SDO pin.
X	P	H	H	Load SR data into RDAC latch based on A1, A0 decode (Table 13).
X	H	H	H	No operation
X	X	L	H	Sets all RDAC latches to midscale, wiper centered, and SDO latch cleared
X	H	P	H	Latches all RDAC latches to 80_H
X	H	H	L	Open-circuits all Resistor A terminals, connects W to B, turns off SDO output transistor.

[1] P = positive edge, X = don't care, SR = shift register

The serial data output (SDO) pin, which exists only on the AD8403 and not on the AD8400 or AD8402, contains an open-drain, n-channel FET that requires a pull-up resistor to transfer data to the SDI pin of the next package. The pull-up resistor termination voltage may be larger than the V_{DD} supply (but less than the max V_{DD} of 8 V) of the AD8403 SDO output device. For example, the AD8403 could operate at V_{DD} = 3.3 V, and the pull-up for interface to the next device could be set at 5 V. This allows for daisy-chaining several RDACs from a single processor serial data line. The clock period needs to be increased when using a pull-up resistor to the SDI pin of the following device in the series. Capacitive loading at the daisy-chain node SDO to SDI between devices must be accounted for in order to transfer data successfully. When daisy chain is used, $\overline{CS}$ should be kept low until all the bits of every package are clocked into their respective serial registers and the address and data bits are in the proper decoding location.

If two AD8403 RDACs are daisy-chained, it requires 20 bits of address and data in the format shown in Table 6. During shutdown ($\overline{SHDN}$ = logic low), the SDO output pin is forced to the off (logic high) state to disable power dissipation in the pull-up resistor. See Figure 50 for equivalent SDO output circuit schematic.

The data setup and hold times in the specification table determine the data valid time requirements. The last 10 bits of the data-word entered into the serial register are held when $\overline{CS}$ returns high. At the same time $\overline{CS}$ goes high it gates the address decoder, which enables one of the two (AD8402) or four (AD8403) positive edge-triggered RDAC latches. See Figure 49 and Table 13.

Table 13. Address Decode Table

A1	A0	Latch Decoded
0	0	RDAC#1
0	1	RDAC#2
1	0	RDAC#3 AD8403 Only
1	1	RDAC#4 AD8403 Only

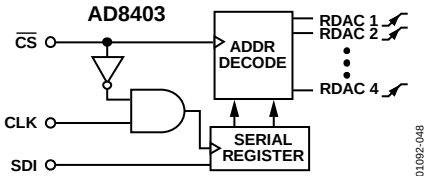


Figure 49. Equivalent Input Control Logic

The target RDAC latch is loaded with the last eight bits of the serial data-word completing one RDAC update. In the case of AD8403, four separate 10-bit data-words must be clocked in to change all four VR settings.

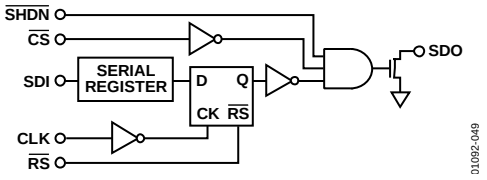


Figure 50. Detailed SDO Output Schematic of the AD8403

All digital pins are protected with a series input resistor and parallel Zener ESD structure shown in Figure 51. This structure applies to digital pins $\overline{CS}$, SDI, SDO, $\overline{RS}$, $\overline{SHDN}$, and CLK. The digital input ESD protection allows for mixed power supply applications where 5 V CMOS logic can be used to drive an AD8400, AD8402, or AD8403 operating from a 3 V power supply. Analog Pin A, Pin B, and Pin W are protected with a 20 Ω series resistor and parallel Zener diode (see Figure 52).

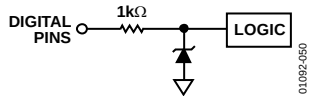


Figure 51. Equivalent ESD Protection Circuits

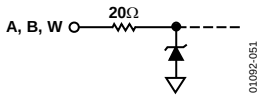


Figure 52. Equivalent ESD Protection Circuit (Analog Pins)

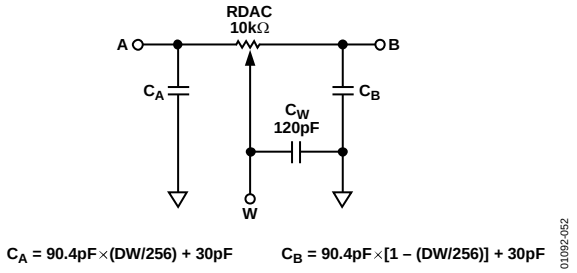


Figure 53. RDAC Circuit Simulation Model for RDAC = 10 kΩ

The AC characteristics of the RDAC are dominated by the internal parasitic capacitances and the external capacitive loads. The −3 dB bandwidth of the AD8403AN10 (10 kΩ resistor) measures 600 kHz at half scale as a potentiometer divider. Figure 30 provides the large signal Bode plot characteristics of the three available resistor versions 10 kΩ, 50 kΩ, and 100 kΩ. The gain flatness vs. frequency graph of the 1 kΩ version predicts filter applications performance (see Figure 33). A parasitic simulation model has been developed and is shown in Figure 53. Listing I provides a macro model net list for the 10 kΩ RDAC.

Listing I. Macro Model Net List for RDAC

```
.PARAM DW=255, RDAC=10E3
*
.SUBCKT DPOT (A,W,)
*
CA A 0 {DW/256*90.4E-12+30E-12}
RAW A W {(1-DW/256)*RDAC+50}
CW W 0 120E-12
RBW W B {DW/256*RDAC+50}
CB B 0 {(1-DW/256)*90.4E-12+30E-12}
*
.ENDS DPOT
```

The total harmonic distortion plus noise (THD + N), shown in Figure 41, is measured at 0.003% in an inverting op amp circuit using an offset ground and a rail-to-rail OP279 amplifier. Thermal noise is primarily Johnson noise, typically 9 nV/√Hz for the 10 kΩ version at f = 1 kHz. For the 100 kΩ device, thermal noise becomes 29 nV/√Hz. Channel-to-channel crosstalk measures less than −65 dB at f = 100 kHz. To achieve this isolation, the extra ground pins provided on the package to segregate the individual RDACs must be connected to circuit ground. AGND and DGND pins should be at the same voltage potential. Any unused potentiometers in a package should be connected to ground. Power supply rejection is typically −35 dB at 10 kHz. Care is needed to minimize power supply ripple in high accuracy applications.

APPLICATIONS

The digital potentiometer (RDAC) allows many of the applications of a mechanical potentiometer to be replaced by a solid-state solution offering compact size and freedom from vibration, shock, and open contact problems encountered in hostile environments. A major advantage of the digital potentiometer is its programmability. Any settings can be saved for later recall in system memory.

The two major configurations of the RDAC include the potentiometer divider (basic 3-terminal application) and the rheostat (2-terminal configuration) connections shown in Figure 37 and Figure 38.

Certain boundary conditions must be satisfied for proper AD8400/AD8402/AD8403 operation. First, all analog signals must remain within the GND to V_{DD} range used to operate the single-supply AD8400/AD8402/AD8403. For standard potentiometer divider applications, the wiper output can be used directly. For low resistance loads, buffer the wiper with a suitable rail-to-rail op amp such as the OP291 or the OP279. Second, for ac signals and bipolar dc adjustment applications, a virtual ground is generally needed. Whichever method is used to create the virtual ground, the result must provide the necessary sink and source current for all connected loads, including adequate bypass capacitance. Figure 41 shows one channel of the AD8402 connected in an inverting programmable gain amplifier circuit. The virtual ground is set at 2.5 V, which allows the circuit output to span a ±2.5 V range with respect to virtual ground. The rail-to-rail amplifier capability is necessary for the widest output swing. As the wiper is adjusted from its midscale reset position (80_H) toward the A terminal (code FF_H), the voltage gain of the circuit is increased in successively larger increments. Alternatively, as the wiper is adjusted toward the B terminal (code 00_H), the signal becomes attenuated. The plot in Figure 54 shows the wiper settings for a 100:1 range of voltage gain (V/V). Note the ±10 dB of pseudologarithmic gain around 0 dB (1 V/V). This circuit is mainly useful for gain adjustments in the range of 0.14 V/V to 4 V/V; beyond this range the step sizes become very large, and the resistance of the driving circuit can become a significant term in the gain equation.

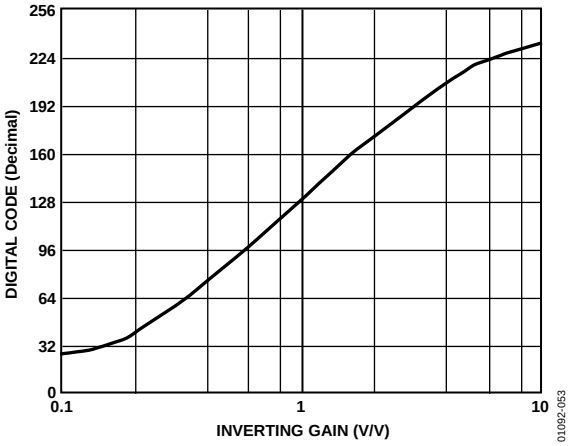


Figure 54. Inverting Programmable Gain Plot

ACTIVE FILTER

The state variable active filter is one of the standard circuits used to generate a low-pass, high-pass, or band-pass filter. The digital potentiometer allows full programmability of the frequency, gain, and Q of the filter outputs. Figure 55 shows the filter circuit using a 2.5 V virtual ground, which allows a ±2.5 V_P input and output swing. RDAC2 and RDAC3 set the LP, HP, and BP cutoff and center frequencies, respectively. These variable resistors should be programmed with the same data (as with ganged potentiometers) to maintain the best Circuit Q. Figure 56 shows the measured filter response at the band-pass output as a function of the RDAC2 and RDAC3 settings that produce a range of center frequencies from 2 kHz to 20 kHz. The filter gain response at the band-pass output is shown in Figure 57. At a center frequency of 2 kHz, the gain is adjusted over a −20 dB to +20 dB range determined by RDAC1. Circuit Q is adjusted by RDAC4. For more detailed reading on the state variable active filter, see Analog Devices' application note AN-318.

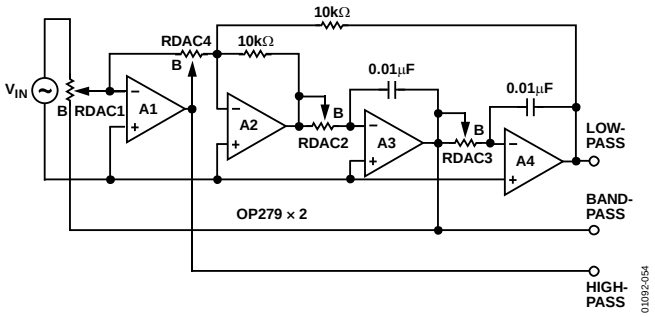


Figure 55. Programmable State Variable Active Filter

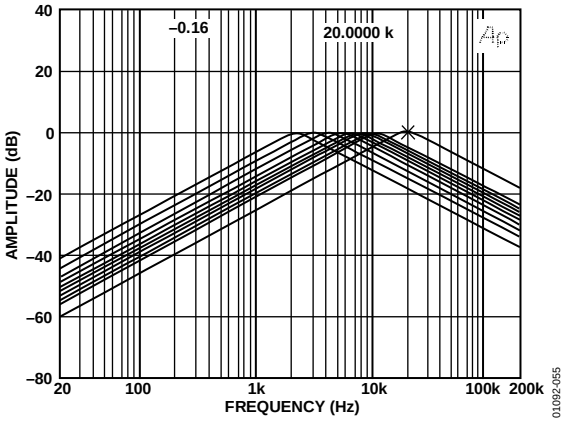


Figure 56. Programmed Center Frequency Band-Pass Response

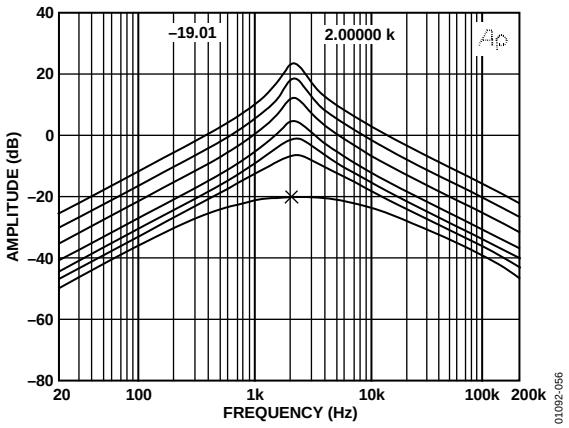
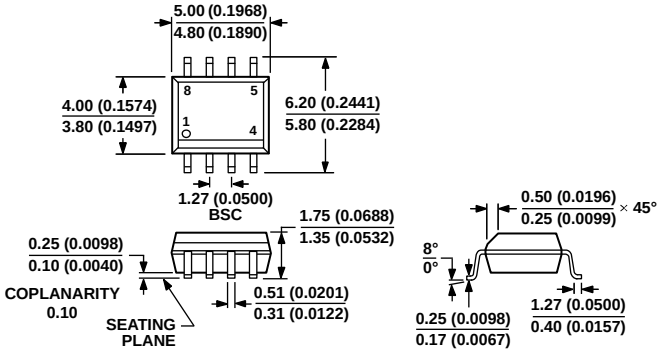


Figure 57. Programmed Amplitude Band-Pass Response

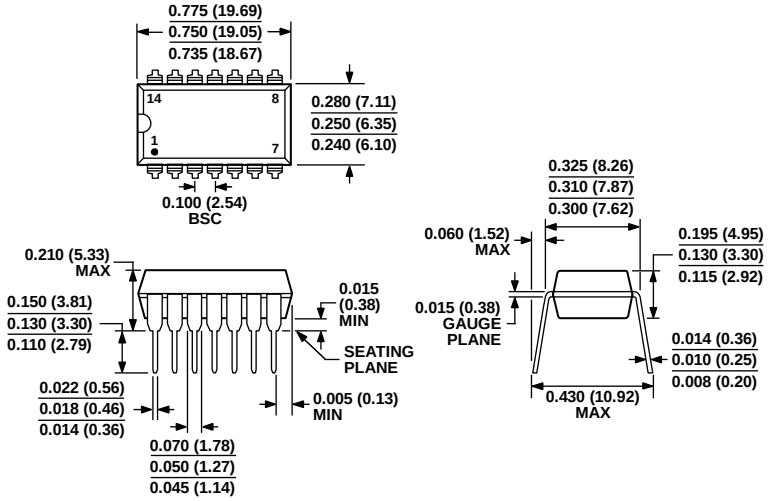
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

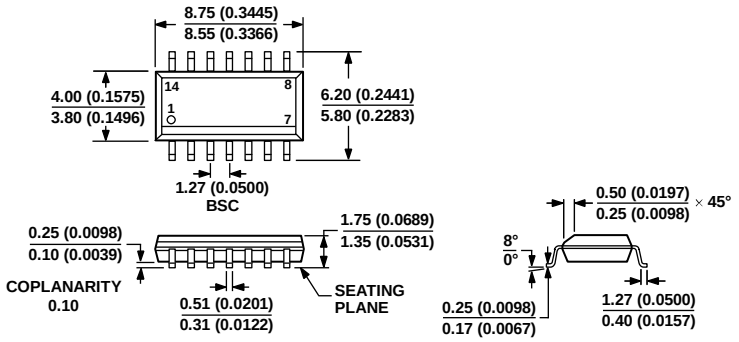
Figure 58. 8-Lead Standard Small outline package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 59. 14-Lead Plastic Dual-In-Line Package [PDIP]
Narrow Body (N-14)
Dimensions shown in inches and (millimeters)

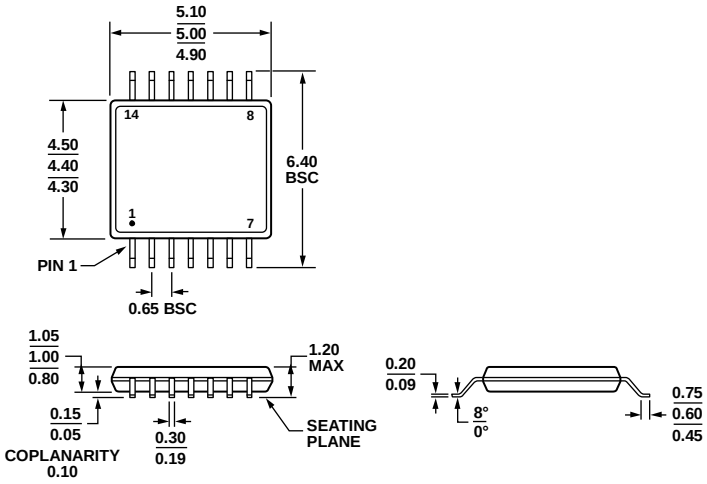


COMPLIANT TO JEDEC STANDARDS MS-012-AB

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

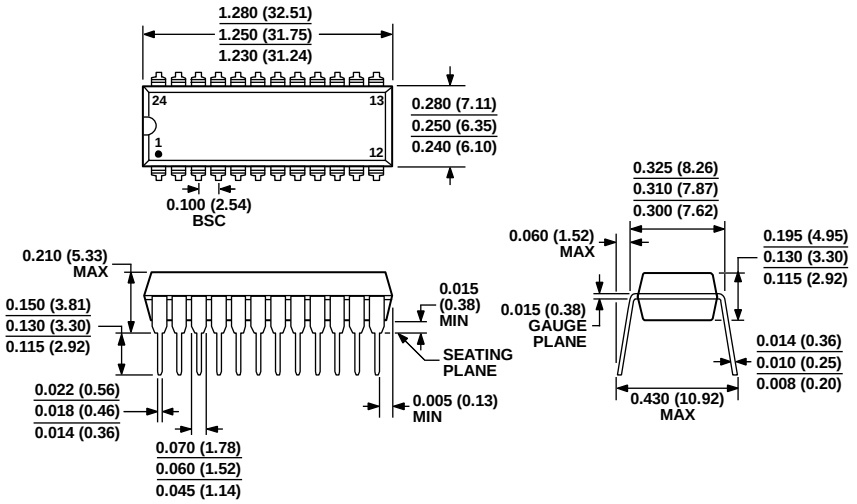
Figure 60. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-14)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

061908-A

Figure 61. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

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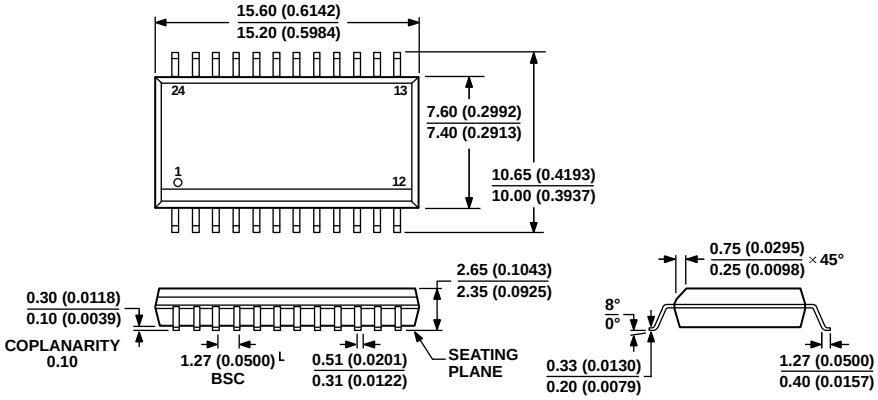
Figure 62. 24-Lead Plastic Dual-In-Line Package [PDIP]
Narrow Body (N-24-1)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013-AD
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

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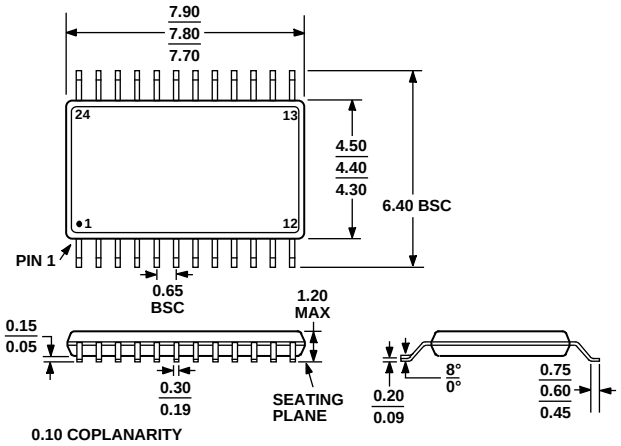
Figure 63. 24-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-24)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AD

Figure 64. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Number of Channels	End-to-End R_{AB} (kΩ)	Temperature Range (°C)	Package Description	Package Option	Ordering Quantity	Branding Information
AD8400AR10	1	10	−40 to +125	8-Lead SOIC_N	R-8	98	AD8400A10
AD8400AR10-REEL	1	10	−40 to +125	8-Lead SOIC_N	R-8	2,500	AD8400A10
AD8400ARZ10	1	10	−40 to +125	8-Lead SOIC_N	R-8	98	AD8400A10
AD8400ARZ10-REEL	1	10	−40 to +125	8-Lead SOIC_N	R-8	2,500	AD8400A10
AD8400AR50	1	50	−40 to +125	8-Lead SOIC_N	R-8	98	AD8400A50
AD8400AR50-REEL	1	50	−40 to +125	8-Lead SOIC_N	R-8	2,500	AD8400A50
AD8400ARZ50	1	50	−40 to +125	8-Lead SOIC_N	R-8	98	AD8400A50
AD8400ARZ50-REEL	1	50	−40 to +125	8-Lead SOIC_N	R-8	2,500	AD8400A50
AD8400AR100	1	100	−40 to +125	8-Lead SOIC_N	R-8	98	AD8400AC
AD8400AR100-REEL	1	100	−40 to +125	8-Lead SOIC_N	R-8	2,500	AD8400AC
AD8400ARZ100	1	100	−40 to +125	8-Lead SOIC_N	R-8	98	AD8400AC
AD8400ARZ100-REEL	1	100	−40 to +125	8-Lead SOIC_N	R-8	2,500	AD8400AC
AD8400AR1	1	1	−40 to +125	8-Lead SOIC_N	R-8	98	AD8400A1
AD8400AR1-REEL	1	1	−40 to +125	8-Lead SOIC_N	R-8	2,500	AD8400A1
AD8400ARZ1	1	1	−40 to +125	8-Lead SOIC_N	R-8	98	AD8400A1
AD8400ARZ1-REEL	1	1	−40 to +125	8-Lead SOIC_N	R-8	2,500	AD8400A1
AD8402AN10	2	10	−40 to +125	14-Lead PDIP	N-14	25	AD8402A10
AD8402ANZ10	2	10	−40 to +125	14-Lead PDIP	N-14	25	AD8402A10
AD8402AR10	2	10	−40 to +125	14-Lead SOIC_N	R-14	56	AD8402A10
AD8402AR10-REEL	2	10	−40 to +125	14-Lead SOIC_N	R-14	2,500	AD8402A10
AD8402ARU10	2	10	−40 to +125	14-Lead TSSOP	RU-14	96	8402A10
AD8402ARU10-REEL	2	10	−40 to +125	14-Lead TSSOP	RU-14	2,500	8402A10
AD8402ARUZ10	2	10	−40 to +125	14-Lead TSSOP	RU-14	96	8402A10
AD8402ARUZ10-REEL	2	10	−40 to +125	14-Lead TSSOP	RU-14	2,500	8402A10
AD8402ARZ10	2	10	−40 to +125	14-Lead SOIC_N	R-14	96	AD8402A10
AD8402ARZ10-REEL	2	10	−40 to +125	14-Lead SOIC_N	R-14	2,500	AD8402A10
AD8402AR50	2	50	−40 to +125	14-Lead SOIC_N	R-14	56	AD8402A50
AD8402AR50-REEL	2	50	−40 to +125	14-Lead SOIC_N	R-14	2,500	AD8402A50
AD8402ARU50	2	50	−40 to +125	14-Lead TSSOP	RU-14	96	8402A50
AD8402ARU50-REEL	2	50	−40 to +125	14-Lead TSSOP	RU-14	2,500	8402A50
AD8402ARUZ50	2	50	−40 to +125	14-Lead TSSOP	RU-14	96	8402A50
AD8402ARUZ50-REEL	2	50	−40 to +125	14-Lead TSSOP	RU-14	2,500	8402A50
AD8402ARZ50	2	50	−40 to +125	14-Lead SOIC_N	R-14	96	AD8402A50
AD8402ARZ50-REEL	2	50	−40 to +125	14-Lead SOIC_N	R-14	2,500	AD8402A50
AD8402AR100	2	100	−40 to +125	14-Lead SOIC_N	R-14	56	AD8402AC
AD8402AR100-REEL	2	100	−40 to +125	14-Lead SOIC_N	R-14	2,500	AD8402AC
AD8402ARU100	2	100	−40 to +125	14-Lead TSSOP	RU-14	96	8402A-C
AD8402ARU100-REEL	2	100	−40 to +125	14-Lead TSSOP	RU-14	2,500	8402A-C
AD8402ARUZ100	2	100	−40 to +125	14-Lead TSSOP	RU-14	96	8402A-C
AD8402ARUZ100-REEL	2	100	−40 to +125	14-Lead TSSOP	RU-14	2,500	8402A-C
AD8402ARZ100	2	100	−40 to +125	14-Lead SOIC_N	R-14	96	AD8402AC
AD8402ARZ100-REEL	2	100	−40 to +125	14-Lead SOIC_N	R-14	2,500	AD8402AC
AD8402AR1	2	1	−40 to +125	14-Lead SOIC_N	R-14	56	AD8402A1
AD8402AR1-REEL	2	1	−40 to +125	14-Lead SOIC_N	R-14	2,500	AD8402A1
AD8402ARU1	2	1	−40 to +125	14-Lead TSSOP	RU-14	96	8402A1
AD8402ARUZ1	2	1	−40 to +125	14-Lead TSSOP	RU-14	96	AD8402A1
AD8402ARUZ1-REEL	2	1	−40 to +125	14-Lead TSSOP	RU-14	2,500	AD8402A1
AD8402ARZ1	2	1	−40 to +125	14-Lead SOIC_N	R-14	56	AD8402A1
AD8402ARZ1-REEL	2	1	−40 to +125	14-Lead SOIC_N	R-14	2,500	AD8402A1

Model[1, 2, 3]	Number of Channels	End-to-End R_{AB} (kΩ)	Temperature Range (°C)	Package Description	Package Option	Ordering Quantity	Branding Information
AD8403AN10	4	10	−40 to +125	24-Lead PDIP	N-24-1	15	AD8403A10
AD8403AR10	4	10	−40 to +125	24-Lead SOIC_W	RW-24	31	AD8403A10
AD8403AR10-REEL	4	10	−40 to +125	24-Lead SOIC_W	RW-24	1,000	AD8403A10
AD8403ARU10	4	10	−40 to +125	24-Lead TSSOP	RU-24	63	8403A10
AD8403ARU10-REEL	4	10	−40 to +125	24-Lead TSSOP	RU-24	2,500	8403A10
AD8403ARUZ10	4	10	−40 to +125	24-Lead TSSOP	RU-24	63	8403A10
AD8403ARUZ10-REEL	4	10	−40 to +125	24-Lead TSSOP	RU-24	2,500	8403A10
AD8403ARZ10	4	10	−40 to +125	24-Lead SOIC_W	RW-24	63	AD8403A10
AD8403ARZ10-REEL	4	10	−40 to +125	24-Lead SOIC_W	RW-24	2,500	AD8403A10
AD8403AN50	4	50	−40 to +125	24-Lead PDIP	N-24-1	15	AD8403A50
AD8403AR50	4	50	−40 to +125	24-Lead SOIC_W	RW-24	31	AD8403A50
AD8403AR50-REEL	4	50	−40 to +125	24-Lead SOIC_W	RW-24	1,000	AD8403A50
AD8403ARU50	4	50	−40 to +125	24-Lead TSSOP	RU-24	63	8403A50
AD8403ARUZ50	4	50	−40 to +125	24-Lead TSSOP	RU-24	2,500	8403A50
AD8403ARUZ50-REEL	4	50	−40 to +125	24-Lead TSSOP	RU-24	2,500	8403A50
AD8403ARZ50	4	50	−40 to +125	24-Lead SOIC_W	RW-24	63	AD8403A50
AD8403ARZ50-REEL	4	50	−40 to +125	24-Lead SOIC_W	RW-24	2,500	AD8403A50
AD8403AR100	4	100	−40 to +125	24-Lead SOIC_W	RW-24	31	AD8403A100
AD8403AR100-REEL	4	100	−40 to +125	24-Lead SOIC_W	RW-24	1,000	AD8403A100
AD8403ARU100	4	100	−40 to +125	24-Lead TSSOP	RU-24	63	8403A100
AD8403ARU100-REEL	4	100	−40 to +125	24-Lead TSSOP	RU-24	2,500	8403A100
AD8403ARUZ100	4	100	−40 to +125	24-Lead TSSOP	RU-24	63	8403A100
AD8403ARUZ100-REEL	4	100	−40 to +125	24-Lead TSSOP	RU-24	2,500	8403A100
AD8403ARZ100	4	100	−40 to +125	24-Lead SOIC_W	RW-24	63	AD8403A100
AD8403ARZ100-REEL	4	100	−40 to +125	24-Lead SOIC_W	RW-24	2,500	AD8403A100
AD8403AR1	4	1	−40 to +125	24-Lead SOIC_W	RW-24	31	AD8403A1
AD8403AR1-REEL	4	1	−40 to +125	24-Lead SOIC_W	RW-24	1,000	AD8403A1
AD8403ARU1	4	1	−40 to +125	24-Lead TSSOP	RU-24	63	8403A1
AD8403ARU1-REEL	4	1	−40 to +125	24-Lead TSSOP	RU-24	2,500	8403A1
AD8403ARUZ1	4	1	−40 to +125	24-Lead TSSOP	RU-24	63	8403A1
AD8403ARUZ1-REEL	4	1	−40 to +125	24-Lead TSSOP	RU-24	2,500	8403A1
AD8403ARZ1	4	1	−40 to +125	24-Lead SOIC_W	RW-24	63	AD8403A1
AD8403ARZ1-REEL	4	1	−40 to +125	24-Lead SOIC_W	RW-24	2,500	AD8403A1
AD8403WARZ50-REEL	4	50	−40 to +125	24-Lead SOIC_W	RW-24	2,500	
EVAL-AD8403SDZ				Evaluation Board			

[1] Non-lead-free parts have date codes in the format of either YWW or YYWW, and lead-free parts have date codes in the format of #YWW, where Y/YY is the year of production and WW is the work week. For example, a non-lead-free part manufactured in the 30th work week of 2005 has the date code of either 530 or 0530, while a lead-free part has the date code of #530.
[2] Z = RoHS Compliant Part.
[3] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The AD8403W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

NOTES

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D01092-0-7/10(E)

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