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FAIRCHILD™

February 2015

FSA2567 — Low-Power, Dual SIM Card Analog Switch

Features

- Low On Capacitance for Data Path: 10 pF Typical
- Low On Resistance for Data Path: 6 Ω Typical
- Low On Resistance for Supply Path: 0.4 Ω Typical
- Wide V_{CC} Operating Range: 1.65 V to 4.3 V
- Low Power Consumption: 1 μA Maximum
  - 15 μA Maximum I_{CCT} Over Expanded Voltage Range (V_{IN}=1.8 V, V_{CC}=4.3 V)
- Wide -3 db Bandwidth: > 160 MHz
- Packaged in:
  - Pb-free 16-Lead MLP & 16-Lead UMLP
- 3 kV ESD Rating, >12 kV Power/GND ESD Rating

Applications

- Cell phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

Description

The FSA2567 is a bi-directional, low-power, dual double-pole, double-throw (4PDT) analog switch targeted at dual SIM card multiplexing. It is optimized for switching the WLAN-SIM data and control signals and dedicates one channel as a supply-source switch.

The FSA2567 is compatible with the requirements of SIM cards and features a low on capacitance (C_{ON}) of 10 pF to ensure high-speed data transfer. The V_{SIM} switch path has a low R_{ON} characteristic to ensure minimal voltage drop in the dual SIM card supply paths.

The FSA2567 contains special circuitry that minimizes current consumption when the control voltage applied to the SEL pin is lower than the supply voltage (V_{CC}). This feature is especially valuable in ultra-portable applications, such as cell phones; allowing direct interface with the general-purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSA2567MPX	FSA2567	-40 to +85°C	16-Lead, Molded Leadless Package (MLP) Quad, JEDEC MO-220, 3 mm Square
FSA2567UMX	GX		16-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 1.8 x 2.6 mm

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

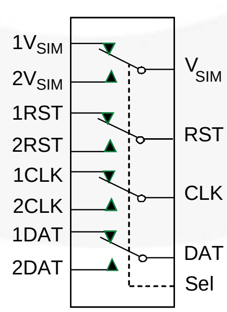


Figure 1. Analog Symbol

Pin Assignments

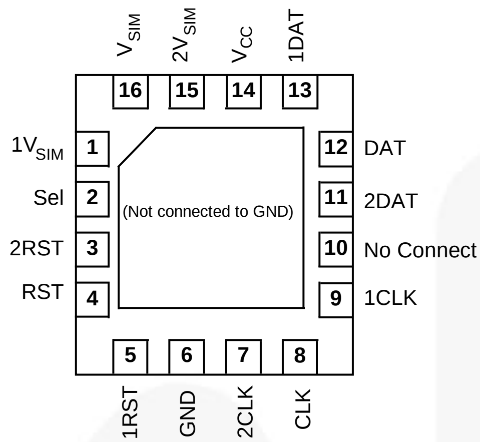


Figure 2. Pad Assignment MLP16 (Top Through View)

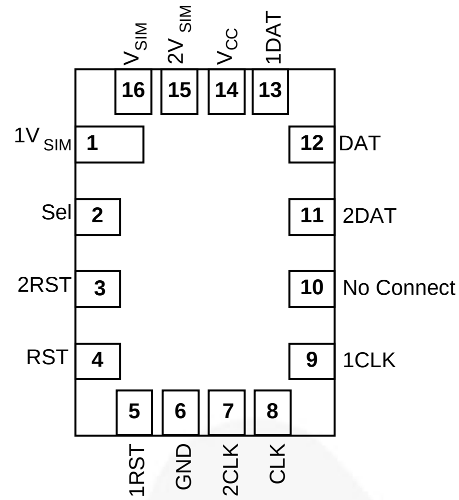


Figure 3. Pad Assignment UMLP16 (Top Through View)

Pin Definitions

Pin	Description
nDAT, nRST, nCLK	Multiplexed Data Source Inputs
nV_{SIM}	Multiplexed SIM Supply Inputs
V_{SIM} , DAT, RST, CLK	Common SIM Ports
Sel	Switch Select

Truth Table

Sel	Function
Logic LOW	1DAT = DAT, 1RST = RST, 1CLK = CLK, $1V_{SIM} = V_{SIM}$
Logic HIGH	2DAT = DAT, 2RST = RST, 2CLK = CLK, $2V_{SIM} = V_{SIM}$

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	+5.5	V
V_{CNTRL}	DC Input Voltage (Sel)[(1)]		-0.5	V_{CC}	V
V_{SW}	DC Switch I/O Voltage[(1)]		-0.5	V_{CC} + 0.3	V
I_{IK}	DC Input Diode Current		-50		mA
I_{SIM}	DC Output Current - V_{SIM}			350	mA
I_{OUT}	DC Output Current – DAT, CLK, RST			35	mA
T_{STG}	Storage Temperature		-65	+150	°C
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins		3	kV
		I/O to GND		12	
	Charged Device Model, JEDEC: JESD22-C101			2	

Note:
1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.65	4.30	V
V_{CNTRL}	Control Input Voltage (Sel)[(2)]	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	-0.5	V_{CC}	V
I_{SIM}	DC Output Current - V_{SIM}		150	mA
I_{OUT}	DC Output Current – DAT, CLK, RST		25	mA
T_A	Operating Temperature	-40	+85	°C

Note:
2. The control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics

All typical values are at 25°C, 3.3 V V_{CC} unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Units
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN} = -18 mA	2.7			-1.2	V
V_{IH}	Input Voltage High		1.65 to 2.3	1.1			V
			2.7 to 3.6	1.3			
			4.3	1.7			
V_{IL}	Input Voltage Low		1.65 to 2.3			0.4	V
			2.7 to 3.6			0.5	
			4.3			0.7	
I_{IN}	Control Input Leakage	V_{SW} = 0 to V_{CC}	4.3	-1		1	µA
$I_{nc(off)}$, $I_{no(off)}$,	Off State Leakage	nRST, nDAT, nCLK, nV_{SIM} = 0.3 V or 3.6 V Figure 10	4.3	-60		60	nA
R_{OND}	Data Path Switch On Resistance(3)	V_{SW} = 0, 1.8 V, I_{ON} = -20 mA Figure 9	1.8		7.0	12.0	Ω
		V_{SW} = 0, 2.3 V, I_{ON} = -20 mA Figure 9	2.7		6.0	10.0	
R_{ONV}	V_{SIM} Switch On Resistance(3)	V_{SW} = 0, 1.8V, I_{ON} = -100mA Figure 9	1.8		0.5	0.7	Ω
		V_{SW} = 0, 2.3 V, I_{ON} = -100 mA Figure 9	2.7		0.4	0.6	
ΔR_{OND}	Data Path Delta On Resistance(4)	V_{SW} = 0 V, I_{ON} = -20 mA	2.7		0.2		Ω
I_{CC}	Quiescent Supply Current	V_{CNTRL} = 0 or V_{CC}, I_{OUT} = 0	4.3			1.0	µA
I_{CCT}	Increase in I_{CC} Current Per Control Voltage and V_{CC}	V_{CNTRL} = 2.6 V, V_{CC} = 4.3 V	4.3		5.0	10.0	µA
		V_{CNTRL} = 1.8 V, V_{CC} = 4.3 V	4.3		7.0	15.0	µA

Notes:

3. Measured by the voltage drop between nDAT, nRST, nCLK and relative common port pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the relative ports.
4. Guaranteed by characterization.

AC Electrical Characteristics

All typical value are for V_{CC}=3.3V at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40°C to +85°C			Units
				Min.	Typ.	Max.	
t_{OND}	Turn-On Time Sel to Output (DAT,CLK,RST)	R_L = 50 Ω, C_L = 35 pF V_{SW} = 1.5 V Figure 11, Figure 12	1.8(5)		65	95	ns
			2.7 to 3.6		42	60	ns
t_{OFFD}	Turn-Off Time Sel to Output (DAT,CLK,RST)	R_L = 50 Ω, C_L= 35 pF V_{SW} = 1.5 V Figure 11, Figure 12	1.8(5)		30	50	ns
			2.7 to 3.6		20	40	ns
t_{ONV}	Turn-On Time Sel to Output (V_{SIM})	R_L = 50 Ω, C_L = 35 pF V_{SW} = 1.5 V Figure 11, Figure 12	1.8(5)		55	80	ns
			2.7 to 3.6		35	55	ns
t_{OFFV}	Turn-Off Time Sel to Output (V_{SIM})	R_L = 50 Ω, C_L = 35 pF V_{SW} = 1.5 V Figure 11, Figure 12	1.8(5)		35	50	
			2.7 to 3.6		22	40	ns
t_{PD}	Propagation Delay(5) (DAT,CLK,RST)	C_L = 35 pF, R_L = 50 Ω Figure 11, Figure 13	3.3		0.25		ns
t_{BBMD}	Break-Before-Make(5) (DAT,CLK,RST)	R_L = 50 Ω, C_L = 35 pF V_{SW1} = V_{SW2} = 1.5 V Figure 15	2.7 to 3.6	3	18		ns
t_{BBMV}	Break-Before-Make(5) (V_{SIM})	R_L = 50 Ω, C_L = 35 pF V_{SW1} = V_{SW2} = 1.5 V Figure 15	2.7 to 3.6	3	12		ns
Q	Charge Injection (DAT,CLK,RST)	C_L = 50 pF, R_{GEN} = 0 Ω, V_{GEN} = 0 V	2.7 to 3.6		10		pC
O_{IRR}	Off Isolation (DAT,CLK,RST)	R_L = 50 Ω, f = 10 MHz Figure 17	2.7 to 3.6		-60		dB
Xtalk	Non-Adjacent Channel Crosstalk (DAT,CLK,RST)	R_L = 50 Ω, f = 10 MHz Figure 18	2.7 to 3.6		-60		dB
BW	-3 db Bandwidth (DAT,CLK,RST)	R_L = 50 Ω, C_L = 5 pF Figure 16	2.7 to 3.6		475		MHz

Note:
5. Guaranteed by characterization.

Capacitance

Symbol	Parameter	Conditions	T_A =- 40°C to +85°C			Units
			Min.	Typ.	Max.	
C_{IN}	Control Pin Input Capacitance	V_{CC} = 0 V		1.5		pF
C_{OND}	RST, CLK, DAT On Capacitance(6)	V_{CC} = 3.3 V, f = 1 MHz Figure 20		10	12	
C_{ONV}	V_{SIM} On Capacitance(6)	V_{CC} = 3.3 V, f = 1 MHz Figure 20		110	150	
C_{OFFD}	RST, CLK, DAT Off Capacitance	V_{CC} = 3.3 V, Figure 19		3		
C_{OFFV}	V_{SIM} Off Capacitance	V_{CC} = 3.3 V, Figure 19		40		

Note:
6. Guaranteed by characterization.

Typical Performance Characteristics

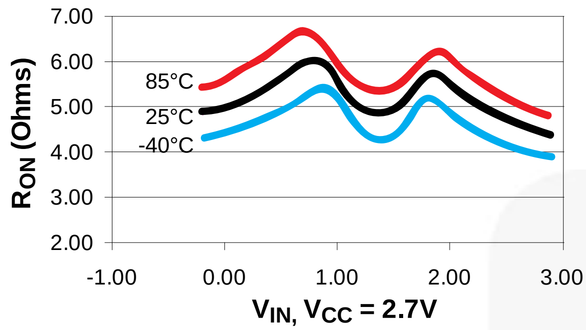


Figure 4. R_{ON} Data Path

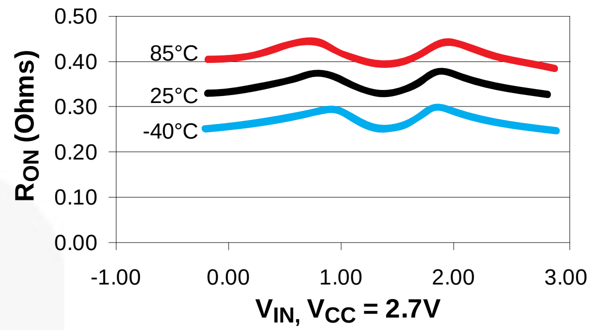


Figure 5. R_{ON} V_{SIM}

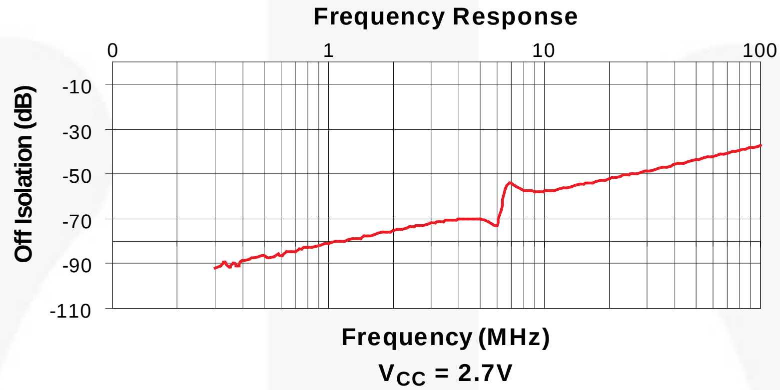


Figure 6. Off Isolation

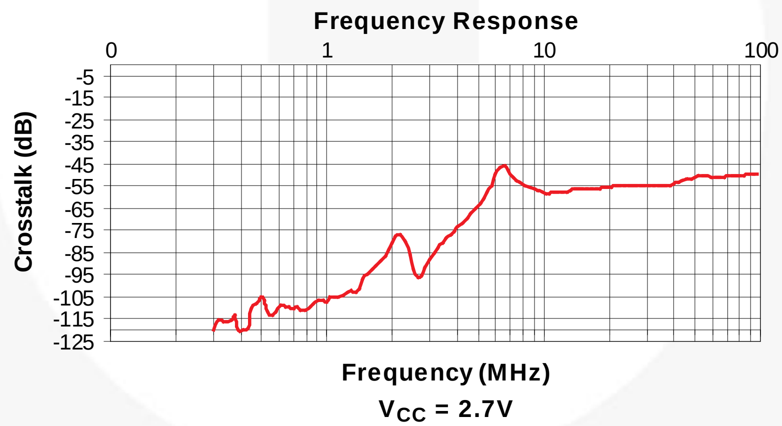


Figure 7. Crosstalk

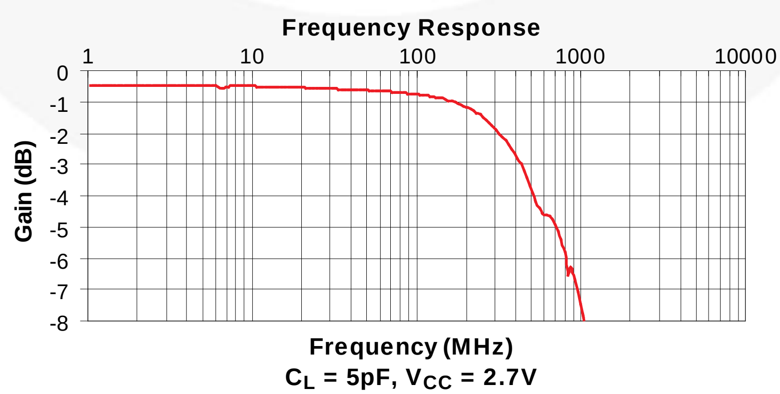


Figure 8. Bandwidth

Test Diagrams

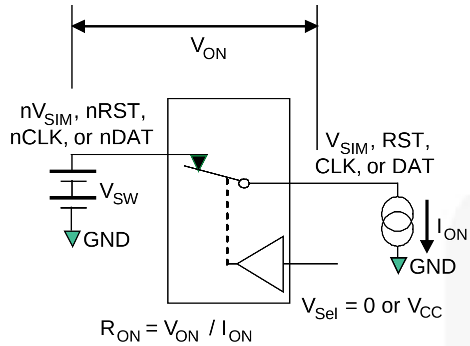


Figure 9. On Resistance

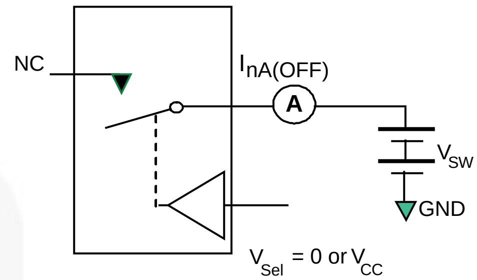


Figure 10. Off Leakage

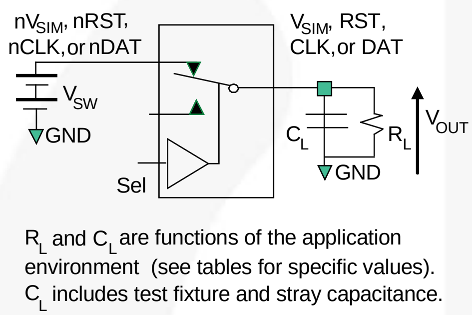


Figure 11. AC Test Circuit Load

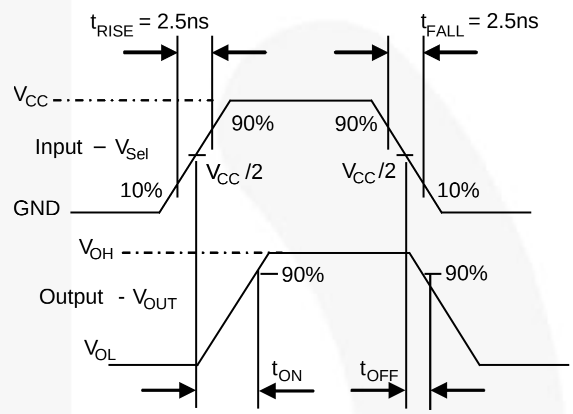


Figure 12. Turn-On / Turn-Off Waveforms

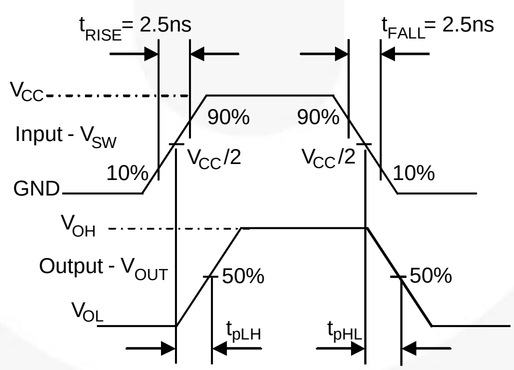


Figure 13. Propagation Delay

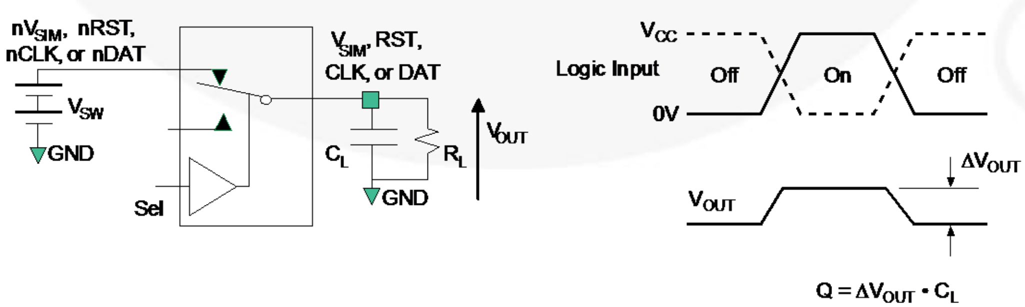
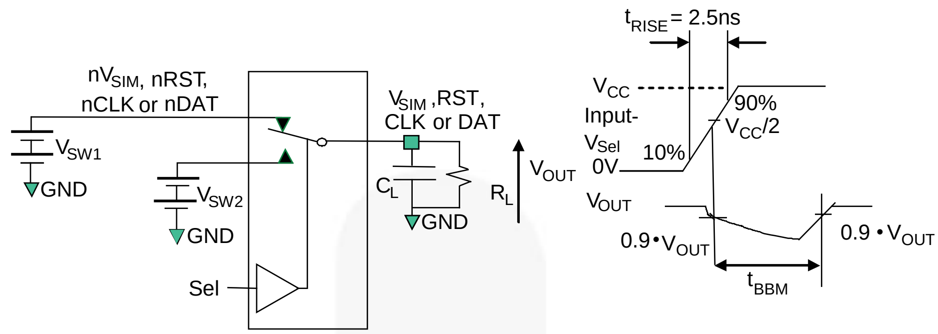


Figure 14. Charge Injection

Test Diagrams (Continued)



R_L and C_L are functions of the application environment (see tables for specific values). C_L includes test fixture and stray capacitance.

Figure 15. Break-Before-Make Interval Timing

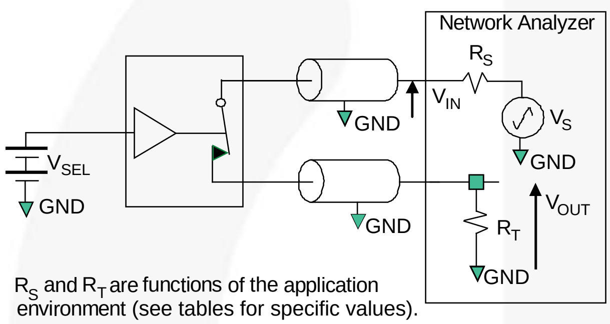


Figure 16. Bandwidth

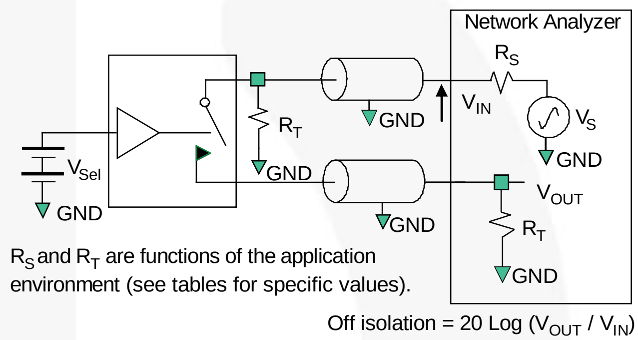


Figure 17. Channel Off Isolation

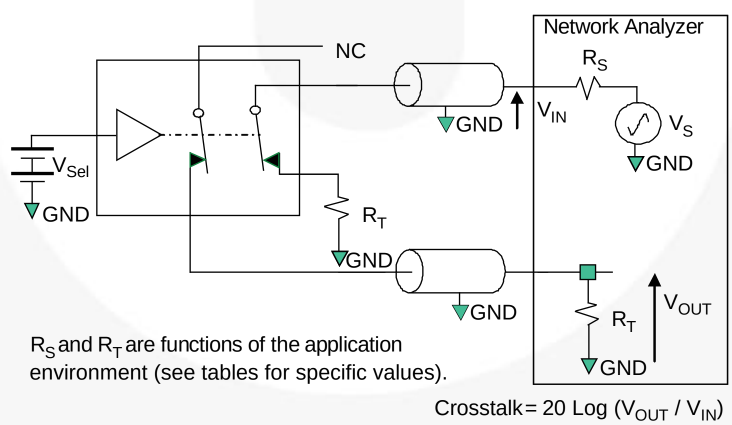


Figure 18. Non-Adjacent Channel-to-Channel Crosstalk

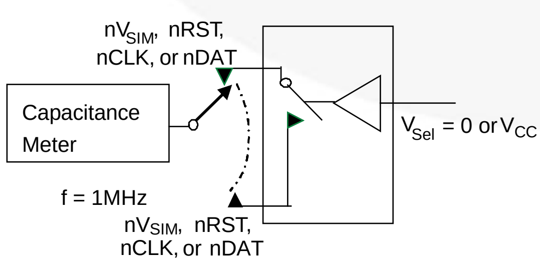


Figure 19. Channel Off Capacitance

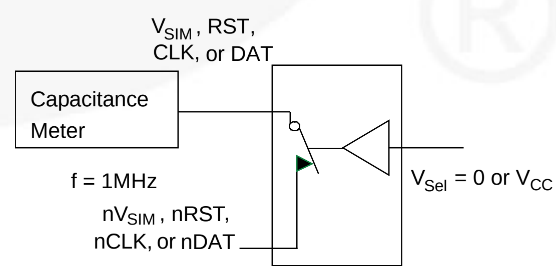
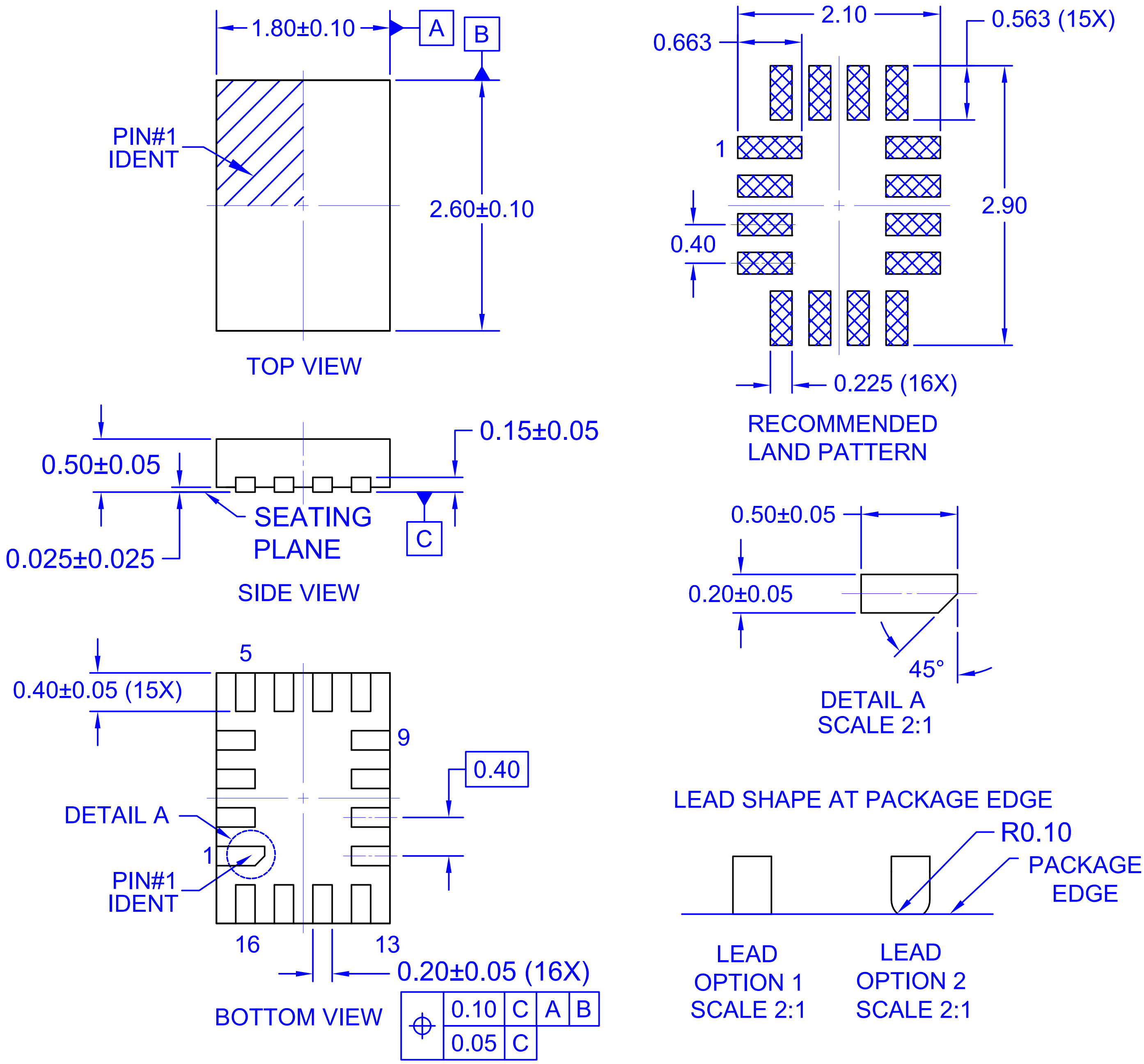


Figure 20. Channel On Capacitance



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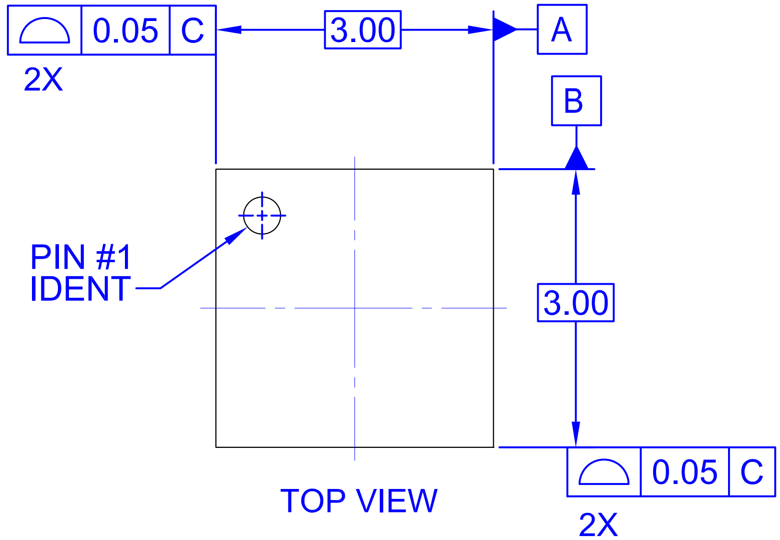
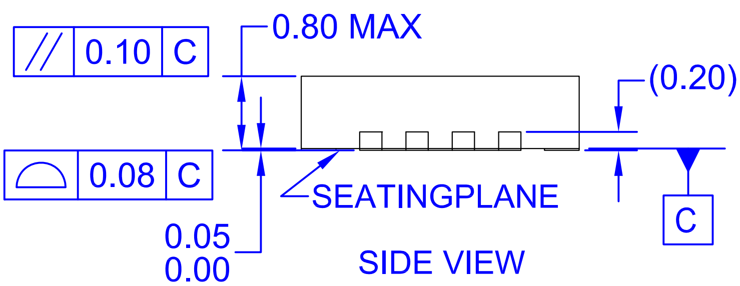
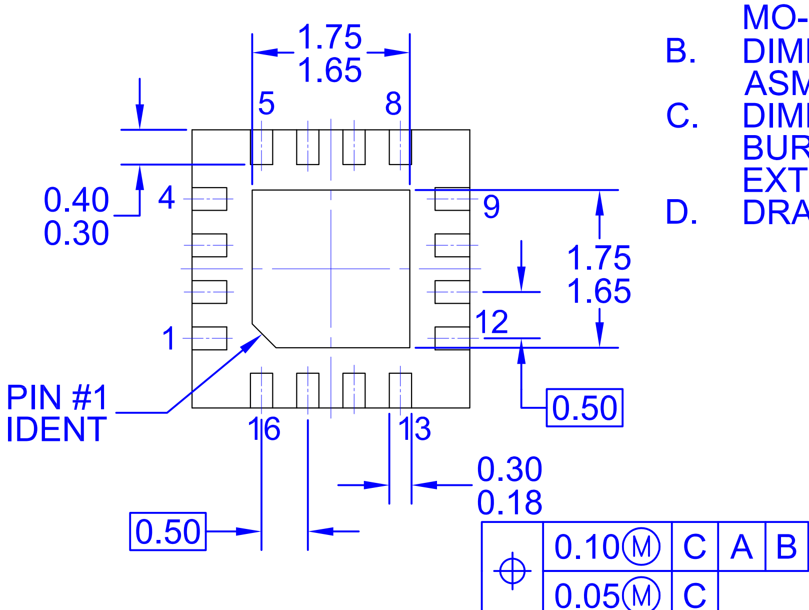


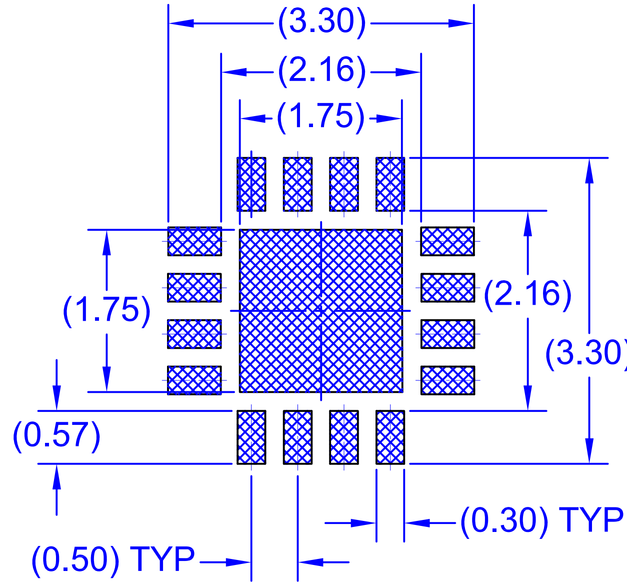
TOP VIEW



SIDE VIEW



BOTTOM VIEW



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