

General Description

EZ-PD™ CCG5 is a dual USB Type-C controller that complies with the latest USB Type-C and PD standards. EZ-PD CCG5 provides a complete dual USB Type-C and USB-Power Delivery port control solution for PCs, notebook, and dock. It can also be used in dual role and downstream-facing port applications. EZ-PD CCG5 uses Cypress' proprietary M0S8 technology with a 32-bit, 48-MHz Arm® Cortex®-M0 processor with 128-KB flash and integrates two complete Type-C Transceivers including the Type-C termination resistors, R_P and R_D . CCG5 also integrates high-voltage regulator. CCG5 is available in 40-QFN (1 port) and 96-BGA (2 ports) packages.

Applications

- PCs, Notebook, and Dock
- Thunderbolt hosts and devices

Features

Type-C and USB-PD Support

- Integrated USB Power Delivery (USB-PD) 3.0 support
- Two integrated USB-PD Type-C ports
- Integrated UFP^[1] (R_D) and current sources for DFP^[2] (R_P) on both Type-C ports
- Integrated dead battery termination for DRP (Power Source/Sink) applications
- Integrated VCONN FETs to power EMCA cables
- Integrated fast role swap and extended data messaging
- Integrated high-voltage LDO, operational up to 21.5 V
- Integrated 2x USB Analog Mux
- Integrated 2x SBU Analog Mux
- Integrated 2x USB Charger detect blocks – BC v1.2, Apple Charging (source only)
- Integrated overvoltage protection (OVP) and overcurrent protection (OCP) on the VBUS
- Integrated OCP protection on the VCONN
- Integrated high-voltage protection on CC and SBU pins to protect against accidental shorts to the VBUS pin on the Type-C connector
- Integrated current sense amplifier that supports high-side current sensing
- Integrated gate drivers for external VBUS PFET control on Type-C Ports
- Supports high-voltage tolerant PFET-controlled GPIOs

32-bit MCU Subsystem

- 48-MHz Arm Cortex-M0 CPU
- 128-KB Flash
- 12-KB SRAM

Integrated Digital Blocks

- Up to two integrated timers and counters to meet response times required by the USB-PD protocol
- Four run-time serial communication blocks (SCBs) with reconfigurable I²C, SPI, or UART functionality

Clocks and Oscillators

- Integrated oscillator eliminating the need for an external clock

Low-Power Operation

- 2.75 V to 21.5 V operation

System-Level ESD on CC, D±, and SBU Pins

- ±8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C

Hot-Swappable I/Os

- Port 1 I²C pins and CC1, CC2 pins are hot-swappable

Packages

- 6.0 mm × 6.0 mm, 0.6 mm, 40-pin QFN
- 6.0 mm × 6.0 mm, 1.0 mm, 96-ball BGA
- Supports industrial temperature range (–40 °C to +85 °C)

Notes

1. UFP refers to Power Sink.
2. DFP refers to Power Source.

Logic Block Diagram



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Functional Overview

USB-PD Subsystem (SS)

USB-PD Physical Layer

The CCG5 has two USB-PD subsystems consisting of the USB-PD physical layer (PHY) block and supporting circuits. The USB-PD PHY consists of a transmitter and receiver that communicate BMC and 4b/5b encoded data over the CC channel based on the PD 3.0 standard. All communication is half-duplex. The PHY practices collision avoidance to minimize communication errors on the channel.

In addition, the CCG5 USB-PD block includes all termination resistors (R_P and R_D) and their switches as required by the USB Type-C spec. R_P and R_D resistors are required to implement connection detection, plug orientation detection, and for establishing the USB source/sink roles.

The integrated R_P resistor enables CCG5 to be configured as a DFP. The R_P resistor is implemented as a current source and can be programmed to support the complete range of current capacity on the VBUS defined in the USB Type-C Spec.

The R_D resistor is used to identify CCG5 as a UFP in a DRP application. The R_D resistor on CC pins is required even when the part is not powered for dead battery termination detection and charging.

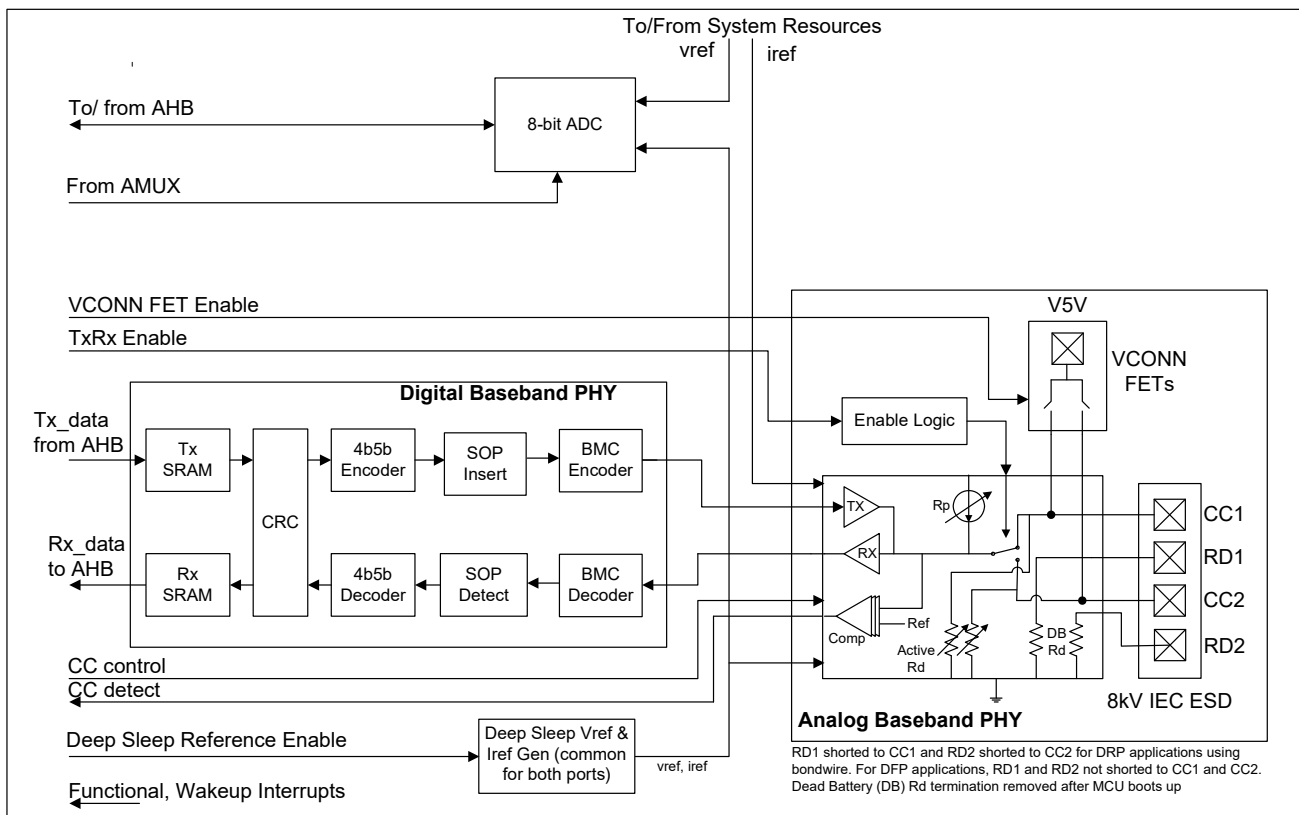
To support the latest USB-PD 3.0 specification, CCG5 has implemented the Fast Role Swap (FRS) feature. The FRS feature enables externally powered docks and hubs to rapidly switch to bus power when their external power supply is removed. CCG5 also supports DeepSleep in notebook systems where CCG5 is expecting FRS detection.

For more details, refer to Section 6.3.17 in the [USB-PD 3.0 specification](#).

CCG5 is designed to be fully interoperable with revision 3.0 of the USB Power Delivery specification as well as revision 2.0 of the USB Power Delivery specification.

CCG5 supports Extended Messages containing data of up to 260 bytes. The Extended Messages will be larger than expected by the USB-PD 2.0 hardware. To accommodate Revision 2.0 based systems, a Chunking mechanism is implemented such that messages are limited to Revision 2.0 sizes unless it is discovered that both systems support longer message lengths.

Figure 1. USB-PD Subsystem



VCONN FET

CCG5 has two power supply inputs, V5V_P1 and V5V_P2 pins, for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs for each PD port to power either CC1 or CC2 pins. These FETs can provide 1.5-W power over VCONN on the CC1 and CC2 pins for the EMCA cables. CCG5 also supports integrated OCP on VCONN.

ADC

The USB-PD subsystem contains one 8-bit successive approximation register (SAR) for analog-to-digital conversions (ADC). The ADCs include an 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex busses, an internal bandgap voltage, and an internal voltage proportional to the absolute temperature. All GPIOs on the chip

have access to the ADCs through the chip-wide analog mux bus. The CC1 and CC2 pins of both Type-C ports are not available to connect to the mux bus.

SBU Mux

The SBU switch mux contains 2x1 Mux and a single 2x2 cross bar SBU switch per the Type-C port. The 2x1 MUX enables you to select between the Display Port or Thunderbolt alternate mode and the single-ended 2x2 switch enables you to route signals to the appropriate SBU1/2 based on CC (Type-C plug) orientation.

The AUX port of the SBU switch supports only differential signals. Non-differential signals on the AUX port cause signal coupling at the output of the SBU switch. The LS port of the SBU switch supports both non-differential and differential signals.

Figure 2. CCG5 SBU Crossbar Switch Block Diagram



USB HS Mux

The HS Mux contains a 2x2 cross bar switch to route the system D± lines to the Type-C top or bottom ports based on the CC (Type-C plug) orientation. The unused D± top or bottom lines can be connected to a UART (Debug) port. The maximum operating frequency of UART must be 1 Mbps.

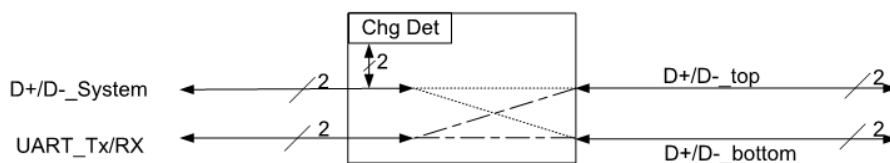
The HS Mux also contains charger detection/emulation for detecting USB BC 1.2 (source only) and Apple terminations. The charger detection block is connected to the D± from the system as shown in Figure 3.

To meet the HS eye diagram requirements with sufficient margin, follow these guidelines:

- Trace lengths of HS signals shall be no more than 2 inches from the USB 2.0 host to the CCG5 device. Similarly, trace length from the CCG5 device to Type-C connector pins shall be no more than 2 inches.
- The differential impedance across the DP/DM signal traces shall be 90 Ω.
- Trace width shall be 6 mils.
- Air Gap (distance between lines) shall be 8 mils.

Increasing the trace length by more than 2 inches on either side of the CCG5 device degrades the HS eye diagram.

Figure 3. CCG5 DP/DM Switch Block Diagram



Overvoltage and Undervoltage Protection on VBUS

CCG5 implements an undervoltage/overvoltage (UV/OV) detection circuit for the VBUS supply. The threshold for OV and UV detection can be set independently. Both UV and OV detector have programmable thresholds and is controlled by the firmware.

Overcurrent Protection on VBUS

CCG5 integrates a high-side current sense amplifier to detect overcurrent on the VBUS. Overcurrent protection is enabled by sensing the current through the 10-mΩ sense resistor connected between the “CSP_Px” and “CSN_Px” pins.

VBUS Discharge

CCG5 also has integrated VBUS discharge FETs and resistors for each port. It is used to discharge VBUS to meet the USB-PD specification timing on a detach condition and negative voltage transition.

VBUS Regulator

CCG5 can operate from three power supplies – V_{SYS} , V_{BUS_P1} , and V_{BUS_P2} . CCG5 integrates the regulator (that supports up to 21.5 V) to derive operating supply voltage. The V_{SYS} always takes priority over V_{BUS_P1}/V_{BUS_P2} . In the absence of V_{SYS} , the regulator powers CCG5 either from V_{BUS_P1} or V_{BUS_P2} .

PFET Gate Driver for VBUS

CCG5 supports the consumer-side and provider-side external power FET Drivers for PFET. The $V_{BUS_P_CTRL}$ and $V_{BUS_C_CTRL}$ gate drivers can drive only low or high-Z, thus requiring an external pull-up. These pins are VBUS voltage-tolerant.

Charger Detect

CCG5 integrates battery charger emulation and detection for USB BC.1.2, Apple charge (source only).

IEC Compliant VBUS, CC, D±, and SBU Lines

The chip supports IEC-compliant ESD protection on VBUS, CC, D±, and SBU lines.

High-Voltage Tolerant SBU and CC Lines

The chip supports high-voltage tolerant SBU and CC lines. In the case of SBU/CC short to VBUS through connectors, these lines will be protected internally.

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG5 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD CCG5 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG5 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver two wait states (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SRAM

A supervisory ROM that contains boot and configuration routines is provided.

SRAM

CCG5 supports 12-KB SRAM.

Power System Overview

Figure 4 provides an overview of the EZ-PD CCG5 power system. CCG5 can operate from three possible external supply sources: V_{BUS_P1}/V_{BUS_P2} (4 V–21.5 V) or V_{SYS} (2.75 V–5.5 V). The V_{BUS_P1} and V_{BUS_P2} supply is regulated inside the chip with a LDO. The switched supply, V_{DDD} , is either used directly inside some analog blocks or further regulated down to V_{CCD} , which powers majority of the core using the regulators. CCG5 has two different power modes: Active and Deep sleep. Transitions between these power modes are managed by the power system. A separate power domain, V_{DDIO} , is provided for the GPIOs. The V_{DDD} and V_{CCD} pins, both outputs of regulators, are brought out for connecting a 1 μ F and 0.1 μ F capacitor respectively for the regulator stability only. The V_{CCD} pin is not supported as a power supply. V_{DDD} can source 2 mA (max) for external load.

Table 1. CCG5 Power Modes

Mode	Description
RESET	Power is valid and XRES is not asserted. An internal reset source is asserted or Sleep Controller is sequencing the system out of reset.
ACTIVE	Power is valid and CPU is executing instructions.
DEEP SLEEP	Main regulator and most blocks are shut off. Deep Sleep regulator powers logic, but only low-frequency clock if available.

Figure 4. EZ-PD CCG5 Power System



Peripherals

Serial Communication Blocks (SCB)

EZ-PD CCG5 has four SCBs, which can be configured to implement an I²C, SPI, or UART interface. The hardware I²C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as a Master/slave.

In the I²C mode, the SCB blocks are capable of operating at speeds up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I²C that creates a mailbox address range in the memory of EZ-PD CCG5 and effectively reduce I²C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I²C peripherals are compatible with the I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/Os are implemented with GPIO in open-drain modes.

The I²C port on SCB 2, SCB 3 and SCB 4 blocks of EZ-PD CCG5 are not completely compliant with the I²C spec in the following:

- The GPIO cells for SCB 2 to SCB 4 I²C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 10-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG5 has up to two TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (TCPWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

GPIO

EZ-PD CCG5 has 28 GPIOs that includes the I²C and SWD pins, which can also be used as GPIOs. The I²C pins from only SCB 1 are overvoltage-tolerant. The number of available GPIOs vary with the part numbers. The GPIO block implements the following:

- Seven drive strength modes:
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Pinouts

Table 2. Pinout for CYPD5125-40LQXIT

Group Name	Pin Name	Port	Pin	Description
USB Type-C	CC1	Analog	9	USB PD connector detect/Configuration Channel 1
	CC2	Analog	7	USB PD connector detect/Configuration Channel 2
Mux	DPLUS_SYS	Analog	23	USB 2.0 DP from the Host System
	DMINUS_SYS	Analog	24	USB 2.0 DM from the Host System
	UART_TX/GPIO	P4.0	29	UART TX from Host System/GPIO
	UART_RX/GPIO	P4.1	30	UART RX from Host System/GPIO
	DPLUS_BOT	Analog	26	USB 2.0 DP from Bottom of Type-C Connector
	DMINUS_BOT	Analog	25	USB 2.0 DM from Bottom of Type-C Connector
	DMINUS_TOP	Analog	27	USB 2.0 DM from Top of Type-C Connector
	DPLUS_TOP	Analog	28	USB 2.0 DP from Top of Type-C Connector
	SBU2	Analog	34	Sideband Use signal
	SBU1	Analog	35	Sideband Use signal
	AUX_P	Analog	36	Auxiliary signal for DisplayPort
	AUX_N	Analog	37	Auxiliary signal for DisplayPort
	LSTX	Analog	38	Thunderbolt Link Management UART Rx
	LSRX	Analog	39	Thunderbolt Link Management UART Tx
VBUS Control	VBUS_P_CTRL	Analog	11	Full rail control I/O for enabling/disabling Provider load PFET of USB Type-C Port 1 0: Path ON High Z: Path OFF
	VBUS_C_CTRL	Analog	12	Full rail control I/O for enabling/disabling Consumer load PFET of USB Type-C port1 0: Path ON High Z: Path OFF
VBUS OCP	CSP	Analog	1	Current Sense positive Input for VBUS side external Rsense
	CSN	Analog	40	Current sense negative for other side of external Rsense
GPIOs and Serial Interfaces	SWD_IO/AR_RST/GPIO	P1.6	6	SWD I/O/GPIO
	SWD_CLK/I2C_CFG_EC/ GPIO	P1.0	2	SWD Clock/ I ² C config line. I ² C config line is used to select the I ² C address of HPI interface. The state of line decides the 7 bit I ² C address for HPI. I ² C Config Line Floating: 0x08 Pulled up with 1 KW: 0x42 Pulled down with 1 KW: 0x40
	I2C_SDA_SCB2_TBT/GPIO	P1.1	3	SCB2 I ² C Data/GPIO
	I2C_SCL_SCB2_TBT/GPIO	P1.2	4	SCB2 I ² C Clock/GPIO
	I2C_INT_TBT/GPIO	P1.3	5	TBT interrupt for port 1/GPIO
	OVP_TRIP/I2C_SDA_SCB4/GPIO	P2.4	14	VBUS overvoltage output indicator for port 1/SCB4 I ² C Data
	UV_OCP_TRIP/I2C_SCL_SCB4/GPIO	P2.3	13	VBUS undervoltage or OCP Output Indicator for Port1 / SCB4 I ² C Clock / GPIO
	I2C_SDA_SCB1_EC/GPIO	P5.0	16	SCB1 I ² C Data / GPIO
	I2C_SCL_SCB1_EC/GPIO	P5.1	17	SCB1 I ² C Clock / GPIO
	I2C_INT_EC/GPIO	P2.5	15	Embedded Controller interrupt/GPIO
	HPD/GPIO	P3.0	18	Hot Plug Detect I/O for port 1/GPIO
	I2C_SDA_SCB3 / GPIO / VSEL_2	P3.6	20	SCB3 I ² C Data or GPIO or voltage selection control for VBUS
	I2C_SCL_SCB3 / GPIO /VSEL_1	P3.7	21	SCB3 I ² C Clock or GPIO or voltage selection control for VBUS
Reset	XRES	Analog	10	Reset input (Active LOW)

Table 2. Pinout for CYPD5125-40LQXIT (continued)

Group Name	Pin Name	Port	Pin	Description
Power	VBUS	Power	22	VBUS Input for Port 1 (4 V to 21.5 V)
	VSYS	Power	19	2.75 V to 5.5 V supply for the system
	VDDD	Power	31	VDDD supply output 1. VSYS powered - (Min: VSYS-50 mV) 2.7 V to 5.5 V 2. VBUS powered - 3.15 V to 3.6 V
	VDDIO	Power	32	At system-level short the VDDD to VDDIO
	VCCD	Power	33	1.8 V regulator output for filter capacitor. This pin cannot drive external load.
	V5V	Power	8	4.85 V to 5.5 V supply for VCONN FET of Type-C Port 1
Ground	VSS	Ground	EPAD	Ground

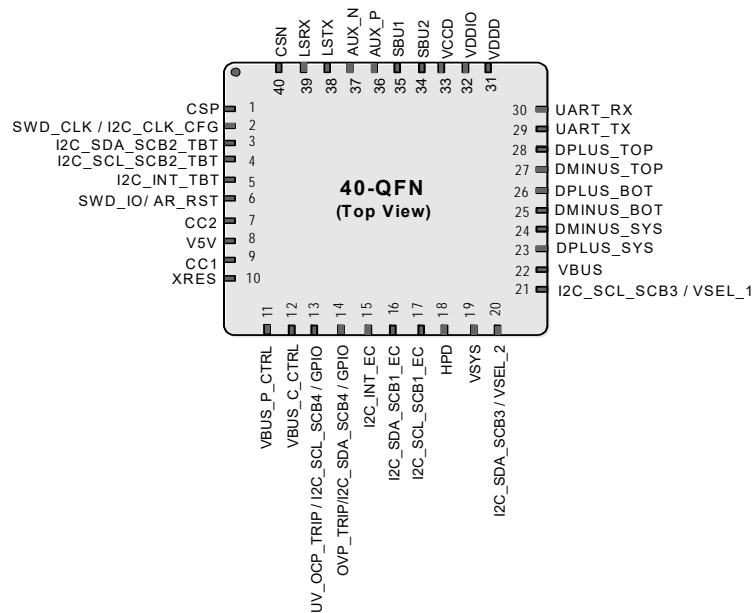
Figure 5. 40-Pin QFN Pin Map (Top View) for CYPD5125-40LQXIT


Table 3. Pinout for CYPD5225-96BZXI, CYPD5235-96BZXI, and CYPD5236-96BZXI

Group Name	Pin Name	Port	Ball Location	Description
USB Type-C Port 1	CC1_P1	Analog	K2	USB PD connector detect/Configuration Channel 1
	CC2_P1	Analog	H2	USB PD connector detect/Configuration Channel 2
USB Type-C Port 2	CC1_P2	Analog	K9	USB PD connector detect/Configuration Channel 1
	CC2_P2	Analog	K10	USB PD connector detect/Configuration Channel 2
MUX Type-C Port 1	AUX_P_P1	Analog	B11	Auxiliary signal for DisplayPort
	AUX_N_P1	Analog	C11	Auxiliary signal for DisplayPort
	LSRX_P1	Analog	A11	Thunderbolt Link Management UART Rx
	LSTX_P1	Analog	A10	Thunderbolt Link Management UART Tx
	SBU1_P1	Analog	A3	Sideband Use signal
	SBU2_P1	Analog	A4	Sideband Use signal
	DMINUS_SYS_P1	Analog	A7	USB 2.0 DM from the Host System
	DPLUS_SYS_P1	Analog	A6	USB 2.0 DP from the Host System
	UART_RX_P1/GPIO	P4.1	A9	UART Rx from Host System/GPIO
	UART_TX_P1/GPIO	P4.0	A8	UART Tx from Host system/GPIO
	DMINUS_BOT_P1	Analog	C1	USB 2.0 DM from Bottom of Type-C Connector
	DPLUS_BOT_P1	Analog	B1	USB 2.0 DP from Bottom of Type-C Connector
	DMINUS_TOP_P1	Analog	A2	USB 2.0 DM from Top of Type-C Connector
DPLUS_TOP_P1	Analog	A1	USB 2.0 DP from Top of Type-C Connector	
MUX Type-C Port 2	AUX_P_P2	Analog	D11	Auxiliary signal for DisplayPort
	AUX_N_P2	Analog	E11	Auxiliary signal for DisplayPort
	LSRX_P2	Analog	L11	Thunderbolt Link Management UART Rx
	LSTX_P2	Analog	K11	Thunderbolt Link Management UART Tx
	SBU1_P2	Analog	E1	Sideband Use signal
	SBU2_P2	Analog	F1	Sideband Use signal
	DMINUS_SYS_P2	Analog	G11	USB 2.0 DM from the Host System
	DPLUS_SYS_P2	Analog	F11	USB 2.0 DP from the Host System
	UART_RX_P2/GPIO	P0.2	J11	UART Rx from Host System/GPIO
	UART_TX_P2/GPIO	P0.1	H11	UART Tx from Host system/GPIO
	DMINUS_BOT_P2	Analog	L1	USB 2.0 DM from Bottom of Type-C Connector
	DPLUS_BOT_P2	Analog	K1	USB 2.0 DP from Bottom of Type-C Connector
	DMINUS_TOP_P2	Analog	H1	USB 2.0 DM from Top of Type-C Connector
DPLUS_TOP_P2	Analog	G1	USB 2.0 DP from Top of Type-C Connector	
VBUS Control Type-C Port1	VBUS_P_CTRL_P1	Analog	K3	Full rail control I/O for enabling/disabling Provider load PFET of USB Type-C Port 1 0: Path ON High Z: Path OFF
	VBUS_C_CTRL_P1	Analog	K4	Full rail control I/O for enabling/disabling Consumer load PFET of USB Type-C Port 1 0: Path ON High Z: Path OFF

Table 3. Pinout for CYPD5225-96BZXI, CYPD5235-96BZXI, and CYPD5236-96BZXI (continued)

Group Name	Pin Name	Port	Ball Location	Description	
VBUS Control Type-C Port2	VBUS_P_CTRL_P2	Analog	B4	Full rail control I/O for enabling/disabling Provider load PFET of USB Type-C Port 2. 0: Path ON High Z: Path OFF	
	VBUS_C_CTRL_P2	Analog	B5	Full rail control I/O for enabling/disabling Consumer load PFET of USB Type-C Port 2. 0: Path ON High Z: Path OFF	
VBUS OCP	CSP_P1	Analog	J1	Current Sense Positive Input for P1	
	CSN_P1	Analog	B3	Current Sense Negative Input for P1	
	CSP_P2	Analog	L2	Current Sense Positive Input for P2	
	CSN_P2	Analog	K8	Current Sense Negative Input for P2	
GPIOs and Serial Interfaces	GPIO	P3.1	L7	GPIO	
	I2C_SDA_SCB4/OVP_TRIP_P1/GPIO	P2.4	K5	VBUS overvoltage output indicator for Port 1 / SCB4 I2C Data/ GPIO	
	OVP_TRIP_P2 / GPIO	P2.2	L8	VBUS overvoltage output indicator for Port 2 / GPIO	
	VSEL_1_P2 / GPIO	P0.0	L4	Voltage selection control for VBUS on Port 2 / GPIO	
	UV_OCP_TRIP_P1/GPIO	P1.4	B6	VBUS undervoltage of OCP output indicator for Port 1/GPIO	
	HPD_P1/GPIO	P3.0	K7	Hot Plug Detect I/O for Port 1 / GPIO	
	HPD_P2/GPIO	P3.4	E10	Hot Plug Detect I/O for Port 2 /GPIO	
	VCONN_OCP_TRIP_P2/ GPIO	P3.3	B9	VCONN OCP output indicator for Port 2 / GPIO	
	VCONN_OCP_TRIP_P1/GPIO	P3.5	B8	VCONN OCP output indicator for Port 1/ GPIO	
	UV_OCP_TRIP_P2/GPIO	P1.5	B7	VBUS undervoltage or OCP output indicator for Port 2/GPIO	
	VSEL_2_P2 / GPIO	P2.0	H10	Voltage selection control for VBUS on Port 2 / GPIO	
	I2C_SCL_SCB1_EC/ GPIO	P5.1	L6	SCB1 I ² C Clock	
	I2C_SDA_SCB1_EC/ GPIO	P5.0	K6	SCB1 I ² C Data	
	I2C_INT_EC/GPIO	P2.5	L5	I ² C interrupt line	
	I2C_SCL_SCB2_TBT/GPIO	P1.2	E2	SCB2 I ² C Clock/GPIO	
	I2C_SDA_SCB2_TBT/GPIO	P1.1	D2	SCB2 I ² C Data /GPIO	
	I2C_INT_TBT_P1/GPIO	P1.3	F2	I ² C interrupt line/GPIO	
	I2C_INT_TBT_P2/GPIO	P2.1	G2	I ² C interrupt line	
	I2C_SCL_SCB3 / VSEL_1_P1 /GPIO	P3.7	L10	SCB3 I ² C Clock/ Voltage selection control for VBUS on Port 1/ GPIO	
	I2C_SDA_SCB3 / VSEL_2_P1 / GPIO	P3.6	J10	SCB3 I ² C Data / Voltage selection control for VBUS on Port 1 /GPIO	
	I2C_SCL_SCB4/GPIO	P2.3	F10	SCB4 I ² C Clock /GPIO	
	I2C_SDA_SCB4/GPIO	P3.2	G10	SCB4 I ² C Data /GPIO	
	SWD_IO/AR_RST#/GPIO	P1.6	B2	SWD I/O / AR Reset / GPIO	
	SWD_CLK/I2C_CFG_EC/GPIO	P1.0	C2	SWD Clock / I ² C config line / GPIO. I ² C config line is used to select the I ² C address of HPI interface. The state of line decides the 7 bit I ² C address for HPI. I ² C Config Line Floating: 0x08 Pulled up with 1 KW: 0x42 Pulled down with 1 KW: 0x40	
	Reset	XRES	Analog	H6	Reset input (Active LOW)

Table 3. Pinout for CYPD5225-96BZXI, CYPD5235-96BZXI, and CYPD5236-96BZXI (continued)

Group Name	Pin Name	Port	Ball Location	Description
Power	VBUS_P1	Power	D1	VBUS Input for Port 1 (4 V to 21.5 V)
	VBUS_P2	Power	L3	VBUS Input for Port 2 (4 V to 21.5 V)
	VSYS	Power	A5	2.75 V to 5.5 V supply for the system
	VDDD	Power	D10	VDDD supply output 1. VSYS powered - (Min: VSYS-50 mV) 2.7 V to 5.5 V 2. VBUS powered - 3.15 V to 3.6 V
	VCCD	Power	B10	1.8 V regulator output for filter capacitor. This pin cannot drive external load.
	VDDIO	Power	C10	At system-level short the VDDD to VDDIO
	V5V_P1	Power	J2	4.85 V to 5.5 V supply for VCONN FET of Type-C Port 1
	V5V_P2	Power	L9	4.85 V to 5.5 V supply for VCONN FET of Type-C Port 2
Ground	GND	Ground	D5	Ground
	GND	Ground	D6	Ground
	GND	Ground	D7	Ground
	GND	Ground	D8	Ground
	GND	Ground	E4	Ground
	GND	Ground	E5	Ground
	GND	Ground	E6	Ground
	GND	Ground	E7	Ground
	GND	Ground	E8	Ground
	GND	Ground	F4	Ground
	GND	Ground	F5	Ground
	GND	Ground	F6	Ground
	GND	Ground	F7	Ground
	GND	Ground	F8	Ground
	GND	Ground	G4	Ground
	GND	Ground	G5	Ground
	GND	Ground	G6	Ground
	GND	Ground	G7	Ground
GND	Ground	H7	Ground	
No Connect	NC	DNU	G8	Not Connect
	NC	DNU	H4	Not Connect
	NC	DNU	H5	Not Connect
	NC	DNU	H8	Not Connect

Figure 6. 96-Pin BGA Pin Map for CYPD5225-96BZXI, CYPD5235-96BZXI, and CYPD5236-96BZXI

	1	2	3	4	5	6	7	8	9	10	11
A	DPLUS_TO_P_P1	DMIN-US_TOP_P1	SBU1_P1	SBU2_P1	VSYS	DPLUS_SY_S_P1	DMIN-US_SYS_P1	UART_Tx_P1 / P4.0	UART_Rx_P1 / P4.1	LSTx_P1	LSRx_P1
B	DPLUS_BO_T_P1	SWD_DATA/TBT_RST#/P1.6	CSN_P1	VBUS_P_C-TRL_P2	VBUS_C_C-TRL_P2	P1.4 / UV_OCP_T RIP_P1	P1.5 / UV_OC_TRIP_P2	P3.5 / VCON_OCP_TRIP_P1	P3.3 / VCON_OCP_TRIP_P2	VCCD	AUX_P_P1
C	DMIN-US_BOT_P1	SWD_CLK/I2C_CFG_EC/P1.0								VDDIO	AUX_N_P1
D	VBUS_P1	I2C_S-DA_SCB2_TB_T/P1.1			GND	GND	GND	GND		VDDD	AUX_P_P2
E	SBU1_P2	I2C_S-CL_SCB2_TB_T/P1.2		GND	GND	GND	GND	GND		HPD_P2 / P3.4	AUX_N_P2
F	SBU2_P2	I2C_INT_TBT_P1/P1.3		GND	GND	GND	GND	GND		SCL_4 / P2.3	DPLUS_SYS_P2
G	DPLUS_TO_P_P2	I2C_INT_TBT_P2/P2.1		GND	GND	GND	GND	DNU		SDA_4 / P3.2	DMIN-US_SYS_P2
H	DMIN-US_TOP_P2	CC2_P1		DNU	DNU	XRES	GND	DNU		VSEL_2_P2/P2.0	UART_Tx_P2/P0.1
J	CSP_P1	V5V_P1								SDA_3/VSEL_2_P1/P3.6	UART_Rx_P2/P0.2
K	DPLUS_BO_T_P2	CC1_P1	VBUS_P_C-TRL_P1	VBUS_C_C-TRL_P1	I2C_S-DA_SCB4/OVP_TRIP_P1/P2.4	I2C_S-DA_SCB1_EC/P5.0	HPD_P1 / P3.0	CSN_P2	CC1_P2	CC2_P2	LSTx_P2
L	DMIN-US_BOT_P2	CSP_P2	VBUS_P2	VSEL_1_P2/P0.0	I2C_INT_EC/P2.5	I2C_S-CL_SCB1_EC/P5.1	P3.1	OVP_TRIP_P2/P2.2	V5V_P2	SCL_3/VSEL_1_P1/P3.7	LSRx_P2

Type-C Port 1
Type-C Port 2
Power Pins
GND
GPIOs

Table 4 through Table 7 provide the various configuration options for the serial interfaces.

Table 4. Serial Communication Block (SCB1) Configuration

QFN Pin	BGA Pin	UART	SPI	I ² C	GPIO Functionality
16	K6	–	–	I2C_SDA_SCB1	GPIO
17	L6	–	–	I2C_SCL_SCB1	GPIO
	B8	UART_CTS_SCB1	–	–	VCONN OCP output indicator for port 1/ GPIO
20	J10	UART_TX_SCB1	SPI_SEL_SCB1	–	I2C_SDA_SCB3/ VSEL_2_P1 /GPIO
21	L10	UART_RX_SCB1	SPI_MISO_SCB1	–	I2C_SCL_SCB3 / VSEL_1_P1/GPIO
18	K7	UART_RTS_SCB1	–	–	HPD_P1/GPIO
29	A8	–	SPI_MOSI_SCB1	–	UART_TX_P1/GPIO
30	A9	–	SPI_CLK_SCB1	–	UART_RX_P1/GPIO

Note: UART TX and RX of the SCB1 is also the I²C SDA and SCL of the SCB3. So if SCB 3 is in use, then SCB1 cannot be used for UART and SPI.

Table 5. Serial Communication Block (SCB2) Configuration

QFN Pin	BGA Pin	UART	SPI Master	I ² C Slave	GPIO Functionality
2	C2	UART_RX_SCB2	SPI_SEL_SCB2	–	SWD_CLK/I2C_CFG_EC/GPIO
3	D2	UART_TX_SCB2	SPI_MOSI_SCB2	I2C_SDA_SCB2	I2C_SDA_SCB2_TBT/GPIO
4	E2	UART_CTS_SCB2	SPI_MISO_SCB2	I2C_SCL_SCB2	I2C_SCL_SCB2_TBT/GPIO
5	F2	UART_RTS_SCB2	SPI_CLK_SCB2	–	I2C_INT_TBT_P1/GPIO

Table 6. Serial Communication Block (SCB3) Configuration

QFN Pin	BGA Pin	UART	SPI Master	I ² C Slave	GPIO Functionality
20	J10	–	–	I2C_SDA_SCB3	UART_TX_SCB1/VSEL_2_P1 /GPIO
21	L10	–	–	I2C_SCL_SCB3	UART_RX_SCB1 / VSEL_1_P1/GPIO
	G2	UART_CTS_SCB3	SPI_MISO_SCB3	–	I2C_INT_TBT_P2/GPIO
	H10	UART_TX_SCB3	SPI_MOSI_SCB3	–	VSEL_2_P2 / GPIO
	L4	UART_RX_SCB3	SPI_SEL_SCB3	–	VSEL_1_P2 / GPIO
	L8	UART_RTS_SCB3	SPI_CLK_SCB3	–	OVP_TRIP_P2 / GPIO

Table 7. Serial Communication Block (SCB4) Configuration

QFN Pin	BGA Pin	UART	SPI Master	I ² C Slave	GPIO Functionality
13	F10	–	–	I2C_SCL_SCB4	GPIO
14	G10	UART_TX_SCB4	SPI_MOSI_SCB4	I2C_SDA_SCB4	GPIO
	L7	UART_CTS_SCB4	SPI_MISO_SCB4	–	GPIO
	B9	UART_RX_SCB4	SPI_SEL_SCB4	–	VCONN_OCP_TRIP_P2/GPIO
	E10	UART_RTS_SCB4	SPI_CLK_SCB4	–	HPD_P2/GPIO

Application Diagrams

Figure 8 and Figure 9 illustrate the Dual Type-C Port and Single Type-C port Thunderbolt Notebook DRP application diagrams using a CCG5 device respectively. The Type-C port can be used as a power provider/power consumer.

The CCG5 device communicates with the embedded controller (EC), which manages the Battery Charger Controller (BCC) to control the charging and discharging of the internal battery. It also updates the Thunderbolt Controller via I²C to route the High-speed signals coming from the Type-C port to the USB host (during normal mode) or the Graphics processor unit (during Display port Alternate mode) or the Thunderbolt Host (during Thunderbolt Alternate mode) based on the alternate mode negotiation.

For the dual Type-C notebook application (Figure 8), these Type-C ports can be power providers or power consumers simultaneously. The CCG5 device controls the transfer of USB 2.0 D± lines from the top and bottom of the Type-C receptacle to the D± lines of the USB Host controller. CCG5 also handles the routing of SBU1 and SBU2 lines from the Type-C receptacle to the Thunderbolt controller for the Link management. CCG5 offers ESD Protection on D± and SBU lines as well as VBUS Short protection on SBU and CC lines.

The CCG5 device has an integrated VCONN FET for applications that need to provide power for accessories and cables using the VCONN pin of the Type-C receptacle. VBUS FETs are also used for providing power over VBUS and for consuming power over VBUS. The 10 mΩ resistor between the 5 V supply and FETs is used for overcurrent detection on the VBUS. The VBUS_P_CTRL pin of CCG5 has an in-built VBUS monitoring circuit that can detect OVP and UVP on VBUS.

CCG5 also has an in-built VBUS discharge circuit that is used to quickly discharge VBUS after the Type-C connection is detached. The internal resistance (as listed in Table 41) of this VBUS discharge circuit is expected to be sufficient for typical CCG5 applications. However, customers can include an optional VBUS discharge circuit as shown in Figure 7 using any available GPIO. This optional circuit can be added to the design if the discharge time using the in-built VBUS discharge circuit needs to be further reduced; that is, VBUS transition time from higher to lower voltages can be further reduced using the external VBUS discharge circuit shown in Figure 7. This optional external circuit comprises of a N-channel MOSFET and the CCG5 device can be used to enable or disable it as appropriate.

Figure 7. Optional External VBUS Discharge Circuit



Figure 8. CCG5 in a Dual Port Notebook Application using CYPD5225-96BZXI

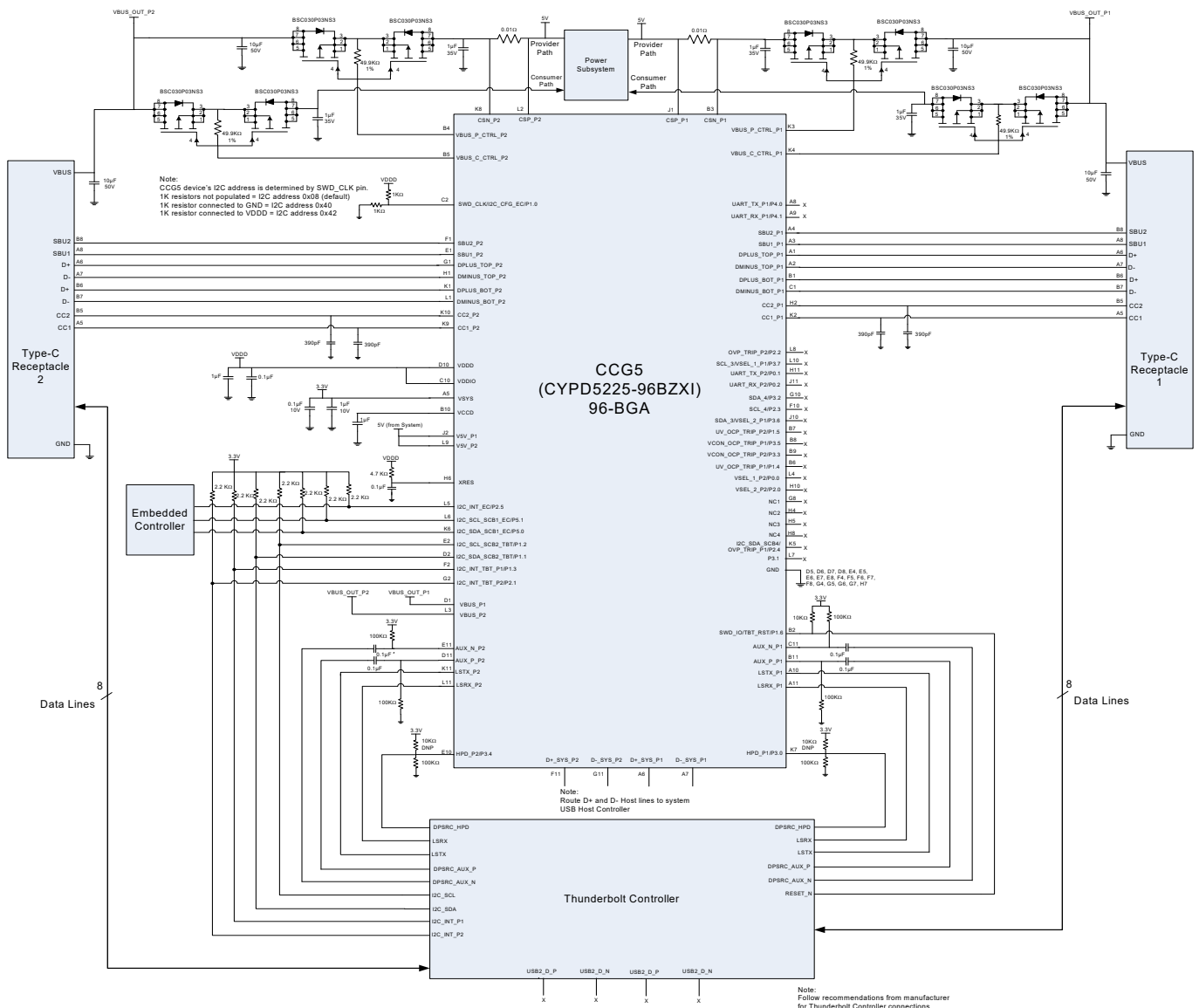


Figure 9 illustrates a Single Port Thunderbolt Notebook DRP application diagram using CYPD5125-40LQXIT.

Figure 9. CCG5 in a Single Port Notebook Application using CYPD5125-40LQXIT



Figure 10 illustrates the Dual Type-C Port Thunderbolt device/dock upstream application diagram using a CCG5 device. The CCG5 device communicates with the power system over I²C, which manages the power provided to the upstream Type-C ports. It also updates the Thunderbolt Controller over I²C based on the alternate mode negotiation to sink Thunderbolt or USB or DisplayPort Data. The CCG5 device controls the transfer of USB 2.0 D± lines from the top and bottom of the Type-C receptacle to the D± lines of the Thunderbolt Controller and Billboard controller. CCG5 also handles the routing of SBU1 and SBU2 lines from the Type-C receptacle to the Thunderbolt controller for the link management. As mentioned in [Features](#), CCG5 offers ESD Protection on D± and SBU lines as well as VBUS Short protection on SBU and CC lines.

Figure 10. CCG5 in a Dual port Thunderbolt Device/Dock Upstream Port Application using CYPD5235-96BXZI

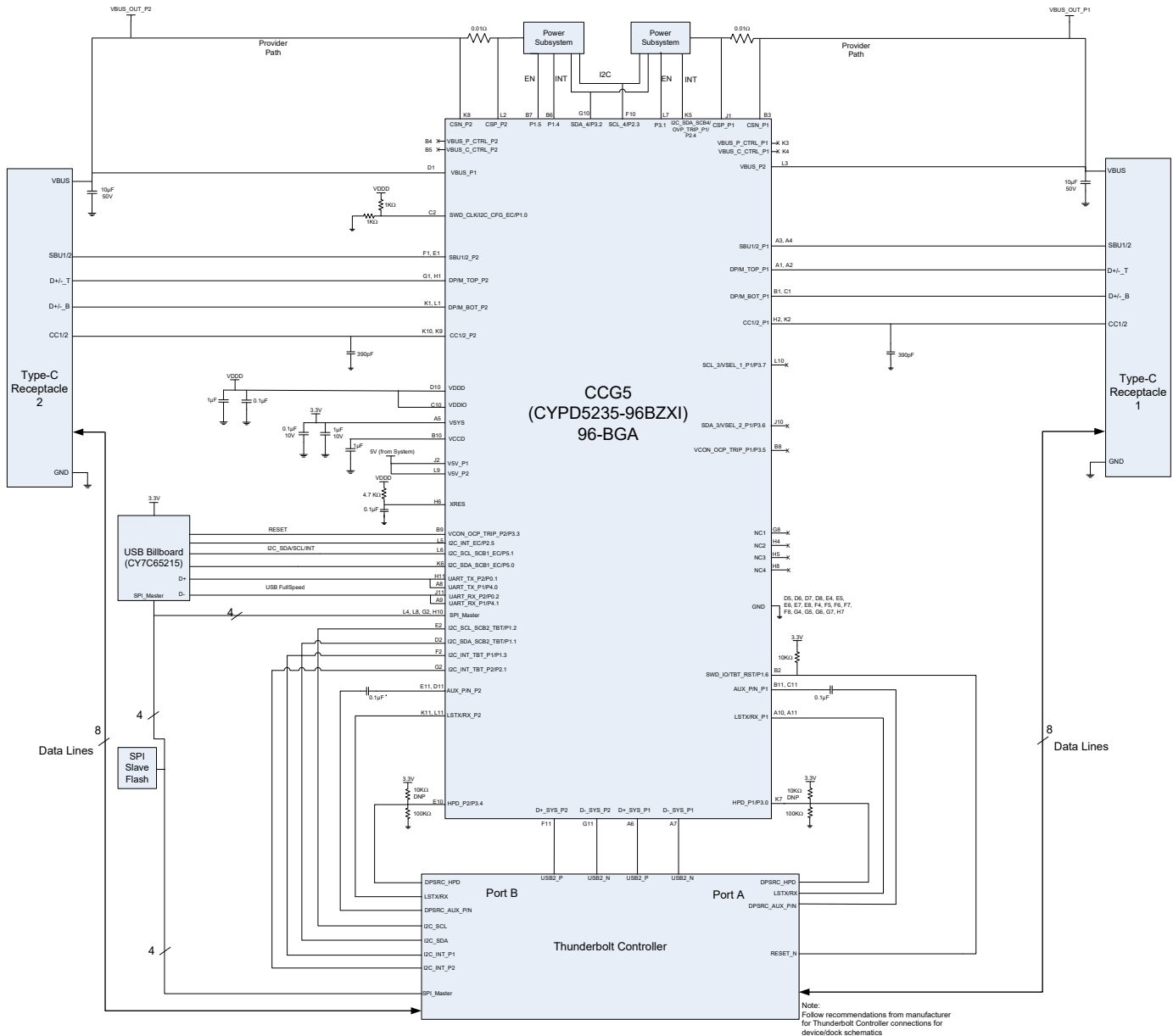
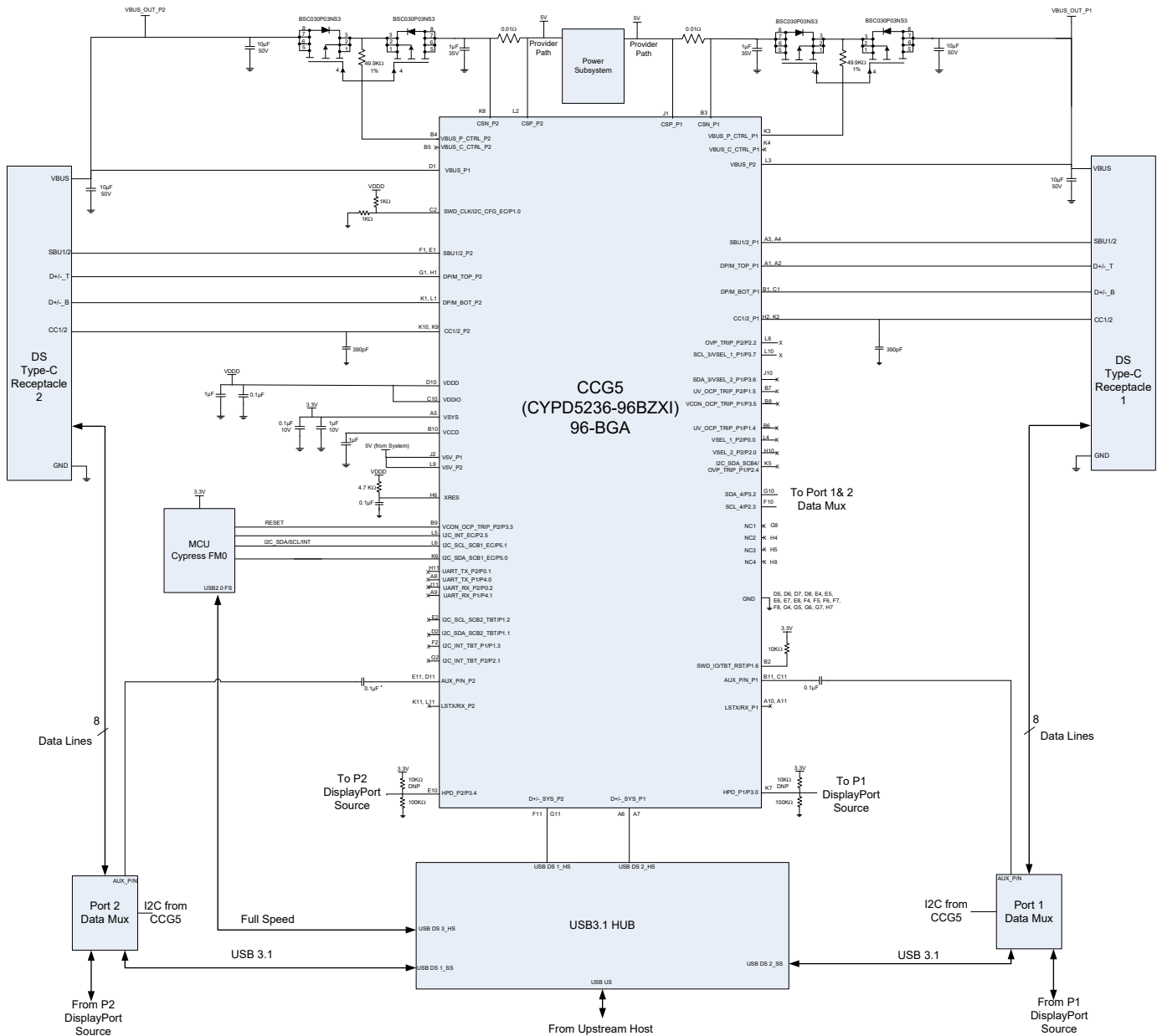


Figure 11 illustrates the Dual Type-C Port dock downstream application diagram using a CCG5 device. The CCG5 negotiates power contract with the connected device on the downstream Type-C port and controls the power system. It also controls the data mux via I²C based on the alternate mode negotiation to source USB SuperSpeed and/or DisplayPort on the downstream Type-C port. As mentioned above, CCG5 device offers ESD Protection on D± and SBU lines as well as VBUS Short protection on SBU and CC lines.

Figure 11. CCG5 in a Dual port Dock Downstream Port Application using CYPD5236-96BX1



Electrical Specifications

Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings^[3]

Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
V _{SYS_MAX}	Digital supply relative to V _{SS}	–	–	6	V	Absolute max
V _{5V_P1_MAX}	Max supply voltage relative to V _{SS}	–	–	6	V	
V _{5V_P2_MAX}	Max supply voltage relative to V _{SS}	–	–	6	V	
V _{BUS_P1_MAX}	Max VBUS voltage relative to V _{SS}	–	–	24	V	
V _{BUS_P2_MAX}	Max VBUS voltage relative to V _{SS}	–	–	24	V	
V _{DDIO_MAX}	Max supply voltage relative to V _{SS}	–	–	V _{DDD}	V	
V _{GPIO_ABS}	Inputs to GPIO, DP/DM mux (UART, SYS, DP/DM top/bot pins), SBU mux (AUX, LS, SBU1/2 pins)	–0.5	–	V _{DDIO} + 0.5	V	
I _{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
I _{GPIO_INJECTION}	GPIO injection current, Max for V _{IH} > V _{DDD} , and Min for V _{IL} < V _{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	Applicable for all pins except SBU pins
ESD_HBM_SBU ^[4]	Electrostatic discharge human body model for SBU1, SBU2 pins	1100	–	–	V	Only applicable to SBU pins
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch up	–200	–	200	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2, contact discharge	8000	–	–	V	Contact Discharge for CC1_P1/P2, CC2_P1/P2, VBUS_P1/P2, SBU1_P1/P2, SBU2_P1/P2, DPLUS_TOP/BOT_P1/P2, DMINUX_TOP/BOT_P1/P2
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2, air discharge	15000	–	–	V	Air Discharge for CC1_P1/P2, CC2_P1/P2, VBUS_P1/P2, SBU1_P1/P2, SBU2_P1/P2, DPLUS_TOP/BOT_P1/P2, DMINUX_TOP/BOT_P1/P2
VCC_PIN_ABS	Max voltage on CC1 and CC2 pins	–	–	24	V	Absolute max
VSBU_PIN_ABS	Max voltage on SBU1 and SBU2 pins	–	–	24	V	
VGPIO_OVT_ABS	OVT GPIO voltage	–0.5	–	6	V	Absolute maximum for OVT pins K6 and L6 of BGA, pins 16 and 17 of QFN

Notes

- Usage above the absolute maximum conditions listed in Table 8 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.
- JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

Device-Level Specifications

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 3.0 V to 5.5 V except where noted.

Table 9. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.PWR#23	V _{SYS}	Power supply input voltage	2.75	–	5.5	V	UFP applications
SID.PWR#23_A	V _{SYS}	Power supply input voltage	3.15	–	5.5	V	DFP/DRP applications
SID.PWR#22	V _{BUS}	VBUS_P1 and VBUS_P2 valid range	4	–	21.5	V	–
SID.PWR#1	V _{DDD}	Regulated output voltage when V _{SYS} is powered	V _{SYS} – 0.05	–	V _{SYS}	V	–
SID.PWR#1_A	V _{DDD}	Regulated output voltage when V _{BUS} powered	3.15	–	3.6	V	–
SID.PWR#26	V _{5V_P1} and V _{5V_P2}	Power supply Input voltage	4.85	–	5.5	V	–
SID.PWR#13	V _{DDIO}	GPIO power supply	V _{DDD}	–	V _{DD} D	V	At system-level short the V _{DDIO} to V _{DDD}
SID.PWR#24	V _{CCD}	Output voltage (for Core Logic)	–	1.8	–	V	–
SID.PWR#15	C _{EFC}	External regulator voltage bypass on V _{CCD}	80	100	120	nF	X5R ceramic or better
SID.PWR#16	C _{EXC}	Power supply decoupling capacitor on V _{DDD}	–	1	–	μF	
SID.PWR#27	C _{EXV}	Power supply decoupling capacitor on V _{5V_P1} and V _{5V_P2}	–	0.1	–	μF	
SID.PWR#5	I _{VDDD_EXT}	External load current on V _{DDD} either in Active or Deep Sleep mode	–	1	2	mA	–
Active Mode, V_{SYS} = 2.75 to 5.5 V. Typical values measured at V_{SYS} = 3.3 V							
SID.PWR#4	I _{DD12}	Supply current	–	10	–	mA	T _A = 25 °C, CC I/O IN Transmit or Receive, no I/O sourcing current, CPU at 24 MHz, two PD ports active
Deep Sleep Mode, V_{SYS} = 2.75 to 3.6 V							
SID34	I _{DD29}	V _{SYS} = 2.75 to 3.6 V, I ² C, wakeup and WDT on.	–	150	–	μA	V _{SYS} = 3.3 V, T _A = 25 °C,
SID34A	I _{DD29A}		–	160	–	μA	V _{SYS} = 3.3 V, T _A = 25 °C for two PD ports
SID_DS1	I _{DD_DS1}	V _{SYS} = 3.3 V, CC wakeup on, Type-C not connected.	–	100	–	μA	Power source = V _{SYS} , Type-C not attached, CC enabled for wakeup, Rp and Rd connected at 70-ms intervals by CPU. Rp, Rd connection should be enabled for both PD ports.
SID_DS3	I _{DD_DS2}	V _{SYS} = 3.3 V, CC wakeup on, DP/DM, SBU ON with ADC/CSA/UVOV On	–	500	–	μA	IDD_DS1 + DP/DM, SBU, CC ON, ADC/CSA/UVOV ON
XRES Current							
SID307	I _{DD_XR}	Supply current while XRES asserted	–	130	–	μA	Power Source = V _{SYS} = 3.3 V, Type-C not attached, T _A = 25 °C

Table 10. AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.CLK#4	F _{CPU}	CPU input frequency	–	–	48	MHz	All V _{DD}
SID.PWR#21	T _{DEEPSLEEP}	Wakeup from Deep Sleep mode	–	35	–	μs	Guaranteed by characterization
SYS.XRES#5	T _{XRES}	External reset pulse width	5	–	–	μs	
SYS.FES#1	T _{PWR_RDY}	Power-up to “Ready to accept I ² C/CC command”	–	5	25	ms	

Table 11. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.GIO#37	V _{IH_CMOS}	Input voltage HIGH threshold	0.7 × V _{DDIO}	–	–	V	CMOS input
SID.GIO#38	V _{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × V _{DDIO}	V	CMOS input
SID.GIO#39	V _{IH_VDDIO2.7-}	LVTTL input, V _{DDIO} < 2.7 V	0.7 × V _{DDIO}	–	–	V	–
SID.GIO#40	V _{IL_VDDIO2.7-}	LVTTL input, V _{DDIO} < 2.7 V	–	–	0.3 × V _{DDIO}	V	–
SID.GIO#41	V _{IH_VDDIO2.7+}	LVTTL input, V _{DDIO} ≥ 2.7 V	2.0	–	–	V	–
SID.GIO#42	V _{IL_VDDIO2.7+}	LVTTL input, V _{DDIO} ≥ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V _{OH}	Output voltage HIGH level	V _{DDIO} – 0.6	–	–	V	I _{OH} = –4 mA at 3 V V _{DDIO}
SID.GIO#34	V _{OH}	Output voltage HIGH level	V _{DDIO} – 0.5	–	–	V	I _{OH} = –1mA at 1.8 V V _{DDIO}
SID.GIO#35	V _{OL}	Output voltage LOW level	–	–	0.6	V	I _{OL} = 4 mA at 1.8 V V _{DDIO}
SID.GIO#36	V _{OL}	Output voltage LOW level	–	–	0.6	V	I _{OL} = 10 mA (IOL_LED) at 3 V V _{DDIO}
SID.GIO#5	R _{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	+25 °C T _A , All V _{DDIO}
SID.GIO#6	R _{PD}	Pull-down resistor value	3.5	5.6	8.5	kΩ	+25 °C T _A , All V _{DDIO}
SID.GIO#16	I _{IL}	Input leakage current (absolute value)	–	–	2	nA	+25 °C T _A , 3-V V _{DDIO}
SID.GIO#17	C _{PIN}	Max pin capacitance	–	3	7	pF	–
SID.GIO#43	V _{HYSTTL}	Input hysteresis, LVTTL	15	40	–	mV	V _{DDIO} > 2.7 V. Guaranteed by characterization.
SID.GIO#44	V _{HYSCMOS}	Input hysteresis CMOS	0.05 × V _{DDIO}	–	–	mV	V _{DDIO} < 4.5 V
SID.GIO#44A	V _{HYSCMOS55}	Input hysteresis CMOS	200	–	–	mV	V _{DDIO} > 4.5 V

Table 12. I/O AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID70	T _{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3-V V _{DDIO} , C _{load} = 25 pF
SID71	T _{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3-V V _{DDIO} , C _{load} = 25 pF
SID.GIO#46	T _{RISES}	Rise time in Slow Strong mode	10	–	60	ns	3.3-V V _{DDIO} , C _{load} = 25 pF
SID.GIO#47	T _{FALLS}	Fall time in Slow Strong mode	10	–	60	ns	3.3-V V _{DDIO} , C _{load} = 25 pF
SID.GIO#48	F _{GPIO_OUT1}	GPIO F _{OUT} ; 3.3 V ≤ V _{DDIO} ≤ 5.5 V. Fast Strong mode.	–	–	16	MHz	90/10%, 25 pF load
SID.GIO#49	F _{GPIO_OUT2}	GPIO F _{OUT} ; 1.7 V ≤ V _{DDIO} ≤ 3.3 V. Fast Strong mode.	–	–	16	MHz	90/10%, 25 pF load
SID.GIO#50	F _{GPIO_OUT3}	GPIO F _{OUT} ; 3.3 V ≤ V _{DDIO} ≤ 5.5 V. Slow Strong mode.	–	–	7	MHz	90/10%, 25 pF load

Table 12. I/O AC Specifications (Guaranteed by Characterization) (continued)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.GIO#51	F _{GPIO_OUT4}	GPIO F _{OUT} ; 1.7 V ≤ V _{DDIO} ≤ 3.3 V. Slow Strong mode.	–	–	3.5	MHz	90/10%, 25 pF load
SID.GIO#52	F _{GPIO_IN}	GPIO input operating frequency; 1.7 V ≤ V _{DDIO} ≤ 5.5 V.	–	–	16	MHz	90/10% V _{IO}

XRES

Table 13. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.XRES#1	V _{IH}	Input voltage HIGH threshold	0.7 x V _{DDIO}	–	–	V	CMOS input
SID.XRES#2	V _{IL}	Input voltage LOW threshold	–	–	0.3 x V _{DDIO}	V	CMOS input
SID.XRES#3	C _{IN}	Input capacitance	–	–	7	pF	–
SID.XRES#4	V _{HYSXRES}	Input voltage hysteresis	–	0.05 x V _{DDIO}	–	mV	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

PWM for GPIO Pins

Table 14. PWM AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.TCPWM.3	T _{CPWMFREQ}	Operating frequency	–	–	F _c	MHz	F _c max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	T _{PWMENEXT}	Input trigger pulse width	2/F _c	–	–	ns	For all trigger events
SID.TCPWM.5	T _{PWMEXT}	Output trigger pulse width	2/F _c	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T _{CRES}	Resolution of counter	1/F _c	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM _{RES}	PWM resolution	1/F _c	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q _{RES}	Quadrature inputs resolution	1/F _c	–	–	ns	Minimum pulse width between quadrature-phase inputs

Table 15. Fixed I²C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID153	F _{I2C1}	Bit rate	–	–	1	Mbps	–

Table 16. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID162	F _{UART}	Bit rate	–	–	1	Mbps	–

Table 17. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID166	F _{SPI}	SPI operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 18. Fixed SPI Master Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID167	T _{DMO}	MOSI valid after SClk driving edge	–	–	15	ns	–
SID168	T _{DSI}	MISO valid before SClk capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	T _{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to slave capturing edge

Table 19. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID170	T _{DMI}	MOSI Valid before Sclck capturing edge	40	–	–	ns	–
SID171	T _{DSO}	MISO Valid after Sclck driving edge	–	–	48 + 3 × T _{SCB}	ns	T _{SCB} = T _{CPU}
SID171A	T _{DSO_EXT}	MISO Valid after Sclck driving edge in Ext Clk mode	–	–	48	ns	–
SID172	T _{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	T _{SSELSCK}	SSEL Valid to first SCK Valid edge	100	–	–	ns	–

Memory
Table 20. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.MEM#4	T _{ROW_WRITE}	Row (Block) write time (erase and program)	–	–	20	ms	–
SID.MEM#3	T _{ROW_ERASE}	Row erase time	–	–	13	ms	–
SID.MEM#8	T _{ROWPROGRAM}	Row program time after erase	–	–	7	ms	25 °C to 55 °C, All V _{DDD}
SID178	T _{BULKERASE}	Bulk erase time (128 KB)	–	–	35	ms	Guaranteed by design
SID180	T _{DEVPROG}	Total device program time	–	–	25	s	Guaranteed by design
SID.MEM#6	F _{END}	Flash endurance	100k	–	–	cycles	–
SID182	F _{RET1}	Flash retention, T _A ≤ 55 °C, 100K P/E cycles	20	–	–	years	–
SID182A	F _{RET2}	Flash retention, T _A ≤ 85 °C, 10K P/E cycles	10	–	–	years	–

System Resources

Power-on-Reset (POR) with Brownout

Table 21. Imprecise Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID185	V _{RISEIPOR}	Rising trip voltage	0.80	–	1.50	V	Guaranteed by characterization
SID186	V _{FALLIPOR}	Falling trip voltage	0.70	–	1.4	V	

Table 22. Precise Power On Reset (POR) (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID190	V _{FALLPPOR}	Brownout Detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	Guaranteed by characterization
SID192	V _{FALLDPSLP}	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	

SWD Interface

Table 23. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.SWD#1	F_SWDCLK1	$3.3\text{ V} \leq V_{DDIO} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCLK \leq 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	$2.7\text{ V} \leq V_{DDIO} \leq 3.3\text{ V}$	–	–	7	MHz	SWDCLK \leq 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	$T = 1/f\text{ SWDCLK}$	$0.25 \times T$	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	$T = 1/f\text{ SWDCLK}$	$0.25 \times T$	–	–	ns	
SID.SWD#5	T_SWDO_VALID	$T = 1/f\text{ SWDCLK}$	–	–	$0.50 \times T$	ns	
SID.SWD#6	T_SWDO_HOLD	$T = 1/f\text{ SWDCLK}$	1	–	–	ns	

Internal Main Oscillator

Table 24. IMO AC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.CLK#13	F _{IMOTOL}	Frequency variation at 48 MHz (trimmed)	–	–	± 2	%	$2.7\text{ V} \leq V_{DD} < 5.5\text{ V}$, $25\text{ }^\circ\text{C} \leq T_A \leq 85\text{ }^\circ\text{C}$
SID.CLK#13A	F _{IMOTOLVCCD}	Frequency variation at 48 MHz (trimmed)	–	–	± 4	%	All conditions
SID226	T _{STARTIMO}	IMO start-up time	–	–	7	μs	–
SID.CLK#1	F _{IMO}	IMO frequency	–	48	–	MHz	–

Internal Low-speed Oscillator

Table 25. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID234	T _{STARTILO1}	I _{LO} start-up time	–	–	2	ms	Guaranteed by characterization
SID238	T _{ILODUTY}	I _{LO} duty cycle	40	50	60	%	
SID.CLK#5	F _{ILO}	I _{LO} frequency	20	40	80	kHz	–

Table 26. PD DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.cc_shvt.1	vSwing	Transmitter Output High Voltage	1.05	–	1.2	V	–
SID.DC.cc_shvt.2	vSwing_low	Transmitter Output Low Voltage		–	0.075	V	–
SID.DC.cc_shvt.3	zDriver	Transmitter output impedance	33	–	75	Ω	–
SID.DC.cc_shvt.4	zBmcRx	Receiver Input Impedance	10	–		MΩ	Guaranteed by design
SID.DC.cc_shvt.5	Idac_std	Source current for USB standard advertisement	64	–	96	μA	–
SID.DC.cc_shvt.6	Idac_1p5a	Source current for 1.5A at 5 V advertisement	165.6	–	194.4	μA	–
SID.DC.cc_shvt.7	Idac_3a	Source current for 3A at 5 V advertisement	303.6	–	356.4	μA	–
SID.DC.cc_shvt.8	Rd	Pull down termination resistance when acting as UFP (upstream facing port)	4.59	–	5.61	kΩ	–
SID.DC.cc_shvt.9	Rd_db	Pull down termination resistance when acting as UFP, with dead battery (upstream facing port)	4.08	–	6.12	kΩ	–
SID.DC.cc_shvt.10	zOPEN	CC impedance to ground when disabled	108	–		kΩ	–
SID.DC.cc_shvt.11	DFP_default_0p2	CC voltages on DFP side-Standard USB	0.15	–	0.25	V	–
SID.DC.cc_shvt.12	DFP_1.5A_0p4	CC voltages on DFP side-1.5A	0.35	–	0.45	V	–
SID.DC.cc_shvt.13	DFP_3A_0p8	CC voltages on DFP side-3A	0.75	–	0.85	V	–
SID.DC.cc_shvt.14	DFP_3A_2p6	CC voltages on DFP side-3A	2.45	–	2.75	V	–
SID.DC.cc_shvt.15	UFP_default_0p66	CC voltages on UFP side-Standard USB	0.61	–	0.7	V	–
SID.DC.cc_shvt.16	UFP_1.5A_1p23	CC voltages on UFP side-1.5A	1.16	–	1.31	V	–
SID.DC.cc_shvt.17	Vattach_ds	Deep sleep attach threshold	0.3	–	0.6	%	–
SID.DC.cc_shvt.18	Rattach_ds	Deep sleep pull-up resistor	10	–	50	kΩ	–
SID.DC.cc_shvt.30	FS_0p53	Voltage threshold for Fast Swap Detect	0.49	–	0.58	V	–

Analog to Digital Converter
Table 27. ADC DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	–
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	–
SID.ADC.4	Gain Error	Gain error	–1.5	–	1.5	LSB	–
SID.ADC.5	VREF_ADC1	Reference voltage of ADC	V_{DDmin}	–	V_{DDmax}	V	Reference voltage generated from V_{DD}
SID.ADC.6	VREF_ADC2	Reference voltage of ADC	1.96	2.0	2.04	V	Reference voltage generate from bandgap

Charger Detect
Table 28. Charger Detect Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC.CHGDET.1	V _{DAT_REF}	Data detect voltage in charger detect mode	250	–	400	mV	–
DC.CHGDET.2	V _{DM_SRC}	Dn voltage source in charger detect mode	500	–	700	mV	–
DC.CHGDET.3	V _{DP_SRC}	Dp voltage source in charger detect mode	500	–	700	mV	–
DC.CHGDET.4	I _{DM_SINK}	Dn sink current in charger detect mode	25	–	175	μA	–
DC.CHGDET.5	I _{DP_SINK}	Dp sink current in charger detect mode	25	–	175	μA	–
DC.CHGDET.6	I _{DP_SRC}	Data contact detect current source	7	–	13	μA	–
DC.CHGDET.27	R _{DP_UP}	Qualcomm pull-up termination on Dp/Dn	0.9	–	1.575	kΩ	–
DC.CHGDET.32	R _{DM_UP}	Dp/Dn pull-up resistance	0.9	–	1.575	kΩ	–
DC.CHGDET.28	R _{DP_DWN}	Qualcomm pull-down termination on Dp/Dn	14.25	–	24.8	kΩ	–
DC.CHGDET.31	R _{DM_DWN}	Dp/Dn pull-down resistance	14.25	–	24.8	kΩ	–
DC.CHGDET.29	R _{DAT_LKG}	Data line leakage on Dp/Dn	300	–	500	kΩ	–
DC.CHGDET.34	V _{SETH}	Logic Threshold	1.26	–	1.54	V	–

Table 29. V_{BUS} Regulator AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.AC.20VREG.1	T _{START}	Total start up time for the regulator supply outputs	–	–	120	μs	Apply V _{BUS} and measure start time on V _{DDD} pin.
SID.AC.20VREG.2	T _{STOP}	Regulator power down time from vreg_en = 0 to regulator disable	–	–	1	μs	Time from assertion of an internal disable signal to for load current on V _{DDD} to decrease from 30 mA to 10 μA.

Table 30. V_{sys} Switch Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.VDDDSW.1	Res _{sw}	Resistance from supply input to output supply V _{DDD}	–	–	1.5	Ω	Measured with a load current of 5 mA to 10 mA on V _{DDD} .

Table 31. CSA DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.CSA.21	Out_E_Trim_15_DS	Cumulative output Error for $A_v = 15$, after trim, using Deep sleep (beta-multiplier) reference	-7	-	7	%	-
SID.DC.CSA.22	Out_E_Trim_15_BG	Cumulative output Error for $A_v = 15$, after trim, using bandgap reference	-4.5	-	4.5	%	-
SID.DC.CSA.23	Out_E_Trim_100_DS	Cumulative output Error for $A_v = 100$, after trim, using Deep sleep (beta-multiplier) reference	-24.5	-	24.5	%	-

Table 32. UV/OV Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.UVOV.1	$V_{THUVOV1}$	Voltage threshold accuracy in active mode using bandgap reference	-	± 3	-	%	-
SID.UVOV.2	$V_{THUVOV2}$	Voltage threshold accuracy in Deep Sleep mode using Deep Sleep reference	-	± 5	-	%	-
SID.COMP_ACC	COMP_ACC	Comparator input offset at 4s	-15	-	15	mV	-

Table 33. PFET Gate Driver DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.PGDO.1	R_{pd}	Resistance when "pull_dn" enabled	-	-	5	k Ω	-

Table 34. PFET Gate Driver AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.AC.PGDO.2	$T_{r_discharge}$	Discharge Rate of output node	-	-	5	V/ μ s	Guaranteed by design

SBU
Table 35. SBU Switch DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.20sbu.1	Ron1	On resistances for Aux switch at 3.3 V input	–	4	7	Ω	–
SID.DC.20sbu.2	Ron2	On resistances for Aux switch at 1 V input	–	3	5	Ω	–
SID.DC.20sbu.4	Ileak1	Pin leakage current for SBU1, SBU2	–4.5	–	4.5	μA	–
SID.DC.20sbu.5	Ileak2	Pin leakage current for LSTX, LSRX, AUX_P, AUX_N	–1	–	1	μA	–
SID.DC.20sbu.6	Rpu_aux_1	Pull-up resistance on AUX_P/N	80	–	320	KΩ	–
SID.DC.20sbu.7	Rpu_aux_2	Pull-up resistance on AUX_P/N	0.8	–	1.4	MΩ	–
SID.DC.20sbu.8	Rpd_aux_1	Pull-down resistance on AUX_P/N	80	–	120	KΩ	–
SID.DC.20sbu.9	Rpd_aux_2	Pull-down resistance on AUX_P/N	0.3	–	1.2	MΩ	–
SID.DC.20sbu.10	Rpd_aux_3	Pull-down resistance on AUX_P/N	250	–	611	KΩ	–
SID.DC.20sbu.11	Rpd_aux_4	Pull-down resistance on AUX_P/N	0.3	–	6.11	MΩ	–
SID.DC.20sbu.16	OVP_threshold	Over-voltage protection detection threshold above V _{DDIO}	200	–	1200	mV	–
SID.DC.20sbu.17	lsx_ron_3p3	On resistances of LSTX/LSRX to SBU1/2 switch at 3.3 V input	–	8.5	17	Ω	–
SID.DC.20sbu.18	lsx_ron_1	On resistances of LSTX/LSRX to SBU1/2 switch at 1 V input	–	5.5	11	Ω	–
SID.DC.20sbu.19	aux_ron_flat_fs	Switch On flat resistances of AUX_P/N to SBU1/2 switch (from 0 to 3.3 V)	–	–	2.5	Ω	Guaranteed by design
SID.DC.20sbu.20	aux_ron_flat_hs	Switch On flat resistances of AUX_P/N to SBU1/2 switch (from 0 to 1 V)	–	–	0.5	Ω	Guaranteed by design
SID.DC.20sbu.21	lsx_ron_flat_fs	Switch On flat resistances of LSTX/LSRX to SBU1/2 switch (from 0 to 3.3 V)	–	–	5	Ω	Guaranteed by design
SID.DC.20sbu.22	lsx_ron_flat_hs	Switch On flat resistances of LSTX/LSRX to SBU1/2 switch (from 0 to 1 V)	–	–	0.5	Ω	Guaranteed by design

Table 36. SBU Switch AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.AC.20sbu.1	Con	Switch ON capacitance	–	–	120	pF	–
SID.AC.20sbu.2	Coff	Switch OFF capacitance - Connector side	–	–	80	pF	–
SID.AC.20sbu.3	Off_isolation	Switch isolation at F = 1 MHz	–50	–	–	dB	–
SID.AC.20sbu.4	T _{ON}	SBU Switch turn-on time	–	–	200	μs	–
SID.AC.20sbu.5	T _{OFF}	SBU Switch turn-off time	–	–	400	μs	Guaranteed by design
SID.AC.20sbu.6	Off_isolation_tran	Coupling on sbu1,2 terminated to 50 ohm, switch-OFF, Rail-to-rail toggling on LSTX/LSRX	–60	–	60	mV	Guaranteed by design
SID.AC.20sbu.7	X_talk_AC	Cross talk of Switch at F=1 MHz SBU1/2 to SBU2/1	–50	–	–	dB	Guaranteed by design
SID.AC.20sbu.8	X_talk_tran	Check voltage coupling on SBU2(1) when Data is transferred from LSTX (RX) to SBU1 (2)	–70	–	70	mV	Guaranteed by design

Table 37. DP/DM Switch DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.dpdm.1	Ron_HS	DPDM On resistance for SYS lines (0 to 0.5 V) - HS mode	–	–	8	Ω	–
SID.DC.dpdm.2	Ron_FS	DPDM On resistance for SYS lines (0 to 3.3 V) - FS mode	–	–	12	Ω	–
SID.DC.dpdm.5	Con_FS	Switch On capacitance at FS at 6 MHz	–	–	50	pF	Guaranteed by design
SID.DC.dpdm.6	Con_HS	Switch on capacitance at HS at 240 MHz	–	–	10	pF	–
SID.DC.dpdm.9	Ileak_pin	pin leakage at DP/DM connector side and host side	–	–	1	μA	–
SID.DC.dpdm.10	RON_UART	DPDM On resistance for UART lines (0 to 3.3 V)	–	–	17	Ω	–
SID.DC.dpdm.11	RON_FLAT_HS	DPDM On Flat resistance in HS mode (0 to 0.4 V)	–	–	0.5	Ω	Guaranteed by design
SID.DC.dpdm.12	RON_FLAT_FS	DPDM On flat resistance in FS mode (0 to 3.3 V)	–	–	4	Ω	Guaranteed by design
SID.DC.dpdm.13	RON_FLAT_UART	DPDM UART On flat resistance (0 to 3.3 V)	–	–	4	Ω	Guaranteed by design

Table 38. DP/DM Switch AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.AC.dpdm.5	T _{ON}	DP/DM Switch turn-on time	–	–	200	μs	–
SID.AC.dpdm.6	T _{OFF}	DP/DM Switch turn-off time	–	–	0.4	μs	Guaranteed by design
SID.AC.dpdm.7	T _{ON_VPUMP}	DP/DM charge pump startup time	–	–	200	μs	Guaranteed by characterization
SID.AC.dpdm.8	Off_isolation_HS	Switch-off isolation for HS	–20	–	–	db	Guaranteed by design
SID.AC.dpdm.9	Off_isolation_FS	Switch-off isolation for FS	–50	–	–	db	Guaranteed by design
SID.AC.dpdm.10	X _{talk}	Cross talk of Switch From FS to HS at F = 12 MHz	–50	–	–	db	Guaranteed by design
SID.AC.dpdm.11	uart_coupling	peak to peak coupling of UART signal to DP lines. (UART swinging from 0 to 3.3 V)	–	–	20	mV	Guaranteed by design

Table 39. VCONN Switch DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.20VCONN.1	R _{on}	Switch ON resistance at V _{5V} = 5 V with 215-mA load current	–	1.4	2	Ω	–
SID.DC.20VCONN.9	I _{OC} P	Overcurrent detection range for CC1/CC2	400	–	600	mA	–
SID.DC.20VCONN.10	OVP_threshold	Overvoltage protection detection threshold above V _{DD} or V _{5V} whichever is higher	200	–	1200	mV	–
SID.DC.20VCONN.11	OVP_hysteresis	Overvoltage protection detection hysteresis	50	–	200	mV	Guaranteed by design
SID.DC.20VCONN.12	OCP_hysteresis	Overcurrent detection hysteresis	20	–	60	mA	–
SID.DC.20vconn.14	OVP_thresh-old_on	Overvoltage protection detection threshold above V _{5V} of CC1/2, with CC1 or CC2 switch enabled. Same threshold triggers reverse current protection circuit	200	–	700	mV	–

Table 40. VCONN Switch AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.AC.20VCONN.1	T _{ON}	VCONN switch turn-on time	–	–	200	μs	–
SID.AC.20VCONN.2	T _{OFF}	VCONN switch turn-off time	–	–	3	μs	Guaranteed by design

Table 41. V_{BUS} Discharge Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.VBUS.DISC.1	R _{on1}	20-V NMOS ON resistance	1500	–	3000	Ω	–
SID.VBUS.DISC.2	R _{on2}	20-V NMOS ON resistance	750	–	1500	Ω	–
SID.VBUS.DISC.3	R _{on3}	20-V NMOS ON resistance	500	–	1000	Ω	–
SID.VBUS.DISC.4	R _{on4}	20-V NMOS ON resistance	375	–	750	Ω	–
SID.VBUS.DISC.5	R _{on5}	20-V NMOS ON resistance	300	–	600	Ω	–

Ordering Information

Table 42 lists the EZ-PD CCG5 part numbers and features.

Table 42. EZ-PD CCG5 Ordering Information

Part Number	Application	Type-C Ports	Dead Battery Termination	Termination Resistor	Role	Package
CYPD5125-40LQXIT	Notebooks, Desktops	1	Yes	$R_p^{[5]}$, $R_D^{[6]}$, $R_{D-DB}^{[7]}$	DRP	40-pin QFN
CYPD5135-40LQXIT	Dock	1	No	$R_p^{[5]}$, $R_D^{[6]}$	DRP	40-pin QFN
CYPD5225-96BZXI	Notebooks, Desktops	2	Yes	$R_p^{[5]}$, $R_D^{[6]}$, $R_{D-DB}^{[7]}$	DRP	96-ball BGA
CYPD5225-96BZXIT						
CYPD5235-96BZXI	Dock, Upstream port	2	No	$R_p^{[5]}$, $R_D^{[6]}$	DRP	96-ball BGA
CYPD5235-96BZXIT						
CYPD5236-96BZXI	Dock, Downstream port	2	No	$R_p^{[5]}$, $R_D^{[6]}$	DRP	96-ball BGA
CYPD5236-96BZXIT						

Ordering Code Definitions



Notes

5. Termination resistor denoting a downstream facing port.
6. Termination resistor denoting an accessory or upstream facing port.
7. Termination resistor denoting dead-battery termination.

Packaging

Table 43. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T _A	Operating ambient temperature	Industrial	-40	25	85	°C
T _J	Operating junction temperature	Industrial	-40	25	100	°C
T _{JA}	Package θ _{JA} (96-ball BGA)	-	-	-	56	°C/W
T _{JC}	Package θ _{JC} (96-ball BGA)	-	-	-	18.5	°C/W
T _{JA}	Package θ _{JA} (40-pin QFN)	-	-	-	19.3	°C/W
T _{JC}	Package θ _{JC} (40-pin QFN)	-	-	-	13.6	°C/W

Table 44. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5 °C of Peak Temperature
96-ball BGA	260 °C	30 seconds
40-pin QFN	260 °C	30 seconds

Table 45. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
96-ball BGA	MSL 3
40-pin QFN	MSL 3

Figure 12. 40-Pin QFN (6 × 6 × 0.6 mm), LR40A/LQ40A 4.6 × 4.6 E-PAD (Sawn) Package Outline, 001-80659

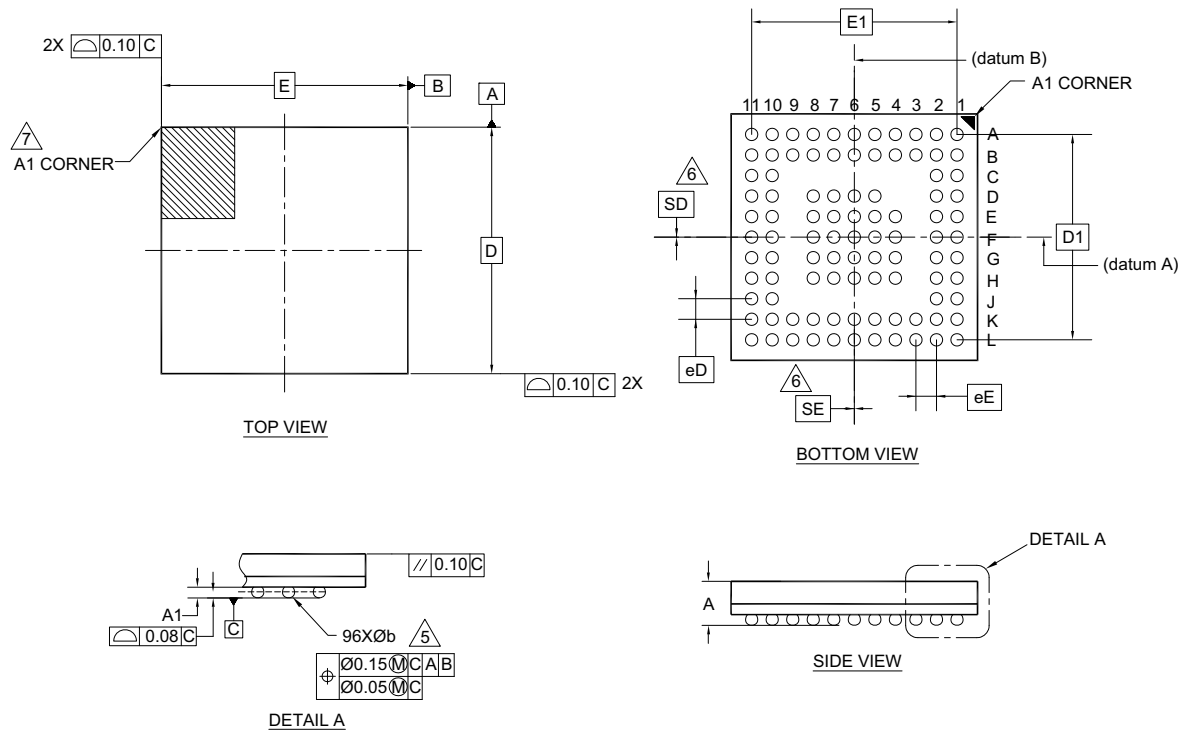


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ± 2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

Figure 13. 96-Ball BGA (6 × 6 × 1.0 mm), Package Outline, 002-10631



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
D	6.00 BSC		
E	6.00 BSC		
D1	5.00 BSC		
E1	5.00 BSC		
MD	11		
ME	11		
N	96		
∅ b	0.25	0.30	0.35
eD	0.50 BSC		
eE	0.50 BSC		
SD	0.00		
SE	0.00		

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
- JEDEC SPECIFICATION NO. REF. : MO-225. 002-10631 *A

Acronyms

Table 46. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
CC	configuration channel
BOD	Brown out Detect
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I ² C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LVD	low-voltage detect
LVTTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller

Table 46. Acronyms Used in this Document (continued)

Acronym	Description
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I ² C serial clock
SDA	I ² C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USBIO	USB input/output, CCG5 pins used to connect to a USB port
XRES	external reset I/O pin

Document Conventions

Units of Measure

Table 47. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μs	microsecond
μV	microvolt

Table 47. Units of Measure (continued)

Symbol	Unit of Measure
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

References and Links To Applications Collaterals

Knowledge Base Articles

- [Key Differences Among EZ-PD™ CCG1, CCG2, CCG3 and CCG5 - KBA210740](#)
- [Programming EZ-PD™ CCG2, EZ-PD™ CCG3 and EZ-PD™ CCG5 Using PSoC® Programmer and MiniProg3 - KBA96477](#)
- [CCGX Frequently Asked Questions \(FAQs\) - KBA97244](#)
- [Handling Precautions for CY4501 CCG1 DVK - KBA210560](#)
- [Cypress EZ-PD™ CCGx Hardware - KBA204102](#)
- [Difference between USB Type-C and USB-PD - KBA204033](#)
- [CCGX Programming Methods - KBA97271](#)
- [Getting started with Cypress USB Type-C Products - KBA04071](#)
- [Type-C to DisplayPort Cable Electrical Requirements](#)
- [Dead Battery Charging Implementation in USB Type-C Solutions - KBA97273](#)
- [Termination Resistors Required for the USB Type-C Connector – KBA97180](#)
- [VBUS Bypass Capacitor Recommendation for Type-C Cable and Type-C to Legacy Cable/Adapter Assemblies – KBA97270](#)
- [Need for Regulator and Auxiliary Switch in Type-C to DisplayPort \(DP\) Cable Solution - KBA97274](#)
- [Need for a USB Billboard Device in Type-C Solutions – KBA97146](#)
- [CCG1 Devices in Type-C to Legacy Cable/Adapter Assemblies – KBA97145](#)
- [Cypress USB Type-C Controller Supported Solutions – KBA97179](#)
- [Termination Resistors for Type-C to Legacy Ports – KBA97272](#)
- [Handling Instructions for CY4502 CCG2 Development Kit – KBA97916](#)
- [Thunderbolt™ Cable Application Using CCG3 Devices - KBA210976](#)
- [Power Adapter Application Using CCG3 Devices - KBA210975](#)
- [Methods to Upgrade Firmware on CCG3 Devices - KBA210974](#)
- [Device Flash Memory Size and Advantages - KBA210973](#)
- [Applications of EZ-PD™ CCG5 - KBA210739](#)

Application Notes

- [AN96527 - Designing USB Type-C Products Using Cypress's CCG1 Controllers](#)
- [AN95615 - Designing USB 3.1 Type-C Cables Using EZ-PD™ CCG2](#)

- [AN95599 - Hardware Design Guidelines for EZ-PD™ CCG2](#)
- [AN210403 - Hardware Design Guidelines for Dual Role Port Applications Using EZ-PD™ USB Type-C Controllers](#)
- [AN210771 - Getting Started with EZ-PD™ CCG5](#)

Reference Designs

- [EZ-PD™ CCG2 Electronically Marked Cable Assembly \(EMCA\) Paddle Card Reference Design](#)
- [EZ-PD™ CCG2 USB Type-C to DisplayPort Cable Solution](#)
- [CCG1 USB Type-C to DisplayPort Cable Solution](#)
- [CCG1 USB Type-C to HDMI/DVI/VGA Adapter Solution](#)
- [EZ-PD™ CCG2 USB Type-C to HDMI Adapter Solution](#)
- [CCG1 Electronically Marked Cable Assembly \(EMCA\) Paddle Card Reference Design](#)
- [CCG1 USB Type-C to Legacy USB Device Cable Paddle Card Reference Schematics](#)
- [EZ-USB GX3 USB Type-C to Gigabit Ethernet Dongle](#)
- [EZ-PD™ CCG2 USB Type-C Monitor/Dock Solution](#)
- [CCG2 20W Power Adapter Reference Design](#)
- [CCG2 18W Power Adapter Reference Design](#)
- [EZ-USB GX3 USB Type-A to Gigabit Ethernet Reference Design Kit](#)

Kits

- [CY4501 CCG1 Development Kit](#)
- [CY4502 EZ-PD™ CCG2 Development Kit](#)
- [CY4531 EZ-PD CCG3 Evaluation Kit](#)
- [CY4541 EZ-PD™ CCG5 Evaluation Kit](#)

Datasheets

- [CCG1 Datasheet: USB Type-C Port Controller with Power Delivery](#)
- [CYPD1120 Datasheet: USB Power Delivery Alternate Mode Controller on Type-C](#)
- [CCG2: USB Type-C Port Controller Datasheet](#)
- [CCG3: USB Type-C Controller Datasheet](#)

Document History Page

Document Title: EZ-PD™ CCG5, USB Type-C Port Controller				
Document Number: 002-17682				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5528106	SOBI	12/07/2016	New datasheet
*A	5606273	SOBI	01/27/2017	Updated EZ-PD™ CCG5, USB Type-C Port Controller and Features. Updated Logic Block Diagram. Updated USB-PD Subsystem (SS) and reordered the Functional Overview section. Updated GPIO. Updated 40-Pin QFN Pin Map (Top View) for CYPD5125-40LQXIT.
*B	5694572	SOBI	06/03/2017	Changed datasheet status to Preliminary. Added Errata. Added Table 4 through Table 7. Added Table 9 through Table 41 in Device-Level Specifications. Updated Logic Block Diagram, GPIO, and VBUS Discharge. Updated Table 2, Table 3, Table 8, and Table 46. Updated Figure 5 through Figure 9. Updated Figure 13 (spec 002-10631 Rev. ** to *A) in Packaging. Updated compliance with USB spec in Sales, Solutions, and Legal Information. Updated template.
*C	5885413	VGT	09/27/2017	Updated USB HS Mux and SBU Mux in Functional Overview. Updated Flash in CPU and Memory Subsystem. Updated Power System Overview. Updated description of BGA pin P2.4 to support SCB4 I2C data. Changed SID.PWR#1_A; VDDD from 3 V to 3.15 V for DFP application. Changed SID.AC.dpdm.3; Trise_HS from 630 ps max to 300 ps min. Changed SID.AC.dpdm.4, Tfall_HS from 630 ps max to 300 ps min. Updated SID.PWR#23 - changed V _{SYS} to V _{SYS_UEP} and changed range to 2.7 to 5.5 V. Added SID.PWR#23_A for DFP/DRP application. Changed max value for SID.20VREG.8, V _{BUSLOADREG} , from 0.2 to 0.3. Updated SID.ADC.2, SID.ADC.4 to ±1.5. Updated SID.PWR#18 description to extend to SBU, DPDM mux pins. Updated SID.PWR#2 - changed V _{DDD_MAX} to V _{SYS_MAX} . Removed min value from SID.PWR#14, VDDIO_MAX. Added min spec of -25mA for SID.PWR#19, I _{gpio_abs} . Removed ADC.AC spec. Updated SID.DC.20vconn.11, OVP_hysteresis max. Added SID.DC.20vconn.14, OVP_threshold_on. Added SID.AC.dpdm.10, SID.AC.dpdm.11. Changed min value of SID.AC.dpdm.1, BW_3dB_HS from 1000 to 700. Changed max value of SID.DC.dpdm.12, SID.DC.dpdm.13 from 4 to 3. Changed max value of SID.DC.dpdm.2, RON_FS to 12. Corrected values for SID.AC.dpdm.8, SID.AC.dpdm.9. Added SID.AC.20sbu.6, SID.AC.20sbu.8, and SID.AC.20sbu.8.

Document Title: EZ-PD™ CCG5, USB Type-C Port Controller				
Document Number: 002-17682				
*C (contd.)	5885413	VGT	09/27/2017	<p>Updated SID.DC.20sbu.12, SID.DC.20sbu.15, SID.DC.20sbu.6, SID.DC.20sbu.7, SID.DC.20sbu.7A, SID.DC.20sbu.8, SID.DC.20sbu.9, SID.DC.20sbu.10, SID.DC.20sbu.11, SID.DC.20sbu.3, and SID.DC.20sbu.3. Changed SBU pins ESD voltage to 750 V.</p> <p>Added new Table 28, new Table 29, Table 43 through Table 45.</p> <p>Updated Figure 5, Figure 8, Figure 9.</p> <p>Added Figure 7.</p> <p>Removed ADC AC specifications and CSAAC specifications (Table 28 and Table 32 from previous revision).</p> <p>Removed Errata.</p>
*D	5943992	VGT	10/24/2017	<p>Added "Thunderbolt hosts and devices" in Applications.</p> <p>Updated Figure 1 to correctly depict "2 x ADC" for entire CCG5.</p> <p>Updated description of VDDD pin in Table 2 and Table 3.</p> <p>Updated the description for pin P2.4 in Table 3.</p> <p>Added "CYPD5235-96BZXI" and "CYPD5236-96BZXI" part numbers to the description of Table 3 and Figure 6.</p> <p>Updated $V_{BUS_P1_MAX}$ and $V_{BUS_P2_MAX}$ values to 24 in Table 8.</p> <p>Updated min value of ESD_HBM_SBU spec from 750 to 1100 V in Table 8.</p> <p>Added "Applicable for all pins except SBU pins" in description of "ESD_HBM" parameter in Table 8.</p> <p>Updated description of $V_{GPIO_OVT_ABS}$ in Table 8.</p> <p>Updated description of ESD_IEC_CON and ESD_IEC_AIR parameters in Table 8.</p> <p>Changed SID.PWR#13 min value from 1.7 to V_{DD} in Table 9.</p> <p>Updated min value of SID.PWR#23 to 2.75 in Table 9.</p> <p>Updated pin description, values, and details/conditions of parameters SID.PWR#1 and SID.PWR#1_A to better define V_{DD} supply in Table 9.</p> <p>Replace V_{DD} with V_{SYS} in supply name and conditions for IDD parameters listed in Table 9.</p> <p>Updated Conditions for SID.CLK#4 to "All V_{DD}" in Table 10.</p> <p>Removed SID.PWR#20 in Table 10.</p> <p>Added Guaranteed by Design for SID178 and SID180 in Table 20.</p> <p>Added description for SID.MEM#8 in Table 20.</p> <p>Added description for SID.CLK#13 and SID.CLK#13A in Table 24.</p> <p>Added Guaranteed by Design for SID.DC.cc_shvt.4 in Table 26.</p> <p>Deleted details and conditions for SID.DC.cc_shvt.14 in Table 26.</p> <p>Removed SID.DC.cc_SHVT.19 in Table 26.</p> <p>Updated spec values in Table 32.</p> <p>Added Guaranteed by Design for SID.AC.PGDO.2 in Table 34.</p> <p>Added Guaranteed by Design for SID.DC.20sbu.19 through SID.DC.20sbu.22 and removed SID.AC.20sbu.3 in Table 35.</p> <p>Added Guaranteed by Design for SID.AC.20SBU.5 in Table 36.</p> <p>Updated max value for SID.AC.20SBU.8 in Table 36.</p> <p>Removed SID.DC.dpdm.3 and SID.DC.dpdm.4 and added Guaranteed by Design for SID.DC.dpdm.5 and SID.DC.dpdm.11 through SID.DC.dpdm.13 in Table 37.</p> <p>Updated SID.DC.dpdm.12 and SID.DC.dpdm.13 max value in Table 37.</p> <p>Removed SID.AC.dpdm.1, SID.AC.dpdm.2, SID.AC.dpdm.3, and SID.AC.dpdm.4 in Table 38.</p>

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*D (contd.)	5943992	VGT	10/24/2017	Added Guaranteed by Design for SID.AC.dpdm.6, SID.AC.dpdm.7, SID.AC.dpdm.8, SID.AC.dpdm.9, SID.AC.dpdm.10, and SID.AC.dpdm.13 in Table 38 . Added Guaranteed by Design for SID.DC.20VCONN.11 in Table 39 . Removed SID.DC.20VCONN.13 in Table 39 . Added Guaranteed by Design for SID.AC.20VCONN.2 in Table 40 . Updated min value of V_{SYS} to 2.75 throughout the document.
*E	5968629	VGT	11/16/2017	Updated Figure 8 . Added Figure 10 and Figure 11 and associated content.
*F	6040630	HPV	02/16/2018	Removed VBUS Regulator DC Specifications.
*G	6111610	VGT/AKK	03/27/2018	Updated pin name and description of P2.4 pin in Table 3 . Updated Power System Overview . Updated pin name of pin K5 in Figure 6 . Updated application diagrams in Figure 8 , Figure 10 , and Figure 11 . Added SID.PWR#5. Added MPN CYPD5135-40LQXIT in Table 42 .
*H	6206852	VGT	06/13/2018	Added MPNs CYPD5225-96BZXIT, CYPD5235-96BZXIT and CYPD5236-96BZXIT in Table 42 .

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Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А