



BUK6D120-40E

40 V, N-channel Trench MOSFET

29 April 2019

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Extended temperature range $T_j = 175^\circ\text{C}$
- Side wettable flanks for optical solder inspection
- ElectroStatic Discharge (ESD) protection > 1 kV HBM (class H1C)
- Trench MOSFET technology
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

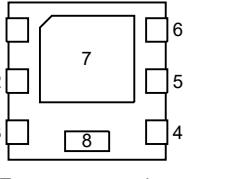
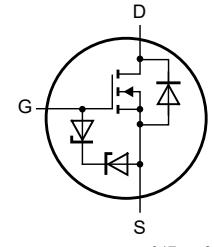
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25^\circ\text{C}$	-	-	40	40	V
V_{GS}	gate-source voltage		-20	-	20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{sp} = 25^\circ\text{C}$	-	-	5.7	5.7	A
P_{tot}	total power dissipation	$T_{sp} = 25^\circ\text{C}$	-	-	7.5	7.5	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 2.9\text{ A}; T_j = 25^\circ\text{C}$	-	85	120	120	$\text{m}\Omega$

nexperia

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 Transparent top view DFN2020MD-6 (SOT1220)	 017aaa255
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK6D120-40E	DFN2020MD-6	plastic, leadless thermal enhanced ultra thin small outline package; 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body	SOT1220

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK6D120-40E	5F

8. Limiting values

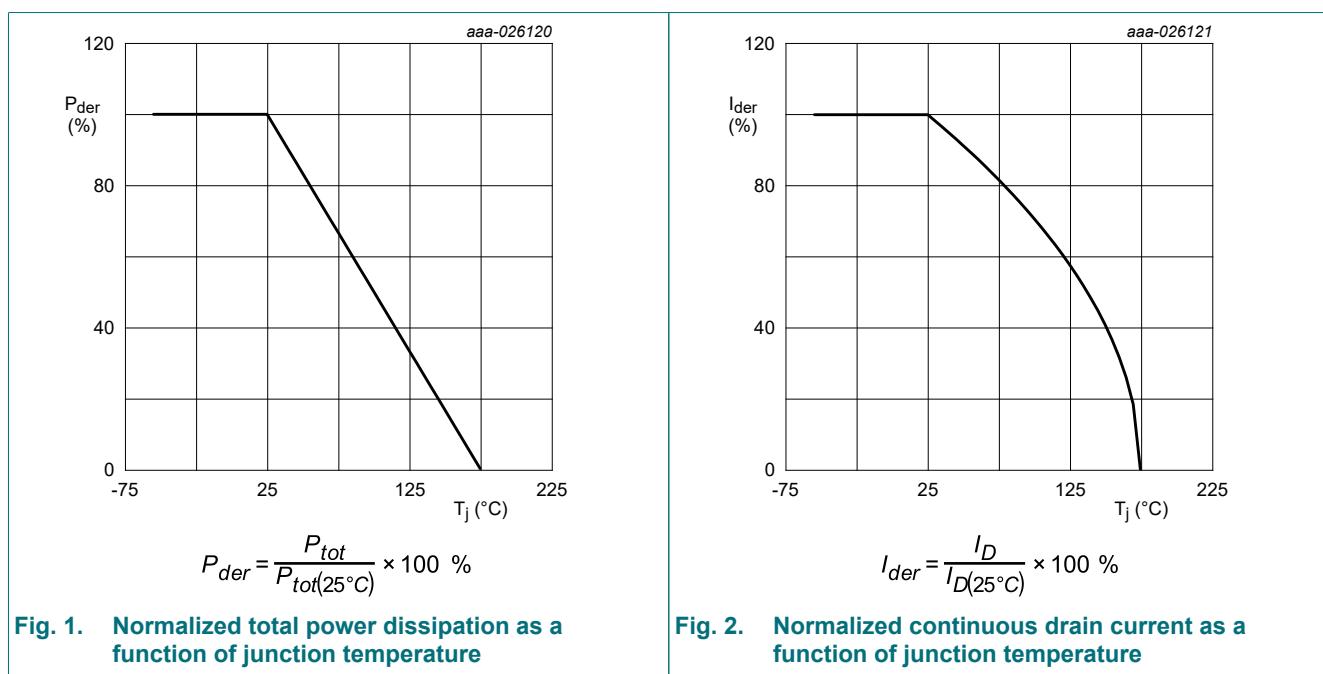
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25^\circ\text{C}$		-	40	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{sp} = 25^\circ\text{C}$		-	5.7	A
		$V_{GS} = 10\text{ V}; T_{sp} = 100^\circ\text{C}$		-	3.6	A
		$V_{GS} = 10\text{ V}; T_{amb} = 25^\circ\text{C}$	[1]	-	2.9	A
I_{DM}	peak drain current	$T_{sp} = 25^\circ\text{C}$; single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	23	A
P_{tot}	total power dissipation	$T_{sp} = 25^\circ\text{C}$		-	7.5	W
		$T_{amb} = 25^\circ\text{C}$	[1]	-	2	W
T_j	junction temperature			-55	175	$^\circ\text{C}$
T_{amb}	ambient temperature			-55	175	$^\circ\text{C}$
T_{stg}	storage temperature			-65	175	$^\circ\text{C}$
Source-drain diode						
I_S	source current	$T_{sp} = 25^\circ\text{C}$		-	5.7	A
		$T_{amb} = 25^\circ\text{C}$	[1]	-	2	A
I_{SM}	peak source current	single pulse; $t_p \leq 10\text{ }\mu\text{s}; T_{sp} = 25^\circ\text{C}$		-	23	A
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[2]	-	1000	V
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(\text{init})} = 25^\circ\text{C}; I_D = 0.26\text{ A}$; DUT in avalanche (unclamped)		-	5.8	mJ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm^2 .

[2] Measured between all pins.



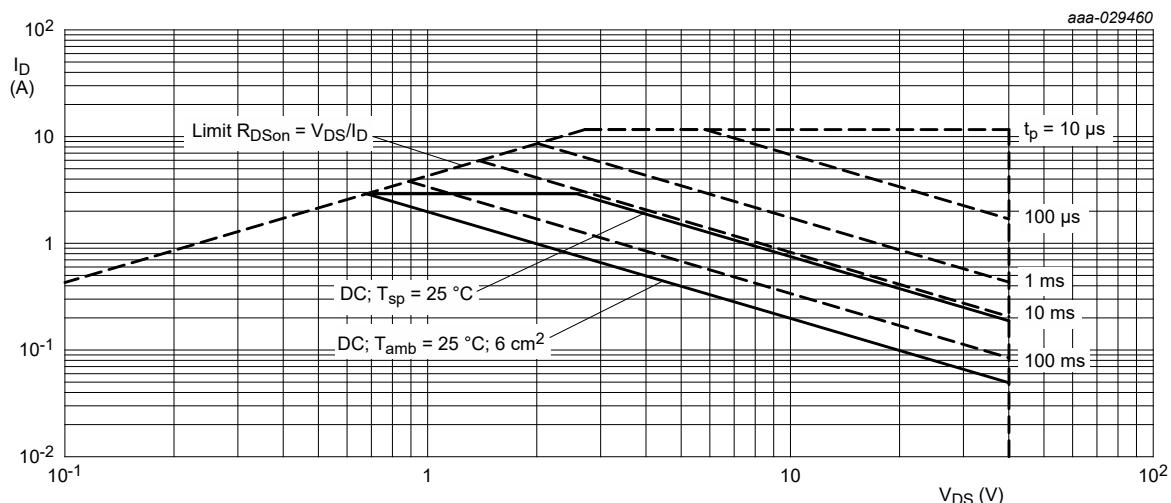


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	66	76	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	15	20	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

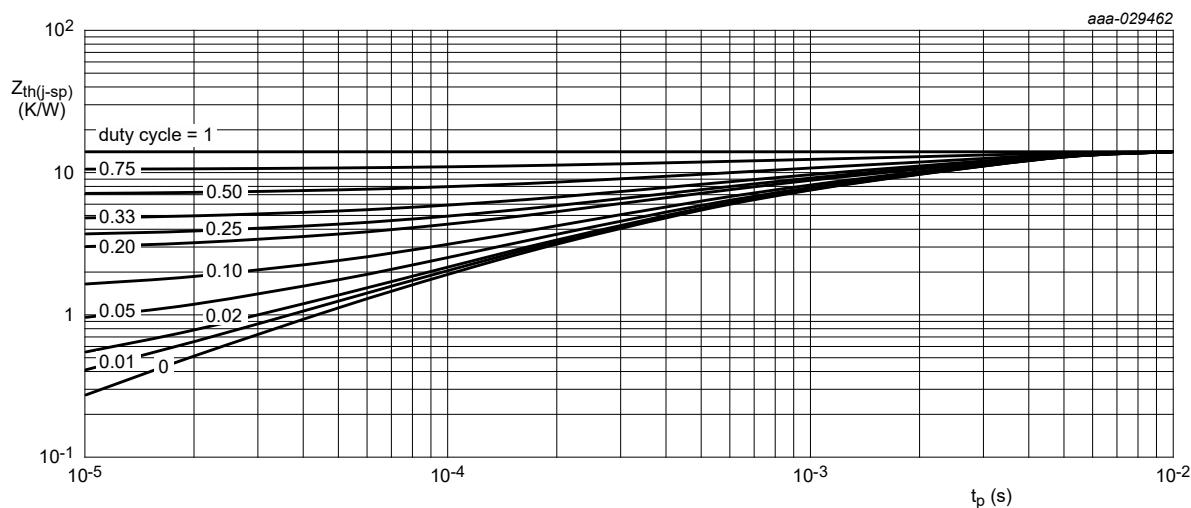
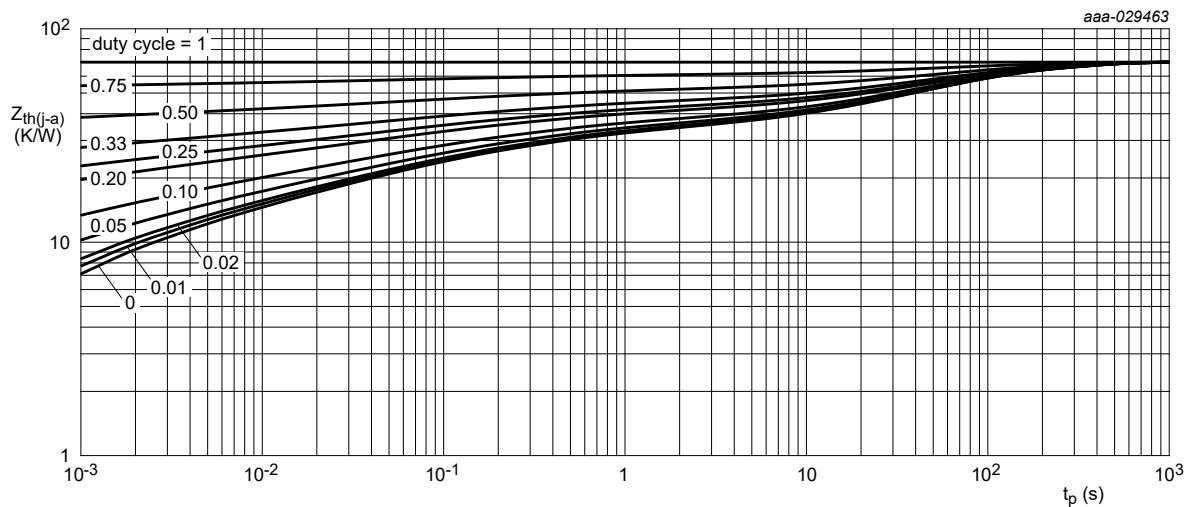


Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration; typical values



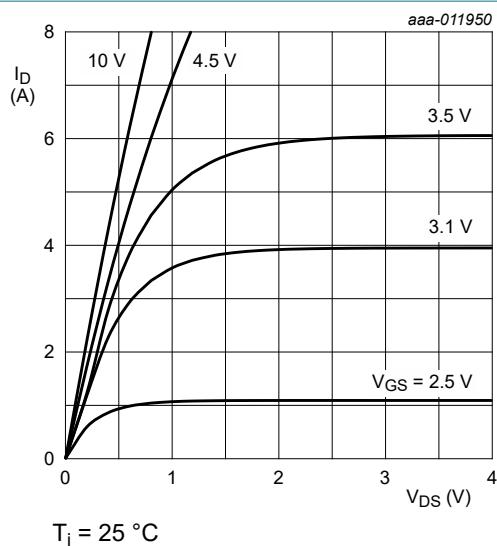
FR4 PCB, mounting pad for drain 6 cm²

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

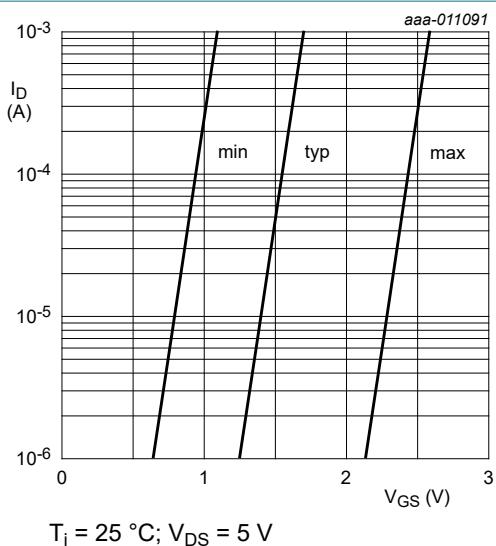
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$		40	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25^\circ C$		1	1.6	2.5	V
I_{DSS}	drain leakage current	$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25^\circ C$		-	-	1	μA
		$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 125^\circ C$		-	-	4	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	10	μA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	-10	μA
		$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	1	μA
		$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	-1	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 2.9 A; T_j = 25^\circ C$		-	85	120	$m\Omega$
		$V_{GS} = 10 V; I_D = 2.9 A; T_j = 175^\circ C$		-	165	233	$m\Omega$
		$V_{GS} = 4.5 V; I_D = 2.5 A; T_j = 25^\circ C$		-	112	160	$m\Omega$
g_{fs}	forward transconductance	$V_{DS} = 10 V; I_D = 2 A; T_j = 25^\circ C$		-	4.5	-	S
R_G	gate resistance	$f = 1 \text{ MHz}$		-	28	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$V_{DS} = 20 V; I_D = 2.9 A; V_{GS} = 10 V; T_j = 25^\circ C$		-	2.4	3.6	nC
Q_{GS}	gate-source charge			-	0.3	-	nC
Q_{GD}	gate-drain charge			-	0.4	-	nC
C_{iss}	input capacitance	$V_{DS} = 20 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25^\circ C$		-	113	-	pF
C_{oss}	output capacitance			-	27	-	pF
C_{rss}	reverse transfer capacitance			-	14	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20 V; I_D = 2.9 A; V_{GS} = 10 V; R_{G(ext)} = 6 \Omega; T_j = 25^\circ C$		-	6	-	ns
t_r	rise time			-	8	-	ns
$t_{d(off)}$	turn-off delay time			-	11	-	ns
t_f	fall time			-	3	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 2 A; V_{GS} = 0 V; T_j = 25^\circ C$		-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 1 A; dI_S/dt = -100 A/\mu s; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25^\circ C$		-	7.2	-	ns
Q_r	recovered charge			-	3	-	nC



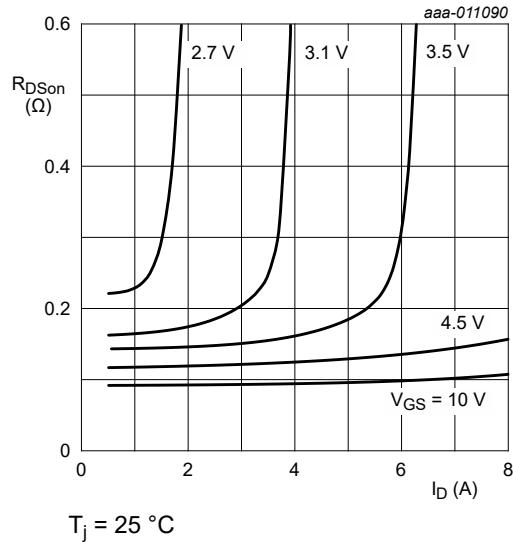
$T_j = 25^\circ\text{C}$

Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values



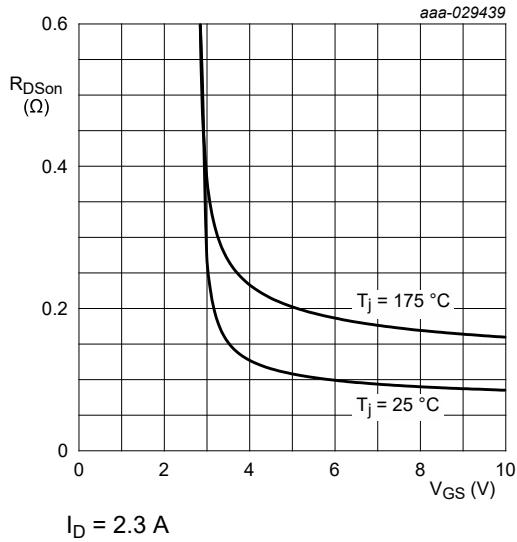
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{ V}$

Fig. 7. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25^\circ\text{C}$

Fig. 8. Drain-source on-state resistance as a function of drain current; typical values



$I_D = 2.3\text{ A}$

Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

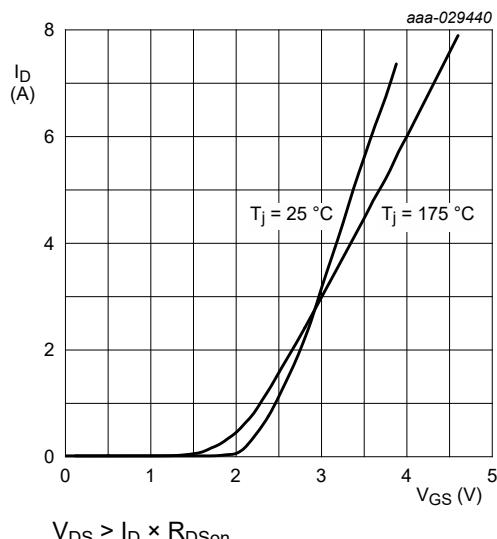


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

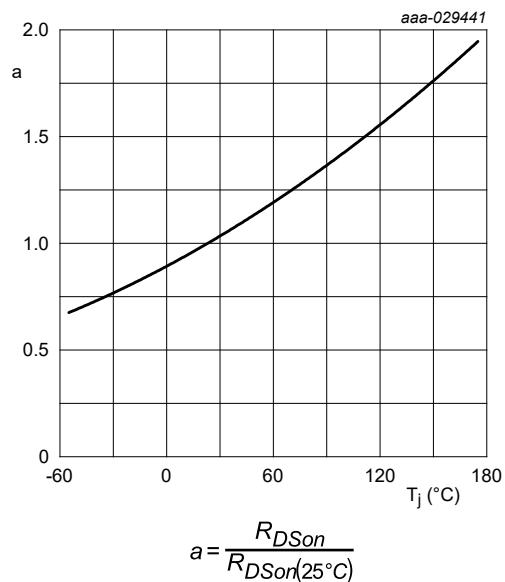


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

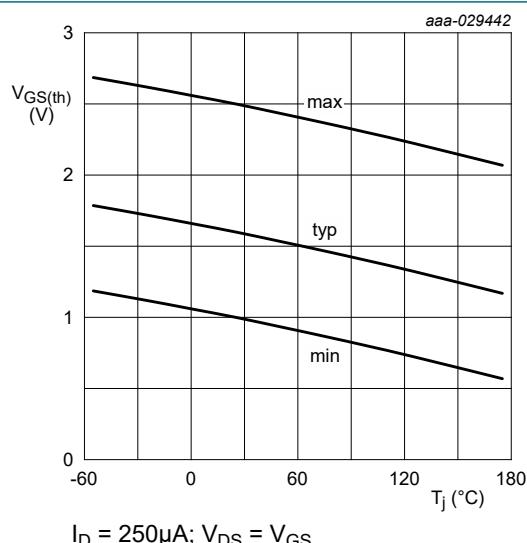


Fig. 12. Gate-source threshold voltage as a function of junction temperature

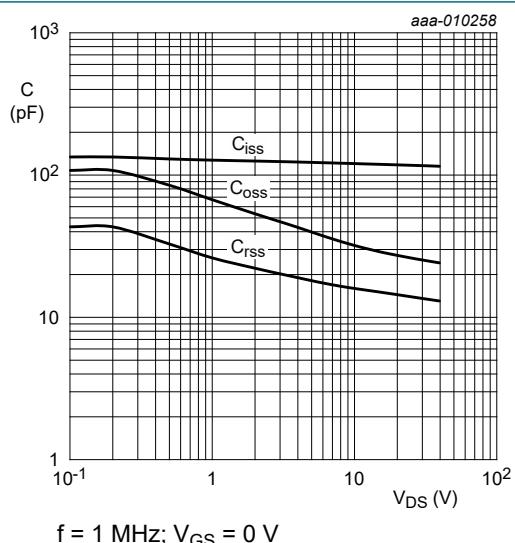


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

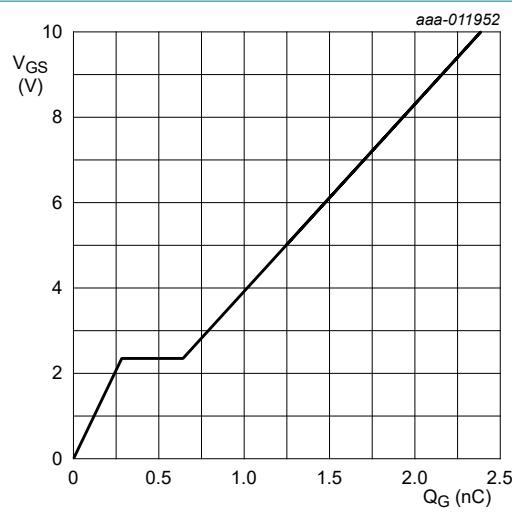


Fig. 14. Gate-source voltage as a function of gate charge; typical values

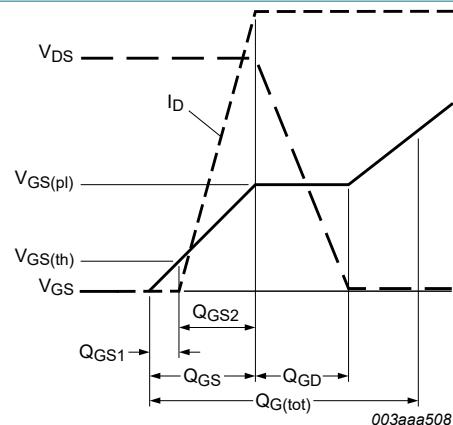


Fig. 15. Gate charge waveform definitions

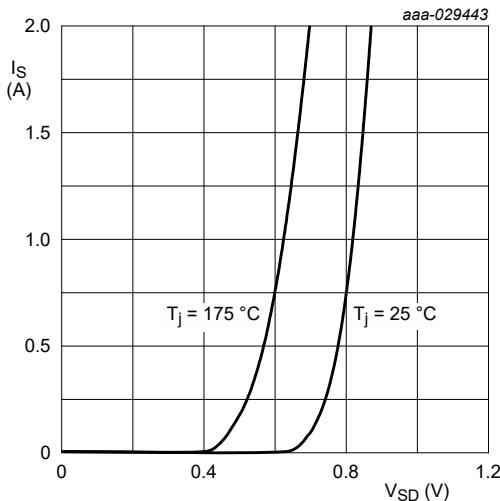


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

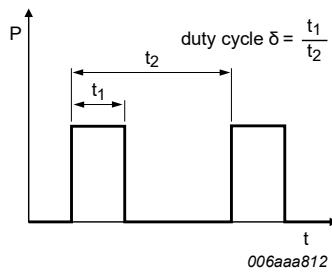


Fig. 17. Duty cycle definition

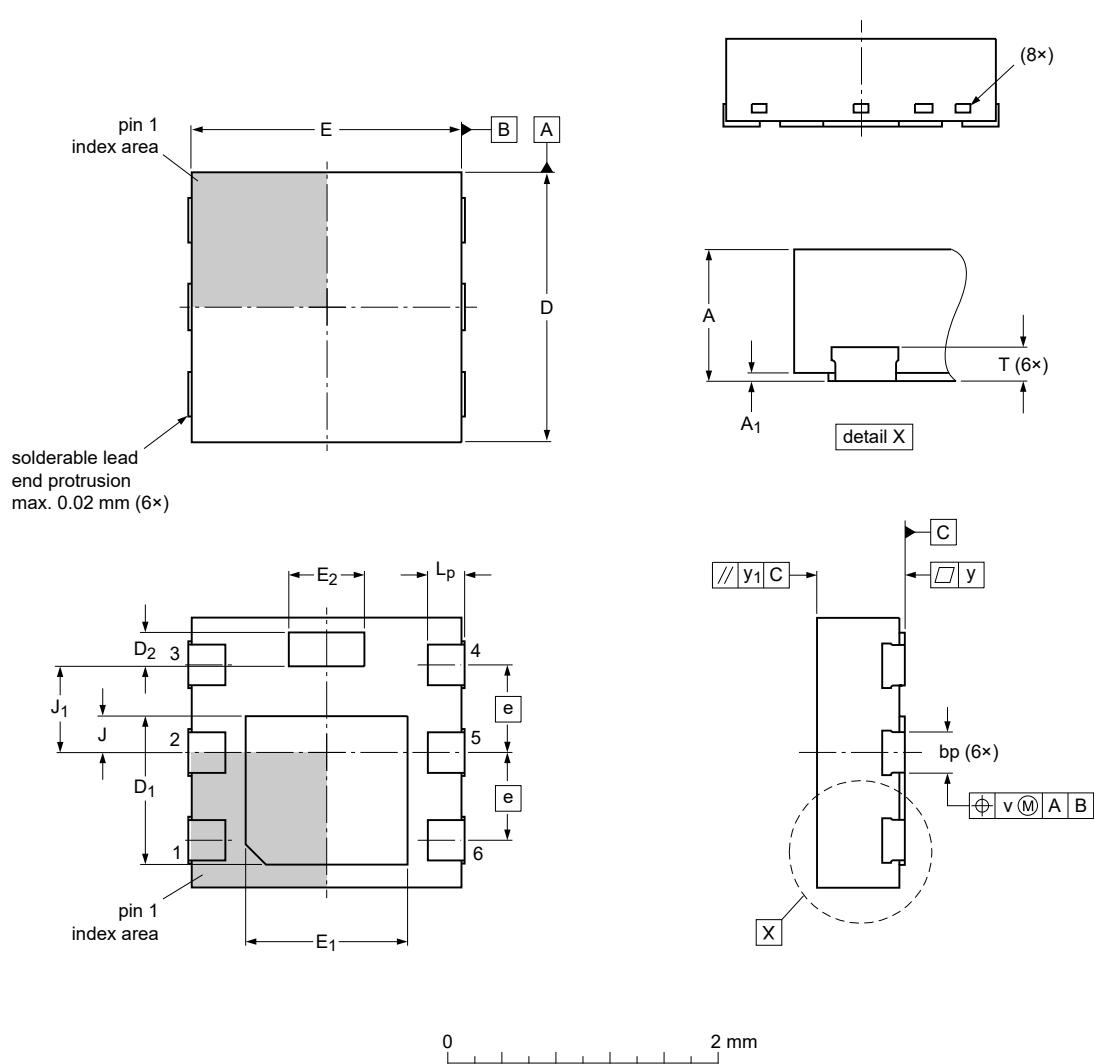
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm

SOT1220



Unit	A	A ₁	bp	D	D ₁	D ₂	E	E ₁	E ₂	e	J	J ₁	L _p	T	v	y	y ₁
mm	min		0.25	1.9	1.0	0.2	1.9	1.1	0.51				0.2	0.10			
mm	nom		0.35	2.1	1.2	0.3	2.1	1.3	0.61				0.65	0.27	0.16	0.1	0.05
mm	max	0.65	0.04	0.35	2.1	1.2	0.3	1.3	0.61				0.3	0.22			0.1

Note

1. Dimension A is including plating thickness.

sot1220_po

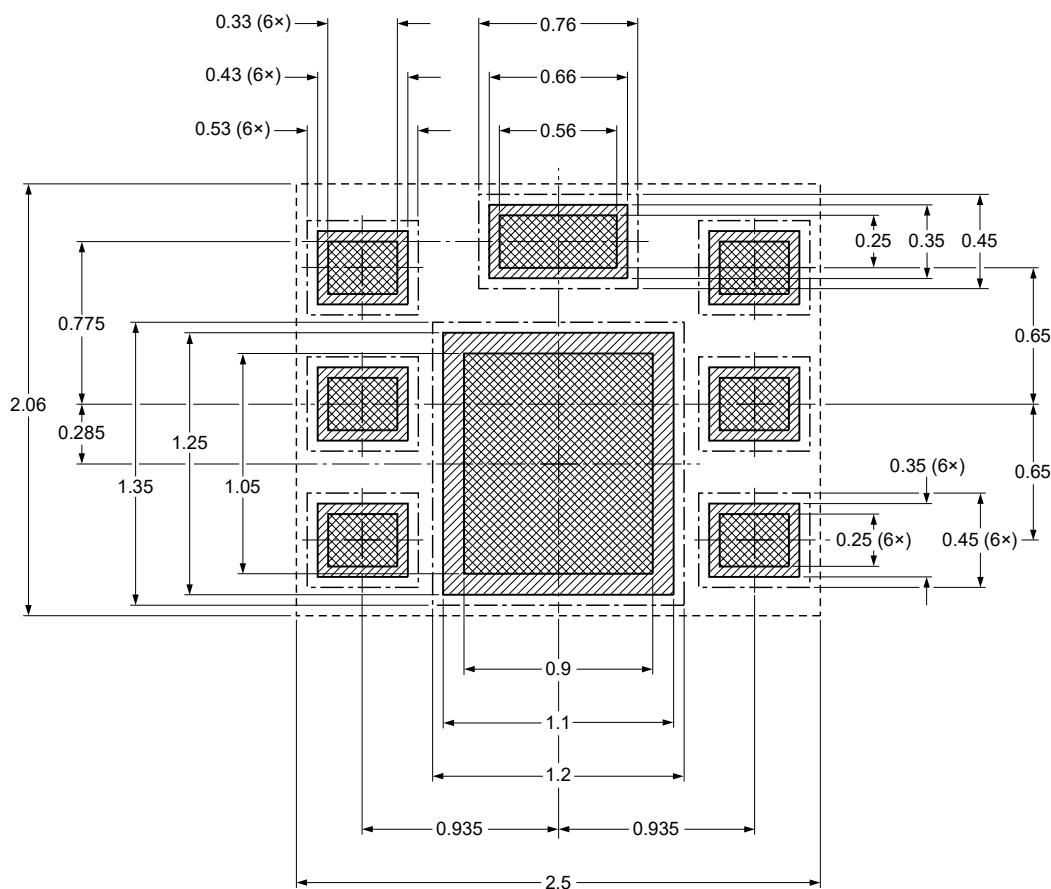
Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1220					18-05-30 18-06-07

Fig. 18. Package outline DFN2020MD-6 (SOT1220)

13. Soldering

Footprint information for reflow soldering of DFN2020MD-6 package

SOT1220

**Fig. 19. Reflow soldering footprint for DFN2020MD-6 (SOT1220)**

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK6D120-40E v.1	20190429	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 29 April 2019



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