



# PCA9515A

I<sup>2</sup>C-bus repeater

Rev. 5 — 23 March 2012

Product data sheet

## 1. General description

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The PCA9515A is a CMOS integrated circuit intended for application in I<sup>2</sup>C-bus and SMBus systems.

While retaining all the operating modes and features of the I<sup>2</sup>C-bus system, it permits extension of the I<sup>2</sup>C-bus by buffering both the data (SDA) and the clock (SCL) lines, thus enabling two buses of 400 pF.

The I<sup>2</sup>C-bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9515A enables the system designer to isolate two halves of a bus, thus more devices or longer length can be accommodated. It can also be used to run two buses, one at 5 V and the other at 3.3 V or a 400 kHz and 100 kHz bus, where the 100 kHz bus is isolated when 400 kHz operation of the other is required.

**Two or more PCA9515As cannot be put in series.** The PCA9515A design does not allow this configuration. Since there is no direction pin, slightly different 'legal' low voltage levels are used to avoid lock-up conditions between the input and the output. A 'regular LOW' applied at the input of a PCA9515A will be propagated as a 'buffered LOW' with a slightly higher value. When this 'buffered LOW' is applied to another PCA9515A, PCA9516A or PCA9518/A in series, the second PCA9515A, PCA9516A or PCA9518/A will not recognize it as a 'regular LOW' and will not propagate it as a 'buffered LOW' again. The PCA9510/A, PCA9511/A, PCA9512/A, PCA9513/A, PCA9514/A cannot be used in series with the PCA9515A, PCA9516A or PCA9518/A, but can be used in series with themselves since they use shifting instead of static offsets to avoid lock-up conditions.

The output pull-down of each internal buffer is set for approximately 0.5 V, while the input threshold of each internal buffer is set about 0.07 V lower, when the output is internally driven LOW. This prevents a lock-up condition from occurring.

## 2. Features and benefits

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- 2-channel, bidirectional buffer
- I<sup>2</sup>C-bus and SMBus compatible
- Active HIGH repeater enable input
- Open-drain input/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard-mode and Fast-mode I<sup>2</sup>C-bus devices and multiple masters
- Powered-off high-impedance I<sup>2</sup>C-bus pins
- Operating supply voltage range of 2.3 V to 3.6 V
- 5.5 V tolerant I<sup>2</sup>C-bus and enable pins



- 0 Hz to 400 kHz clock frequency (the maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater)
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8 (MSOP8), HWSO8

### 3. Ordering information

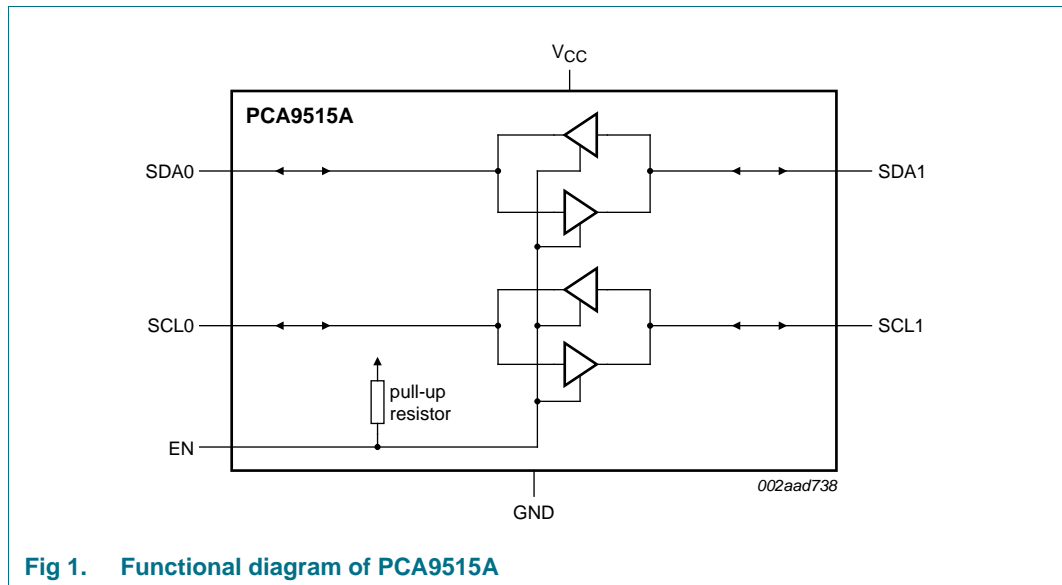
**Table 1. Ordering information**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

Type number	Topside mark	Package		
		Name	Description	Version
PCA9515AD	PA9515A	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9515ADP	9515A	TSSOP8 <sup>[1]</sup>	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9515ATP	15A	HWSO8	plastic thermal enhanced very very thin small outline package; no leads; 8 terminals; body 2 × 3 × 0.8 mm	SOT1069-2

[1] Also known as MSOP8.

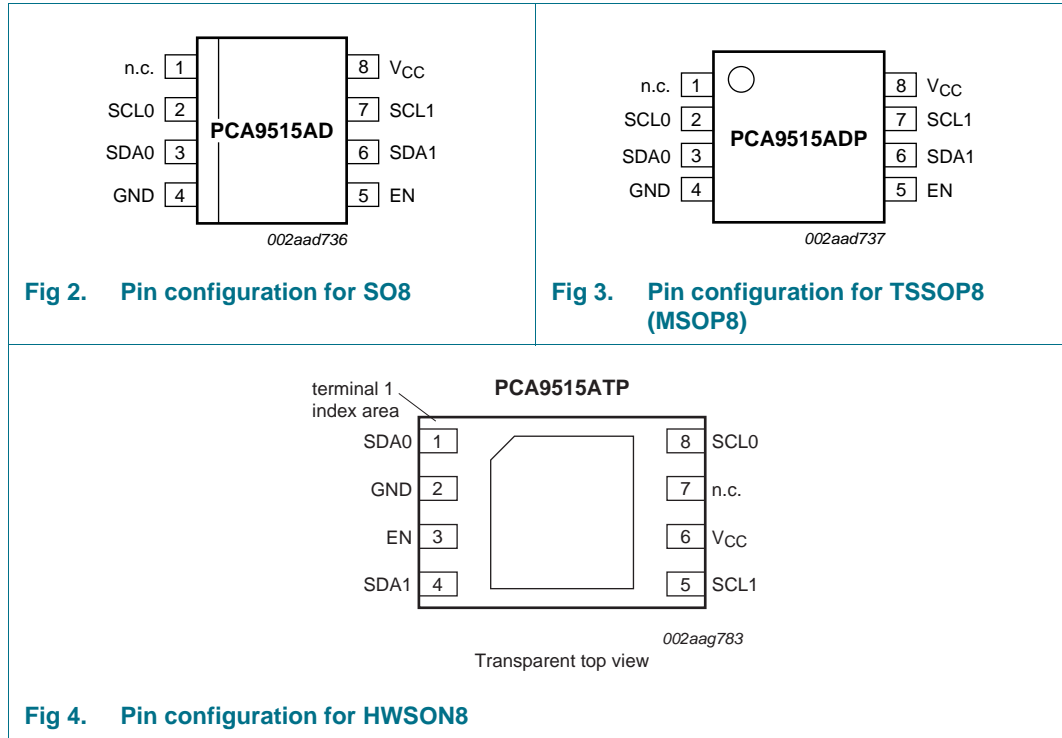
### 4. Functional diagram



**Fig 1. Functional diagram of PCA9515A**

## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin		Description
	SO8, TSSOP8	HWSO8	
n.c.	1	7	not connected
SCL0	2	8	serial clock bus 0; open-drain 5 V tolerant I/O
SDA0	3	1	serial data bus 0; open-drain 5 V tolerant I/O
GND	4	2 <sup>[1]</sup>	supply ground (0 V)
EN	5	3	active HIGH repeater enable input (internal pull-up with 100 kΩ)
SDA1	6	4	serial data bus 1; open-drain 5 V tolerant I/O
SCL1	7	5	serial clock bus 1; open-drain 5 V tolerant I/O
V <sub>CC</sub>	8	6	supply voltage

[1] HWSO8 package die supply ground is connected to both GND pin and exposed center pad. GND pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper head conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

## 6. Functional description

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Refer to [Figure 1 “Functional diagram of PCA9515A”](#).

The PCA9515A integrated circuit contains two identical buffer circuits which enable I<sup>2</sup>C-bus and similar bus systems to be extended without degradation of system performance.

The PCA9515A contains two bidirectional, open-drain buffers specifically designed to support the standard LOW-level contention arbitration of the I<sup>2</sup>C-bus. Except during arbitration or clock stretching, the PCA9515A acts like a pair of non-inverting, open-drain buffers, one for SDA and one for SCL.

### 6.1 Enable

The EN pin is active HIGH with an internal pull-up and allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I<sup>2</sup>C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I<sup>2</sup>C-bus parts being enabled.

The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

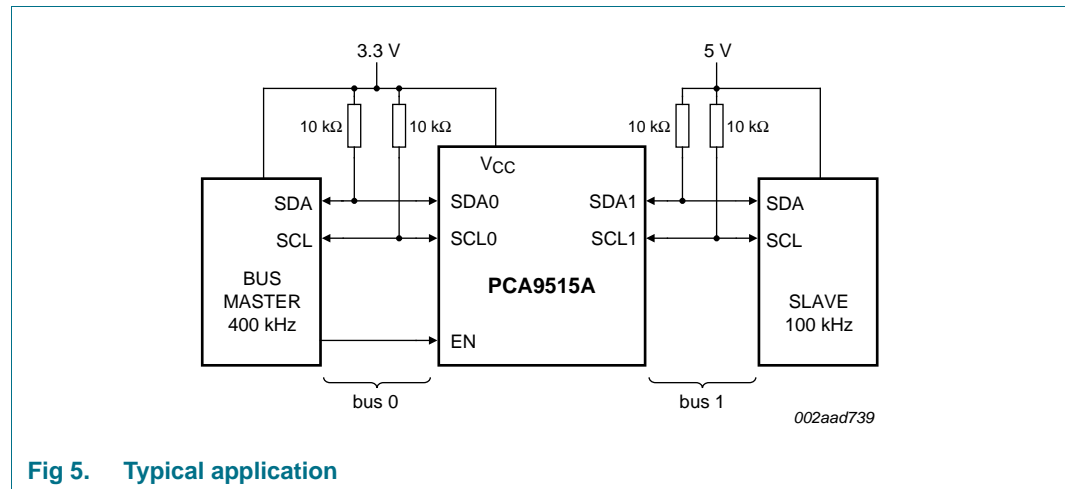
### 6.2 I<sup>2</sup>C-bus systems

As with the standard I<sup>2</sup>C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I<sup>2</sup>C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with Standard-mode and Fast-mode I<sup>2</sup>C-bus devices in addition to SMBus devices. Standard-mode I<sup>2</sup>C-bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I<sup>2</sup>C-bus system where Standard-mode devices and multiple masters are possible. Under certain conditions higher termination currents can be used.

Please see Application Note *AN255, I<sup>2</sup>C/SMBus Repeaters, Hubs and Expanders* for additional information on sizing resistors and precautions when using more than one PCA9515A/PCA9516A in a system or using the PCA9515A/PCA9516A in conjunction with the P82B96.

## 7. Application design-in information

A typical application is shown in [Figure 5](#). In this example, the system master is running on a 3.3 V I<sup>2</sup>C-bus while the slave is connected to a 5 V bus. Both buses run at 100 kHz unless the slave bus is isolated and then the master bus can run at 400 kHz. Master devices can be placed on either bus.



**Fig 5. Typical application**

The PCA9515A is 5 V tolerant, so it does not require any additional circuitry to translate between the different bus voltages.

When one side of the PCA9515A is pulled LOW by a device on the I<sup>2</sup>C-bus, a CMOS hysteresis type input detects the falling edge and causes the internal driver on the other side to turn on, thus causing the other side to also go LOW. The side driven LOW by the PCA9515A will typically be at  $V_{OL} = 0.5$  V.

In order to illustrate what would be seen in a typical application, refer to [Figure 6](#) and [Figure 7](#). If the bus master in [Figure 5](#) were to write to the slave through the PCA9515A, we would see the waveform shown in [Figure 6](#) on bus 0. This looks like a normal I<sup>2</sup>C-bus transmission until the falling edge of the eighth clock pulse. At that point, the master releases the data line (SDA) while the slave pulls it LOW through the PCA9515A. Because the  $V_{OL}$  of the PCA9515A is typically round 0.5 V, a step in the SDA will be seen. After the master has transmitted the ninth clock pulse, the slave releases the data line.

On the bus 1 side of the PCA9515A, the clock and data lines would have a positive offset from ground equal to the  $V_{OL}$  of the PCA9515A. After the eighth clock pulse the data line will be pulled to the  $V_{OL}$  of the slave device, which is very close to ground in this example. It is important to note that any arbitration or clock stretching events on bus 1 require that the  $V_{OL}$  of the PCA9515A (see  $V_{OL} - V_{ILC}$  in [Section 9 "Static characteristics"](#)) to be recognized by the PCA9515A and then transmitted to bus 0.

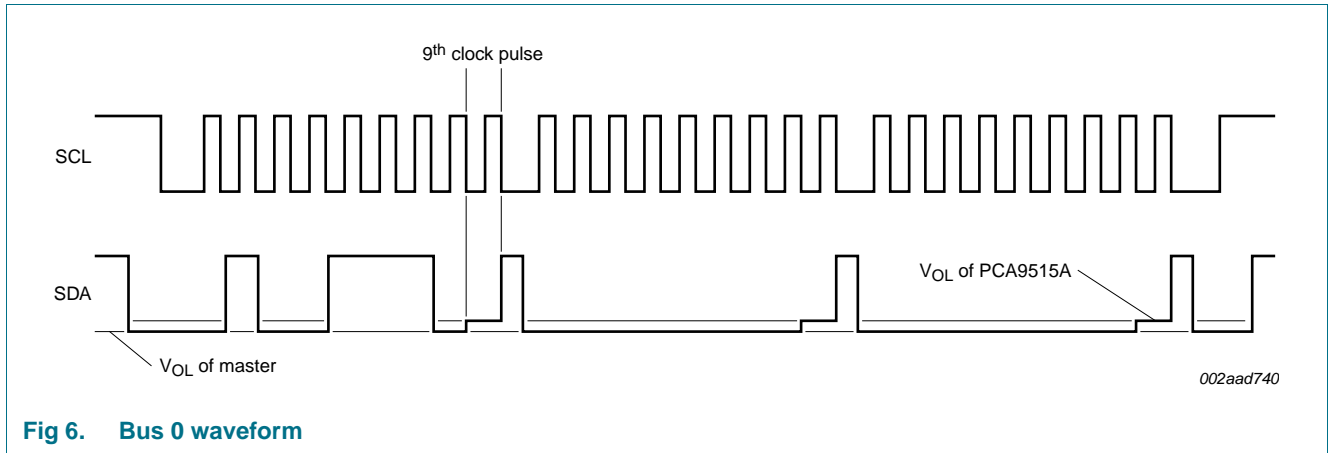


Fig 6. Bus 0 waveform

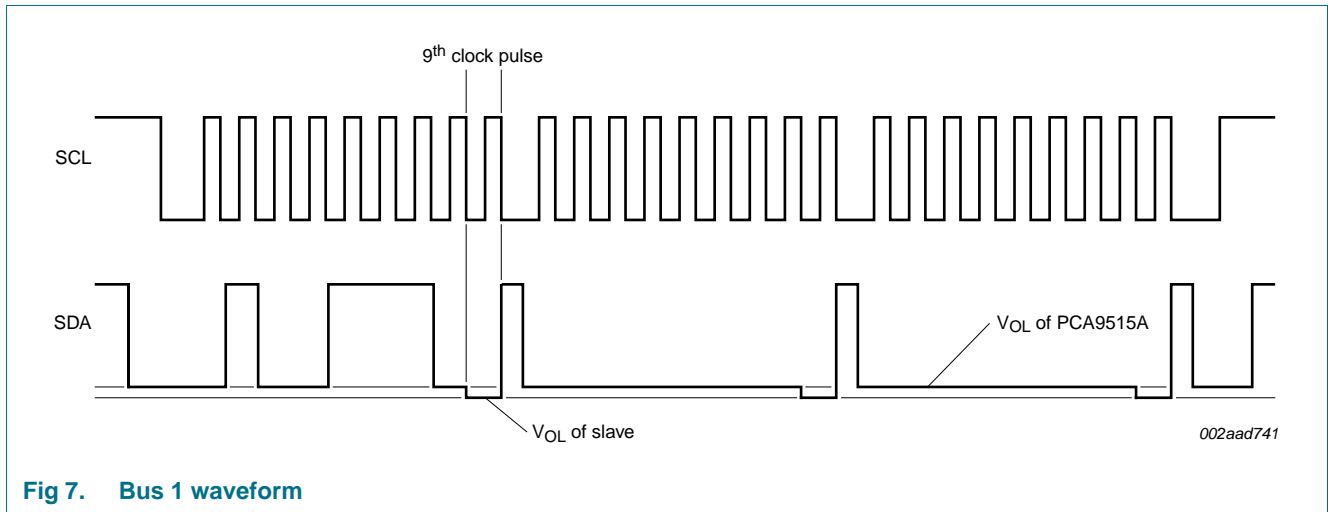


Fig 7. Bus 1 waveform

## 8. Limiting values

**Table 3. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).  
 Voltages with respect to pin GND.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$V_{I2C-bus}$	I <sup>2</sup> C-bus voltage	SCL or SDA	-0.5	+7	V
$I_{I/O}$	input/output current	DC; any pin	-	50	mA
$P_{tot}$	total power dissipation		-	100	mW
$T_{stg}$	storage temperature		-55	+125	°C
$T_{amb}$	ambient temperature	operating in free air	-40	+85	°C

## 9. Static characteristics

**Table 4. Static characteristics (V<sub>CC</sub> = 3.0 V to 3.6 V)**

V<sub>CC</sub> = 3.0 V to 3.6 V<sup>[1]</sup>; GND = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[2]</sup>	Max	Unit
<b>Supplies</b>						
V <sub>CC</sub>	supply voltage		3.0	-	3.6	V
I <sub>CCH</sub>	HIGH-level supply current	both channels HIGH; V <sub>CC</sub> = 3.6 V; SDAn = SCLn = V <sub>CC</sub>	-	0.8	5	mA
I <sub>CCL</sub>	LOW-level supply current	both channels LOW; V <sub>CC</sub> = 3.6 V; one SDA and one SCL = GND; other SDA and SCL open	-	1.7	5	mA
I <sub>CCLc</sub>	contention LOW-level supply current	V <sub>CC</sub> = 3.6 V; SDAn = SCLn = GND	-	1.6	5	mA
<b>Input SCLn; input/output SDAn</b>						
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>CC</sub>	-	5.5	V
V <sub>IL</sub>	LOW-level input voltage		<sup>[3]</sup> -0.5	-	+0.3V <sub>CC</sub>	V
V <sub>ILc</sub>	contention LOW-level input voltage		<sup>[3]</sup> -0.5	-	+0.4	V
V <sub>IK</sub>	input clamping voltage	I <sub>I</sub> = -18 mA	-	-	-1.2	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 3.6 V	-1	-	+1	μA
I <sub>IL</sub>	LOW-level input current	SDAn, SCLn; V <sub>I</sub> = 0.2 V	-	-	5	μA
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 20 μA or 6 mA	0.47	0.52	0.6	V
V <sub>OL</sub> -V <sub>ILc</sub>	difference between LOW-level output and LOW-level input voltage contention	guaranteed by design	-	-	70	mV
C <sub>i</sub>	input capacitance	V <sub>I</sub> = 3 V or 0 V	-	6	7	pF
<b>Enable</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	-	+0.8	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	5.5	V
I <sub>IL(EN)</sub>	LOW-level input current on pin EN	V <sub>I</sub> = 0.2 V	-	-10	-30	μA
I <sub>LI</sub>	input leakage current		-1	-	+1	μA
C <sub>i</sub>	input capacitance	V <sub>I</sub> = 3.0 V or 0 V	-	6	7	pF

- [1] For operation between published voltage ranges (Table 4 for V<sub>CC</sub> = 3.0 V to 3.6 V; Table 5 for V<sub>CC</sub> = 2.3 V to 2.7 V), refer to worst-case parameter in both ranges.
- [2] Typical value taken at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.
- [3] V<sub>IL</sub> specification is for the first LOW level seen by the SDAn/SCLn lines. V<sub>ILc</sub> is for the second and subsequent LOW levels seen by the SDAn/SCLn lines.

**Table 5. Static characteristics (V<sub>CC</sub> = 2.3 V to 2.7 V)**

V<sub>CC</sub> = 2.3 V to 2.7 V<sup>[1]</sup>; GND = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[2]</sup>	Max	Unit
<b>Supplies</b>						
V <sub>CC</sub>	supply voltage		2.3	-	2.7	V
I <sub>CCH</sub>	HIGH-level supply current	both channels HIGH; V <sub>CC</sub> = 2.7 V; SDAn = SCLn = V <sub>CC</sub>	-	0.8	5	mA
I <sub>CCL</sub>	LOW-level supply current	both channels LOW; V <sub>CC</sub> = 2.7 V; one SDA and one SCL = GND; other SDA and SCL open	-	1.6	5	mA
I <sub>CCLc</sub>	contention LOW-level supply current	V <sub>CC</sub> = 2.7 V; SDAn = SCLn = GND	-	1.6	5	mA
<b>Input SCLn; input/output SDAn</b>						
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>CC</sub>	-	5.5	V
V <sub>IL</sub>	LOW-level input voltage		<sup>[3]</sup> -0.5	-	+0.3V <sub>CC</sub>	V
V <sub>ILc</sub>	contention LOW-level input voltage		<sup>[3]</sup> -0.5	-	+0.4	V
V <sub>IK</sub>	input clamping voltage	I <sub>I</sub> = -18 mA	-	-	-1.2	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 2.7 V	-1	-	+1	μA
I <sub>IL</sub>	LOW-level input current	SDAn, SCLn; V <sub>I</sub> = 0.2 V	-	-	10	μA
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 20 μA or 6 mA	0.47	0.52	0.6	V
V <sub>OL</sub> -V <sub>ILc</sub>	difference between LOW-level output and LOW-level input voltage contention	guaranteed by design	-	-	70	mV
C <sub>i</sub>	input capacitance	V <sub>I</sub> = 3 V or 0 V	-	6	7	pF
<b>Enable</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	-	+0.8	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	5.5	V
I <sub>IL(EN)</sub>	LOW-level input current on pin EN	V <sub>I</sub> = 0.2 V	-	-10	-30	μA
I <sub>LI</sub>	input leakage current		-1	-	+1	μA
C <sub>i</sub>	input capacitance	V <sub>I</sub> = 3.0 V or 0 V	-	6	7	pF

[1] For operation between published voltage ranges (Table 4 for V<sub>CC</sub> = 3.0 V to 3.6 V; Table 5 for V<sub>CC</sub> = 2.3 V to 2.7 V), refer to worst-case parameter in both ranges.

[2] Typical value taken at V<sub>CC</sub> = 2.5 V and T<sub>amb</sub> = 25 °C.

[3] V<sub>IL</sub> specification is for the first LOW level seen by the SDAn/SCLn lines. V<sub>ILc</sub> is for the second and subsequent LOW levels seen by the SDAn/SCLn lines.



## 10. Dynamic characteristics

**Table 6. Dynamic characteristics (V<sub>CC</sub> = 2.3 V to 2.7 V)**

V<sub>CC</sub> = 2.3 V to 2.7 V; GND = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
t <sub>PHL</sub>	HIGH to LOW propagation delay	<a href="#">Figure 8</a>	45	82	130	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	<a href="#">Figure 8</a>	[2] 33	113	190	ns
t <sub>THL</sub>	HIGH to LOW output transition time	<a href="#">Figure 8</a>	-	57	-	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	<a href="#">Figure 8</a>	[2] -	148	-	ns
t <sub>su</sub>	set-up time	EN HIGH before START condition	100	-	-	ns
t <sub>h</sub>	hold time	EN HIGH after STOP condition	130	-	-	ns

[1] Typical values taken at V<sub>CC</sub> = 2.5 V and T<sub>amb</sub> = 25 °C.

[2] Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.

**Table 7. Dynamic characteristics (V<sub>CC</sub> = 3.0 V to 3.6 V)**

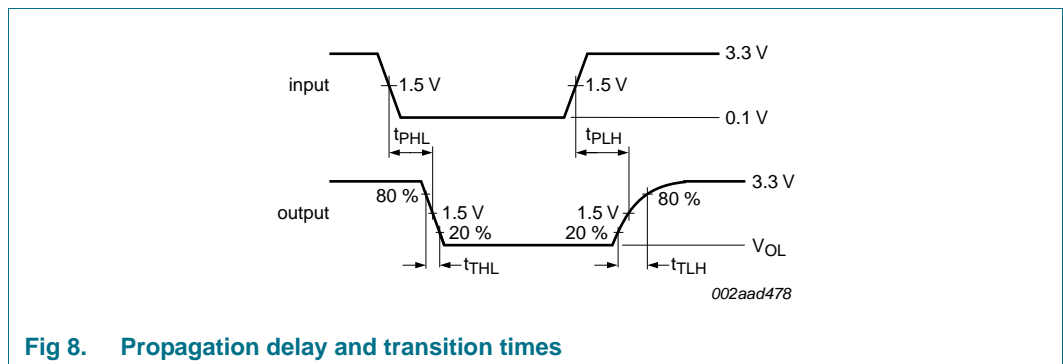
V<sub>CC</sub> = 3.0 V to 3.6 V; GND = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
t <sub>PHL</sub>	HIGH to LOW propagation delay	<a href="#">Figure 8</a>	45	68	120	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	<a href="#">Figure 8</a>	[2] 33	102	180	ns
t <sub>THL</sub>	HIGH to LOW output transition time	<a href="#">Figure 8</a>	-	58	-	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	<a href="#">Figure 8</a>	[2] -	147	-	ns
t <sub>su</sub>	set-up time	EN HIGH before START condition	100	-	-	ns
t <sub>h</sub>	hold time	EN HIGH after STOP condition	100	-	-	ns

[1] Typical values taken at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

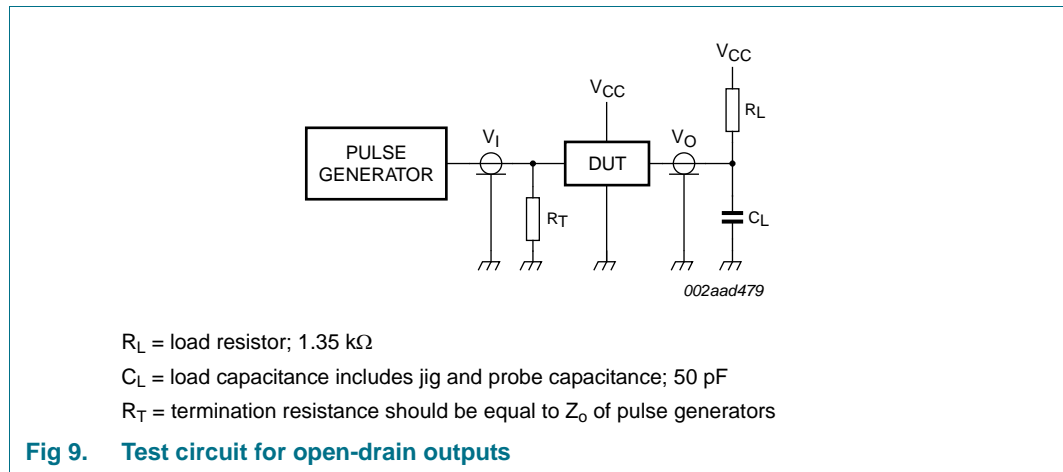
[2] Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.

### 10.1 AC waveforms



**Fig 8. Propagation delay and transition times**

## 11. Test information



## 12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

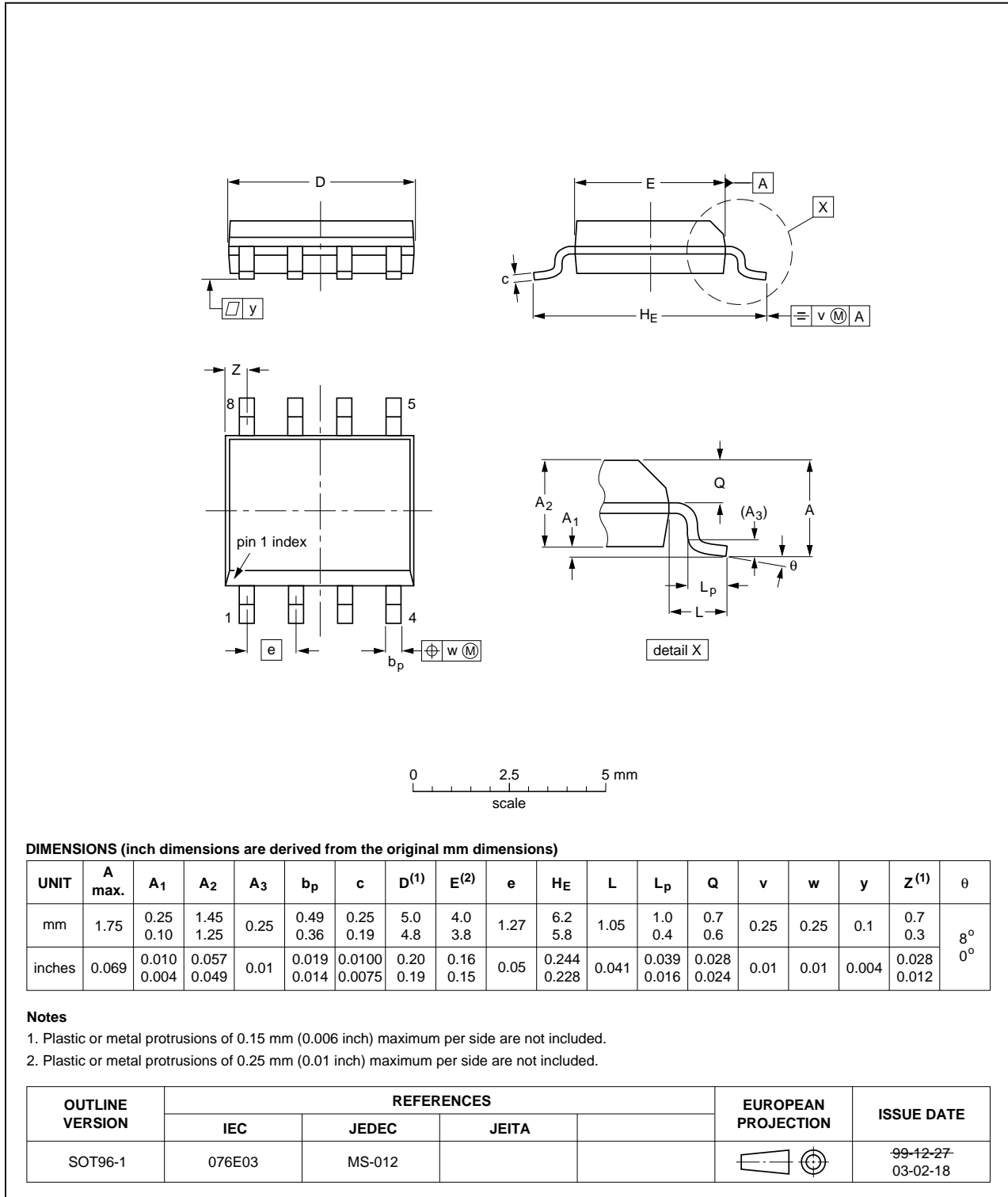


Fig 10. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1

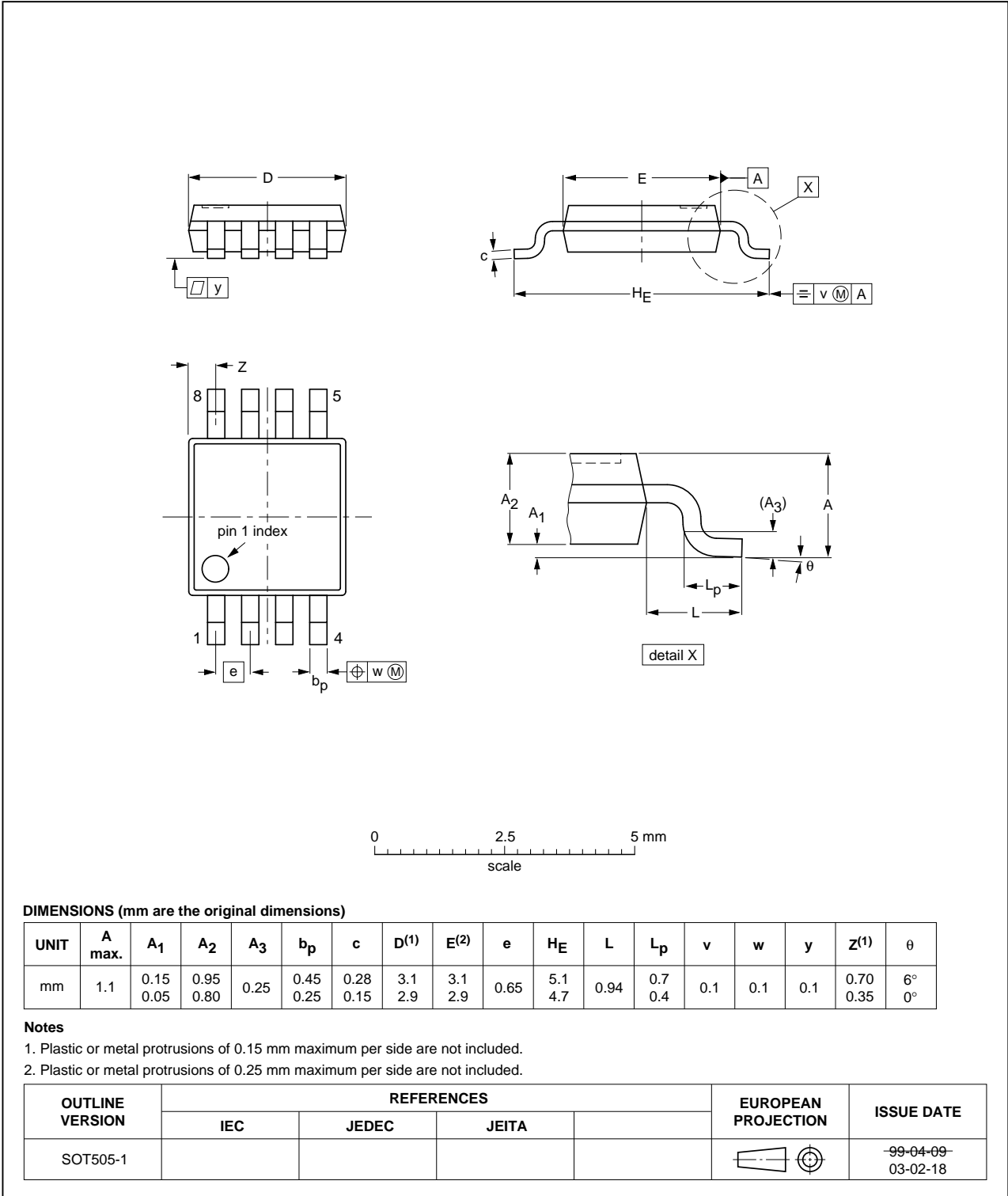


Fig 11. Package outline SOT505-1 (TSSOP8)

HWSON8: plastic thermal enhanced very very thin small outline package; no leads;  
8 terminals; body 2 x 3 x 0.8 mm

SOT1069-2

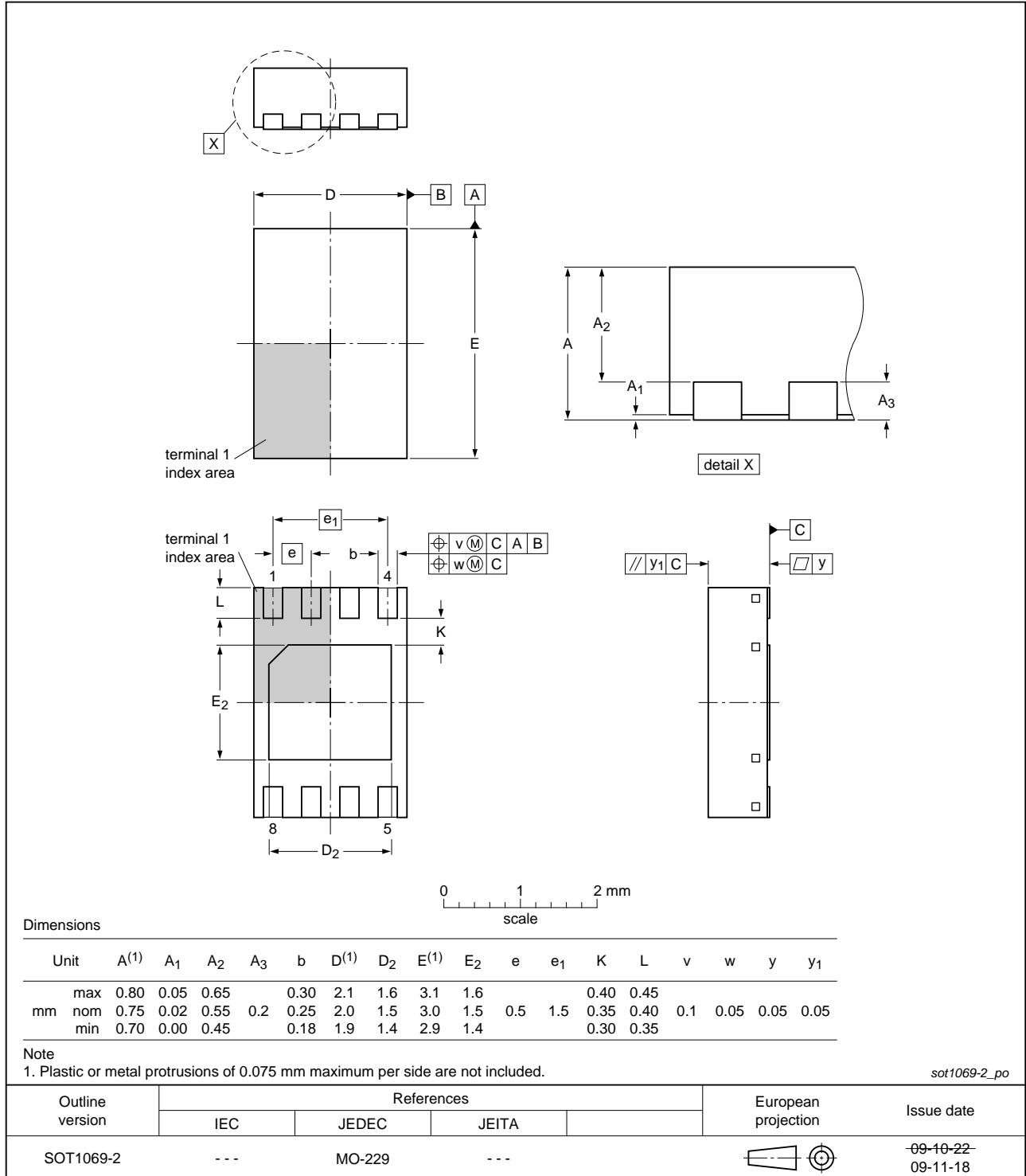


Fig 12. Package outline SOT1069-2 (HWSON8)

## 13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “Surface mount reflow soldering description”.

### 13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 13](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 8](#) and [9](#)

**Table 8. SnPb eutectic process (from J-STD-020C)**

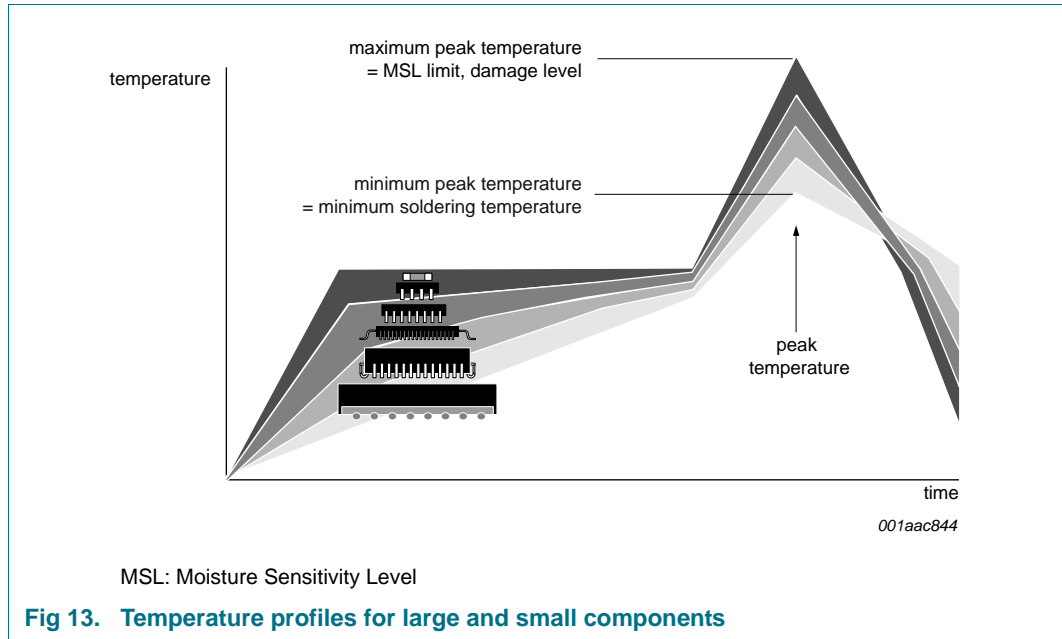
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 9. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 13](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 14. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
I/O	Input/Output
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
SMBus	System Management Bus



## 15. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9515A v.5	20120323	Product data sheet	-	PCA9515A v.4
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PCA9515A v.4	20080411	Product data sheet	-	PCA9515A v.3
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PCA9515A v.2 (9397 750 13709)	20040709	Product data sheet	-	PCA9515A v.1
PCA9515A v.1 (9397 98 13237)	20040617	Objective data sheet	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: [ocean@oceanchips.ru](mailto:ocean@oceanchips.ru)

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А