



Z86E04/E08

CMOS Z8 OTP MICROCONTROLLERS

PRODUCT DEVICES

| Part Number | Oscillator Type | Operating V_{CC} | Operating Temperature | ROM (KB) | Package |
|-----------------|-----------------|--------------------|-----------------------|----------|-------------|
| Z86E0412PEC | Crystal | 4.5V–5.5V | –40°C/105°C | 1 | 18-Pin DIP |
| Z86E0412PSC1866 | Crystal | 4.5V–5.5V | 0°C/70°C | 1 | 18-Pin DIP |
| Z86E0412PSC1903 | RC | 4.5V–5.5V | 0°C/70°C | 1 | 18-Pin DIP |
| Z86E0412PEC1903 | RC | 4.5V–5.5V | –40°C/105°C | 1 | 18-Pin DIP |
| Z86E0412SEC | Crystal | 4.5V–5.5V | –40°C/105°C | 1 | 18-Pin SOIC |
| Z86E0412SSC1866 | Crystal | 4.5V–5.5V | 0°C/70°C | 1 | 18-Pin SOIC |
| Z86E0412SSC1903 | RC | 4.5V–5.5V | 0°C/70°C | 1 | 18-Pin SOIC |
| Z86E0412SEC1903 | RC | 4.5V–5.5V | –40°C/105°C | 1 | 18-Pin SOIC |
| Z86E0812PEC | Crystal | 4.5V–5.5V | –40°C/105°C | 2 | 18-Pin DIP |
| Z86E0812PSC1866 | Crystal | 4.5V–5.5V | 0°C/70°C | 2 | 18-Pin DIP |
| Z86E0812PSC1903 | RC | 4.5V–5.5V | 0°C/70°C | 2 | 18-Pin DIP |
| Z86E0812PEC1903 | RC | 4.5V–5.5V | –40°C/105°C | 2 | 18-Pin DIP |
| Z86E0812SEC | Crystal | 4.5V–5.5V | –40°C/105°C | 2 | 18-Pin SOIC |
| Z86E0812SSC1866 | Crystal | 4.5V–5.5V | 0°C/70°C | 2 | 18-Pin SOIC |
| Z86E0812SSC1903 | RC | 4.5V–5.5V | 0°C/70°C | 2 | 18-Pin SOIC |
| Z86E0812SEC1903 | RC | 4.5V–5.5V | –40°C/105°C | 2 | 18-Pin SOIC |

Several key product features of the extensive family of Zilog Z86E04/E08 CMOS OTP microcontrollers are presented in the above table. This table enables the user to identify which of the E04/E08 product variants most closely match the user's application requirements.

FEATURES

- 14 Input/Output Lines
- Six Vectored, Prioritized Interrupts (3 falling edge, 1 rising edge, 2 timers)
- Two Analog Comparators
- Program Options:
 - Low Noise
 - ROM Protect
 - Auto Latch
 - Watch-Dog Timer (WDT)
 - EPROM/Test Mode Disable
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- WDT/ Power-On Reset (POR)
- On-Chip Oscillator that Accepts XTAL, Ceramic Resonance, LC, RC, or External Clock
- Clock-Free WDT Reset
- Low-Power Consumption (50 mw typical)
- Fast Instruction Pointer (1 μ s @ 12 MHz)
- RAM Bytes (125)

GENERAL DESCRIPTION

Zilog's Z86E04/E08 Microcontrollers (MCU) are One-Time Programmable (OTP) members of Zilog's single-chip Z8[®] MCU family that allow easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z86E04/E08's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Two on-chip counter/timers, with a large number of user selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

Note: All signals with an overline, " $\bar{}$ ", are active Low, for example: $\overline{B/W}$ (WORD is active Low); \overline{B}/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

| Connection | Circuit | Device |
|------------|-----------------|-----------------|
| Power | V _{CC} | V _{DD} |
| Ground | GND | V _{SS} |



Figure 1. Functional Block Diagram

GENERAL DESCRIPTION (Continued)



Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTION



Figure 3. 18-Pin EPROM Mode Configuration

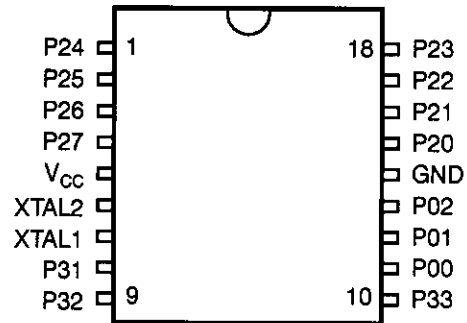


Figure 4. 18-Pin DIP/SOIC Mode Configuration

Table 1. 18-Pin DIP Pin Identification

| EPROM Programming Mode | | | |
|------------------------|-----------------|-----------------|-----------|
| Pin # | Symbol | Function | Direction |
| 1-4 | D4-D7 | Data 4, 5, 6, 7 | In/Output |
| 5 | V _{CC} | Power Supply | |
| 6 | NC | No Connection | |
| 7 | CE | Chip Enable | Input |
| 8 | OE | Output Enable | Input |
| 9 | EPM | EPROM Prog Mode | Input |
| 10 | V _{PP} | Prog Voltage | Input |
| 11 | Clear | Clear Clock | Input |
| 12 | Clock | Address | Input |
| 13 | PGM | Prog Mode | Input |
| 14 | GND | Ground | |
| 15-18 | D0-D3 | Data 0,1, 2, 3 | In/Output |

Table 2. 18-Pin DIP/SOIC Pin Identification

| Standard Mode | | | |
|---------------|-----------------|----------------------|-----------|
| Pin # | Symbol | Function | Direction |
| 1-4 | P24-P27 | Port 2, Pins 4,5,6,7 | In/Output |
| 5 | V _{CC} | Power Supply | |
| 6 | XTAL2 | Crystal Osc. Clock | Output |
| 7 | XTAL1 | Crystal Osc. Clock | Input |
| 8 | P31 | Port 3, Pin 1, AN1 | Input |
| 9 | P32 | Port 3, Pin 2, AN2 | Input |
| 10 | P33 | Port 3, Pin 3, REF | Input |
| 11-13 | P00-P02 | Port 0, Pins 0,1,2 | In/Output |
| 14 | GND | Ground | |
| 15-18 | P20-P23 | Port 2, Pins 0,1,2,3 | In/Output |

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power

dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

$$\begin{aligned} \text{Total Power Dissipation} = & V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] \\ & + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] \\ & + \text{sum of } (V_{OL} \times I_{OL}) \end{aligned}$$

| Parameter | Min | Max | Units | Note |
|---|------|------------|---------------|------|
| Ambient Temperature under Bias | -40 | +105 | C | |
| Storage Temperature | -65 | +150 | C | |
| Voltage on any Pin with Respect to V_{SS} | -0.7 | +12 | V | 1 |
| Voltage on V_{DD} Pin with Respect to V_{SS} | -0.3 | +7 | V | |
| Voltage on Pins 7, 8, 9, 10 with Respect to V_{SS} | -0.6 | $V_{DD}+1$ | V | 2 |
| Total Power Dissipation | | 1.65 | W | |
| Maximum Allowable Current out of V_{SS} | | 300 | mA | |
| Maximum Allowable Current into V_{DD} | | 220 | mA | |
| Maximum Allowable Current into an Input Pin | -600 | +600 | μA | 3 |
| Maximum Allowable Current into an Open-Drain Pin | -600 | +600 | μA | 4 |
| Maximum Allowable Output Current Sunked by Any I/O Pin | | 25 | mA | |
| Maximum Allowable Output Current Sourced by Any I/O Pin | | 25 | mA | |
| Total Maximum Output Current Sunked by a Port | | 60 | mA | |
| Total Maximum Output Current Sourced by a Port | | 45 | mA | |

Notes:

1. This applies to all pins except where otherwise noted. Maximum current into pin must be $\pm 600 \mu\text{A}$.
2. There is no input protection diode from pin to V_{DD} (not applicable to EPROM Mode).
3. This excludes Pin 6 and Pin 7.
4. Device pin is not at an output Low state.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 5).



Figure 5. Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{ MHz}$, unmeasured pins returned to GND.

| Parameter | Min | Max |
|--------------------|-----|-------|
| Input capacitance | 0 | 10 pF |
| Output capacitance | 0 | 20 pF |
| I/O capacitance | 0 | 25 pF |

DC ELECTRICAL CHARACTERISTICS

Standard Temperature

| Sym | Parameter | V _{CC} [4] | T _A = 0°C to +70°C | | Typical @ 25°C | Units | Conditions | Notes |
|---------------------|--|---------------------|-------------------------------|----------------------|-------------------|-------|---------------------------------------|-------|
| | | | Min | Max | | | | |
| V _{INMAX} | Max Input Voltage | 4.5V | | 12 | | V | I _{in} < 250 μA | 1 |
| | | 5.5V | | 12 | | V | I _{in} < 250 μA | 1 |
| V _{CH} | Clock Input High Voltage | 4.5V | 0.8 V _{CC} | V _{CC} +0.3 | 2.8 | V | Driven by External Clock Generator | |
| | | 5.5V | 0.8 V _{CC} | V _{CC} +0.3 | 2.8 | V | Driven by External Clock Generator | |
| V _{CL} | Clock Input Low Voltage | 4.5V | V _{SS} -0.3 | 0.2 V _{CC} | 1.7 | V | Driven by External Clock Generator | |
| | | 5.5V | V _{SS} -0.3 | 0.2 V _{CC} | 1.7 | V | Driven by External Clock Generator | |
| V _{IH} | Input High Voltage | 4.5V | 0.7 V _{CC} | V _{CC} +0.3 | 2.8 | V | | |
| | | 5.5V | 0.7 V _{CC} | V _{CC} +0.3 | 2.8 | V | | |
| V _{IL} | Input Low Voltage | 4.5V | V _{SS} -0.3 | 0.2 V _{CC} | 1.5 | V | | |
| | | 5.5V | V _{SS} -0.3 | 0.2 V _{CC} | 1.5 | V | | |
| V _{OH} | Output High Voltage | 4.5V | V _{CC} -0.4 | | 4.8 | V | I _{OH} = -2.0 mA | 5 |
| | | 5.5V | V _{CC} -0.4 | | 4.8 | V | I _{OH} = -2.0 mA | 5 |
| | | 4.5V | V _{CC} -0.4 | | 4.8 | V | Low Noise @ I _{OH} = -0.5 mA | |
| | | 5.5V | V _{CC} -0.4 | | 4.8 | V | Low Noise @ I _{OH} = -0.5 mA | |
| V _{OL1} | Output Low Voltage | 4.5V | | 0.8 | 0.1 | V | I _{OL} = +4.0 mA | 5 |
| | | 5.5V | | 0.4 | 0.1 | V | I _{OL} = +4.0 mA | 5 |
| | | 4.5V | | 0.4 | 0.1 | V | Low Noise @ I _{OL} = 1.0 mA | |
| | | 5.5V | | 0.4 | 0.1 | V | Low Noise @ I _{OL} = 1.0 mA | |
| V _{OL2} | Output Low Voltage | 4.5V | | 0.8 | 0.8 | V | I _{OL} = +12 mA, | 5 |
| | | 5.5V | | 0.8 | 0.8 | V | I _{OL} = +12 mA, | 5 |
| V _{OFFSET} | Comparator Input Offset Voltage | 4.5V | | 25.0 | 10.0 | mV | | |
| | | 5.5V | | 25.0 | 10.0 | mV | | |
| V _{LV} | V _{CC} Low Voltage Auto Reset | | 2.2 | 3.0 | 2.8 | V | @ 6 MHz Max. Int. CLK Freq. | |
| I _{IL} | Input Leakage (Input Bias Current of Comparator) | 4.5V | -1.0 | 1.0 | | μA | V _{IN} = 0V, V _{CC} | |
| | | 5.5V | -1.0 | 1.0 | | μA | V _{IN} = 0V, V _{CC} | |
| I _{OL} | Output Leakage | 4.5V | -1.0 | 1.0 | | μA | V _{IN} = 0V, V _{CC} | |
| | | 5.5V | -1.0 | 1.0 | | μA | V _{IN} = 0V, V _{CC} | |
| V _{ICR} | Comparator Input Common Mode Voltage Range | | 0 | V _{CC} -1.0 | | V | | |

| Sym | Parameter | V _{CC} [4] | T _A = 0°C to +70°C Typical | | Units | Conditions | Notes |
|------------------|---------------------------------|---------------------|---------------------------------------|------------|-------|--|-------|
| | | | Min | Max @ 25°C | | | |
| I _{CC} | Supply Current | 4.5V | 11.0 | 6.8 | mA | All Output and I/O Pins Floating @ 2 MHz | 5,7 |
| | | 5.5V | 11.0 | 6.8 | mA | All Output and I/O Pins Floating @ 2 MHz | 5,7 |
| | | 4.5V | 15.0 | 8.2 | mA | All Output and I/O Pins Floating @ 8 MHz | 5,7 |
| | | 5.5V | 15.0 | 8.2 | mA | All Output and I/O Pins Floating @ 8 MHz | 5,7 |
| | | 4.5V | 20.0 | 12.0 | mA | All Output and I/O Pins Floating @ 12 MHz | 5,7 |
| | | 5.5V | 20.0 | 12.0 | mA | All Output and I/O Pins Floating @ 12 MHz | 5,7 |
| I _{CC1} | Standby Current | 4.5V | 4.0 | 2.5 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz | 5,7 |
| | | 5.5V | 4.0 | 2.5 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz | 5,7 |
| | | 4.5V | 5.0 | 3.0 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 8 MHz | 5,7 |
| | | 5.5V | 5.0 | 3.0 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 8 MHz | 5,7 |
| | | 4.5V | 7.0 | 4.0 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 12 MHz | 5,7 |
| | | 5.5V | 7.0 | 4.0 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 12 MHz | 5,7 |
| I _{CC} | Supply Current (Low Noise Mode) | 4.5V | 11.0 | 6.8 | mA | All Output and I/O Pins Floating @ 1 MHz | 7 |
| | | 5.5V | 11.0 | 6.8 | mA | All Output and I/O Pins Floating @ 1 MHz | 7 |
| | | 4.5V | 13.0 | 7.5 | mA | All Output and I/O Pins Floating @ 2 MHz | 7 |
| | | 5.5V | 13.0 | 7.5 | mA | All Output and I/O Pins Floating @ 2 MHz | 7 |
| | | 4.5V | 15.0 | 8.2 | mA | All Output and I/O Pins Floating @ 4 MHz | 7 |
| | | 5.5V | 15.0 | 8.2 | mA | All Output and I/O Pins Floating @ 4 MHz | 7 |

DC ELECTRICAL CHARACTERISTICS (Continued)

| Sym | Parameter | V _{CC} [4] | T _A = 0°C to +70°C | | Typical @ 25°C | Units | Conditions | Notes |
|------------------|-------------------------------------|---------------------|-------------------------------|------|-------------------|---|------------|-------|
| | | | Min | Max | | | | |
| I _{CC1} | Standby Current (Low Noise Mode) | 4.5V | 4.0 | 2.5 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 1 MHz | 7 | |
| | | 5.5V | 4.0 | 2.5 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 1 MHz | 7 | |
| | | 4.5V | 4.5 | 2.8 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz | 7 | |
| | | 5.5V | 4.5 | 2.8 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz | 7 | |
| | | 4.5V | 5.0 | 3.0 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 4 MHz | 7 | |
| | | 5.5V | 5.0 | 3.0 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 4 MHz | 7 | |
| I _{CC2} | Standby Current | 4.5V | 10.0 | 1.0 | μA | STOP Mode V _{IN} = 0V, V _{CC} WDT is not Running | 7,8 | |
| | | 5.5V | 10.0 | 1.0 | μA | STOP Mode V _{IN} = 0V, V _{CC} WDT is not Running | 7,8 | |
| I _{ALL} | Auto Latch Low Current | 4.5V | 32.0 | 16 | μA | 0V < V _{IN} < V _{CC} | | |
| | | 5.5V | 32.0 | 16 | μA | 0V < V _{IN} < V _{CC} | | |
| I _{ALH} | Auto Latch High Current | 4.5V | -16.0 | -8.0 | μA | 0V < V _{IN} < V _{CC} | | |
| | | 5.5V | -16.0 | -8.0 | μA | 0V < V _{IN} < V _{CC} | | |

Notes:

1. Port 2 and Port 0 only
2. V_{SS} = 0V = GND
3. The device operates down to V_{LV} of the specified frequency for V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. V_{CC} = 4.5 to 5.5V, typical values measured at V_{CC} = 5.0V.
The V_{CC} voltage specification of 5.5 V guarantees 5.0 V ± 0.5V with typical values measured at V_{CC} = 5.0V.
5. Standard Mode (not Low EMI Mode)
6. Z86E08 only
7. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
8. If analog comparator is selected, then the comparator inputs must be at V_{CC} level.

DC ELECTRICAL CHARACTERISTICS

Extended Temperature

| Sym | Parameter | V _{CC} [4] | T _A = -40°C to +105°C | | Typical @ 25°C | Units | Conditions | Notes |
|---------------------|--|---------------------|----------------------------------|----------------------|-------------------|-------|---------------------------------------|-------|
| | | | Min | Max | | | | |
| V _{INMAX} | Max Input Voltage | 4.5V | | 12.0 | | V | I _{IN} < 250 μA | 1 |
| | | 5.5V | | 12.0 | | V | I _{IN} < 250 μA | 1 |
| V _{CH} | Clock Input High Voltage | 4.5V | 0.8 V _{CC} | V _{CC} +0.3 | 2.8 | V | Driven by External Clock Generator | |
| | | 5.5V | 0.8 V _{CC} | V _{CC} +0.3 | 2.8 | V | Driven by External Clock Generator | |
| V _{CL} | Clock Input Low Voltage | 4.5V | V _{SS} -0.3 | 0.2 V _{CC} | 1.7 | V | Driven by External Clock Generator | |
| | | 5.5V | V _{SS} -0.3 | 0.2 V _{CC} | 1.7 | V | Driven by External Clock Generator | |
| V _{IH} | Input High Voltage | 4.5V | 0.7 V _{CC} | V _{CC} +0.3 | 2.8 | V | | |
| | | 5.5V | 0.7 V _{CC} | V _{CC} +0.3 | 2.8 | V | | |
| V _{IL} | Input Low Voltage | 4.5V | V _{SS} -0.3 | 0.2 V _{CC} | 1.5 | V | | |
| | | 5.5V | V _{SS} -0.3 | 0.2 V _{CC} | 1.5 | V | | |
| V _{OH} | Output High Voltage | 4.5V | V _{CC} -0.4 | | 4.8 | V | I _{OH} = -2.0 mA | 5 |
| | | 5.5V | V _{CC} -0.4 | | 4.8 | V | I _{OH} = -2.0 mA | 5 |
| | | 4.5V | V _{CC} -0.4 | | | V | Low Noise @ I _{OH} = -0.5 mA | |
| | | 5.5V | V _{CC} -0.4 | | | V | Low Noise @ I _{OH} = -0.5 mA | |
| V _{OL1} | Output Low Voltage | 4.5V | | 0.4 | 0.1 | V | I _{OL} = +4.0 mA | 5 |
| | | 5.5V | | 0.4 | 0.1 | V | I _{OL} = +4.0 mA | 5 |
| | | 4.5V | | 0.4 | 0.1 | V | Low Noise @ I _{OL} = 1.0 mA | |
| | | 5.5V | | 0.4 | 0.1 | V | Low Noise @ I _{OL} = 1.0 mA | |
| V _{OL2} | Output Low Voltage | 4.5V | | 1.0 | 0.3 | V | I _{OL} = +12 mA, | 5 |
| | | 5.5V | | 1.0 | 0.3 | V | I _{OL} = +12 mA, | 5 |
| V _{OFFSET} | Comparator Input Offset Voltage | 4.5V | | 25.0 | 10.0 | mV | | |
| | | 5.5V | | 25.0 | 10.0 | mV | | |
| V _{LV} | V _{CC} Low Voltage Auto Reset | | 1.8 | 3.8 | 2.8 | V | @ 6 MHz Max. Int. CLK Freq. | 3 |
| I _{IL} | Input Leakage (Input Bias Current of Comparator) | 4.5V | | -1.0 | 1.0 | μA | V _{IN} = 0V, V _{CC} | |
| | | 5.5V | | -1.0 | 1.0 | μA | V _{IN} = 0V, V _{CC} | |
| I _{OL} | Output Leakage | 4.5V | | -1.0 | 1.0 | μA | V _{IN} = 0V, V _{CC} | |
| | | 5.5V | | -1.0 | 1.0 | μA | V _{IN} = 0V, V _{CC} | |
| V _{ICR} | Comparator Input Common Mode Voltage Range | | 0 | V _{CC} -1.5 | | V | | |

DC ELECTRICAL CHARACTERISTICS (Continued)

| Sym | Parameter | V _{CC} [4] | T _A = -40°C to +105°C | | Typical @ 25°C | Units | Conditions | Notes |
|------------------|---------------------------------|---------------------|----------------------------------|------|-------------------|-------|--|-------|
| | | | Min | Max | | | | |
| I _{CC} | Supply Current | 4.5V | | 11.0 | 6.8 | mA | All Output and I/O Pins Floating @ 2 MHz | 5,7 |
| | | 5.5V | | 11.0 | 6.8 | mA | All Output and I/O Pins Floating @ 2 MHz | 5,7 |
| | | 4.5V | | 15.0 | 8.2 | mA | All Output and I/O Pins Floating @ 8 MHz | 5,7 |
| | | 5.5V | | 15.0 | 8.2 | mA | All Output and I/O Pins Floating @ 8 MHz | 5,7 |
| | | 4.5V | | 20.0 | 12.0 | mA | All Output and I/O Pins Floating @ 12 MHz | 5,7 |
| | | 5.5V | | 20.0 | 12.0 | mA | All Output and I/O Pins Floating @ 12 MHz | 5,7 |
| I _{CC1} | Standby Current | 4.5V | | 5.0 | 2.5 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz | 5,7 |
| | | 5.5V | | 5.0 | 2.5 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz | 5,7 |
| | | 4.5V | | 5.0 | 3.0 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 8 MHz | 5,7 |
| | | 5.5V | | 5.0 | 3.0 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 8 MHz | 5,7 |
| | | 4.5V | | 7.0 | 4.0 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 12 MHz | 5,7 |
| | | 5.5V | | 7.0 | 4.0 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 12 MHz | 5,7 |
| I _{CC} | Supply Current (Low Noise Mode) | 4.5V | | 11.0 | 6.8 | mA | All Output and I/O Pins Floating @ 1 MHz | 7 |
| | | 5.5V | | 11.0 | 6.8 | mA | All Output and I/O Pins Floating @ 1 MHz | 7 |
| | | 4.5V | | 13.0 | 7.5 | mA | All Output and I/O Pins Floating @ 2 MHz | 7 |
| | | 5.5V | | 13.0 | 7.5 | mA | All Output and I/O Pins Floating @ 2 MHz | 7 |
| | | 4.5V | | 15.0 | 8.2 | mA | All Output and I/O Pins Floating @ 4 MHz | 7 |
| | | 5.5V | | 15.0 | 8.2 | mA | All Output and I/O Pins Floating @ 4 MHz | 7 |

| Sym | Parameter | V _{CC} [4] | T _A = -40°C to +105°C | | Typical @ 25°C | Units | Conditions | Notes |
|------------------|-------------------------------------|---------------------|----------------------------------|-------|-------------------|-------|---|-------|
| | | | Min | Max | | | | |
| I _{CC1} | Standby Current (Low Noise Mode) | 4.5V | | 4.0 | 2.5 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 1 MHz | 7 |
| | | 5.5V | | 4.0 | 2.5 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 1 MHz | 7 |
| | | 4.5V | | 4.5 | 2.8 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz | 7 |
| | | 5.5V | | 4.5 | 2.8 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz | 7 |
| | | 4.5V | | 5.0 | 3.0 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 4 MHz | 7 |
| | | 5.5V | | 5.0 | 3.0 | mA | HALT Mode V _{IN} = 0V, V _{CC} @ 4 MHz | 7 |
| I _{CC2} | Standby Current | 4.5V | | 20 | 1.0 | μA | STOP Mode V _{IN} = 0V, V _{CC} WDT is not Running | 7,8 |
| | | 5.5V | | 20 | 1.0 | μA | STOP Mode V _{IN} = 0V, V _{CC} WDT is not Running | 7,8 |
| I _{ALL} | Auto Latch Low Current | 4.5V | | 40 | 16 | μA | 0V < V _{IN} < V _{CC} | |
| | | 5.5V | | 40 | 16 | μA | 0V < V _{IN} < V _{CC} | |
| I _{ALH} | Auto Latch High Current | 4.5V | | -20.0 | -8.0 | μA | 0V < V _{IN} < V _{CC} | |
| | | 5.5V | | -20.0 | -8.0 | μA | 0V < V _{IN} < V _{CC} | |

Notes:

1. Port 2 and Port 0 only
2. V_{SS} = 0V = GND
3. The device operates down to V_{LV} of the specified frequency for V_{LV}. The minimum operational V_{CC} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.
4. V_{CC} = 4.5V to 5.5V, typical values measured at V_{CC} = 5.0V
5. Standard Mode (not Low EMI Mode)
6. Z86E08 only
7. All outputs unloaded and all inputs are at V_{CC} or V_{SS} level.
8. If analog comparator is selected, then the comparator inputs must be at V_{CC} level.

AC ELECTRICAL CHARACTERISTICS



Figure 6. AC Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

Standard Temperature

| 15 | | $T_A = 0\text{ }^\circ\text{C to } +70\text{ }^\circ\text{C}$ | | | | | | | |
|----|--------------|---|----------|-------|------|--------|-----|-------|-------|
| No | Symbol | Parameter | V_{CC} | 8 MHz | | 12 MHz | | Units | Notes |
| | | | | Min | Max | Min | Max | | |
| 1 | TpC | Input Clock Period | 4.5V | 125 | DC | 83 | DC | ns | 1 |
| | | | 5.5V | 125 | DC | 83 | DC | ns | 1 |
| 2 | TrC,TfC | Clock Input Rise and Fall Times | 4.5V | | 25 | | 15 | ns | 1 |
| | | | 5.5V | | 25 | | 15 | ns | 1 |
| 3 | TwC | Input Clock Width | 4.5V | 62 | | 41 | | ns | 1 |
| | | | 5.5V | 62 | | 41 | | ns | 1 |
| 4 | TwTinL | Timer Input Low Width | 4.5V | 100 | | 100 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 4.5V | 5TpC | | 5TpC | | | 1 |
| | | | 5.5V | 5TpC | | 5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 4.5V | | 8TpC | 8TpC | | | 1 |
| | | | 5.5V | | 8TpC | 8TpC | | | 1 |
| 7 | TrTin, TtTin | Timer Input Rise and Fall Time | 4.5V | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | ns | 1 |
| 8 | TwIL | Int. Request Input Low Time | 4.5V | 70 | | 70 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2 |
| 9 | TwIH | Int. Request Input High Time | 4.5V | | 5TpC | 5TpC | | | 1,2 |
| | | | 5.5V | | 5TpC | 5TpC | | | 1,2 |
| 10 | Twdt | Watch-Dog Timer Delay Time for Timeout | 4.5V | 12 | | 12 | | ms | 1 |
| | | | 5.5V | 12 | | 12 | | ms | 1 |
| 11 | Tpor | Power-On Reset Time | 4.5V | 20 | 80 | 20 | 80 | ms | 1 |
| | | | 5.5V | 20 | 80 | 20 | 80 | ms | 1 |

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)
Extended Temperature

| No | Symbol | Parameter | V _{CC} | T _A = -40 °C to +105 °C | | | | Units | Notes |
|----|--------------|--|-----------------|------------------------------------|-----|--------|-----|-------|-------|
| | | | | 8 MHz | | 12 MHz | | | |
| | | | | Min | Max | Min | Max | | |
| 1 | TpC | Input Clock Period | 4.5V | 125 | DC | 83 | DC | ns | 1 |
| | | | 5.5V | 125 | DC | 83 | DC | ns | 1 |
| 2 | TrC, TfC | Clock Input Rise and Fall Times | 4.5V | | 25 | | 15 | ns | 1 |
| | | | 5.5V | | 25 | | 15 | ns | 1 |
| 3 | TwC | Input Clock Width | 4.5V | | 62 | | 41 | ns | 1 |
| | | | 5.5V | | 62 | | 41 | ns | 1 |
| 4 | TwTinL | Timer Input Low Width | 4.5V | 70 | | 70 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 4.5V | 5TpC | | 5TpC | | | 1 |
| | | | 5.5V | 5TpC | | 5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 4.5V | 8TpC | | 8TpC | | | 1 |
| | | | 5.5V | 8TpC | | 8TpC | | | 1 |
| 7 | TrTin, TtTin | Timer Input Rise and Fall Time | 4.5V | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | ns | 1 |
| 8 | TwIL | Int. Request Input Low Time | 4.5V | 70 | | 70 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2 |
| 9 | TwIH | Int. Request Input High Time | 4.5V | 5TpC | | 5TpC | | | 1,2 |
| | | | 5.5V | 5TpC | | 5TpC | | | 1,2 |
| 10 | Twdt | Watch-Dog Timer Delay Time for Timeout | 4.5V | 10 | | 10 | | ms | 1 |
| | | | 5.5V | 10 | | 10 | | ms | 1 |
| 11 | Tpor | Power-On Reset Time | 4.5V | 12 | 100 | 12 | 100 | ms | 1 |
| | | | 5.5V | 12 | 100 | 12 | 100 | ms | 1 |

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request made through Port 3 (P33–P31).

AC ELECTRICAL CHARACTERISTICS

Low Noise Mode, Standard Temperature

| No | Symbol | Parameter | V _{CC} | T _A = 0 °C to +70 °C | | | | Units | Notes |
|----|-------------------|---|-----------------|---------------------------------|-------|--------|-----|-------|-------|
| | | | | 1 MHz | 4 MHz | Min | Max | | |
| 1 | TPC | Input Clock Period | 4.5V | 1000 | DC | 250 | DC | ns | 1 |
| | | | 5.5V | 1000 | DC | 250 | DC | ns | 1 |
| 2 | TrC TfC | Clock Input Rise and Fall Times | 4.5V | | 25 | | 25 | ns | 1 |
| | | | 5.5V | | 25 | | 25 | ns | 1 |
| 3 | TwC | Input Clock Width | 4.5V | 500 | | 125 | | ns | 1 |
| | | | 5.5V | 500 | | 125 | | ns | 1 |
| 4. | TwTinL | Timer Input Low Width | 4.5V | 70 | | 70 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 4.5V | 2.5TpC | | 2.5TpC | | | 1 |
| | | | 5.5V | 2.5TpC | | 2.5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 4.5V | 4TpC | | 4TpC | | | 1 |
| | | | 5.5V | 4TpC | | 4TpC | | | 1 |
| 7 | TrTin, TtTin | Timer Input Rise and Fall Time | 4.5V | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | ns | 1 |
| 8 | TwIL Low Time | Int. Request Input | 4.5V | 70 | | 70 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2 |
| 9 | TwIH High Time | Int. Request Input | 4.5V | 2.5TpC | | 2.5TpC | | | 1,2 |
| | | | 5.5V | 2.5TpC | | 2.5TpC | | | 1,2 |
| 10 | Twdt | Watch-Dog Timer Delay Time for Timeout | 4.5V | 12 | | 12 | | ms | 1 |
| | | | 5.5V | 12 | | 12 | | ms | 1 |

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

AC ELECTRICAL CHARACTERISTICS (Continued)

Low Noise Mode, Extended Temperature

| No | Symbol | Parameter | V _{CC} | T _A = -40 °C to +105 °C | | | | Units | Notes |
|----|-----------------|---|-----------------|------------------------------------|------|--------|-----|-------|-------|
| | | | | 1 MHz | | 4 MHz | | | |
| | | | | Min | Max | Min | Max | | |
| 1 | TPC | Input Clock Period | 4.5V | 1000 | DC | 250 | DC | ns | 1 |
| | | | 5.5V | 1000 | DC | 250 | DC | ns | 1 |
| 2 | TrC TfC | Clock Input Rise and Fall Times | 4.5V | | 25 | | 25 | ns | 1 |
| | | | 5.5V | | 25 | | 25 | ns | 1 |
| 3 | TwC | Input Clock Width | 4.5V | 500 | | 125 | | ns | 1 |
| | | | 5.5V | 500 | | 125 | | ns | 1 |
| 4 | TwTinL | Timer Input Low Width | 4.5V | 70 | | 70 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 4.5V | 2.5TpC | | 2.5TpC | | | 1 |
| | | | 5.5V | 2.5TpC | | 2.5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 4.5V | | 4TpC | 4TpC | | | 1 |
| | | | 5.5V | | 4TpC | 4TpC | | | 1 |
| 7 | TrTin, TtTin | Timer Input Rise and Fall Time | 4.5V | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | ns | 1 |
| 8 | TwIL | Int. Request Input Low Time | 4.5V | 70 | | 70 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2 |
| 9 | TwIH | Int. Request Input High Time | 4.5V | 2.5TpC | | 2.5TpC | | | 1,2 |
| | | | 5.5V | 2.5TpC | | 2.5TpC | | | 1,2 |
| 10 | Twdt | Watch-Dog Timer Delay Time for Timeout | 4.5V | 10 | | 10 | | ms | 1 |
| | | | 5.5V | 10 | | 10 | | ms | 1 |

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).

LOW NOISE VERSION

Low EMI Emission

The Z86E04/E08 can be programmed to operate in a Low EMI Emission Mode by means of a mask ROM bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz–250 ns cycle time.

- Output drivers have resistances of 500 Ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI Mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.

PIN FUNCTIONS

OTP Programming Mode

D7–D0 Data Bus. Data can be read from, or written to, the EPROM through this data bus.

V_{CC} Power Supply. It is typically 5V during EPROM Read Mode and 6.4V during the other modes (Program, Program Verify, and so on).

\overline{CE} Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

\overline{OE} Output Enable (active Low). This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

EPM EPROM Program Mode. This pin controls the different EPROM Program Modes by applying different voltages.

V_{PP} Program Voltage. This pin supplies the program voltage.

Clear Clear (active High). This pin resets the internal address counter at the High Level.

Clock Address Clock. This pin is a clock input. The internal address counter increases by one with one clock cycle.

\overline{PGM} Program Mode (active Low). A Low level at this pin programs the data to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if **excessive noise** surges above V_{CC} occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by **excessive noise** surges on the V_{PP}, \overline{CE} , EPM, \overline{OE} pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP Mode include the following:

- Using a clamping diode to V_{CC}.
- Adding a capacitor to the affected pin.

Note: Programming the EPROM/Test Mode Disable option will prevent accidental entry into EPROM Mode or Test Mode.

PIN FUNCTIONS (Continued)

XTAL1, XTAL2 *Crystal In, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (8 MHz or 12 MHz max) to the on-chip clock oscillator and buffer.

Port 0, P02–P00. Port 0 is a 3-bit bidirectional, Schmitt-triggered CMOS-compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs (Figure 7).

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. On Power-up and Reset, the Auto Latch will set the ports to an undetermined state of 0 or 1. Default condition is Auto Latches enabled.



Figure 7. Port 0 Configuration

Port 2, P27–P20. Port 2 is an 8-bit, bit programmable, bi-directional, Schmitt-triggered CMOS-compatible I/O port. These eight I/O lines can be configured under software

control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 8).

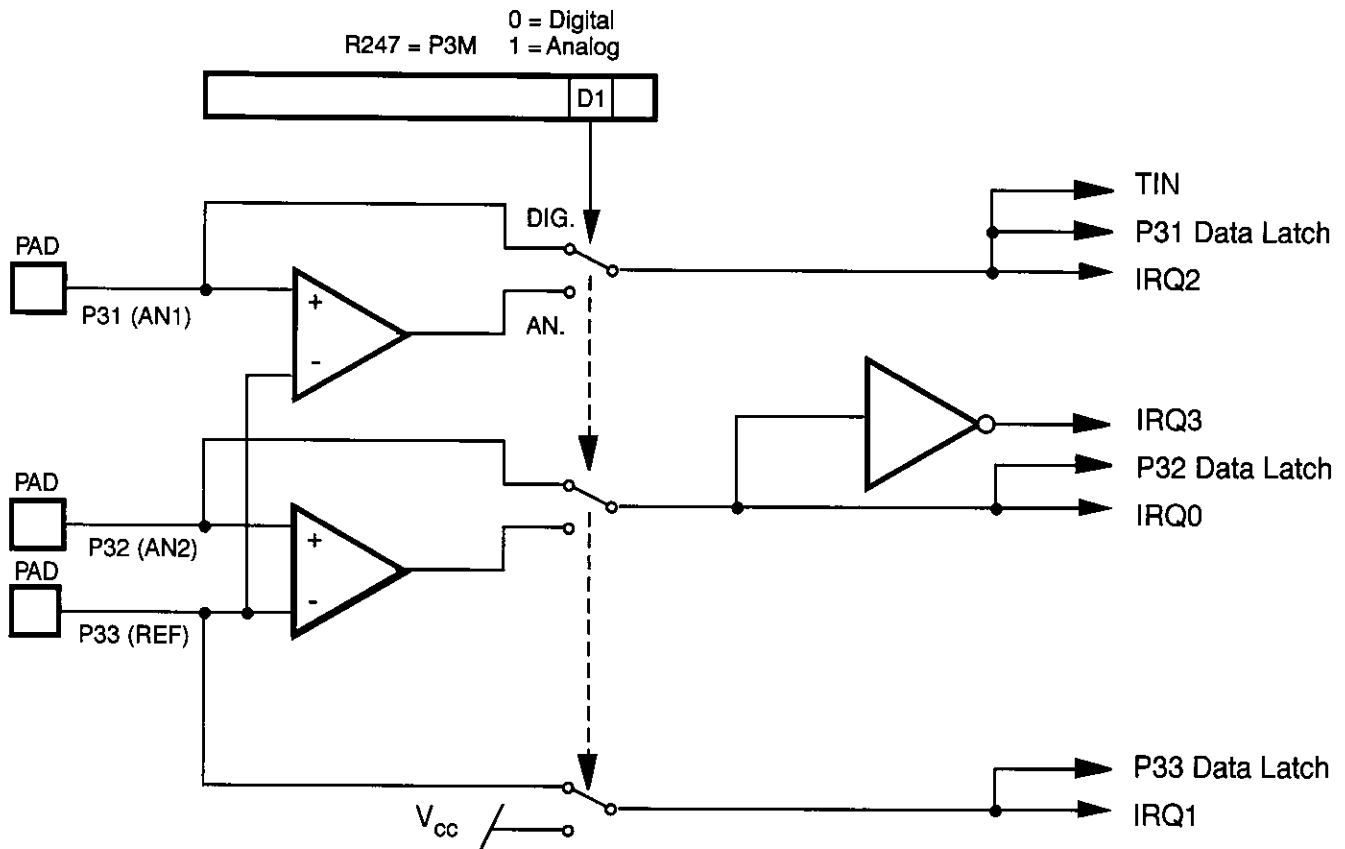
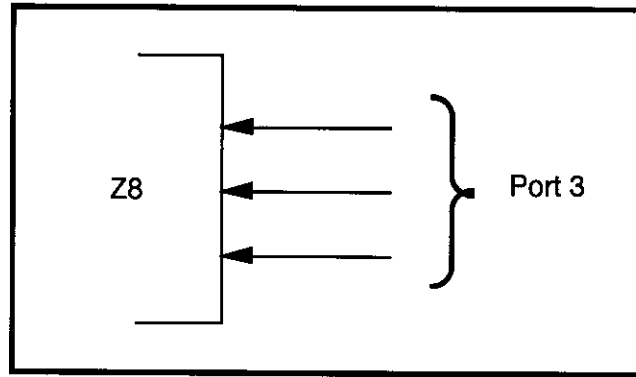


Figure 8. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3, P33–P31. Port 3 is a 3-bit, CMOS-compatible port with three fixed input (P33–P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs or analog inputs.

These three input lines are also used as the interrupt sources IRQ0–IRQ3, and as the timer input signal T_{IN} (Figure 9).



IRQ 0,1,2 = Falling Edge Detection
IRQ3 = Rising Edge Detection

Figure 9. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to input of Port 3, P31, and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In Analog Mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP

Mode. The common voltage range is 0–4 V when the V_{CC} is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z8 devices to enhance the standard Z8 core architecture to provide the user with increased design flexibility.

RESET. This function is accomplished by means of a Power-On Reset or a Watch-Dog Timer Reset. Upon power-up, the Power-On Reset circuit waits for T_{POR} ms, plus 18 clock cycles, then starts program execution at address 000C (Hex) (Figure 10). The Z8 control registers' reset value is shown in Table 3.



Figure 10. Internal Reset Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the four following conditions:

- Power-bad to power-good status
- Stop-Mode Recovery
- WDT time-out
- WDH time-out

Watch-Dog Timer Reset. The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

FUNCTIONAL DESCRIPTION (Continued)

Table 3. Control Registers

| Addr. | Reg. | Reset Condition | | | | | | | | Comments |
|-------|-------|-----------------|----|----|----|----|----|----|----|--|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| FF | SPL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| FD | RP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| FC | FLAGS | U | U | U | U | U | U | U | U | |
| FB | IMR | 0 | U | U | U | U | U | U | U | |
| FA | IRQ | U | U | 0 | 0 | 0 | 0 | 0 | 0 | IRQ3 is used for positive edge detection |
| F9 | IPR | U | U | U | U | U | U | U | U | |
| F8* | P01M | U | U | U | 0 | U | U | 0 | 1 | |
| F7* | P3M | U | U | U | U | U | U | 0 | 0 | |
| F6* | P2M | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Inputs after reset |
| F5 | PRE0 | U | U | U | U | U | U | U | 0 | |
| F4 | T0 | U | U | U | U | U | U | U | U | |
| F3 | PRE1 | U | U | U | U | U | U | 0 | 0 | |
| F2 | T1 | U | U | U | U | U | U | U | U | |
| F1 | TMR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Note: *Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 4 and the user must avoid bus contention on the port pins or it may affect device reliability.

Program Memory. The Z86E04/E08 addresses up to 1K/2KB of Internal Program Memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0–1024/2048 are on-chip one-time programmable ROM.

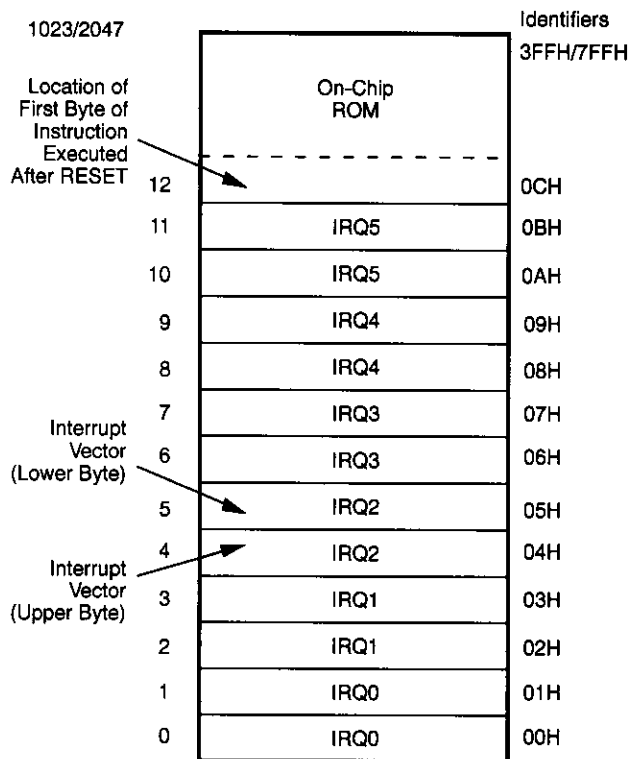


Figure 11. Program Memory Map

Register File. The Register File consists of three I/O port registers, 124 general-purpose registers, and 14 control and status registers R0–R3, R4–R127 and R241–R255, respectively (Figure 12). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8.

| Location | Identifiers |
|-----------|---------------------------|
| 255 (FFH) | SPL |
| 254 (FE) | GPR |
| 253 (FD) | RP |
| 252 (FC) | FLAGS |
| 251 (FB) | IMR |
| 250 (FA) | IRQ |
| 249 (F9) | IPR |
| 248 (F8) | P01M |
| 247 (F7) | P3M |
| 246 (F6) | P2M |
| 245 (F5) | PRE0 |
| 244 (F4) | T0 |
| 243 (F3) | PRE1 |
| 242 (F2) | T1 |
| 241 (F1H) | TMR |
| | Not Implemented |
| 128 | |
| 127 (7FH) | General-Purpose Registers |
| 4 | |
| 3 | P3 |
| 2 | P2 |
| 1 | P1 |
| 0 (00H) | P0 |

Figure 12. Register File

FUNCTIONAL DESCRIPTION (Continued)

The Z8 instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer.

In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 13) addresses the starting location of the active working-register group.



Figure 13. Register Pointer

Stack Pointer. The Z8 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register and is set to 00 Hex after any reset or Stop-Mode Recovery.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 can be driven by the internal clock source only (Figure 14).

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (Single-Pass Mode) or to automatically reload the initial value and continue counting (Modulo-N Continuous Mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.



* Note: By passed, if Low EMI Mode is selected.

Figure 14. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z8 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 15). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Note: User must select any Z86E08 mode in Zilog's C12 ICEBOX™ emulator. The rising edge interrupt is not supported on the CCP emulator (a hardware/software workaround must be employed).

Table 4. Interrupt Types, Sources, and Vectors

| Name | Source | Vector Location | Comments |
|------|----------|-----------------|------------------|
| IRQ0 | AN2(P32) | 0,1 | External (F)Edge |
| IRQ1 | REF(P33) | 2,3 | External (F)Edge |
| IRQ2 | AN1(P31) | 4,5 | External (F)Edge |
| IRQ3 | AN2(P32) | 6,7 | External (R)Edge |
| IRQ4 | T0 | 8,9 | Internal |
| IRQ5 | T1 | 10,11 | Internal |

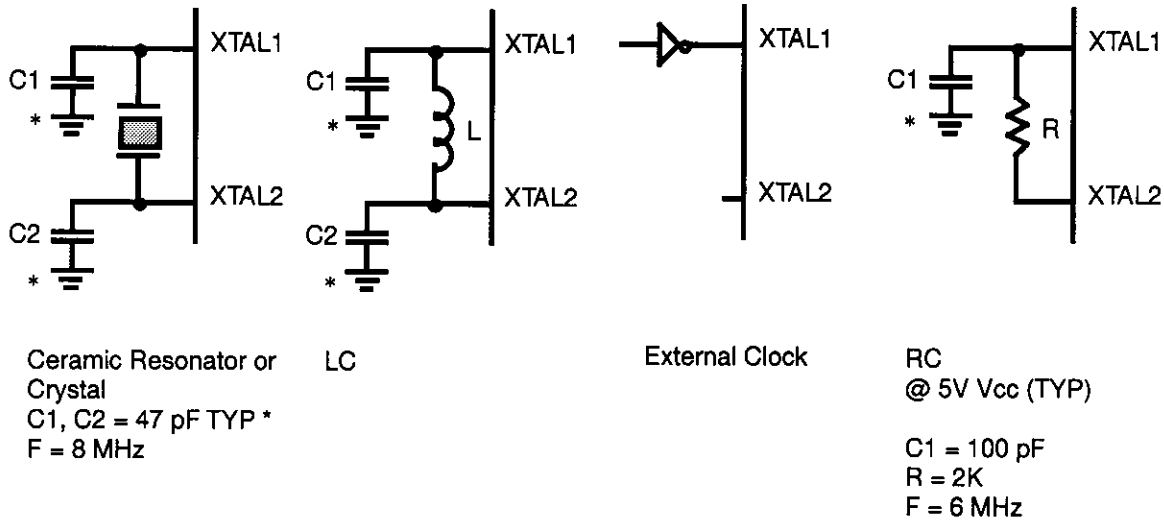
Notes:
F = Falling edge triggered
R = Rising edge triggered



Figure 15. Interrupt Block Diagram

Clock. The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT cut, up to 12 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendors crystal recommended capacitors from each pin directly to device ground pin 14 (Figure 16). Note that the crystal capacitor loads should be connected to V_{SS}, Pin 14 to reduce Ground noise injection.



* Typical value including pin parasitics

Figure 16. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Table 5. Typical Frequency vs. RC Values
 $V_{CC} = 5.0V @ 25^{\circ}C$

| Resistor (R) | Load Capacitor | | | | | | | |
|--------------|----------------|-------|--------|-------|---------|-------|-----------------|-------|
| | 33 pFd | | 56 pFd | | 100 pFd | | 0.00 1 μ Fd | |
| | A(Hz) | B(Hz) | A(Hz) | B(Hz) | A(Hz) | B(Hz) | A(Hz) | B(Hz) |
| 1.0M | 33K | 31K | 20K | 20K | 12K | 11K | 1.4K | 1.4K |
| 560K | 56K | 52K | 34K | 32K | 20K | 19K | 2.5K | 2.4K |
| 220K | 144K | 130K | 84K | 78K | 48K | 45K | 6K | 6K |
| 100K | 315K | 270K | 182K | 164K | 100K | 95K | 12K | 12K |
| 56K | 552K | 480K | 330K | 300K | 185K | 170K | 23K | 22K |
| 20K | 1.4M | 1M | 884K | 740K | 500K | 450K | 65K | 61K |
| 10K | 2.6M | 2M | 1.6M | 1.3M | 980K | 820K | 130K | 123K |
| 5K | 4.4M | 3M | 2.8M | 2M | 1.7K | 1.3M | 245K | 225K |
| 2K | 8M | 5M | 6M | 4M | 3.8K | 2.7M | 600K | 536K |
| 1K | 12M | 7M | 8.8M | 6M | 6.3K | 4.2M | 1.0M | 950K |

Notes:

A = STD Mode Frequency.

B = Low EMI Mode Frequency.

Table 6. Typical Frequency vs. RC Values
 $V_{CC} = 3.3V @ 25^{\circ}C$

| Resistor (R) | Load Capacitor | | | | | | | |
|--------------|----------------|-------|--------|-------|---------|-------|-----------------|-------|
| | 33 pFd | | 56 pFd | | 100 pFd | | 0.00 1 μ Fd | |
| | A(Hz) | B(Hz) | A(Hz) | B(Hz) | A(Hz) | B(Hz) | A(Hz) | B(Hz) |
| 1.0M | 18K | 18K | 12K | 12K | 7.4K | 7.7K | 1K | 1K |
| 560K | 30K | 30K | 20K | 20K | 12K | 12K | 1.6K | 1.6K |
| 220K | 70K | 70K | 47K | 47K | 30K | 30K | 4K | 4K |
| 100K | 150K | 148K | 97K | 96K | 60K | 60K | 8K | 8K |
| 56K | 268K | 250K | 176K | 170K | 100K | 100K | 15K | 15K |
| 20K | 690M | 600K | 463K | 416K | 286K | 266K | 40K | 40K |
| 10K | 1.2M | 1M | 860K | 730K | 540K | 480K | 80K | 76K |
| 5K | 2M | 1.7M | 1.5M | 1.2M | 950K | 820K | 151K | 138K |
| 2K | 4.6M | 3M | 3.3M | 2.4M | 2.2M | 1.6M | 360K | 316K |
| 1K | 7M | 4.6M | 5M | 3.6M | 3.6K | 2.6M | 660K | 565K |

Notes:

A = STD Mode Frequency.

B = Low EMI Mode Frequency.

HALT Mode. This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

Note: On the C12 ICEBOX, the IRQ3 does not wake the device out of HALT Mode.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 μ A. The STOP Mode is released by a RESET through a Stop-Mode Recovery (pin P27). A Low input condition on P27 releases the STOP Mode. Program execution begins at location 000C(Hex). However, when P27 is used to release the STOP Mode, the I/O port Mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP Mode, use the following instruction:

```
LD          P2M, #1XXX XXXXB
NOP
STOP
```

X = Dependent on user's application.

Note: A low level detected on P27 pin will take the device out of STOP Mode even if configured as an output.

In order to enter STOP or HALT Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate SLEEP instruction, such as:

```
FF      NOP      ; clear the pipeline
6F      STOP     ; enter STOP Mode
        or
FF      NOP      ; clear the pipeline
7F      HALT     ; enter HALT Mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 Twdt period; otherwise, the controller resets itself. The WDT instruction affects the flags accordingly; Z=1, S=0, V=0.

WDT = 5F (Hex)

Opcode WDT (5FH). The first time Opcode 5FH is executed, the WDT is enabled and subsequent execution clears the WDT counter. This must be done at least every T_{WDT} ; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of T_{POR} , plus 18 XTAL clock cycles. The software enabled WDT does not run in STOP Mode.

Opcode WDH (4FH). When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT running during HALT Mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Permanent WDT. Selecting the hardware enabled Permanent WDT option, will automatically enable the WDT upon exiting reset. The permanent WDT will always run in HALT Mode and STOP Mode, and it cannot be disabled.

Auto Reset Voltage (V_{LV}). The Z8 has an auto-reset built-in. The auto-reset circuit resets the Z8 when it detects the V_{CC} below V_{LV} .

Figure 17 shows the Auto Reset Voltage versus temperature. If the V_{CC} drops below the VCC operating voltage range, the Z8 will function down to the V_{LV} unless the internal clock frequency is higher than the specified maximum V_{LV} frequency.

FUNCTIONAL DESCRIPTION (Continued)



Figure 17. Typical Auto Reset Voltage (V_{LV}) vs. Temperature

Low EMI Emission

The Z8 can be programmed to operate in a low EMI Emission (Low Noise) Mode by means of an EPROM programmable bit option. Use of this feature results in:

- Less than 1 mA consumed during HALT Mode.
- All drivers slew rates reduced to 10 ns (typical).
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz–250 ns cycle time.
- Output drivers have resistances of 500 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

In addition to V_{DD} and GND (V_{SS}), the Z8 changes all its pin functions in the EPROM Mode. XTAL2 has no function, XTAL1 functions as \overline{CE} , P31 functions as \overline{OE} , P32 functions as EPM, P33 functions as V_{PP} , and P02 functions as \overline{PGM} .

ROM Protect. ROM Protect fully protects the Z8 ROM code from being read externally. When ROM Protect is selected, the instructions LDC and LDCI are supported (Z86E04/E08 and Z86C04/C08 do not support the instructions of LDE and LDEI). When the device is programmed for ROM Protect, the Low Noise feature will not automatically be enabled.

Please note that when using the device in a noisy environment, it is suggested that the voltages on the EPM and \overline{CE} pins be clamped to V_{CC} through a diode to V_{CC} to prevent accidentally entering the OTP Mode. The V_{PP} requires both a diode and a 100 pF capacitor.

Auto Latch Disable. Auto Latch Disable option bit when programmed will globally disable all Auto Latches.

WDT Enable. The WDT Enable option bit, when programmed, will have the hardware enabled Permanent WDT enabled after exiting reset and can not be stopped in Halt or Stop Mode.

EPROM/Test Mode Disable. The EPROM/Test Mode Disable option bit, when programmed, will disable the EPROM Mode and the Factory Test Mode. Reading, verifying, and programming the Z8 will be disabled. To fully verify that this mode is disabled, the device must be power cycled.

User Modes. Table 7 shows the programming voltage of each mode.

Table 7. OTP Programming Table

| Programming Modes | V_{PP} | EPM | \overline{CE} | \overline{OE} | \overline{PGM} | ADDR | DATA | V_{CC}^* |
|--------------------|----------|----------|-----------------|-----------------|------------------|------|------|------------|
| EPROM READ | NU | V_H | V_{IL} | V_{IL} | V_{IH} | ADDR | Out | 5.0V |
| PROGRAM | V_H | V_{IH} | V_{IL} | V_{IH} | V_{IL} | ADDR | In | 6.4V |
| PROGRAM VERIFY | V_H | V_{IH} | V_{IL} | V_{IL} | V_{IH} | ADDR | Out | 6.4V |
| EPROM PROTECT | V_H | V_H | V_H | V_{IH} | V_{IL} | NU | NU | 6.4V |
| LOW NOISE SELECT | V_H | V_{IH} | V_H | V_{IH} | V_{IL} | NU | NU | 6.4V |
| AUTO LATCH DISABLE | V_H | V_{IH} | V_H | V_{IL} | V_{IL} | NU | NU | 6.4V |
| WDT ENABLE | V_H | V_{IL} | V_H | V_{IH} | V_{IL} | NU | NU | 6.4V |
| EPROM/TEST MODE | V_H | V_{IL} | V_H | V_{IL} | V_{IL} | NU | NU | 6.4V |

Notes:

1. $V_H = 12.75V \pm 0.25 V_{DC}$.
2. V_{IH} = As per specific Z8 DC specification.
3. V_{IL} = As per specific Z8 DC specification.
4. X = Not used, but must be set to V_H or V_{IH} level.
5. NU = Not used, but must be set to either V_{IH} or V_{IL} level.
6. I_{PP} during programming = 40 mA maximum.
7. I_{CC} during programming, verify, or read = 40 mA maximum.
8. * V_{CC} has a tolerance of $\pm 0.25V$.

FUNCTIONAL DESCRIPTION (Continued)

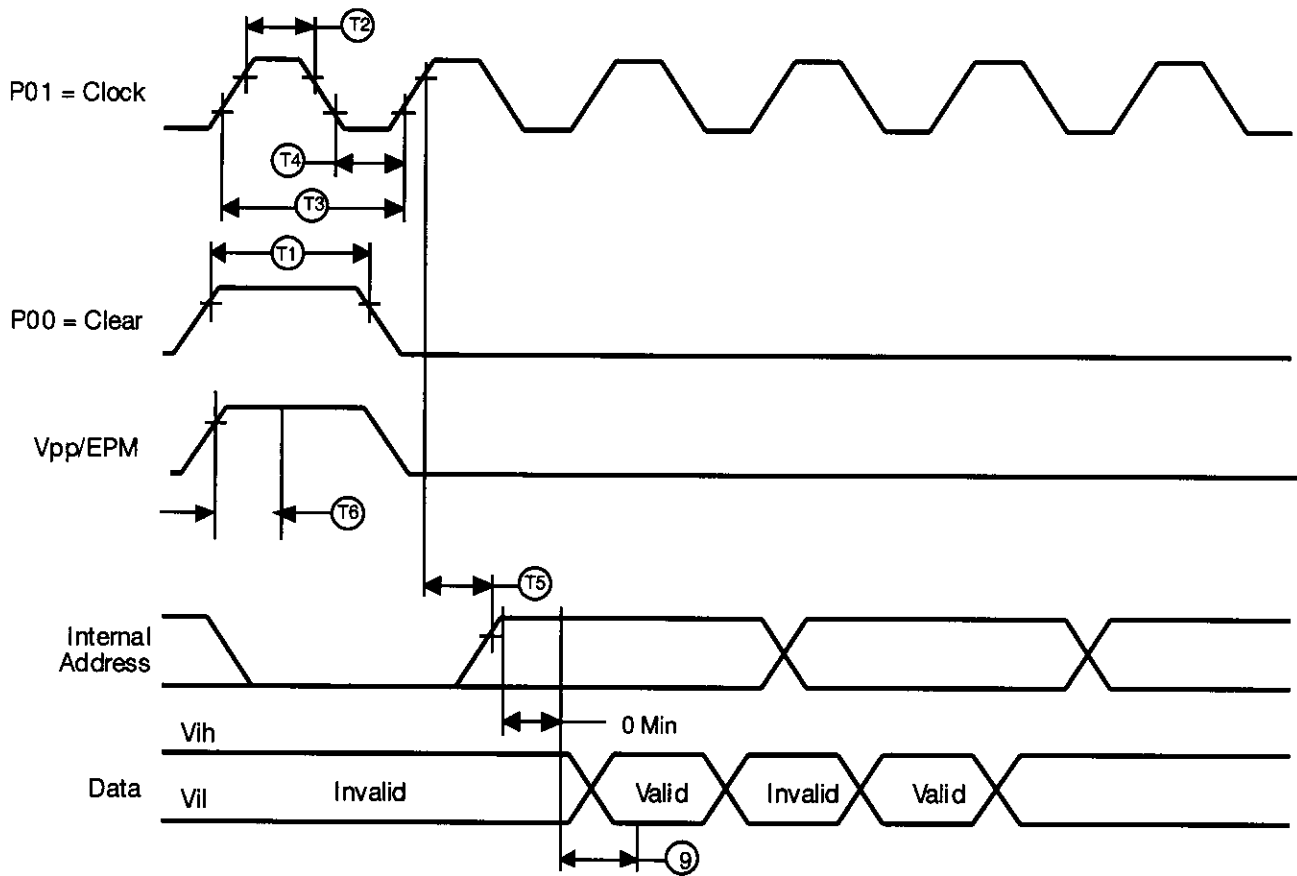
Internal Address Counter. The address of Z8 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 18 shows the setup time of the serial address input.

Programming Waveform. Figures 19, 20, 21 and 22 show the programming waveforms of each mode. Table 8 shows the timing of programming waveforms.

Programming Algorithm. Figure 23 shows the flow chart of the Z8 programming algorithm.

Table 8. Timing of Programming Waveforms

| Parameters | Name | Min | Max | Units |
|------------|----------------------------|------|-----|---------|
| 1 | Address Setup Time | 2 | | μ s |
| 2 | Data Setup Time | 2 | | μ s |
| 3 | V _{pp} Setup | 2 | | μ s |
| 4 | V _{cc} Setup Time | 2 | | μ s |
| 5 | Chip Enable Setup Time | 2 | | μ s |
| 6 | Program Pulse Width | 0.95 | | ms |
| 7 | Data Hold Time | 2 | | μ s |
| 8 | OE Setup Time | 2 | | μ s |
| 9 | Data Access Time | 188 | | ns |
| 10 | Data Output Float Time | | 100 | ns |
| 11 | Overprogram Pulse Width | 2.85 | | ms |
| 12 | EPM Setup Time | 2 | | μ s |
| 13 | PGM Setup Time | 2 | | μ s |
| 14 | Address to OE Setup Time | 2 | | μ s |
| 15 | Option Program Pulse Width | 78 | | ms |
| 16 | OE Width | 250 | | ns |
| 17 | Address Valid to OE Low | 125 | | ns |



| Legend: | |
|---------------------------------------|----------------|
| T1 Reset Clock Width | 30 ns Min |
| T2 Input Clock High | 100 ns Min |
| T3 Input Clock Period | 200 ns Min |
| T4 Input Clock Low | 100 ns Min |
| T5 Clock to Address Counter Out Delay | 15 ns Max |
| T6 Epm/Vpp Set up Time | 40 μ s Min |

Figure 18. Z86E04/E08 Address Counter Waveform

FUNCTIONAL DESCRIPTION (Continued)

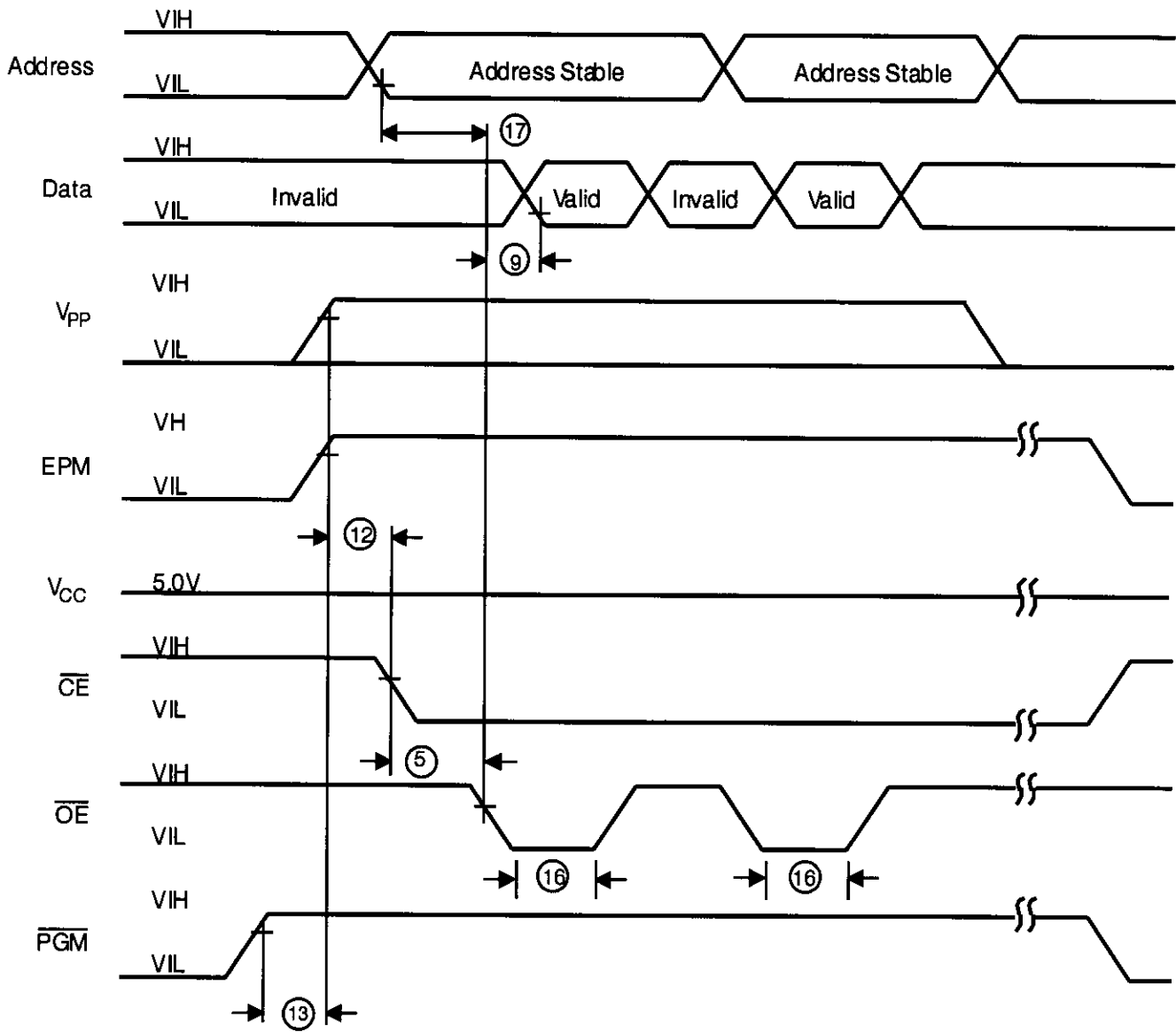


Figure 19. Z86E04/E08 Programming Waveform
(EPROM Read)

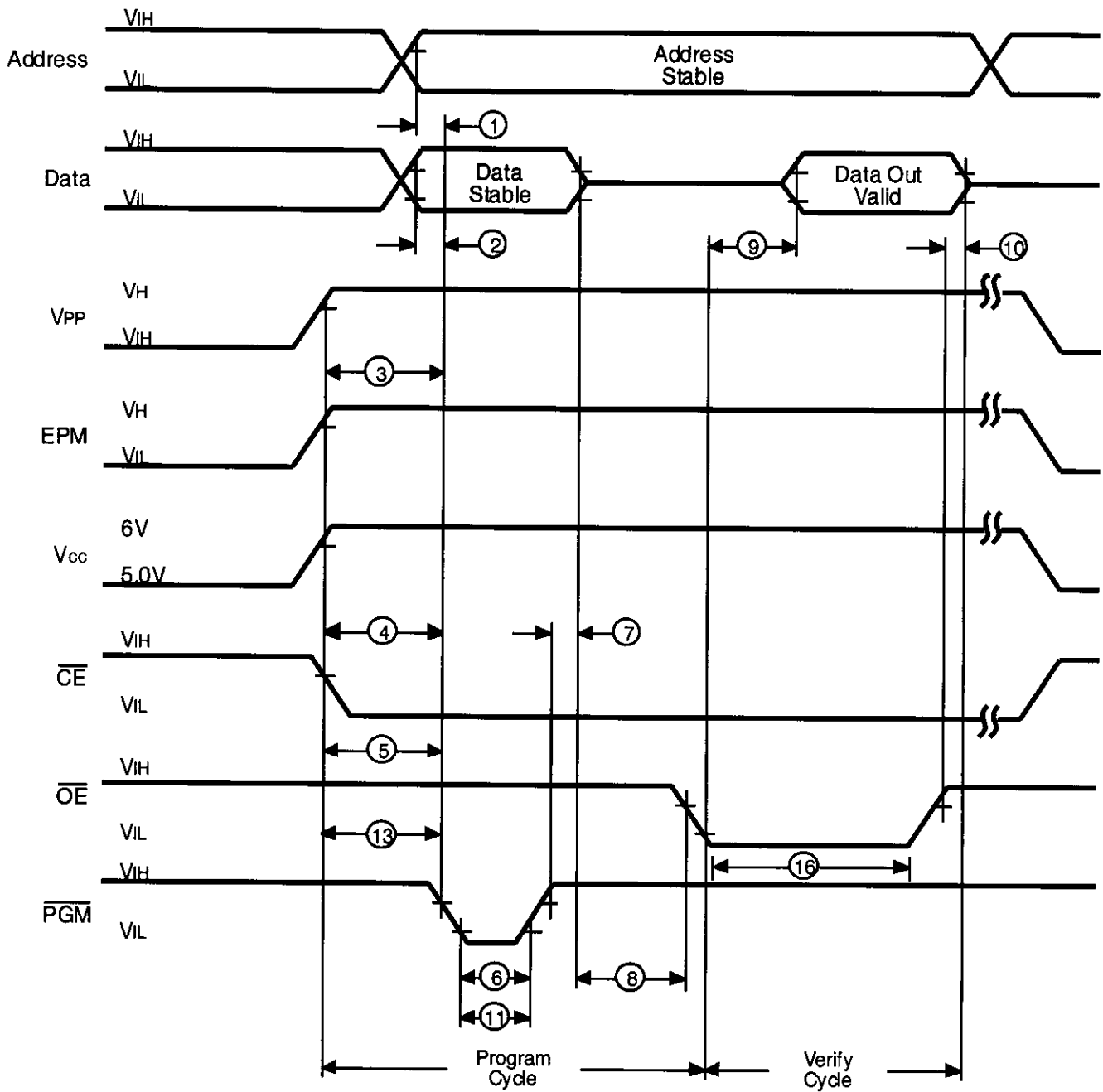


Figure 20. Z86E04/E08 Programming Waveform
(Program and Verify)

FUNCTIONAL DESCRIPTION (Continued)



Figure 21. Z86E04/E08 Programming Options Waveform (EPROM Protect and Low Noise Program)



**Figure 22. Z86E04/E08 Programming Options Waveform
(Auto Latch Disable, Permanent WDT Enable and
EPROM/Test Mode Disable)**

FUNCTIONAL DESCRIPTION (Continued)

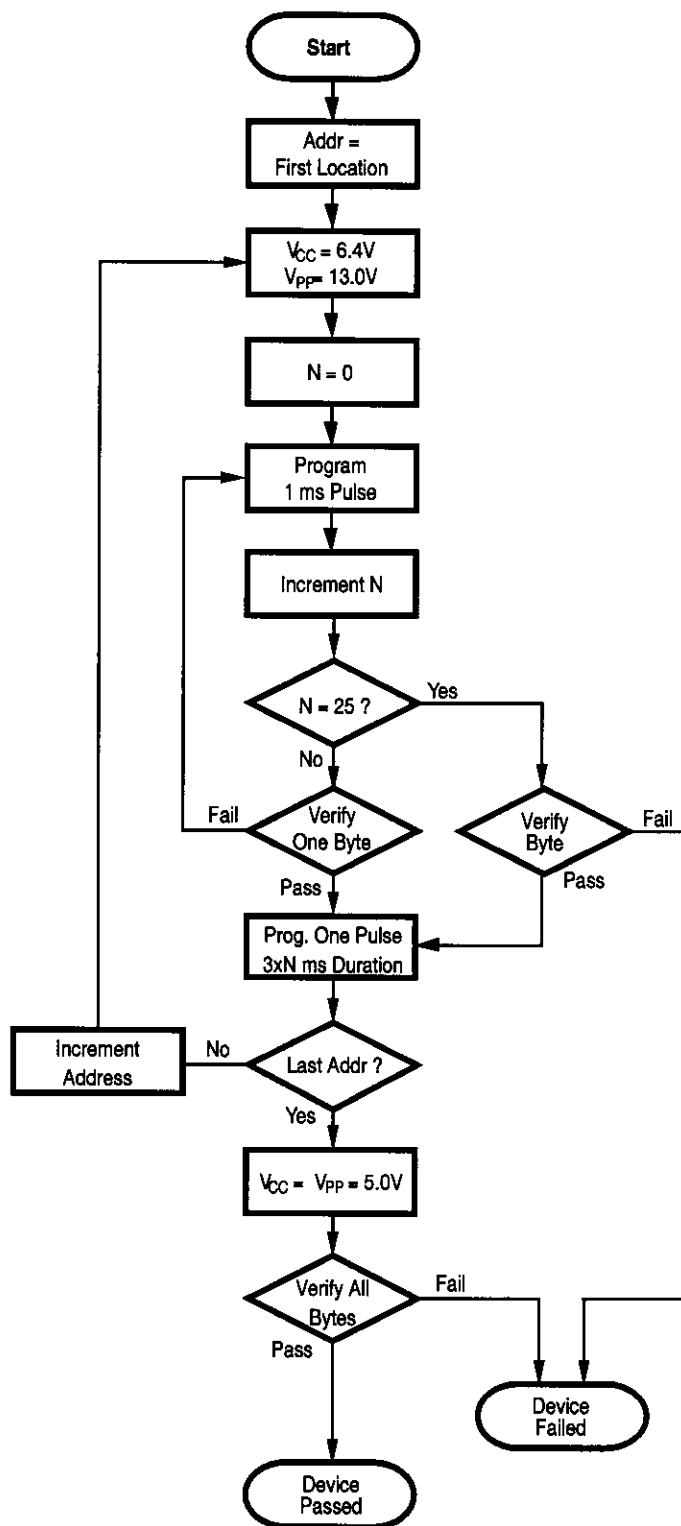


Figure 23. Z86E04/E08 Programming Algorithm

Z8 CONTROL REGISTERS

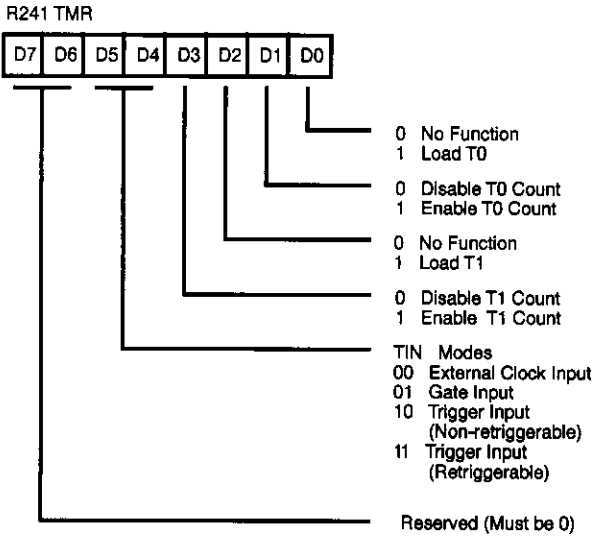


Figure 24. Timer Mode Register (F1_H: Read/Write)

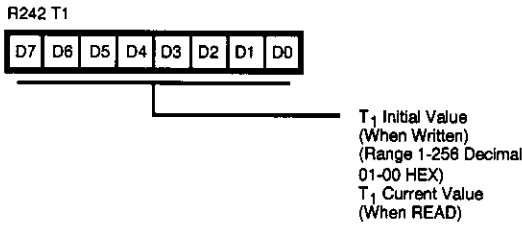


Figure 25. Counter Timer 1 Register (F2_H: Read/Write)



Figure 26. Prescaler 1 Register (F3_H: Write Only)



Figure 27. Counter/Timer 0 Register (F4_H: Read/Write)

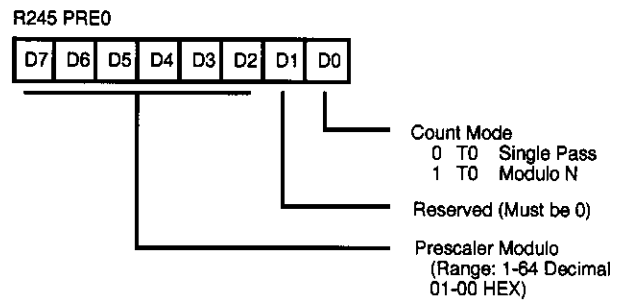


Figure 28. Prescaler 0 Register (F5_H: Write Only)

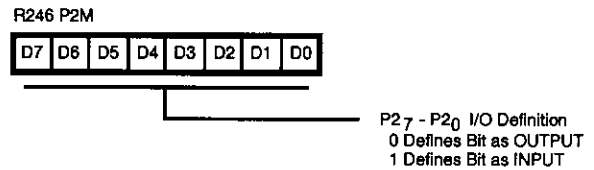


Figure 29. Port 2 Mode Register (F6_H: Write Only)

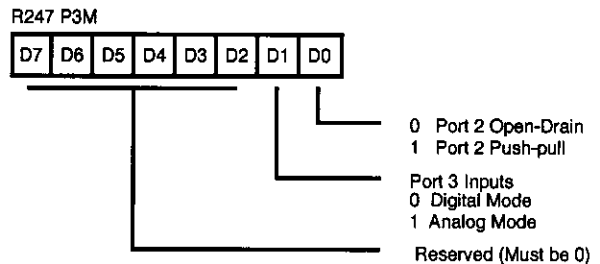


Figure 30. Port 3 Mode Register (F7_H: Write Only)

Z8 CONTROL REGISTERS (Continued)



Figure 31. Port 0 and 1 Mode Register (F8_H: Write Only)



Figure 34. Interrupt Mask Register (FB_H: Read/Write)

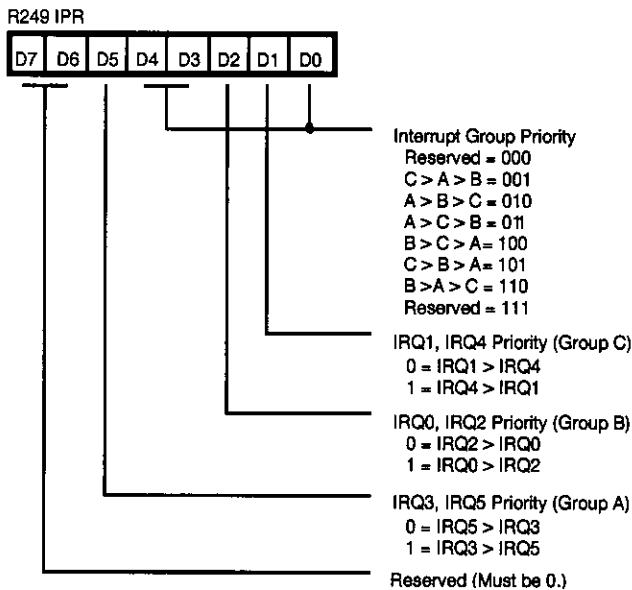


Figure 32. Interrupt Priority Register (F9_H: Write Only)



Figure 35. Flag Register (FC_H: Read/Write)



Figure 36. Register Pointer (FD_H: Read/Write)

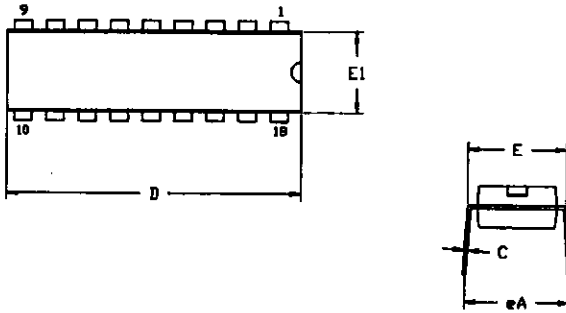


Figure 33. Interrupt Request Register (FA_H: Read/Write)

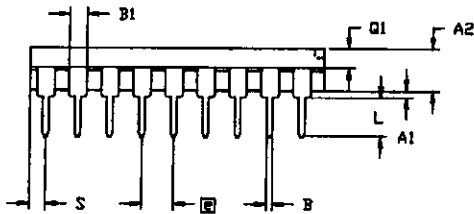


Figure 37. Stack Pointer (FF_H: Read/Write)

PACKAGE INFORMATION

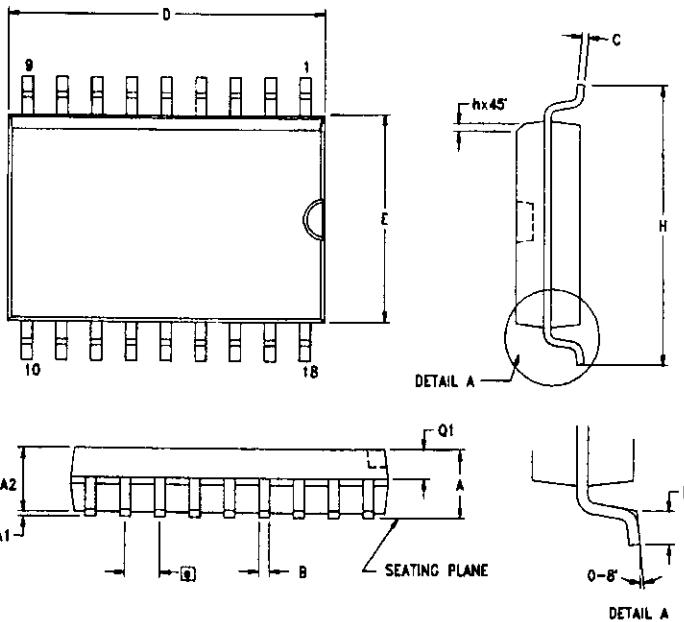


| SYMBOL | MILLIMETER | | INCH | |
|--------|------------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| A1 | 0.51 | 0.81 | .020 | .032 |
| A2 | 3.25 | 3.43 | .128 | .135 |
| B | 0.38 | 0.53 | .015 | .021 |
| B1 | 1.14 | 1.65 | .045 | .065 |
| C | 0.23 | 0.38 | .009 | .015 |
| D | 22.35 | 23.37 | .880 | .920 |
| E | 7.62 | 8.13 | .300 | .320 |
| E1 | 6.22 | 6.48 | .245 | .255 |
| □ | 2.54 TYP | | .100 TYP | |
| eA | 7.87 | 8.89 | .310 | .350 |
| L | 3.18 | 3.81 | .125 | .150 |
| Q1 | 1.52 | 1.65 | .060 | .065 |
| S | 0.89 | 1.65 | .035 | .065 |



CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram



| SYMBOL | MILLIMETER | | INCH | |
|--------|------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.40 | 2.65 | 0.094 | 0.104 |
| A1 | 0.10 | 0.30 | 0.004 | 0.012 |
| A2 | 2.24 | 2.44 | 0.088 | 0.096 |
| B | 0.36 | 0.46 | 0.014 | 0.018 |
| C | 0.23 | 0.30 | 0.009 | 0.012 |
| D | 11.40 | 11.75 | 0.449 | 0.463 |
| E | 7.40 | 7.60 | 0.291 | 0.299 |
| □ | 1.27 TYP | | 0.050 TYP | |
| H | 10.00 | 10.65 | 0.394 | 0.419 |
| h | 0.30 | 0.50 | 0.012 | 0.020 |
| L | 0.60 | 1.00 | 0.024 | 0.039 |
| Q1 | 0.97 | 1.07 | 0.038 | 0.042 |

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86E04

Standard Temperature

| 18-Pin DIP | 18-Pin SOIC |
|-------------|-------------|
| Z86E0412PSC | Z86E0412SSC |
| Z86E0412PEC | Z86E0412SEC |

Z86E08

Standard Temperature

| 18-Pin DIP | 18-Pin SOIC |
|-------------|-------------|
| Z86E0812PSC | Z86E0812SSC |
| Z86E0812PEC | Z86E0812SEC |

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

Codes

Preferred Package

P = Plastic DIP

Longer Lead Time

S = SOIC

Preferred Temperature

S = 0°C to +70°C

E = -40°C to +105°C

Speeds

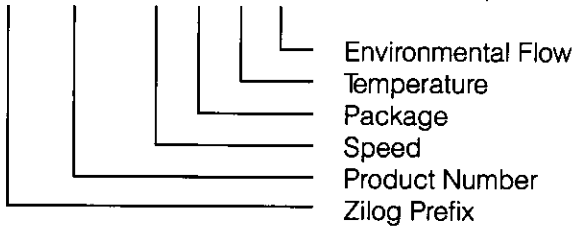
12 = 12 MHz

Environmental

C = Plastic Standard

Example:

Z 86E04 12 P S C is a Z86E04, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



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Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
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Телефон: 8 (812) 309-75-97 (многоканальный)

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Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А