

# MAX16997/MAX16998

# High-Voltage Watchdog Timers with Adjustable Timeout Delay

## General Description

The MAX16997/MAX16998 are microprocessor ( $\mu$ P) supervisory circuits for high-input-voltage and low-quiescent-current applications. These devices detect downstream circuit failures and provide switchover to redundant circuitry. See the *Selector Guide* for the different versions of this product family.

The MAX16997/MAX16998 family has four independent inputs for reset and watchdog functions. SWT and SRT inputs independently set the timeout periods of watchdog and reset timers through external capacitors. RESETIN/EN monitor voltages at respective inputs. A resistive voltage-divider sets the reset threshold.

The MAX16998A/B/D generate two output signals,  $\overline{\text{RESET}}$  and  $\overline{\text{ENABLE}}$ .  $\overline{\text{RESET}}$  asserts whenever RESETIN drops below its threshold voltage or when the watchdog timer detects a timing fault at WDI. Once asserted, and after all reset conditions are removed,  $\overline{\text{RESET}}$  remains low for the reset timeout period,  $t_{\text{RESET}}$ , and then goes high. The MAX16997A generates one output signal ( $\overline{\text{ENABLE}}$ ) based on the voltage level at EN and the signal at WDI.

The MAX16997A does not have a  $\overline{\text{RESET}}$  output. The watchdog is disabled if the voltage at EN is below its threshold. The MAX16997A watchdog timer starts timing when the voltage at EN becomes higher than the preset threshold voltage level. Each time EN rises above the preset threshold voltage, the initial watchdog timeout period is 8 times the normal watchdog timeout period ( $t_{\text{WP}}$ ).

The MAX16997/MAX16998 are available in 8-pin lead(Pb)-free  $\mu$ MAX<sup>®</sup> packages and are fully specified over the  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  automotive temperature range.

## Applications

- Automotive
- Industrial

## Selector Guide

PART	WATCHDOG WINDOW SIZE (%)	$\overline{\text{ENABLE}}$	$\overline{\text{RESET}}$	EN	RESETIN
MAX16997A	100	✓	—	✓	—
MAX16998A	100	✓	✓	—	✓
MAX16998B	50	✓	✓	—	✓
MAX16998D	75	✓	✓	—	✓

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## Features

- Wide 5V to 40V Input Voltage Range
- 18 $\mu$ A Quiescent Current (Typical at  $+125^{\circ}\text{C}$ )
- Capacitor-Adjustable Timeout Period for Watchdog and Reset
- Windowed Watchdog Timer Options (MAX16998B/D)
- External Voltage Monitoring (RESETIN for the MAX16998A/B/D and EN for the MAX16997A)
- Car Battery-Compatible EN Input
- TTL- and CMOS-Compatible Open-Drain Outputs
- 18V Maximum Open-Drain Reset Output Voltage
- 28V Maximum Open-Drain Enable Output Voltage
- Power-On/Power-Off Reset Functionality (MAX16998A/B/D Only)
- AEC-Q100 Qualified
- $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Operating Temperature Range
- Small (3mm x 3mm)  $\mu$ MAX Package
- WDI Narrow Pulse Immunity

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16997AAUA+	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	8 $\mu$ MAX
MAX16998AAUA+	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	8 $\mu$ MAX
MAX16998AAUA/V+	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	8 $\mu$ MAX
MAX16998BAUA+	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	8 $\mu$ MAX
MAX16998BAUA/V+	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	8 $\mu$ MAX
MAX16998DAUA+	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	8 $\mu$ MAX
MAX16998DAUA/V+	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	8 $\mu$ MAX

+Denotes a lead(Pb)-free/RoHS-compliant package.  
/V denotes an automotive qualified part.

*Pin Configurations* appear at end of data sheet.



**Absolute Maximum Ratings**

(All pins referenced to GND, unless otherwise noted.)

IN, ENABLE.....	-0.3V to +45V
WDI, RESET, EN.....	-0.3V to +20V
RESETIN.....	-0.3V to +20V
SRT, SWT.....	-0.3V to +12V
Maximum Current (all pins).....	30mA

Continuous Power Dissipation (T<sub>A</sub> = +70°C)

8-Pin μMAX (derate 4.8mW/°C above +70°C).....	387.8mW
Operating Temperature Range (T <sub>A</sub> ).....	-40°C to +125°C
Junction Temperature (T <sub>J</sub> ).....	+150°C
Storage Temperature Range.....	-65°C to +150°C
Lead Temperature (soldering, 10s).....	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Package Thermal Characteristics (Note 1)**

Junction-to-Case Thermal Resistance (θ <sub>JC</sub> .....)	42°C/W
Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ).....	206.3°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

**Electrical Characteristics**

(V<sub>IN</sub> = 14V, T<sub>A</sub> = T<sub>J</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V <sub>IN</sub>		5.0		40.0	V
Supply Current	I <sub>IN</sub>	T <sub>A</sub> = -40°C to +85°C		18	30	μA
		T <sub>A</sub> = -40°C to +125°C		18	60	
SWT Ramp Current	I <sub>RAMP_SWT</sub>	V <sub>SWT</sub> = 1.0V	450	500	550	nA
SRT Ramp Current	I <sub>RAMP_SRT</sub>	V <sub>SRT</sub> = 1.0V	410	500	600	nA
SWT/SRT Ramp Threshold Voltage	V <sub>RAMP</sub>		1.115	1.235	1.363	V
<b>RESET TIMER</b>						
Power-On Reset Input Threshold Voltage	V <sub>PON</sub>	V <sub>RESETIN</sub> rising	1.135	1.255	1.383	V
		V <sub>RESETIN</sub> falling	1.115	1.235	1.363	
RESETIN Input Leakage Current	I <sub>LPON</sub>	V <sub>RESETIN</sub> = 2V		0.1		μA
RESET Output Low Voltage	V <sub>OLRST</sub>	RESET asserted, I <sub>SINK</sub> = 1mA			0.9	V
		V <sub>IN</sub> = 1.1V, I <sub>SINK</sub> = 160μA, RESET asserted			0.4	
		RESET asserted, I <sub>SINK</sub> = 0.4mA			0.4	
RESET Leakage Current	I <sub>LKGR</sub>	V <sub>RESET</sub> = 20V, RESET not asserted		0.1		μA
ENABLE Output Low Voltage	V <sub>OLEN</sub>	ENABLE asserted, I <sub>SINK</sub> = 5mA			0.4	V
ENABLE Leakage Current	I <sub>LKGE</sub>	V <sub>ENABLE</sub> = 14V, ENABLE not asserted		0.1		μA
Minimum Reset Timeout Period	t <sub>RESETmin</sub>	C <sub>SRT</sub> = 390pF (Note 3)		1		ms
Reset Timeout Period	t <sub>RESET</sub>	C <sub>SRT</sub> = 2000pF (Note 3)		5		ms
Maximum Reset Time Period	t <sub>RESETmax</sub>	C <sub>SRT</sub> = 47nF		116.09		ms
RESET to ENABLE Delay	t <sub>REDL</sub>			1.5		μs
RESETIN to RESET Delay	t <sub>RRDL</sub>	RESETIN falling below V <sub>PON</sub> to RESET falling edge		1		μs

Electrical Characteristics (continued)

( $V_{IN} = 14V$ ,  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>WATCHDOG TIMER</b>						
WDI Input Threshold	$V_{IH}$		2.25			V
	$V_{IL}$				0.9	
WDI Input Hysteresis	$WDI_{HYST}$			200		mV
WDI Minimum Pulse Width	$t_{WDImin}$	(Note 4)	6.5			$\mu s$
WDI Input Current	$I_{WDI}$	WDI = 0 or 14V		0.1		$\mu A$
Minimum Watchdog Timeout Period	$t_{WPmin}$	$C_{SWT} = 680pF$ (Note 3)		6.8		ms
Watchdog Timeout Period	$t_{WP}$	$C_{SWT} = 1200pF$ (Note 3)		12		ms
Maximum Watchdog Timeout	$t_{WPmax}$	$C_{SWT} = 22nF$		217.36		ms
Watchdog Window	$D_{WDI}$	MAX16998B	45	50	55	% $t_{WP}$
		MAX16998D	67.5	75	82.5	
WDI to $\overline{ENABLE}$ Output Delay		Start from WDI third wrong trigger		100		$\mu s$
$\overline{RESET}$ Pullup Resistor Supply Voltage		(Note 5)	2.25	2.5	18.00	V
$\overline{ENABLE}$ Pullup Resistor Supply Voltage		(Note 5)	2.25	2.5	28.00	V

**Note 2:**  $R_{\overline{RESET}}$  and  $R_{\overline{ENABLE}}$  are external pullup resistors for open-drain outputs. Connect  $R_{\overline{RESET}}$  and  $R_{\overline{ENABLE}}$  to a minimum 2.5V voltage. Connect  $R_{\overline{RESET}}$  to a maximum voltage of 18V and connect  $R_{\overline{ENABLE}}$  to a maximum voltage of 28V.

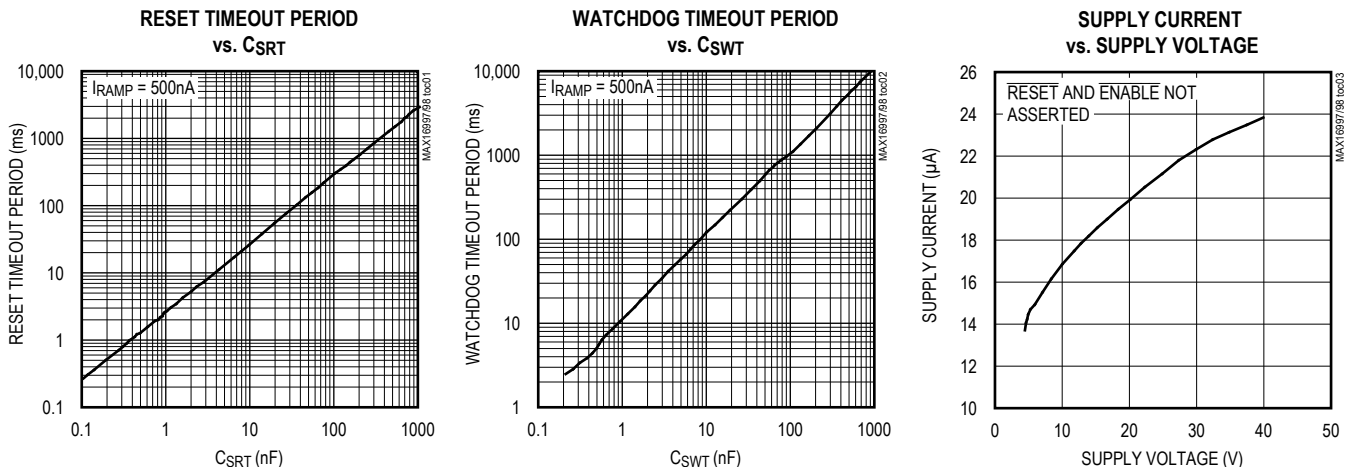
**Note 3:** Calculated based on  $V_{RAMP} = 1.235V$  and  $I_{RAMP} = 500nA$ .

**Note 4:** WDI pulses narrower than  $1\mu s$  will be ignored. WDI pulses wider than  $6.5\mu s$  will be recognized.

**Note 5:** Not production tested, guaranteed by design.

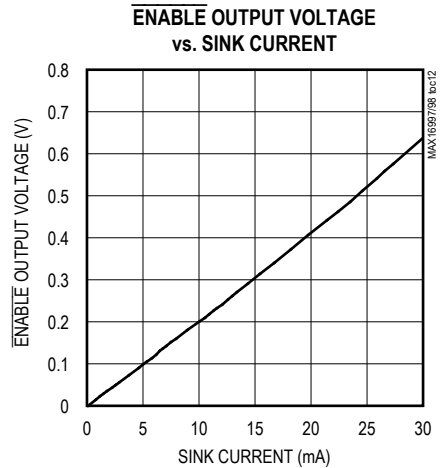
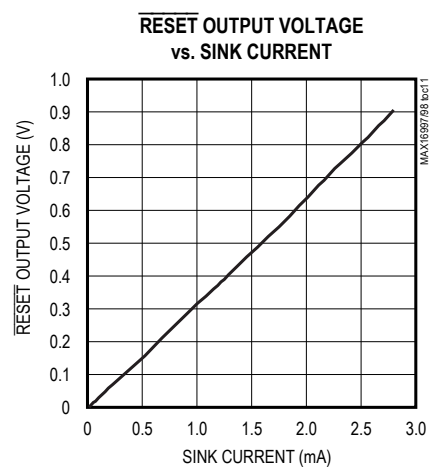
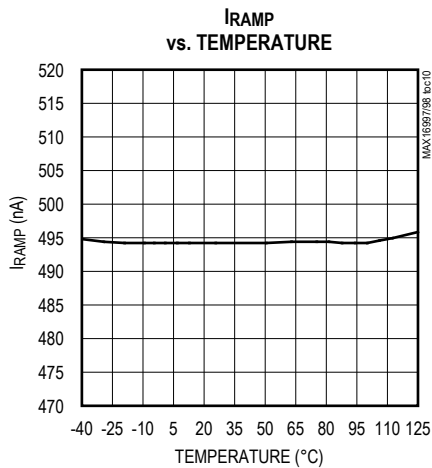
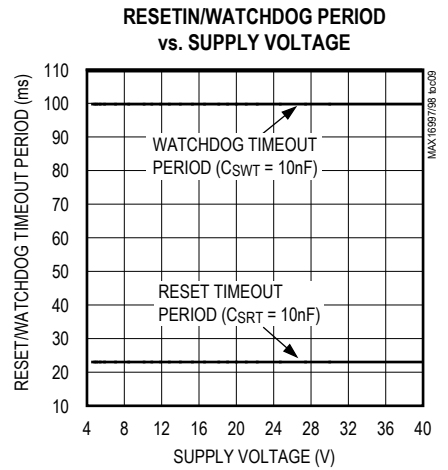
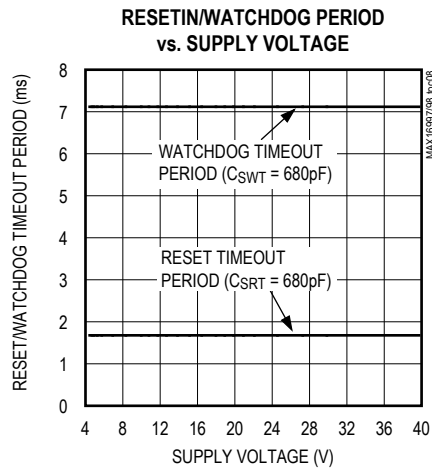
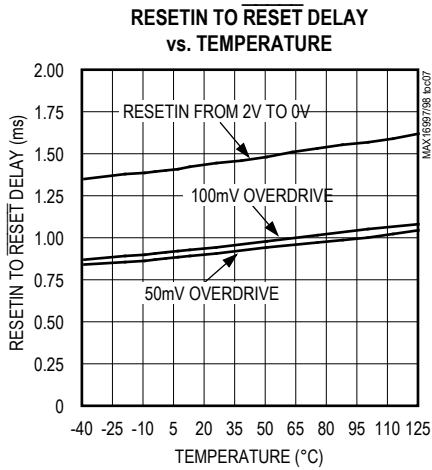
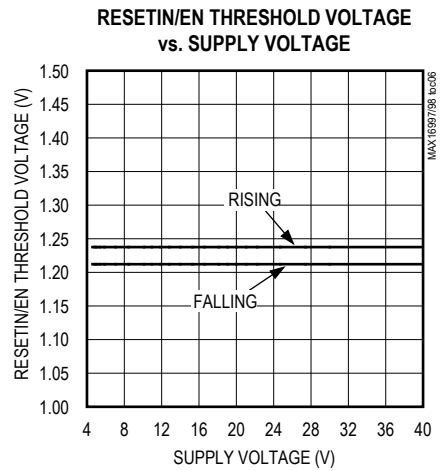
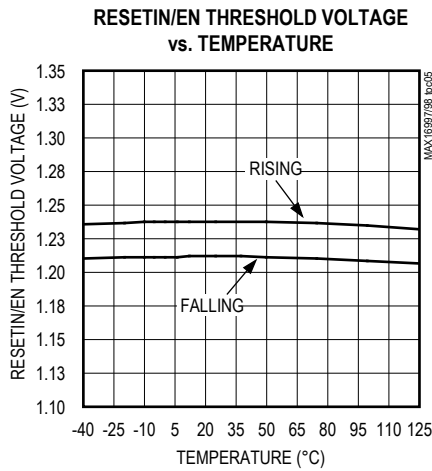
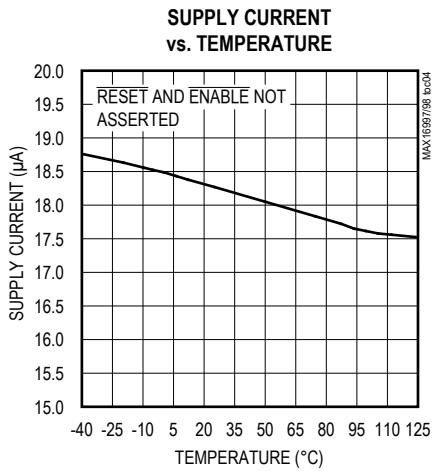
Typical Operating Characteristics

( $C_{SWT} = C_{SRT} = 1500pF$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.)



Typical Operating Characteristics (continued)

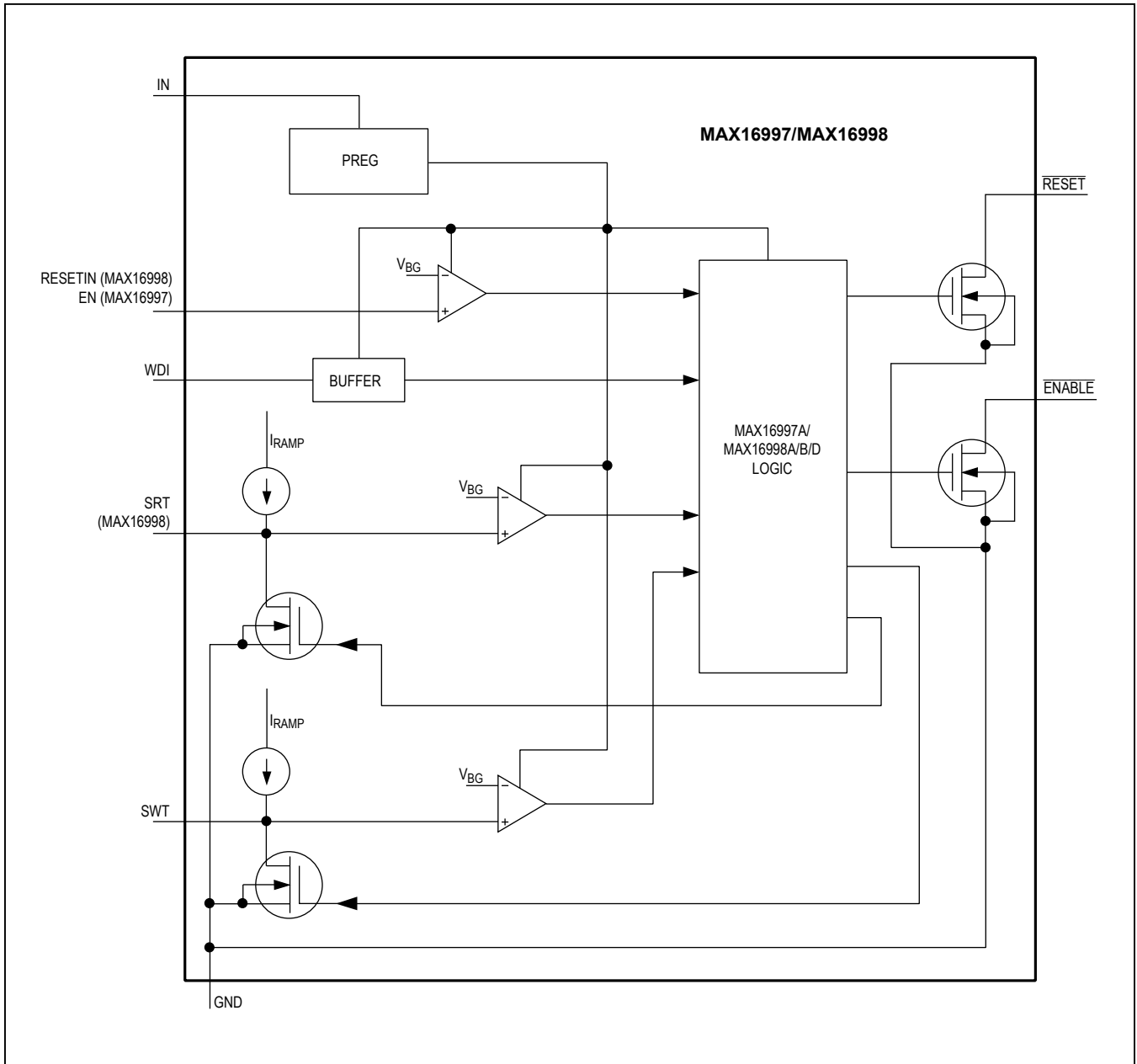
( $C_{SWT} = C_{SRT} = 1500\text{pF}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



## Pin Configuration

PIN		NAME	FUNCTION
MAX16997A	MAX16998A/B/D		
1	1	IN	Power-Supply Input. Bypass IN to GND with a 0.1µF capacitor.
2	—	EN	High-Impedance Input to the Enable Comparator. Depending on the voltage level at EN, the internal watchdog timer is turned on or off (see the <i>EN Input</i> section).
3, 7	—	N.C.	No Connection. Not internally connected.
4	4	SWT	Watchdog Timeout Adjustment Input. Connect a capacitor between SWT and GND to set the basic watchdog timeout period. Connect SWT to ground to disable the watchdog timer function. See the <i>Selecting the Watchdog Timeout Capacitor</i> section.
5	5	GND	Ground
6	6	WDI	Watchdog Input. <b>MAX16997A/MAX16998A (Timeout Watchdog):</b> Two consecutive WDI falling edges must occur at WDI within the watchdog timeout period or $\overline{\text{RESET}}$ asserts. The watchdog timer clears when a falling edge occurs on WDI or whenever $\overline{\text{RESET}}$ is asserted. $\overline{\text{ENABLE}}$ asserts if three consecutive watchdog timeout periods have expired without a falling edge at WDI. WDI is a high-impedance input. Leaving WDI unconnected will cause improper operation of the watchdog timer. <b>MAX16998B/D (Window Watchdog):</b> WDI falling transitions within periods shorter than the closed window width or longer than the basic watchdog timeout period force $\overline{\text{RESET}}$ to assert low for the reset timeout period. The watchdog timer begins to count after $\overline{\text{RESET}}$ is deasserted. The watchdog timer clears when a WDI falling edge occurs or whenever $\overline{\text{RESET}}$ is asserted. $\overline{\text{ENABLE}}$ asserts if three consecutive watchdog timeout periods have expired without a falling edge at WDI. WDI is a high-impedance input. Leaving WDI unconnected will cause improper operation of the watchdog timer.
8	8	$\overline{\text{ENABLE}}$	Open-Drain Enable Output. $\overline{\text{ENABLE}}$ asserts when three consecutive WDI faults occur. $\overline{\text{ENABLE}}$ remains low until three consecutive good WDI falling edges occur. $\overline{\text{ENABLE}}$ does not assert if the voltage at $\overline{\text{RESETIN}}$ (EN) is below its threshold. These devices are guaranteed to be in correct $\overline{\text{ENABLE}}$ output logic state when $V_{\text{IN}}$ remains greater than 1.1V.
—	2	RESETIN	Reset Input. High-impedance input to the reset comparator. When $V_{\text{RESETIN}}$ falls below 1.235V, $\overline{\text{RESET}}$ asserts. $\overline{\text{RESET}}$ remains asserted as long as $V_{\text{RESETIN}}$ is low and for the reset timeout period after RESETIN goes high. Connect $V_{\text{RESETIN}}$ to the center point of an external resistive divider to set the threshold for the externally monitored voltage. Connect RESETIN to a defined voltage logic-level.
—	3	SRT	Reset Timeout Adjustment Input. Connect a capacitor between SRT and GND to set the reset timeout period. See the <i>Selecting the Reset Timeout Capacitor</i> section.
—	7	$\overline{\text{RESET}}$	Open-Drain Reset Output. $\overline{\text{RESET}}$ asserts whenever RESETIN drops below the selected reset threshold voltage ( $V_{\text{PON}}$ ). $\overline{\text{RESET}}$ remains low for the reset timeout period after all reset conditions are removed, and then goes high. $\overline{\text{RESET}}$ asserts for a period of $t_{\text{RESET}}$ whenever a WDI fault occurs. Connect $\overline{\text{RESET}}$ to a pullup resistor connected to a voltage higher than 2.5V (typ).

Functional Diagram



Timing Diagrams

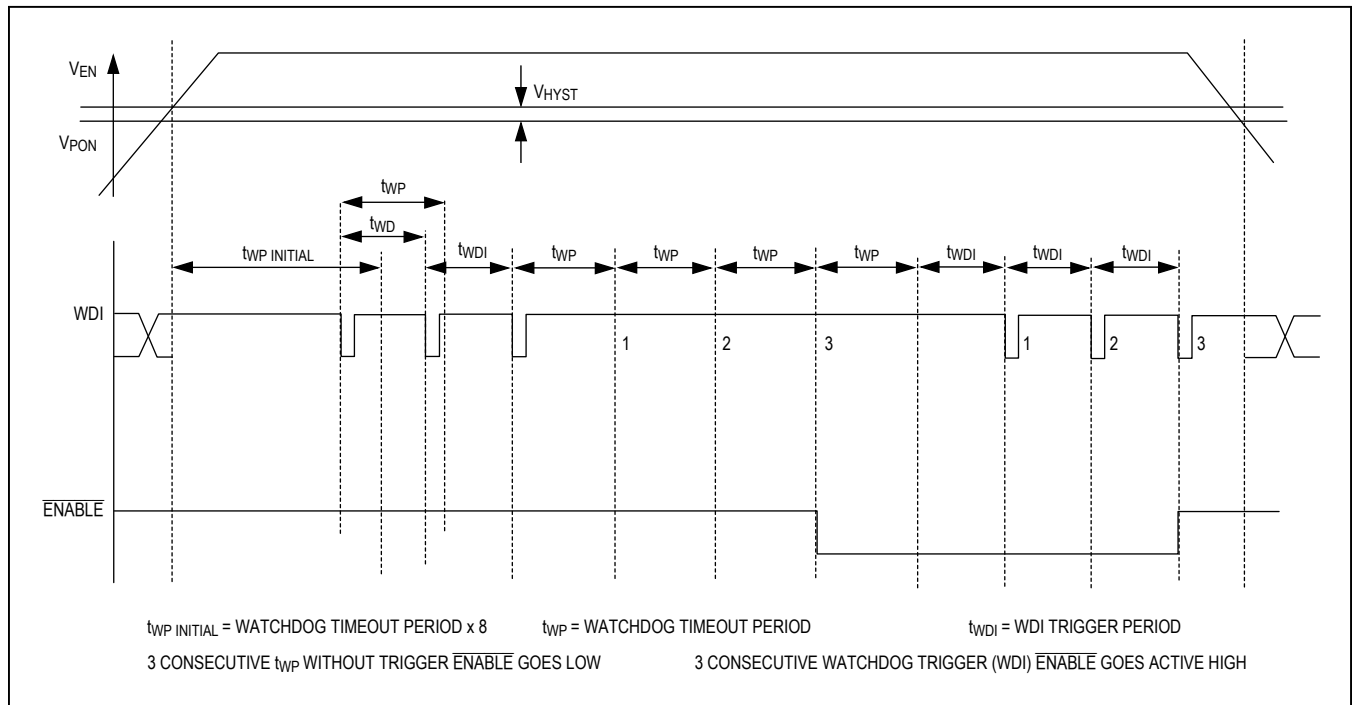


Figure 1. MAX16997A Timing Diagram

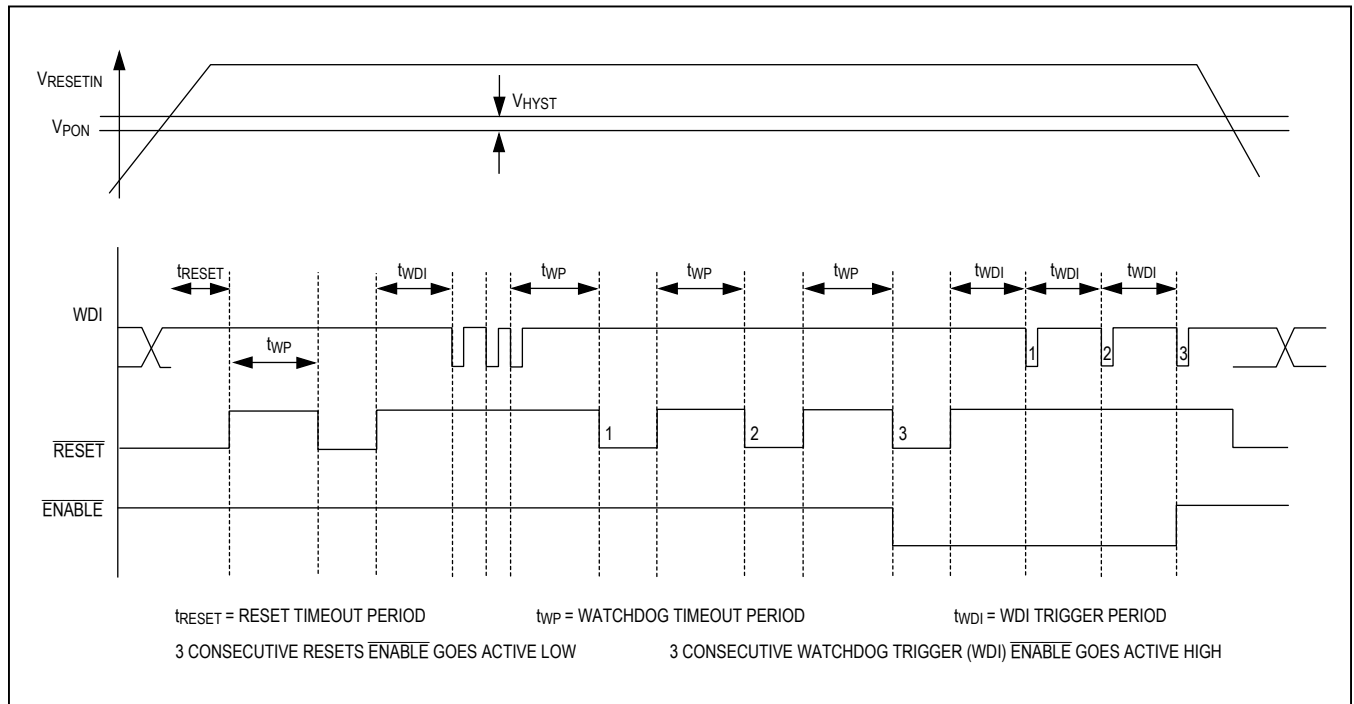


Figure 2. MAX16998A Timing Diagram

Timing Diagrams (continued)

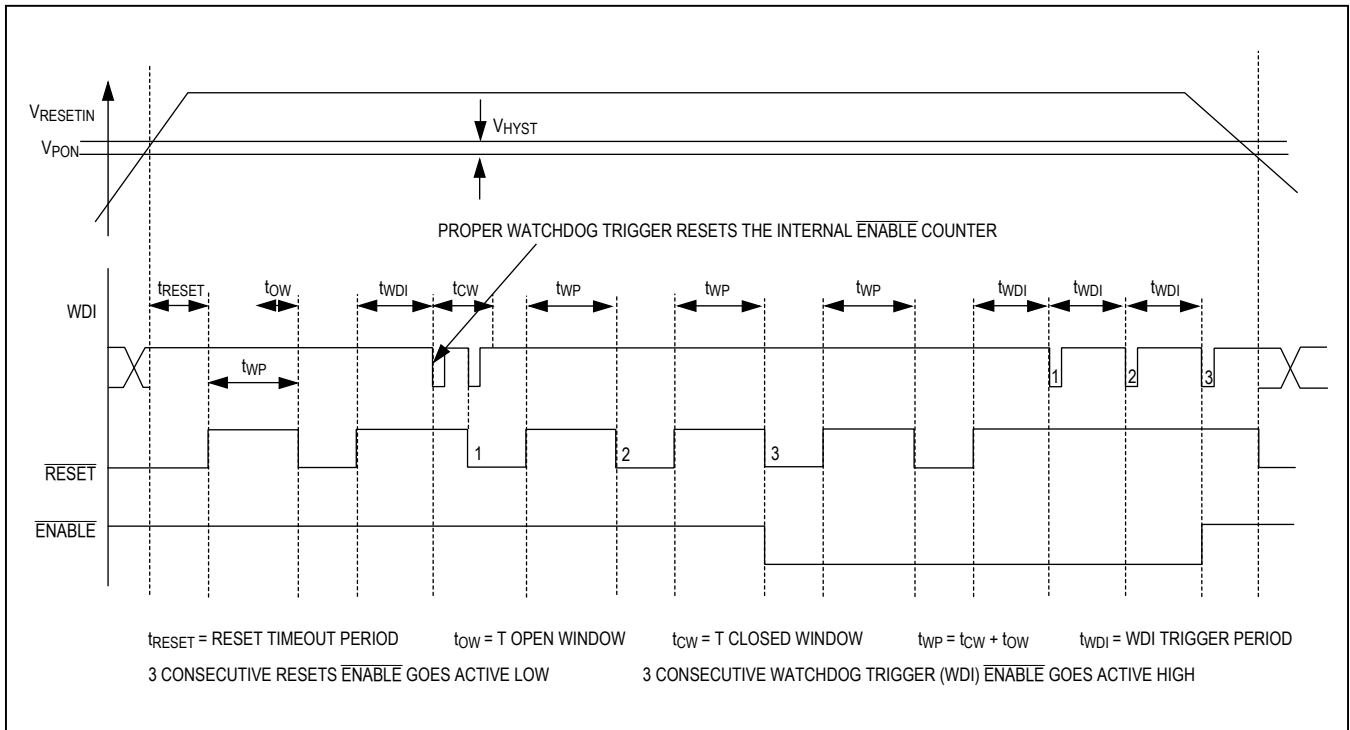


Figure 3. MAX16998B/D Timing Diagram

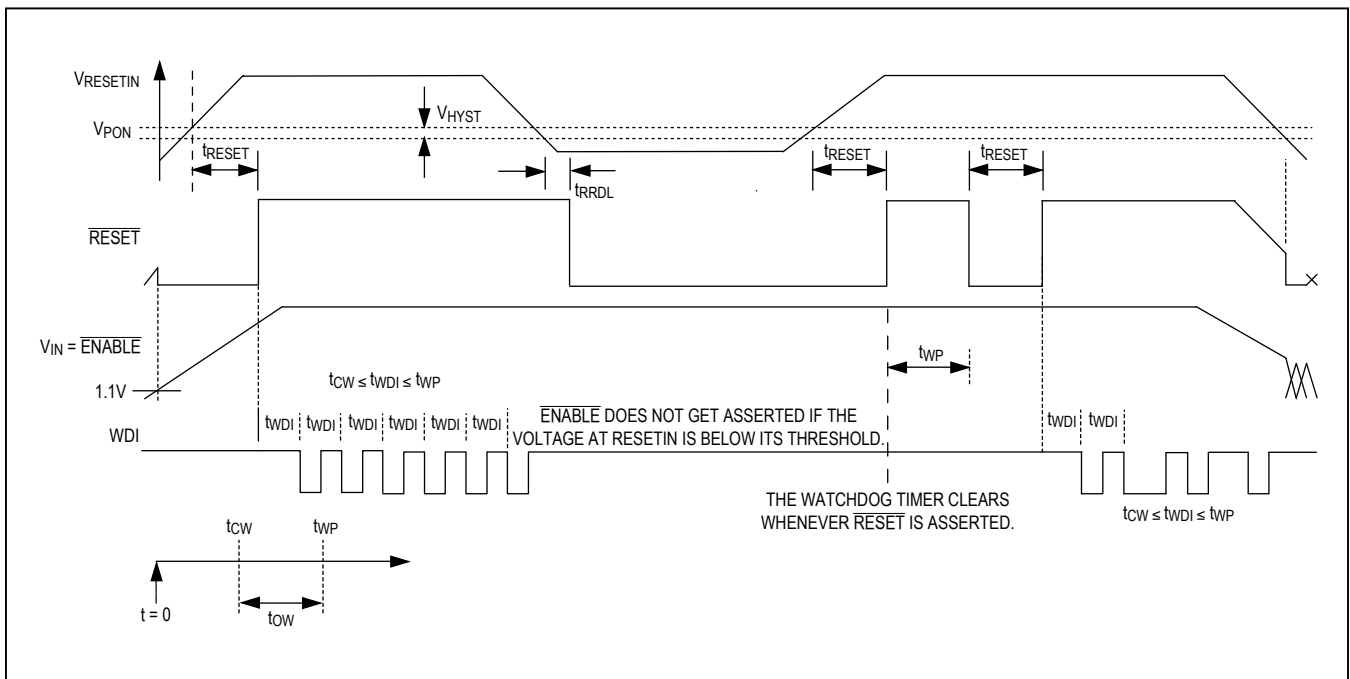


Figure 4. RESETIN, RESET, VIN, ENABLE, and WDI Voltage Monitoring



## Detailed Description

The MAX16997/MAX16998 are  $\mu\text{P}$  supervisory circuits for high-input-voltage and low-quiescent-current applications. These devices improve system reliability by monitoring the sub-system for software code execution errors. The MAX16997A/MAX16998A/B/D detect downstream circuit failures, and provide switchover to redundant circuitry. These devices provide complete adjustability for reset and watchdog functions.

The MAX16998A/B/D generate two output signals,  $\overline{\text{RESET}}$  and  $\overline{\text{ENABLE}}$ , that depend on the voltage level at RESETIN and the signal at WDI.  $\overline{\text{RESET}}$  asserts whenever RESETIN drops below the selected reset threshold voltage.  $\overline{\text{RESET}}$  remains low for the reset timeout period after all reset conditions are deasserted, and then goes high.  $\overline{\text{RESET}}$  also asserts for a period of  $t_{\overline{\text{RESET}}}$  whenever a WDI fault occurs. The MAX16997A generates one output signal ( $\overline{\text{ENABLE}}$ ) based on the voltage level at EN and the signal at WDI.

The MAX16997A/MAX16998A provide watchdog timeout adjustability with an external capacitor. The MAX16998A asserts  $\overline{\text{RESET}}$  when two consecutive WDI falling edges do not occur within the watchdog timeout period. This device also asserts  $\overline{\text{ENABLE}}$  if three consecutive watchdog timeout periods have elapsed without a falling edge at WDI.  $\overline{\text{ENABLE}}$  remains low until three consecutive good WDI falling edges occur.  $\overline{\text{ENABLE}}$  does not assert if the voltage at RESETIN (EN) is below its threshold. For the MAX16997A, the watchdog timer starts timing if the voltage at EN is higher than a preset threshold level. Each time the voltage at EN rises from below to above the preset threshold voltage, the initial watchdog timeout period is 8 times the normal watchdog timeout period ( $t_{\text{WDP}}$ ). Other than described above, the MAX16997A behaves the same as the MAX16998A.

The MAX16998B/MAX16998D contain a window watchdog timer that looks for activity outside an expected window of operation. The window size is factory-set to 50% (MAX16998B) or 75% (MAX16998D) of the adjusted watchdog timeout period.

### Reset Output ( $\overline{\text{RESET}}$ ) (MAX16998A/B/D)

The reset output is typically connected to the reset input of the  $\mu\text{C}$  to start or restart it in a known state. The MAX16998A/B/D provide an active-low open-drain reset logic to prevent code execution errors.

For the MAX16998A/B/D,  $\overline{\text{RESET}}$  asserts whenever RESETIN drops below the selected reset threshold voltage ( $V_{\text{PON}}$ ).  $\overline{\text{RESET}}$  remains low for the reset timeout period after RESETIN exceeds the selected threshold voltage, and then goes high.

The MAX16998A asserts  $\overline{\text{RESET}}$  for a period of  $t_{\overline{\text{RESET}}}$  when two consecutive WDI falling edges do not occur within the adjusted watchdog timeout period. The MAX16998B/D also assert  $\overline{\text{RESET}}$  for a period of  $t_{\overline{\text{RESET}}}$  when a WDI falling edge does not occur within the open window period.

Anytime reset asserts, the watchdog timer clears. At the end of the reset timeout period,  $\overline{\text{RESET}}$  goes high, and the watchdog timer is restarted from zero (see the [Selecting the Watchdog Timeout Capacitor](#) section).

### Enable Output ( $\overline{\text{ENABLE}}$ )

If the  $\mu\text{C}$  fails to operate correctly (e.g., the software execution is stuck in a loop), WDI does not trigger any more and  $\overline{\text{RESET}}$  pulls low, resetting the  $\mu\text{C}$ . If the  $\mu\text{C}$  does not work properly in the next loop either, the device asserts  $\overline{\text{RESET}}$  again. After three watchdog timeout periods elapse with no falling edges at WDI,  $\overline{\text{ENABLE}}$  asserts and flags a backup circuit that can take over the operation.

$\overline{\text{ENABLE}}$  remains low until three consecutive WDI falling edges with periods shorter than the watchdog timeout occur.  $\overline{\text{ENABLE}}$  does not assert if the voltage at RESETIN (EN) is below its threshold. These devices are guaranteed to be in correct  $\overline{\text{ENABLE}}$  output logic state when  $V_{\text{IN}}$  remains greater than 1.1V.

### Power-On/Power-Off Sequence

[Figure 5](#) shows the power-up and power-down sequence for  $\overline{\text{RESET}}$  and  $\overline{\text{ENABLE}}$  for the MAX16998A/B/D.

On power-up, once  $V_{\text{IN}}$  reaches 1.1V,  $\overline{\text{RESET}}$  goes logic-low. As RESETIN rises,  $\overline{\text{RESET}}$  remains low. When RESETIN rises above  $V_{\text{PON}}$ , the reset timer starts and  $\overline{\text{RESET}}$  remains low. When the reset timeout period ends,  $\overline{\text{RESET}}$  goes high.

For proper  $\overline{\text{RESET}}$  operation,  $V_{\text{IN}}$  must rise above the minimum operating voltage of 5V for longer than 270 $\mu\text{s}$  before the RESETIN signal crosses the  $V_{\text{PON}}$  rising threshold of 1.135V (minimum). See [Figure 6](#) for details.

On power-down, once RESETIN goes below  $V_{\text{PON}}$ ,  $\overline{\text{RESET}}$  goes low and remains low until  $V_{\text{IN}}$  drops below 1.1V. [Figure 6](#) shows the detailed power-up sequence for the MAX16998A/B/D.

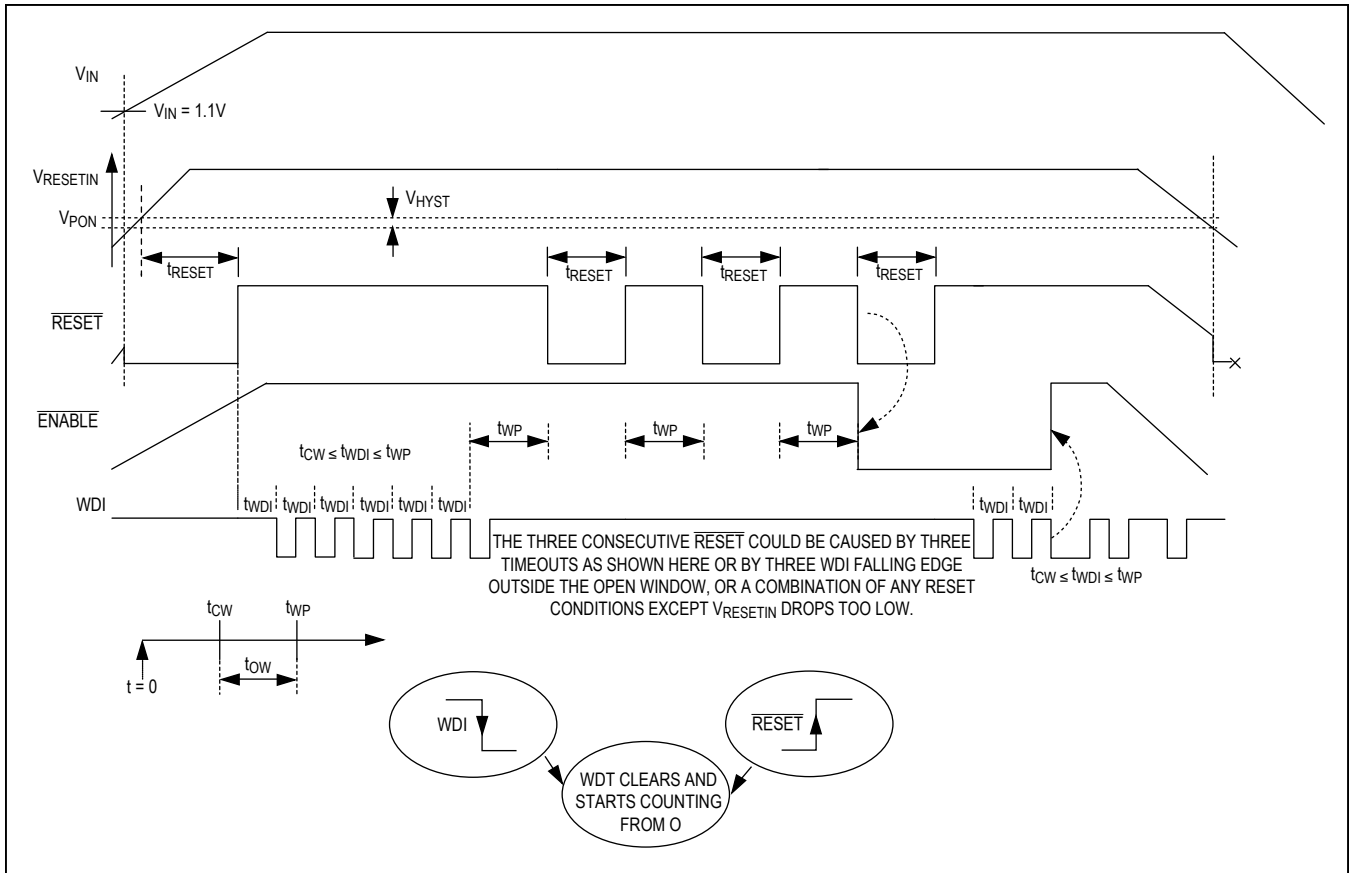


Figure 5. Power-On Reset and Power-Down Reset for the MAX16998A/B/D

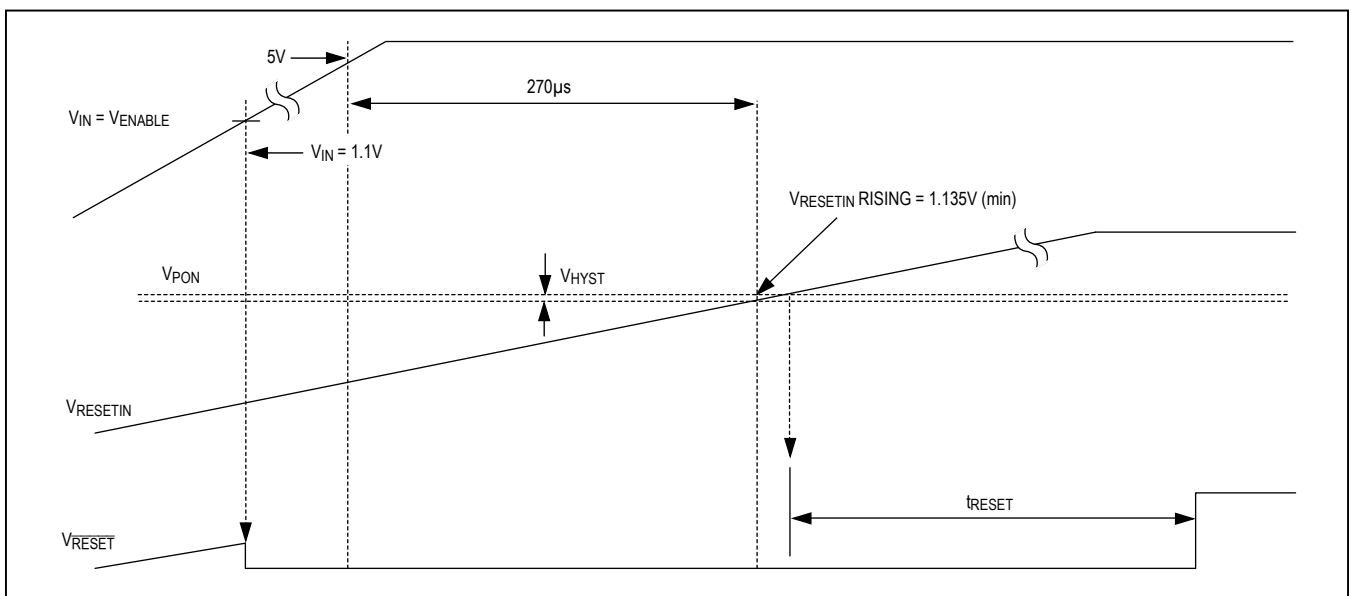


Figure 6. Detailed Power-Up Sequence for the MAX16998A/B/D

**RESETIN Input (MAX16998A/B/D)**

The MAX16998A/B/D monitor the voltage at RESETIN using an adjustable reset threshold, set with an external resistive divider (see Figure 7).  $\overline{\text{RESET}}$  asserts when  $V_{\text{RESETIN}}$  is below 1.235V.

Use the following equations to calculate the externally monitored voltage ( $V_{\text{CC}}$ ).

$$V_{\text{TH}} = V_{\text{PON}} \left[ \frac{R_1}{R_2} + 1 \right]$$

where  $V_{\text{TH}}$  is the desired reset threshold voltage, and  $V_{\text{PON}} = 1.235\text{V}$ . To simplify the resistor selection, choose a value for  $R_2$  (< than  $1\text{M}\Omega$ ) and calculate  $R_1$ .

$$R_1 = R_2 \left[ \frac{V_{\text{TH}}}{V_{\text{PON}}} - 1 \right]$$

**EN Input**

The MAX16997A provides a high-impedance input (EN) to the enable comparator. Based on the voltage level at EN, the watchdog timer is turned on or off. The watchdog timer starts timing if the voltage level at EN is higher than a preset threshold voltage ( $V_{\text{PON}}$ ). Each time the voltage at EN rises from below to above the preset threshold voltage, the initial watchdog timeout period is 8 times the normal watchdog timeout period ( $t_{\text{WP}}$ ).

**Watchdog Timer**

**MAX16997A**

The watchdog circuit monitors the  $\mu\text{C}$ 's activity. For the MAX16997A, the watchdog timer starts timing once the voltage at EN is higher than a preset threshold voltage.  $\overline{\text{ENABLE}}$  asserts if three consecutive watchdog timeout periods have elapsed without a falling edge at WDI.  $\overline{\text{ENABLE}}$  remains low until three consecutive WDI falling edges with periods shorter than the watchdog timeout period occur.

Each time the voltage at EN rises from below to above the preset threshold voltage, the first watchdog timeout period extends by a factor of 8 ( $8 \times t_{\text{WP}}$ ). If a WDI falling edge occurs during that time, then the watchdog timeout period is immediately switched over to a single  $t_{\text{WP}}$ . If no watchdog falling edge occurs during this prolonged watchdog timeout period,  $\overline{\text{ENABLE}}$  goes low at the end of this period and stays low. After this, the first falling edge at WDI switches the watchdog timeout period to a single  $t_{\text{WP}}$ . See Figure 1. The MAX16997A watchdog timeout period ( $t_{\text{WP}}$ ) is adjustable by a single capacitor at SWT.

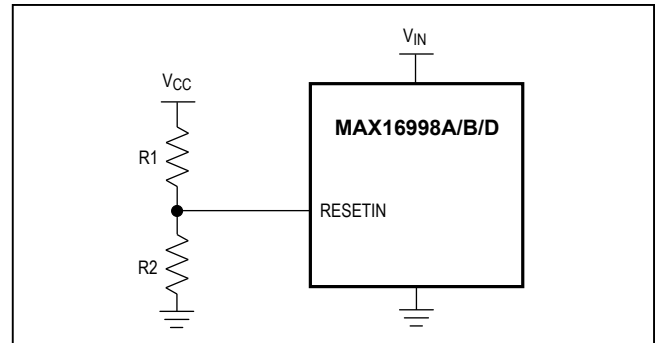


Figure 7. Setting RESETIN Voltage for the MAX16998A/B/D

**MAX16998A**

The MAX16998A asserts  $\overline{\text{RESET}}$  when two consecutive WDI falling edges do not occur within the adjusted watchdog timeout period ( $t_{\text{WP}}$ ).  $\overline{\text{RESET}}$  remains asserted for the reset timeout period ( $t_{\text{RESET}}$ ) and then goes high. This device also asserts  $\overline{\text{ENABLE}}$  if three consecutive watchdog timeout periods have elapsed without a falling edge at WDI.  $\overline{\text{ENABLE}}$  remains low until three consecutive WDI falling edges with periods shorter than the watchdog timeout period occur (see Figure 2).

The internal watchdog timer is cleared by a  $\overline{\text{RESET}}$  rising edge or by a falling edge at WDI. The watchdog timer remains cleared while  $\overline{\text{RESET}}$  is asserted; as soon as  $\overline{\text{RESET}}$  is released, the timer starts counting. WDI falling edges are ignored when  $\overline{\text{RESET}}$  is low. If no WDI falling edge occurs within the watchdog timeout period,  $\overline{\text{RESET}}$  immediately goes low and stays low for the adjusted reset timeout period.

**MAX16998B/D**

The MAX16998B/D have a windowed watchdog timer. The watchdog timeout period ( $t_{\text{WP}}$ ) is the sum of a closed window period ( $t_{\text{CW}}$ ) and an open window period ( $t_{\text{OW}}$ ). If the  $\mu\text{C}$  issues a WDI falling edge within the open window period,  $\overline{\text{RESET}}$  stays high. Once a WDI falling edge occurs within the closed window period,  $\overline{\text{RESET}}$  immediately goes low and stays low for the adjusted reset timeout period (see Figure 3). If no WDI falling edge occurs within the watchdog timeout period,  $\overline{\text{RESET}}$  immediately goes low and stays low for the adjusted reset timeout period. The open window size is factory-set to 50% of the watchdog timeout period for the MAX16998B and 75% for the MAX16998D.

Figure 8 shows a WDI falling edge identified as a good or a bad WDI signal edge. In case 1, the WDI falling edge occurs within the closed window period and is considered a bad WDI falling edge (early fault); therefore, it asserts  $\overline{\text{RESET}}$ . Case 2 also shows another fault. In this case,

no WDI falling edge occurs within the watchdog timeout period ( $t_{WP}$ ) and is considered a late fault that asserts  $\overline{\text{RESET}}$ . In case 3, the WDI falling edge occurs within the open window period and is considered a good WDI signal falling edge. In this case,  $\overline{\text{RESET}}$  stays high. In case 4, the WDI falling edge occurs within the indeterminate region. In this case, the  $\overline{\text{RESET}}$  state is indeterminate.

These devices assert  $\overline{\text{ENABLE}}$  after three consecutive bad WDI falling edges.  $\overline{\text{ENABLE}}$  returns high after three consecutive good WDI signal falling edges (see Figure 3).

Either a rising edge at  $\overline{\text{RESET}}$  or a falling edge at WDI clears the internal watchdog timer. The watchdog timer remains cleared while  $\overline{\text{RESET}}$  is asserted. The watchdog timer begins counting when  $\overline{\text{RESET}}$  goes high. WDI falling edges are ignored when  $\overline{\text{RESET}}$  is low.

### Applications Information

#### Selecting the Reset Timeout Capacitor

The reset timeout period is adjustable to accommodate a variety of  $\mu\text{P}$  applications. Adjust the reset timeout period ( $t_{\overline{\text{RESET}}}$ ) by connecting a capacitor ( $C_{\text{SRT}}$ ) between SRT and ground. See the Reset Timeout Period vs.  $C_{\text{SRT}}$  graph in the *Typical Operating Characteristics* section. Calculate the reset timeout capacitance using the equation below:

$$C_{\text{SRT}} = t_{\overline{\text{RESET}}} \times \frac{I_{\text{RAMP}}}{V_{\text{RAMP}}}$$

where  $V_{\text{RAMP}}$  is in volts,  $t_{\overline{\text{RESET}}}$  is in seconds,  $I_{\text{RAMP}}$  is in nA, and  $C_{\text{SRT}}$  is in nF.

Leakage currents and stray capacitance (e.g., a scope probe, which induces both) at SRT may cause errors in the reset timeout period. If precise time control is required, use capacitors with low leakage current and high stability.

#### Selecting the Watchdog Timeout Capacitor

The watchdog timeout period is adjustable to accommodate a variety of  $\mu\text{P}$  applications. With this feature, the watchdog timeout can be optimized for software execution. The programmer determines how often the watchdog timer should be serviced. Adjust the watchdog timeout period ( $t_{\text{WP}}$ ) by connecting a capacitor ( $C_{\text{SWT}}$ ) between SWT and GND. For normal mode operation, calculate the watchdog timeout capacitance using the following equation:

$$C_{\text{SWT}} = t_{\text{WP}} \times \frac{I_{\text{RAMP}}}{4 \times V_{\text{RAMP}}}$$

where  $V_{\text{RAMP}}$  is in volts,  $t_{\text{WP}}$  is in seconds,  $I_{\text{RAMP}}$  is in nA, and  $C_{\text{SWT}}$  is in nF. See the Watchdog Timeout Period vs.  $C_{\text{SWT}}$  graph in the *Typical Operating Characteristics* section.

For the MAX16998B/MAX16998D, the open window size is factory-set to 50% (MAX16998B) or 75% (MAX16998D) of the watchdog period. Leakage currents and stray capacitance (e.g., a scope probe, which induces both) at SWT may cause errors in the watchdog timeout period. If precise time control is required, use capacitors with low leakage current and high stability. To disable the watchdog timer function, connect SWT to ground and connect WDI to either the high- or low-logic state.

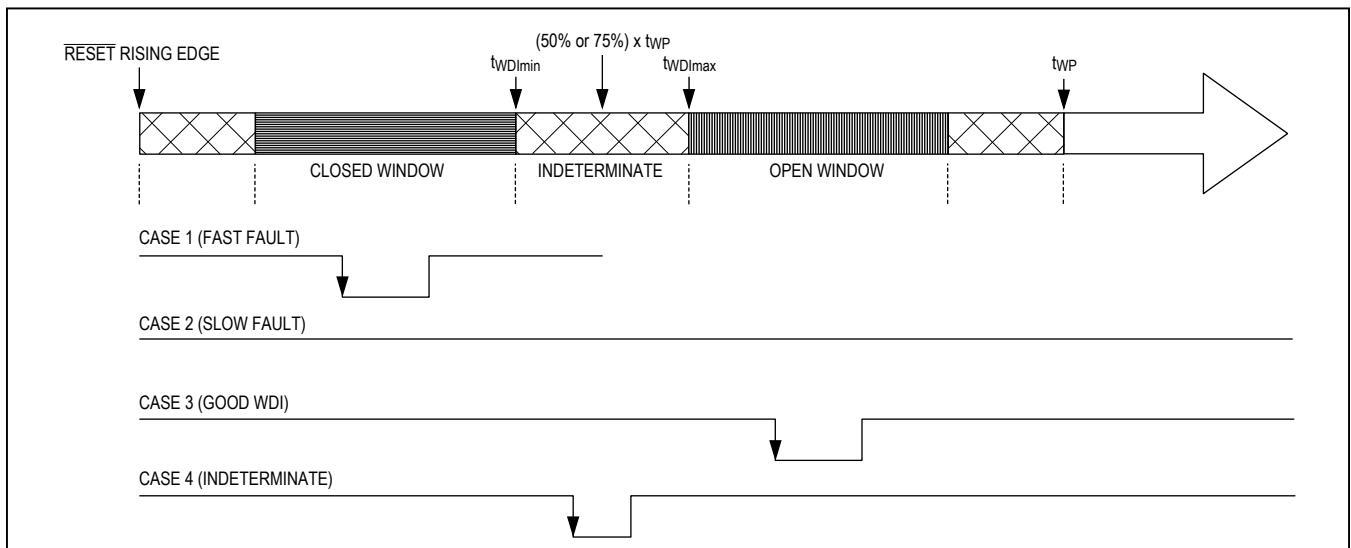


Figure 8. The MAX16998B/D Window Watchdog Diagram

**Interfacing to Other Voltages for Logic Compatibility**

As shown in [Figure 9](#), the open-drain  $\overline{\text{RESET}}$  output can operate in the 2.5V to 18V range. This allows the device to interface a  $\mu\text{P}$  with other logic levels.

**WDI Glitch Immunity**

For additional glitch immunity, connect an RC lowpass filter as close as possible to WDI (see [Figure 10](#)).

For example, for glitches with duration of  $1\mu\text{s}$ , a  $12\text{k}\Omega$  resistor and a  $47\text{pF}$  capacitor will provide immunity.

**Layout Considerations**

SRT and SWT are connected to internal precision current sources. When developing the layout for the application, minimize stray capacitance attached to SRT and SWT as well as leakage currents that can reach those nodes. SRT and SWT traces should be as short as possible. Route traces carrying high-speed digital signals and traces with large voltage potentials as far from SRT and SWT as possible. Leakage currents and stray capacitance (e.g., a scope probe, which induces both) at these pins may cause errors in the reset and/or watchdog timeout period. When evaluating these parts, use clean prototype boards to ensure accurate reset and watchdog timeout periods.

RESETIN is a high-impedance input and a high-impedance resistive divider (e.g.,  $100\text{k}\Omega$  to  $1\text{M}\Omega$ ) sets the threshold level. Minimize coupling to transient signals by keeping the connections to this input short. Any DC leakage current at RESETIN (e.g., a scope probe) causes errors in the programmed reset threshold.

**Typical Operating Circuits**

$\overline{\text{RESET}}$  remains asserted as long as RESETIN is below the regulated voltage and for the reset timeout period after RESETIN goes high to assure that the monitored LDO voltage is settled. Then, the  $\mu\text{C}$  starts operating and triggers WDI.

If the  $\mu\text{C}$  fails to operate correctly (e.g., the software execution is stuck in a loop), the WDI signal does not trigger the watchdog timer any more, and  $\overline{\text{RESET}}$  is pulled low, resetting the  $\mu\text{C}$ . If the  $\mu\text{C}$  does not work properly in the next loop either, the device asserts  $\overline{\text{RESET}}$  again. After three watchdog timeout periods with no WDI falling edges,  $\overline{\text{ENABLE}}$  asserts and flags backup or safety circuits that take over the operation.

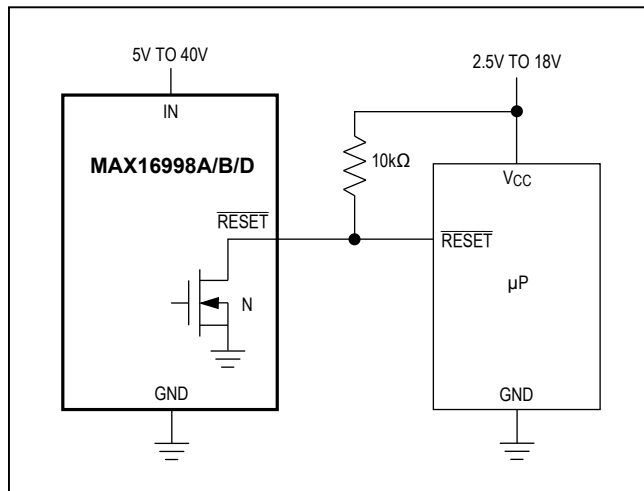


Figure 9. Interfacing to Other Voltage Levels

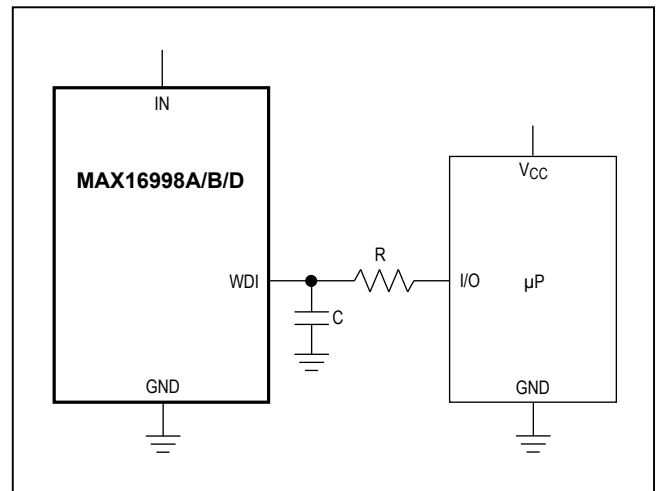


Figure 10. Additional WDI Glitch Immunity Circuit

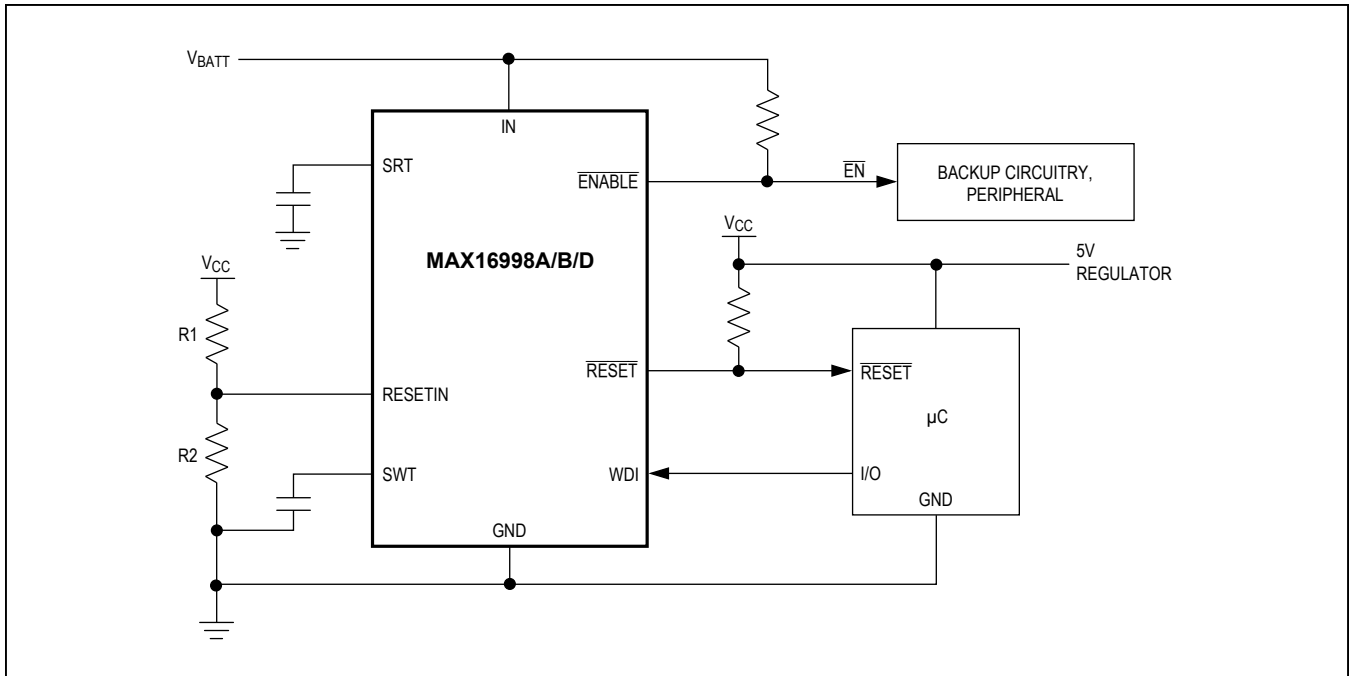


Figure 11. MAX16998A/B/D Switch Over to Backup Circuitry

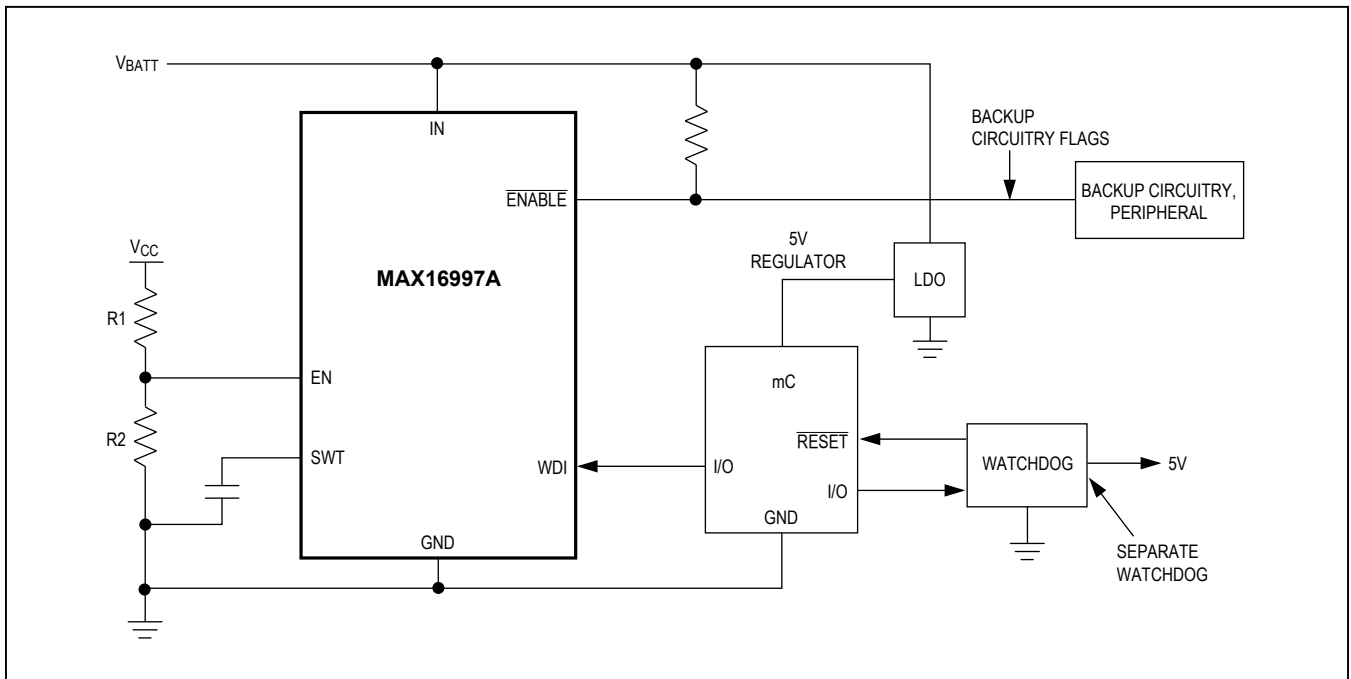
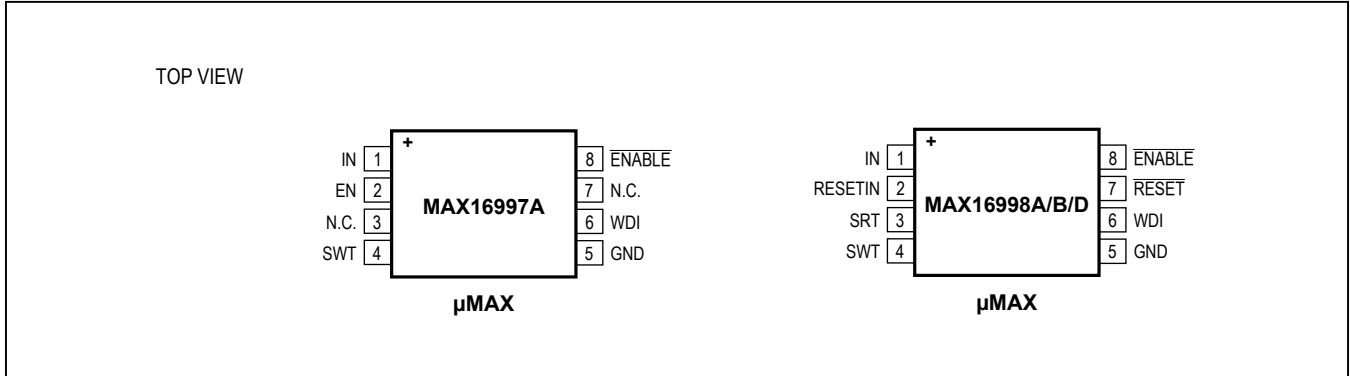


Figure 12. MAX16997A Application Diagram

Pin Configurations



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 μMAX	U8+1, U8+4	<a href="#">21-0036</a>	<a href="#">90-0092</a>

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/08	Initial release	—
1	4/09	Added bullet to <i>Features</i> section, revised <i>Electrical Characteristics</i> table	1, 2, 3
2	8/09	Added automotive qualified parts	1
3	11/15	Updated package code and rebranded data sheet	15
4	3/16	Deleted MAX16997AAUA/V+ variant from <i>Ordering Information</i>	1
5	4/19	Changes to Power-on/Power-off Sequence section and updated Figure 6	9, 10

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

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