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January 1996 Revised March 2001

#### 74LCX821

# Low Voltage 10-Bit D-Type Flip-Flop with 5V Tolerant Inputs and Outputs

#### **General Description**

The LCX821 consists of ten D-type Flip-Flops with 3-STATE outputs for bus organized system applications. The device is designed for low voltage (2.5V or 3.3V)  $\rm V_{CC}$  applications with capability of interfacing to a 5V signal environment.

The LCX821 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

#### **Features**

- 5V tolerant inputs and outputs
- $\blacksquare$  2.3V–3.6V  $\rm V_{CC}$  specifications provided
- $\blacksquare$  7.0 ns t<sub>PD</sub> max (V<sub>CC</sub> = 3.3V), 10  $\mu$ A I<sub>CC</sub> max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- $\pm$ 24 mA output drive ( $V_{CC} = 3.0V$ )
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:

Human Body Model > 2000V Machine Model > 200V

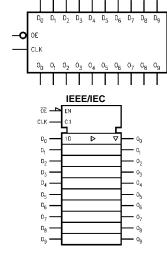
**Note 1:** To ensure the high-impedance state during power up or down,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

#### **Ordering Code:**

Order Number	Package Number	Package Description
74LCX821WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74LCX821MSA	MSA24	24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LCX821MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix "X" to the ordering code.

#### **Logic Symbols**



#### **Connection Diagram**



#### **Pin Descriptions**

Pin Names	Description
D <sub>0</sub> –D <sub>9</sub>	Data Inputs
CLK	Clock Input
ŌĒ	Output Enable Input
O <sub>0</sub> -O <sub>9</sub>	3-STATE Latch Outputs

#### **Function Table**

l	nputs		Internal	Outputs	
ŌE	CLK	D	Q	O <sub>n</sub>	Function
Н	Н	L	NC	Z	Hold
Н	Н	Н	NC	Z	Hold
Н	~	L	L	Z	Load
Н	~	Н	Н	Z	Load
L	~	L	L	L	Data Available
L	~	Н	Н	Н	Data Available
L	Н	L	NC	NC	No Change in Data
L	Н	Н	NC	NC	No Change in Data

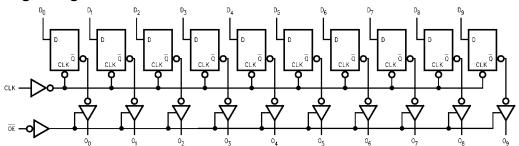
H = HIGH Voltage Level L = LOW Voltage Level

- X = Immaterial
- Z = High Impendance = LOW-to-HIGH Transition
- NC = No Change

#### **Functional Description**

The LCX821 consists of ten edge-triggered flip-flops with individual D-type inputs with 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The ten flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CLK) transition. With the Output Enable  $(\overline{OE})$  LOW, the contents of the ten flip-flops are available at the outputs. When  $\overline{\text{OE}}$  is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops.

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### Absolute Maximum Ratings(Note 2) Symbol Parameter Value Conditions Units -0.5 to +7.0 ٧ Supply Voltage $V_{CC}$ ٧ DC Input Voltage -0.5 to +7.0 $V_{I}$ DC Output Voltage Output in 3-STATE Vo -0.5 to +7.0 ٧ Output in HIGH or LOW State (Note 3) -0.5 to $V_{CC} + 0.5$ DC Input Diode Current -50 V<sub>I</sub> < GND mΑ $I_{IK}$ DC Output Diode Current -50 V<sub>O</sub> < GND mΑ +50 $V_O > V_{CC}$ DC Output Source/Sink Current ±50 mΑ lο $I_{CC}$ DC Supply Current per Supply Pin ±100 mΑ DC Ground Current per Ground Pin ±100 mΑ $I_{GND}$ Storage Temperature -65 to +150 °C T<sub>STG</sub>

#### **Recommended Operating Conditions** (Note 4)

Symbol	Parameter	Min	Max	Units	
V <sub>CC</sub>	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	V
V <sub>I</sub>	Input Voltage		0	5.5	V
V <sub>O</sub>	Output Voltage	HIGH or LOW State	0	V <sub>CC</sub>	V
		3-STATE	0	5.5	V
I <sub>OH</sub> /I <sub>OL</sub>	Output Current	$V_{CC} = 3.0V - 3.6V$		±24	
		$V_{CC} = 2.7V - 3.0V$ $V_{CC} = 2.3V - 2.7V$		±12	mA
		$V_{CC} = 2.3V - 2.7V$		±8	
T <sub>A</sub>	Free-Air Operating Temperature		-40	85	°C
Δt/ΔV	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$ , $V_{CC} = 3.0V$		0	10	ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I<sub>O</sub> Absolute Maximum Rating must be observed.

Note 4: Unused inputs must be held HIGH or LOW. They may not float.

#### **DC Electrical Characteristics**

Symbol	Parameter	Conditions	V <sub>CC</sub>	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units
Зуппон		Conditions	(V)	Min	Max	Ullits
√ <sub>IH</sub>	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 - 3.6	2.0		. •
/ <sub>IL</sub>	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		8.0	Ť v
/он	HIGH Level Output Voltage	$I_{OH} = -100  \mu A$	2.3 – 3.6	V <sub>CC</sub> - 0.2		
		$I_{OH} = -8 \text{ mA}$	2.3	1.8		Ì
		$I_{OH} = -12 \text{ mA}$	2.7	2.2		V
		$I_{OH} = -18 \text{ mA}$	3.0	2.4		
		$I_{OH} = -24 \text{ mA}$	3.0	2.2		Ì
V <sub>OL</sub>	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.3 – 3.6		0.2	
		$I_{OL} = 8 \text{ mA}$	2.3		0.6	
		I <sub>OL</sub> = 12 mA	2.7		0.4	V
		I <sub>OL</sub> = 16 mA	3.0		0.4	Ì
		I <sub>OL</sub> = 24 mA	3.0		0.55	İ
ı	Input Leakage Current	$0 \le V_1 \le 5.5V$	2.3 – 3.6		±5.0	μΑ
OZ	3-STATE Output Leakage	$0 \le V_O \le 5.5V$	2.3 – 3.6		±5.0	
		$V_I = V_{IH}$ or $V_{IL}$	2.3 – 3.6		±3.0	μΑ
OFF	Power-Off Leakage Current	V <sub>I</sub> or V <sub>O</sub> = 5.5V	0		10	μΑ

#### DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V <sub>CC</sub>	T <sub>A</sub> = -40°0	C to +85°C	Units
Cymbol	i arameter	Conditions	(V)	Min	Max	Onito
Icc	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 3.6		10	цΑ
		3.6V ≤ V <sub>I</sub> , V <sub>O</sub> ≤ 5.5V (Note 5)	2.3 – 3.6		±10	μΑ
$\Delta I_{CC}$	Increase in I <sub>CC</sub> per Input	$V_{IH} = V_{CC} - 0.6V$	2.3 – 3.6		500	μΑ

Note 5: Outputs disabled or 3-STATE only.

### **AC Electrical Characteristics**

			$T_A = -40$ °C to +85 °C, $R_L = 500\Omega$					
Symbol	Parameter	V <sub>CC</sub> = 3.	$\rm V_{CC}=3.3V\pm0.3V$		V <sub>CC</sub> = 2.7V		$\rm V_{CC}=2.5V\pm0.2V$	
	Faranteter	C <sub>L</sub> =	50 pF	C <sub>L</sub> =	C <sub>L</sub> = 50 pF		C <sub>L</sub> = 30 pF	
		Min	Max	Min	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency	150						MHz
t <sub>PHL</sub>	Propagation Delay	1.5	7.0	1.5	7.5	1.5	8.4	ns
t <sub>PLH</sub>	CLK to O <sub>n</sub>	1.5	7.0	1.5	7.5	1.5	8.4	115
t <sub>PZL</sub>	Output Enable Time	1.5	7.5	1.5	8.0	1.5	9.8	ns
$t_{PZH}$		1.5	7.5	1.5	8.0	1.5	9.8	115
t <sub>PLZ</sub>	Output Disable Time	1.5	6.5	1.5	7.0	1.5	7.8	ns
$t_{PHZ}$		1.5	6.5	1.5	7.0	1.5	7.8	115
toshl	Output to Output Skew		1.0					ns
toslh	(Note 6)		1.0					115
t <sub>S</sub>	Setup Time, D <sub>n</sub> to CLK	2.5		2.5		4.0		ns
t <sub>H</sub>	Hold Time, D <sub>n</sub> to CLK	1.5		1.5		2.0		ns
t <sub>W</sub>	CLK Pulse Width	3.3		3.3		4.0		ns

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

#### **Dynamic Switching Characteristics**

Symbol	Parameter	Conditions	V <sub>CC</sub>	$T_A = 25^{\circ}C$	Units
Oyillboi	T drameter	Conditions	(V)	Typical	Oille
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	3.3	0.8	V
		$C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{V}, V_{IL} = 0 \text{V}$	2.5	0.6	
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	$C_L = 50 \text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$	3.3	-0.8	V
1		$C_L = 30 \text{ pF, } V_{IH} = 2.5 \text{V, } V_{IL} = 0 \text{V}$	2.5	-0.6	

### Capacitance

Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	$V_{CC} = Open, V_I = 0V \text{ or } V_{CC}$	7	pF
Co	Output Capacitance	$V_{CC} = 3.3V$ , $V_I = 0V$ or $V_{CC}$	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	$V_{CC} = 3.3V$ , $V_{I} = 0V$ or $V_{CC}$ , $f = 10$ MHz	20	pF

#### AC LOADING and WAVEFORMS Generic for LCX Family

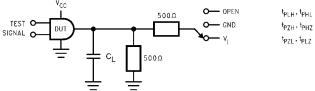
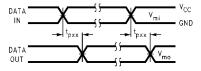
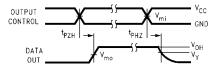


FIGURE 1. AC Test Circuit (C<sub>L</sub> includes probe and jig capacitance)

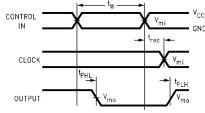
Test	Switch
t <sub>PLH</sub> , t <sub>PHL</sub>	Open
t <sub>PZL</sub> , t <sub>PLZ</sub>	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC}$ x 2 at $V_{CC} = 2.5 \pm 0.2V$
$t_{PZH}, t_{PHZ}$	GND



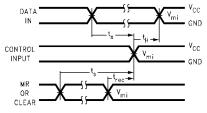
Waveform for Inverting and Non-Inverting Functions



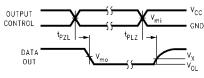
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay. Pulse Width and  $t_{\text{rec}}$  Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

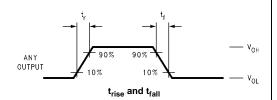
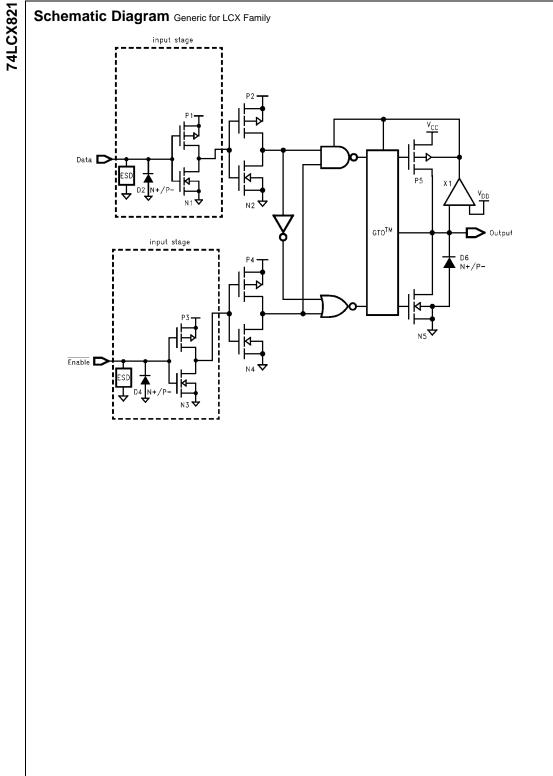
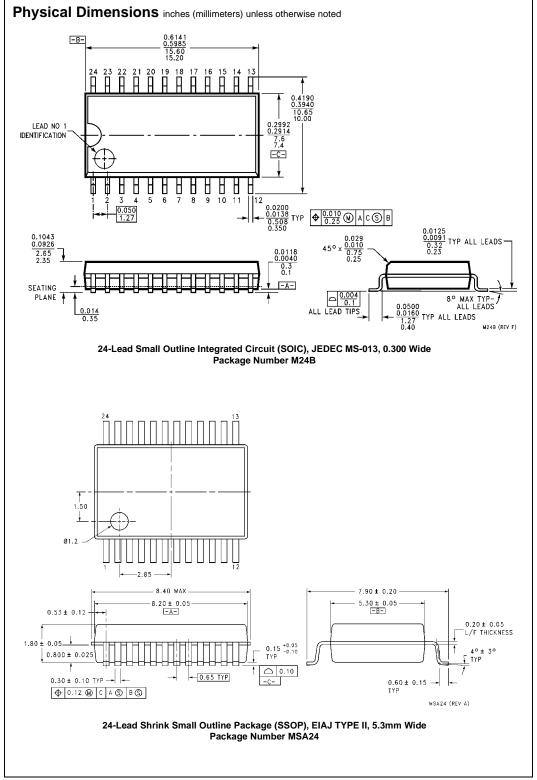
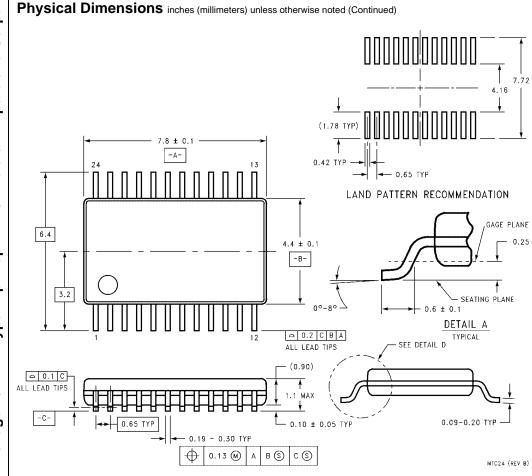


FIGURE 2. Waveforms (Input Characteristics; f = 1 MHz,  $t_r = t_f = 3 \text{ns}$ )

Symbol	V <sub>cc</sub>					
Symbol	$3.3V \pm 0.3V$	2.7V	2.5V ± 0.2V			
V <sub>mi</sub>	1.5V	1.5V	V <sub>CC</sub> /2			
$V_{mo}$	1.5V	1.5V	V <sub>CC</sub> /2			
V <sub>x</sub>	V <sub>OL</sub> + 0.3V	V <sub>OL</sub> + 0.3V	V <sub>OL</sub> + 0.15V			
V <sub>y</sub>	V <sub>OH</sub> – 0.3V	V <sub>OH</sub> – 0.3V	V <sub>OH</sub> – 0.15V			







24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC24

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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: http://oceanchips.ru/

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А