

# 74LVC162373A; 74LVCH162373A

16-bit D-type transparent latch; 30  $\Omega$  series termination resistors; 5 V tolerant inputs/outputs; 3-state

Rev. 4 — 14 May 2013

Product data sheet

## 1. General description

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The 74LVC162373A and 74LVCH162373A are 16-bit D-type transparent latches with separate D-type inputs with bus hold (74LVCH162373A only) for each latch and 3-state outputs for bus-oriented applications. One latch enable (pin nLE) input and one output enable (pin n $\overline{\text{OE}}$ ) are provided for each octal. Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications. The device consists of two sections of eight D-type transparent latches with 3-state true outputs. When pin nLE is HIGH, data at the corresponding data inputs (pins nDn) enter the latches. In this condition, the latches are transparent, that is, the latch output changes each time its corresponding data inputs changes. When pin nLE is LOW, the latches store the information that was present at the data inputs a set-up time preceding the HIGH to LOW transition of pin nLE. When pin n $\overline{\text{OE}}$  is LOW, the contents of the eight latches are available at the outputs. When pin n $\overline{\text{OE}}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of the n $\overline{\text{OE}}$  input does not affect the state of the latches.

The device is designed with 30  $\Omega$  series termination resistors in both HIGH and LOW output stages to reduce line noise. Bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

## 2. Features and benefits

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- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Multibyte flow-through standard pinout architecture
- Multiple low inductance supply pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74LVCH162373A only)
- High-impedance when  $V_{\text{CC}} = 0$  V
- Complies with JEDEC standard:
  - ◆ JESD8-7A (1.65 V to 1.95 V)
  - ◆ JESD8-5A (2.3 V to 2.7 V)
  - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)

- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-B exceeds 200 V
  - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC162373ADGG 74LVCH162373ADGG	-40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVC162373ADL 74LVCH162373ADL	-40 °C to +125 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1

### 4. Functional diagram



Fig 1. Logic symbol

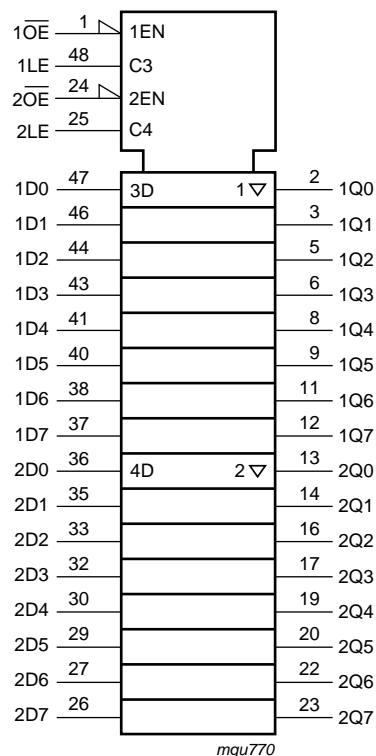


Fig 2. IEC logic symbol



**Fig 3. Logic diagram**



**Fig 4. Bus hold circuit**

## 5. Pinning information

### 5.1 Pinning



Fig 5. Pin configuration (T)SSOP48

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$	1	output enable input (active LOW)
$2\overline{OE}$	24	output enable input (active LOW)
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC</sub>	7, 18, 31, 42	supply voltage
1LE	48	latch enable input (active HIGH)
2LE	25	latch enable input (active HIGH)
1D[0:7]	47, 46, 44, 43, 41, 40, 38, 37	data input
2D[0:7]	36, 35, 33, 32, 30, 29, 27, 26	data input
1Q[0:7]	2, 3, 5, 6, 8, 9, 11, 12	data output
2Q[0:7]	13, 14, 16, 17, 19, 20, 22, 23	data output

## 6. Functional description

Table 3. Functional table (per section of 8 bits)<sup>[1]</sup>

Operating modes	Input			Internal Latch	Output nQn
	nOE	nLE	nDn		
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

- [1] H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition  
 Z = high-impedance OFF-state

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		<sup>[1]</sup> -0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$V_O$	output voltage	output HIGH or LOW state	<sup>[2]</sup> -0.5	$V_{CC} + 0.5$	V
		output 3-state	<sup>[2]</sup> -0.5	+6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	$^{\circ}$ C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ $^{\circ}$ C to +125 $^{\circ}$ C	<sup>[3]</sup> -	500	mW

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.  
 [2] The output voltage ratings may be exceeded if the output current ratings are observed.  
 [3] Above 60  $^{\circ}$ C, the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW state	0	-	V <sub>CC</sub>	V
		output 3-state	0	-	5.5	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.65 V to 2.7 V	0	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	0.65 × V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V <sub>CC</sub> - 0.3	-	V
		I <sub>O</sub> = -2 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 2.3 V	1.7	-	-	1.55	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 3.0 V	2.2	-	-	2.0	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I <sub>O</sub> = 2 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND <sup>[2]</sup>	-	±0.1	±5	-	±20	μA

**Table 6. Static characteristics ...continued**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 3.6$ V; $V_O = 5.5$ V or GND <sup>[2]</sup>	-	0.1	$\pm 5$	-	$\pm 20$	$\mu$ A
$I_{OFF}$	power-off leakage current	$V_{CC} = 0$ V; $V_I$ or $V_O = 5.5$ V	-	0.1	$\pm 10$	-	$\pm 20$	$\mu$ A
$I_{CC}$	supply current	$V_{CC} = 3.6$ V; $V_I = V_{CC}$ or GND; $I_O = 0$ A	-	0.1	20	-	80	$\mu$ A
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 2.7$ V to 3.6 V; $V_I = V_{CC} - 0.6$ V; $I_O = 0$ A	-	5	500	-	5000	$\mu$ A
$C_I$	input capacitance	$V_{CC} = 0$ V to 3.6 V; $V_I = \text{GND}$ to $V_{CC}$	-	5.0	-	-	-	pF
$I_{BHL}$	bus hold LOW current	$V_{CC} = 1.65$ ; $V_I = 0.58$ V <sup>[3][4]</sup>	10	-	-	10	-	$\mu$ A
		$V_{CC} = 2.3$ ; $V_I = 0.7$ V	30	-	-	25	-	$\mu$ A
		$V_{CC} = 3.0$ ; $V_I = 0.8$ V	75	-	-	60	-	$\mu$ A
$I_{BHH}$	bus hold HIGH current	$V_{CC} = 1.65$ ; $V_I = 1.07$ V <sup>[3][4]</sup>	-10	-	-	-10	-	$\mu$ A
		$V_{CC} = 2.3$ ; $V_I = 1.7$ V	-30	-	-	-25	-	$\mu$ A
		$V_{CC} = 3.0$ ; $V_I = 2.0$ V	-75	-	-	-60	-	$\mu$ A
$I_{BHLO}$	bus hold LOW overdrive current	$V_{CC} = 1.95$ V <sup>[3][5]</sup>	200	-	-	200	-	$\mu$ A
		$V_{CC} = 2.7$ V	300	-	-	300	-	$\mu$ A
		$V_{CC} = 3.6$ V	500	-	-	500	-	$\mu$ A
$I_{BHHO}$	bus hold HIGH overdrive current	$V_{CC} = 1.95$ V <sup>[3][5]</sup>	-200	-	-	-200	-	$\mu$ A
		$V_{CC} = 2.7$ V	-300	-	-	-300	-	$\mu$ A
		$V_{CC} = 3.6$ V	-500	-	-	-500	-	$\mu$ A

[1] All typical values are measured at  $V_{CC} = 3.3$  V (unless stated otherwise) and  $T_{amb} = 25$  °C.[2] The bus hold circuit is switched off when  $V_I > V_{CC}$  allowing 5.5 V on the input pin.

[3] Valid for data inputs (74LVCH162373A) only; control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data inputs holds the input below the specified  $V_I$  level.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nDn to nQn; see <a href="#">Figure 6</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	12	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	6.6	15.0	1.5	17.2	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	3.5	7.4	1.0	8.5	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.5	6.7	1.5	8.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.0	5.9	1.0	7.5	ns
		nLE to nQn; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 1.2 V	-	14	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.4	7.6	16.0	2.4	18.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	4.0	7.9	1.7	9.1	ns
t <sub>en</sub>	enable time	nOE to nQn; see <a href="#">Figure 8</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	18	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.7	7.1	15.6	1.7	17.9	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	4.0	8.2	1.5	9.4	ns
		V <sub>CC</sub> = 2.7 V	1.5	4.2	7.5	1.5	9.5	ns
t <sub>dis</sub>	disable time	nOE to nQn; see <a href="#">Figure 8</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	11	-	-	-	ns
		V <sub>CC</sub> = 1.65 V	2.5	4.2	8.5	2.5	9.8	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.3	4.6	1.0	5.3	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.2	4.8	1.5	6.0	ns
t <sub>w</sub>	pulse width	nLE HIGH; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	5.0	-	-	5.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns
		V <sub>CC</sub> = 2.7 V	3.0	-	-	3.0	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	3.0	2.0	-	3.0	-	ns
t <sub>su</sub>	set-up time	nDn to nLE; see <a href="#">Figure 9</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	3.0	-	-	3.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.5	-	-	2.5	-	ns
		V <sub>CC</sub> = 2.7 V	2.0	-	-	2.0	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	1.0	-	2.0	-	ns



**Table 7. Dynamic characteristics ...continued**Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			-40 °C to +125 °C		Unit	
			Min	Typ <sup>[1]</sup>	Max	Min	Max		
t <sub>h</sub>	hold time	nDn to nLE; see <a href="#">Figure 9</a>							
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.5	-	-	2.5	-	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.0	-	-	2.0	-	ns	
		V <sub>CC</sub> = 2.7 V	0.9	-	-	0.9	-	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	+0.9	-1.0	-	+0.9	-	ns	
t <sub>sk(o)</sub>	output skew time	V <sub>CC</sub> = 3.0 V to 3.6 V	<a href="#">[3]</a>	-	-	1.0	-	1.5	ns
C <sub>PD</sub>	power dissipation capacitance	per input; V <sub>I</sub> = GND to V <sub>CC</sub>	<a href="#">[4]</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	10.8	-	-	-	-	pF
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	13.0	-	-	-	-	pF
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	15.0	-	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz

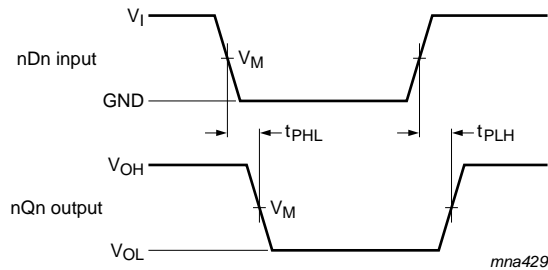
C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs

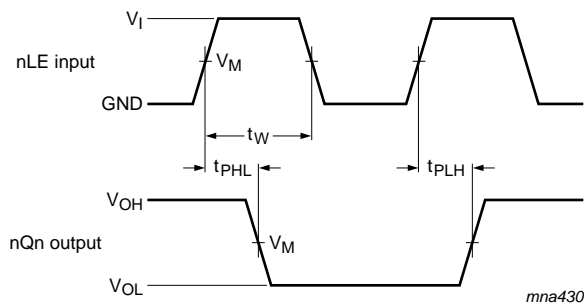
## 11. AC waveforms



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 6. Input (nDn) to output (nQn) propagation delays**



Measurement points are given in [Table 8](#).

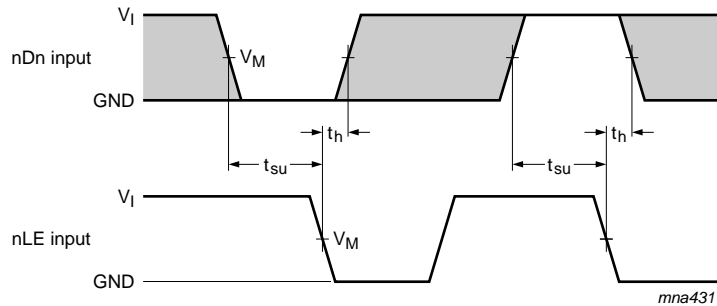
$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 7. Latch enable (nLE) pulse width, and the latch enable input to output (nQn) propagation delays**



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 8. 3-state enable and disable times**



Measurement points are given in [Table 8](#). The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 9. Data set-up and hold times for the nDn input to the nLE input**

**Table 8. Measurement points**

Supply voltage	Input		Output		
	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
1.2 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.65 V to 1.95 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 10. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

## 12. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



Fig 11. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

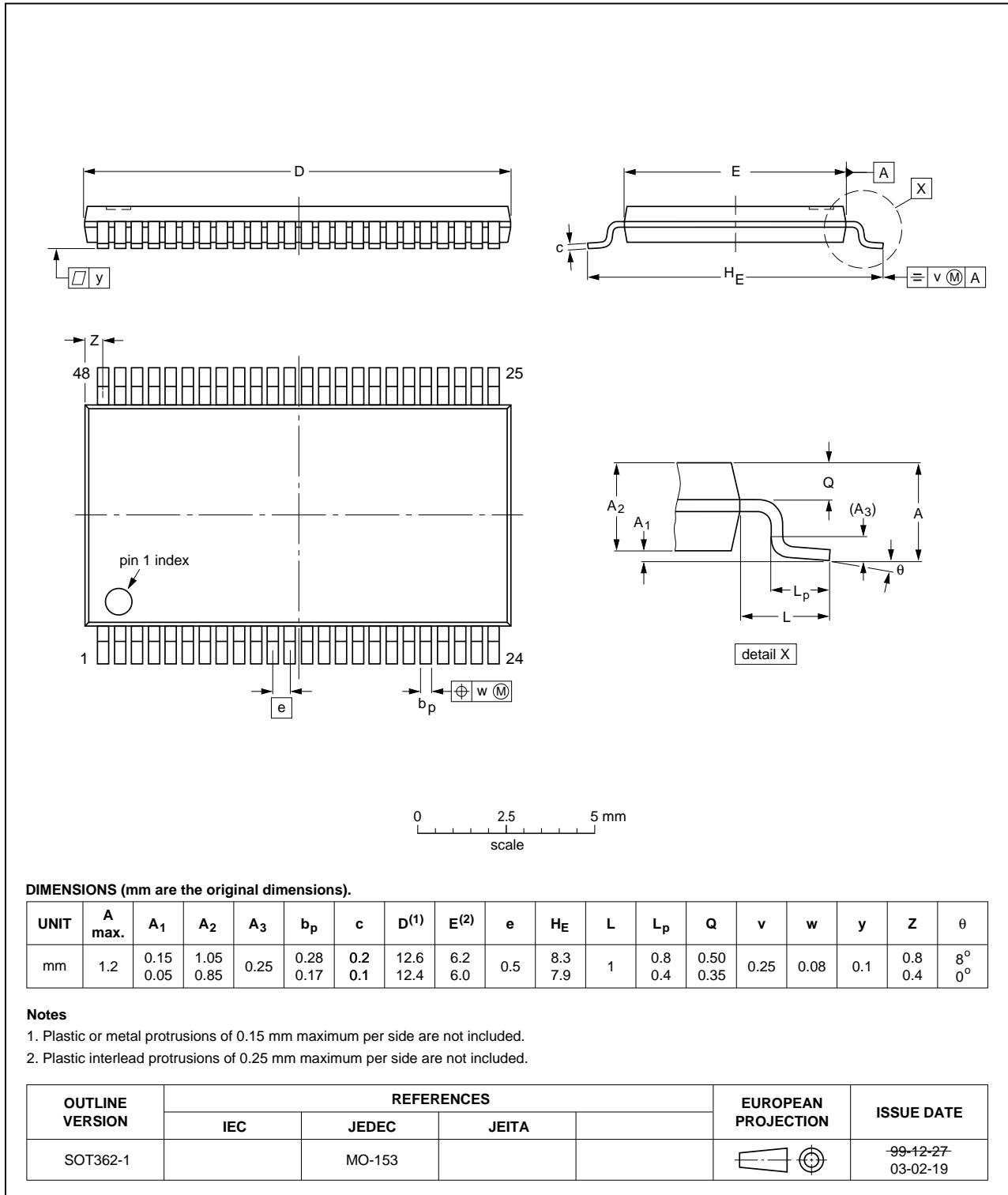


Fig 12. Package outline SOT362-1 (TSSOP48)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH162373A v.4	20130514	Product data sheet	-	74LVC_LVCH162373A v.3
Modifications:	<ul style="list-style-type: none"> <li>• Typenumbers: 74LVC162373ADGG and 74LVC162373ADL added.</li> </ul>			
74LVC_LVCH162373A v.3	20130118	Product data sheet	-	74LVC_LVCH162373A v.2
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Table 5</a>, <a href="#">Table 6</a>, <a href="#">Table 7</a>, <a href="#">Table 8</a> and <a href="#">Table 9</a>: values added for lower voltage ranges.</li> </ul>			
74LVC_LVCH162373A v.2	20040205	Product specification	-	74LVC_LVCH162373A v.1
74LVC_LVCH162373A v.1	19980805	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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