

## PI3HDX1204E

# HDMI 2.0 6Gbps Linear Redriver Level Shifter Near to the Sink/DFE-side application

## Description

PI3HDX1204E is the HDMI 2.0 Linear Redriver with the Level Shifter, supporting the minimum additive jitters. The linear Redriver provides the easiness of handling the signal integrity issues known in the component placement and the setting parameters of Equalization and Flat Gain compensation between Source-side and Sink-side link system.

The advantage of Linear Redriver does not block the original source differential signals to maximize the Sink-side Receiver Digital Feedback Equalization (DFE) Feedback circuits to improve the high-speed linked signal quality. The output swing range can set by Swing control for the power saving.

The optimization of the signal quality over a variety of physical mediums by reducing Inter-symbol Interference (ISI) jitters can be done by the pin-strapping or I2C programming.

In EEPROM mode, the Equalization, Voltage Swing and Gain controls can be automatically loaded during the system power-up to eliminate the need of external microprocessor or software driver.

## Features

- **HDMI 2.0 Compliant TMDS Linear Redriver with 2x Improved Jitter Performance than conventional technology**
- **DP++ Level Shifting for HDMI output**
- **Linear Redriver increases TMDS Link Margin supporting Sink-side DFE (Decision Feedback Equalizers) receiver**
- **Every Channel's Equalizations, Swings and Gains are programmable Independently**
- **Support Pin- strap and I2C Programming**
- **Flexible 4-bit I2C address selectable (42-pin, ZH package)**
- **Power supply: 3.3V**
- **Package (Pb-Free & Green):**
  - 32-pin TQFN (3x6mm)
  - 42-pin TQFN (3.5x9mm)

## Applications

- **TVs and Monitors near to the Sink-side Devices**

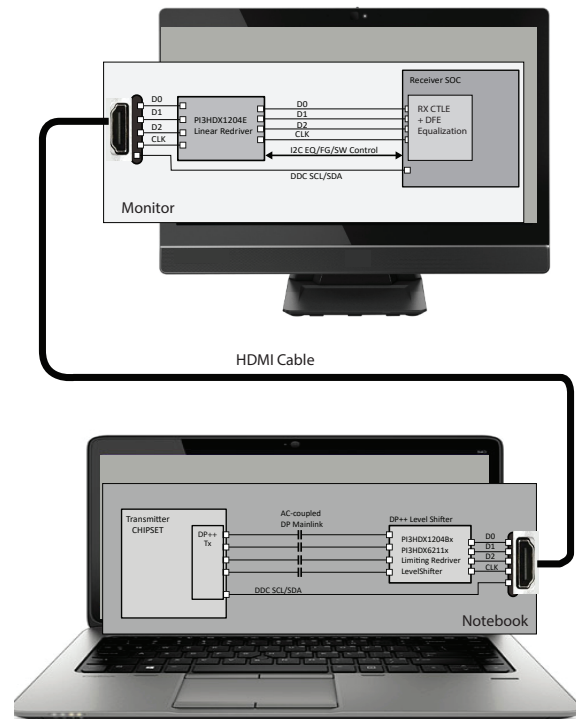


Figure 1. Monitor for sink-side with Rx DFE receiver

## Ordering Information

| Ordering Number  | Package Code | Eco Plan                     |
|------------------|--------------|------------------------------|
| PI3HDX1204E ZLEX | ZL           | Pb-free & Green, 32-pin TQFN |
| PI3HDX1204E ZHEX | ZH           | Pb-free & Green, 42pin TQFN  |

## 2. General Information

### 2.1 Revision History

| Revision   | Description   |
|------------|---|
| March 2016 | Pin-out (p8): FGx(x=0,1) Pin name typo fixed.   |
| April 2016 | Electrical(p17): tSK_INTRA_OUT changed 5 typ, 10 max ps   |
| May 2016   | Application(p30): More informative system EE contents added. DDC source-side pull-up changed to 10 kOhm from 2 kOhm   |
| June 2016  | Mechanical (p39): EPAD outline changed  |
| Oct 2016   | Diodes Disclaimer added   |
| Aug 2017   | Clarified Output Swing range control in functional description.<br>PI3HDX1204B1 limiting and PI3HDX1204E linear pin-out comparison added in generic information session |
| Dec 2017   | Updated package mechanical drawing with latest (p46).   |

### 2.2 PI3HDX1204D to PI3HDX1204E PDN Notice

PI3HDX1204E is a production part number of PI3HDX1204D. The detail comparison is summarized below.

|                  | PI3HDX1204E  | PI3HDX1204D  |
|------------------|--|--|
| Changes          | 32-pin TQFN package added  | EOL (End of Life).<br>PI3HDX1204D was engineering version of PI3HDX1204E |
| Pin-out          | No change  |  |
| Function control | No change  |  |
| Application Note | PI3HDX1204D application note and schematics are applicable to the PI3HDX1204E. |  |

### 2.3 Similar Products Comparison

|                                | PI3HDX1204B1   | PI3HDX1204E                                       |
|--------------------------------|--|---|
| Redriver Type                  | Limiting type  | Linear type                                       |
| EQ at 6Gbps                    | 22 dB  | 10 dB   |
| Output TMDS peak-to-peak Swing | Output Swing Amplitude / Pre-Emphasis control. Blocking type | Follow Source Swing Amplitude. Non-blocking type. |
| DDC Switch/Buffer              | No   | No  |
| HDMI1.4/2.0 Type ID            | No   | No  |
| Ioff Protection                | External Power Switch  | External Power Switch                             |
| Data Rate (Gbps)               | 6 Gbps   | 6 Gbps  |
| Application                    | Near to Source-side device                                   | Near to Sink-side device                          |
| Availability                   | Production   | Production  |

| PI3HDX1204B1 / PI3HDX1204E Pin out Co-layout Comparison  | Connection Description   |
|--|--|
| <p>SW1<br/>SW0</p> <p>DNC<br/>DNC</p> <p>PI3HDX1204B1</p> <p>PI3HDX1204E</p> <p>PRCNT#<br/>ENI2C</p> <p>EQ3/AD3<br/>EQ2/AD2<br/>EQ1/AD1<br/>EQ0/AD0</p> <p>BST3<br/>BST2<br/>BST1<br/>BST0</p> <p>42 41 40 39</p> <p>DE1 1<br/>DE0 2<br/>VCC 3<br/>A0RX+ 4<br/>A0RX- 5<br/>GND 6<br/>A1RX+ 7<br/>A1RX- 8<br/>VCC 9<br/>A2RX+ 10<br/>A2RX- 11<br/>GND 12<br/>A3RX+ 13<br/>A3RX- 14<br/>VCC 15<br/>A1 16<br/>A4 17</p> <p>38 PS1<br/>37 PS0<br/>36 VCC<br/>35 A0TX+<br/>34 A0TX-<br/>33 VCC<br/>32 A1TX+<br/>31 A1TX-<br/>30 VCC<br/>29 A2TX+<br/>28 A2TX-<br/>27 VCC<br/>26 A3TX+<br/>25 A3TX-<br/>24 VCC<br/>23 VOD1<br/>22 A0</p> <p>FG1/I2C_RESET#<br/>FG0</p> <p>DNC<br/>I2C_DONE</p> | <p>Connection Description</p> <p>Pin 16,17,23: Do not connect in PI3HDX1204E<br/>Pin 1,2,20,21,22,37,38,39,40,41,42: Pull-up and Pull-down pin mode control pins</p> |

## 2.4 Related Products

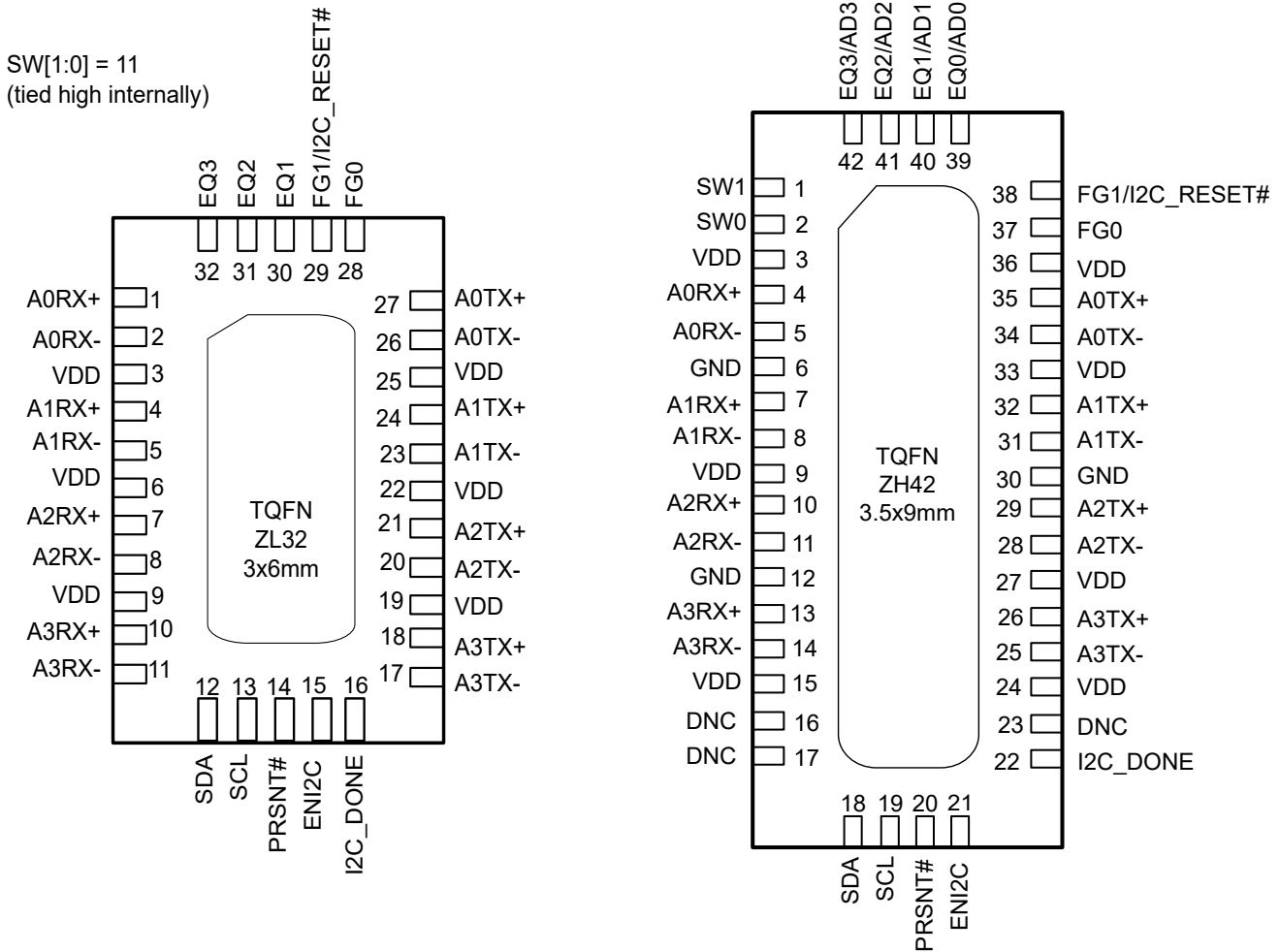
| Part Numbers                | Products Description  |
|-----------------------------|---|
| Retimers / Jitter Cleaner   |   |
| PI3HDX2711B                 | HDMI 2.0 and DP++ Retimer (Jitter Cleaner)  |
| PI3HDX711B                  | HDMI 1.4 and DP++ ReTimer (Jitter Cleaner)  |
| Redrivers                   |   |
| PI3DPX1203B                 | DisplayPort 1.4 Redriver for Source/Sink/Cable Application, Linear-type                         |
| PI3HDX1204B1                | HDMI 2.0 Redriver (DP++ Level Shifter), High EQ, place near to the source-side, Limiting type   |
| PI3HDX1204E                 | HDMI 2.0 Linear Redriver (DP++ Level Shifter) , Link transparent, place near to the sink-side   |
| PI3DPX1207B                 | DisplayPort 1.4 Alt Type-C Redriver, 8.1 Gbps and USB3.1 10 Gbps, Link Transparent              |
| PI3DPX1202A                 | Low Power DisplayPort 1.2 Redriver with built-in AUX Listener, Limiting-type                    |
| PI3HDX511F                  | High EQ HDMI 1.4b Redriver and DP++ Level Shifter for Sink/Source Application, Limiting-type    |
| Active Switches & Splitters |   |
| PI3DPX1205A                 | DisplayPort 1.4 Alt Type-C Mux Redriver, 8.1 Gbps and USB3.1 10 Gbps, Link Transparent          |
| PI3HDX231                   | HDMI 2.0 3:1 ports Mux Redriver, Linear-type  |
| PI3HDX414                   | HDMI 1.4b 1:4 Demux Redriver & Splitter for 3.4 Gbps Application, Limiting-type                 |
| PI3HDX412BD                 | HDMI 1.4b 1:2 Demux Redriver & Splitter for 3.4 Gbps Application, Limiting-type                 |
| PI3HDX621                   | HDMI 1.4 Redriver 2:1 Active Switch with built-in ARC and Fast Switching support, Limiting-type |

## Contents

|   |    |
|---|----|
| <b>1. Product Brief</b>                   | 1  |
| <b>2. General Information</b>             | 2  |
| 2.1 Revision History                      | 2  |
| 2.2 PI3HDX1204D to PI3HDX1204E PDN Notice | 2  |
| 2.3 Similar Products Comparison           | 2  |
| 2.4 Related Products                      | 4  |
| <b>3. Pin Configuration</b>               | 6  |
| 3.1 Package Pin-out                       | 6  |
| 3.2 Pin Description                       | 7  |
| <b>4. Functional</b>                      | 11 |
| 4.1 Functional Block                      | 11 |
| 4.2 Function Description                  | 12 |
| <b>5. I2C Programming</b>                 | 16 |
| 5.1 Programming registers                 | 16 |
| 5.2 I2C operation                         | 18 |
| <b>6. Electrical Specification</b>        | 20 |
| 6.1 Absolute Maximum ratings              | 20 |
| 6.2 Recommended operating conditions      | 20 |
| 6.3 Electrical characteristics            | 20 |
| 6.4 I2C Interface Bus                     | 25 |
| <b>7. Applications</b>                    | 27 |
| 7.1 DC/AC-coupled Application             | 27 |
| 7.2 Sink-side Redriver Application        | 28 |
| 7.3 Channels/Polarity Swap                | 28 |
| 7.4 Output Eye Diagram                    | 29 |
| 7.5 Layout Guidelines                     | 33 |
| 7.6 HDMI 2.0 Compliance Test              | 39 |
| <b>8. Mechanical/Packaging</b>            | 42 |
| 8.1 Mechanical Outline                    | 42 |
| 8.2 Part Marking Information              | 45 |
| 8.3 Tape & Reel Materials and Design      | 46 |
| <b>9. Important Notice</b>                | 49 |

### 3. Pin Configuration

#### 3.1 Package Pin-out



**Figure 3-1 32/42-pin package pin-out**

**Note:** In TMDS Data and Clock Differential Pairs of Input and Output, the polarity (+/- or P/N) of each pairs and high-speed data channels A[3:0] can use interchangeably. Output pins of polarity and data channel will always follow the input polarity and data channel assignment changes.

## 3.2 Pin Description

### 3.2.1 32-pin package

| Pin #                  | Pin Name       | Type | Description  |
|------------------------|----------------|------|--|
| <b>Data Signals</b>    |                |      |  |
| 1<br>2                 | A0RX+<br>A0RX- | I    | TMDS differential positive/negative input for Channel A0, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.  |
| 27<br>26               | A0TX+<br>A0TX- | O    | TMDS differential positive/negative outputs for Channel A0, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.  |
| 4<br>5                 | A1RX+<br>A1RX- | I    | TMDS differential positive/negative inputs for Channel A1, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.   |
| 24<br>23               | A1TX+<br>A1TX- | O    | TMDS differential positive/negative outputs for Channel A1, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.  |
| 7<br>8                 | A2RX+<br>A2RX- | I    | TMDS differential positive/negative inputs for Channel A2, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.   |
| 21<br>20               | A2TX+<br>A2TX- | O    | TMDS differential positive/negative outputs for Channel A2, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.  |
| 10<br>11               | A3RX+<br>A3RX- | I    | TMDS differential positive/negative inputs for Channel A3, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.   |
| 18<br>17               | A3TX+<br>A3TX- | O    | TMDS differential positive/negative outputs for Channel A3, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.  |
| <b>Control Signals</b> |                |      |  |
| 12                     | SDA            | I/O  | I <sup>2</sup> C Serial Data line  |
| 13                     | SCL            | I/O  | I <sup>2</sup> C Serial Clock line<br>In Master mode (ENI2C pin floating), SCL is an output. Otherwise it is an input as a slave mode.   |
| 14                     | PRSNT#         | I    | Cable Present Detect input. This pin has internal 100KΩ pull-up.<br>The pin is active when both PIN mode ( ENI2C = LOW) and I2C mode ( ENI2C = HIGH).<br>When High, a cable is not present, and the device is put in lower power mode.<br>When Low, the device is enabled and in normal operation. |
| 15                     | ENI2C          | I    | I2C Enable pin.<br>When LOW, each channel is programmed by the external pin voltage.<br>When HIGH, each channel is programmed by the data stored in the I <sup>2</sup> C bus.<br>When floating, master mode (Read External EEPROM)   |
| 32,31,30               | EQ[3:1]        | I    | EQ Control pin. Inputs with internal 100kΩ pull-up.<br>This pins set the amount of Equalizer Boost in all channels when ENI2C is low.  |
|                        | AD[3:1]        | I    | Address bits control pins for I2C programming with internal 100kΩ pull-up.   |

| Pin #             | Pin Name        | Type | Description   |
|-------------------|-----------------|------|---|
| 29                | FG1/I2C_RE-SET# | I    | Shared pin for Gain Control bit-1 and I2C Reset pin. Inputs with internal 100kΩ pull up resistor.<br>(1) Sets the output flat gain level bit-1 on all channels when ENI2C is Low.<br>(2) I2C Reset pin. Active Low to reset the registers to default state. |
| 28                | FG0             | I    | Flat Gain control bit-0 pin. Inputs with internal 100kΩ pull up resistor.<br>Sets the output flat gain level on all channels when ENI2C is low.   |
| 16                | I2C_DONE        | O    | I2C Done pin. Valid register load status output for using the daisy chain I2C master.<br>Low = External EEPROM load failed<br>High = External EEPROM load passed  |
| <b>Power Pins</b> |                 |      |   |
| 3,6,9,19,22,25    | VDD             | PWR  | 3.3V Power supply pins  |
| Center Pad        | GND             | GND  | Exposed Ground pad.   |



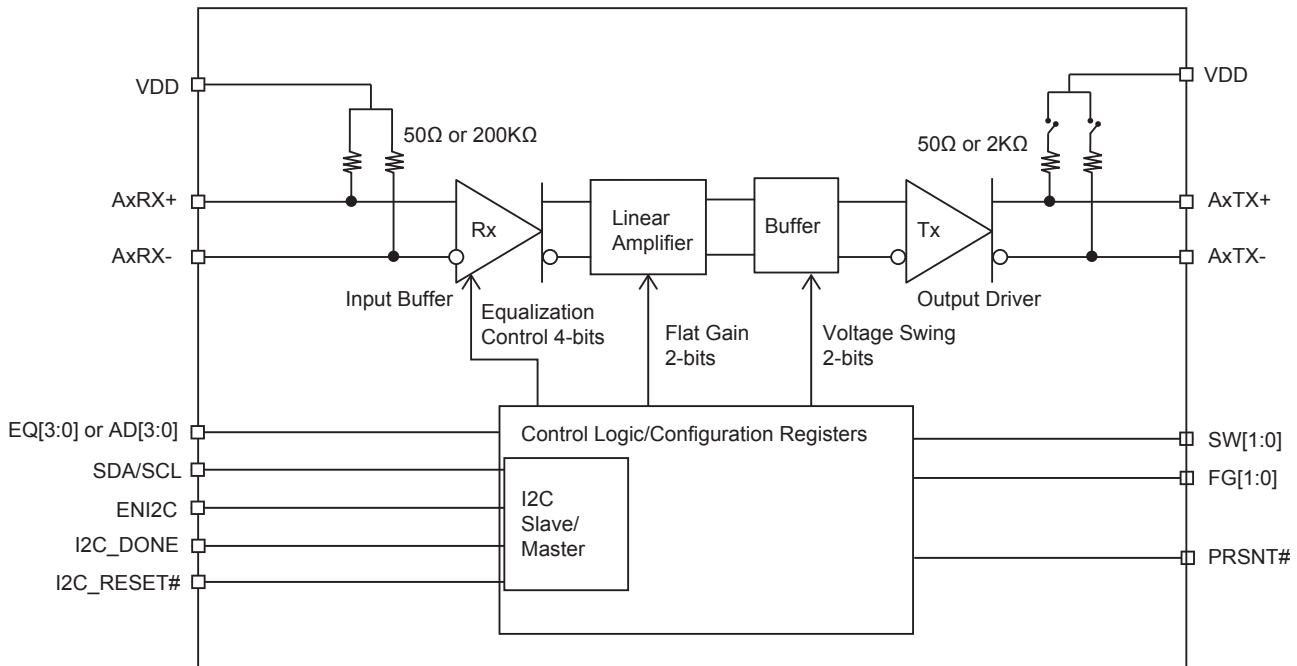
### 3.2.2 42-pin package

| Pin #                  | Pin Name       | Type | Description  |
|------------------------|----------------|------|--|
| <b>Data Signals</b>    |                |      |  |
| 4<br>5                 | A0RX+<br>A0RX- | I    | TMDS differential positive/negative input for Channel A0, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.  |
| 35<br>34               | A0TX+<br>A0TX- | O    | TMDS differential positive/negative outputs for Channel A0, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.  |
| 7<br>8                 | A1RX+<br>A1RX- | I    | TMDS differential positive/negative inputs for Channel A1, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.   |
| 32<br>31               | A1TX+<br>A1TX- | O    | TMDS differential positive/negative outputs for Channel A1, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.  |
| 10<br>11               | A2RX+<br>A2RX- | I    | TMDS differential positive/negative inputs for Channel A2, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.   |
| 29<br>28               | A2TX+<br>A2TX- | O    | TMDS differential positive/negative outputs for Channel A2, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.  |
| 13<br>14               | A3RX+<br>A3RX- | I    | TMDS differential positive/negative inputs for Channel A3, with internal 50Ω Pull-Up and ~200kΩ Pull-Up otherwise.   |
| 26<br>25               | A3TX+<br>A3TX- | O    | TMDS differential positive/negative outputs for Channel A3, with internal 50Ω Pull-Up and ~2kΩ Pull-Up otherwise.  |
| <b>Control Signals</b> |                |      |  |
| 16,17,23               | DNC            |      | Do Not Connect   |
| 19                     | SCL            | I/O  | I <sup>2</sup> C Serial Clock line<br>In Master mode (ENI2C pin floating), SCL is an output. Otherwise it is an input as a slave mode.   |
| 18                     | SDA            | I/O  | I <sup>2</sup> C Serial Data line  |
| 20                     | PRSNT#         | I    | Cable Present Detect input.<br>This pin has internal 100KΩ pull-up. The pin is active when both PIN mode ( ENI2C = LOW) and I2C mode ( ENI2C = HIGH).<br>When High, a cable is not present, and the device is put in lower power mode.<br>When Low, the device is enabled and in normal operation. |
| 21                     | ENI2C          | I    | I2C Enable pin.<br>When LOW, each channel is programmed by the external pin voltage.<br>When HIGH, each channel is programmed by the data stored in the I <sup>2</sup> C bus.<br>When floating, master mode (Read External EEPROM)   |

| Pin #                    | Pin Name       | Type | Description   |
|--------------------------|----------------|------|---|
| 39,40,41,42              | EQ[3:0]        | I    | EQ Control pin.<br>Inputs with internal 100kΩ pull-up. This pins set the amount of Equalizer Boost in all channel when ENI2C is LOW.  |
|                          | AD[3:0]        | I    | I <sup>2</sup> C address bits control pins for programming with internal 100kΩ pull-up.   |
| 1,2                      | SW[1:0]        | I    | Output Swing control pins. Inputs with internal 100kΩ pull-up. This pin sets the output Voltage Level in all channel when ENI2C is LOW.   |
| 37                       | FG0            | I    | Gain Control pin bit 0<br>Inputs with internal 100kΩ pull up resistor. Sets the output flat gain level on all channels when ENI2C is low.   |
| 38                       | FG1/I2C_RESET# | I    | Shared pin for Flat Gain control bit-1 or I2C Reset pin. Inputs with internal 100kΩ pull up resistor.<br>(1) Sets the output flat gain level bit-1 on all channels when ENI2C is Low.<br>(2) I2C Reset pin. Active Low to reset the registers to default state. |
| 22                       | I2C_DONE       | O    | I2C Done pin. Valid register load status output, use for daisy chain master<br>Low = External EEPROM load failed<br>High = External EEPROM load passed  |
| <b>Power Pins</b>        |                |      |   |
| 3, 9, 15, 24, 27, 33, 36 | VDD            | PWR  | 3.3V Power Supply pins  |
| 6, 12, 30,<br>Center Pad | GND            | GND  | Exposed Ground pad.   |

## 4. Functional

### 4.1 Functional Block



**Figure 4-1 Functional Block Diagram**

## 4.2 Function Description

### 4.2.1 Power-Down/Enable

When PRSNT# is set to "1", device enter to the power-down mode. When Input 200k $\Omega$  and Output High Impedance (HIZ) termination resistors set, each individual channels Ax(x=0,1,2,3) can program the I2C register.

### 4.2.2 Input Equalization Setting

The EQx(x=0,1,2,3) pins are the pin-strap option for each Ax(x=0,1,2,3) channels. It can also be programmable by the I2C mode.

Table 4-1. Equalization Setting for 42-pin

| EQ3 | EQ2 | EQ1 | EQ0 | 6Gbps Input(dB) |
|-----|-----|-----|-----|-----------------|
| 0   | 0   | 0   | 0   | 3.6             |
| 0   | 0   | 0   | 1   | 4.0             |
| 0   | 0   | 1   | 0   | 4.4             |
| 0   | 0   | 1   | 1   | 4.7             |
| 0   | 1   | 0   | 0   | 5.1             |
| 0   | 1   | 0   | 1   | 5.5             |
| 0   | 1   | 1   | 0   | 5.9             |
| 0   | 1   | 1   | 1   | 6.2             |
| 1   | 0   | 0   | 0   | 6.6             |
| 1   | 0   | 0   | 1   | 6.9             |
| 1   | 0   | 1   | 0   | 7.3             |
| 1   | 0   | 1   | 1   | 7.6             |
| 1   | 1   | 0   | 0   | 8.0             |
| 1   | 1   | 0   | 1   | 8.2             |
| 1   | 1   | 1   | 0   | 8.6             |
| 1   | 1   | 1   | 1   | 8.9             |

**Table 4-2. Equalization Setting for 32-pin**

| EQ3 | EQ2 | EQ1 | 6 Gbps Input EQ(dB) | Notes  |
|-----|-----|-----|---------------------|--|
| 0   | 0   | 0   | 4.0                 | (1) EQ0 pin always tied to "1" internally in 32-pin package. |
| 0   | 0   | 1   | 4.7                 |  |
| 0   | 1   | 0   | 5.5                 |  |
| 0   | 1   | 1   | 6.2                 |  |
| 1   | 0   | 0   | 6.9                 |  |
| 1   | 0   | 1   | 7.6                 |  |
| 1   | 1   | 0   | 8.2                 |  |
| 1   | 1   | 1   | 8.9                 |  |

#### 4.2.3 Output -1 dB Compression Swing setting

SW<sub>x</sub>(x=0,1) affects the linearity of the output when input amplitude changes.

**Table 4-3. SW[1:0] Output Swing Setting**

| SW1 | SW0 | Voltage Swing<br>mVpp @100MHz | Voltage Swing<br>mVpp @ 6Gbps | Notes                                      |
|-----|-----|-------------------------------|-------------------------------|--|
| 0   | 0   | 920                           | 1100                          |  |
| 0   | 1   | 1040                          | 1200                          |  |
| 1   | 0   | 1280                          | 1300                          |  |
| 1   | 1   | 1370                          | 1400                          | Default Setting. Internally 100kΩ pull-up. |

Note

(1) SW[1:0]=11 setting support by I2C programming in 32-pin package

#### 4.2.4 Flat Gain Setting

FG<sub>x</sub>(x=0,1) two pins are the selection 2 bits for the DC Flat Gain value.

**Table 4-4. Flat Gain FG[1:0] Control**

| FG1 | FG0 | Gain (dB) |
|-----|-----|-----------|
| 0   | 0   | -3.5 dB   |
| 0   | 1   | -1.5 dB   |
| 1   | 0   | +0.5 dB   |
| 1   | 1   | +2.5 dB   |

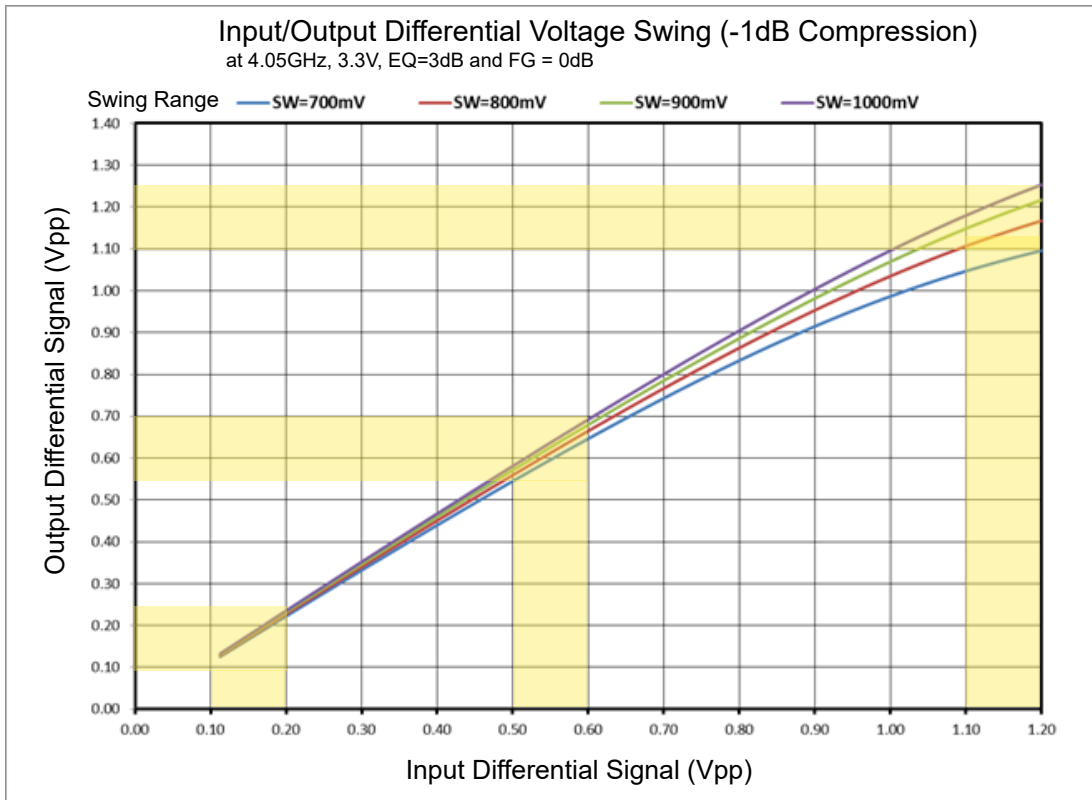


Figure 4-2 Example of Output voltage swing with different SW setting

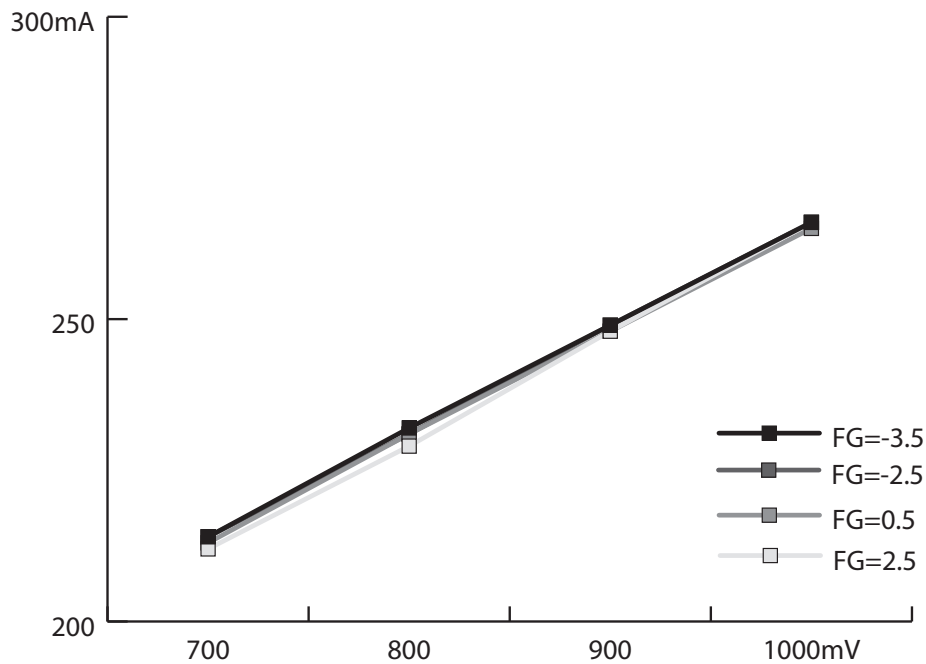
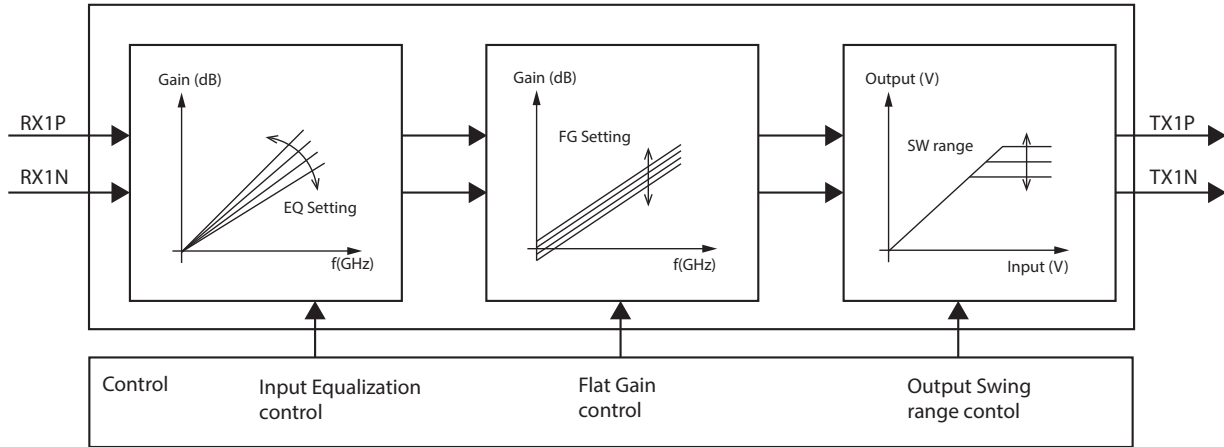


Figure 4-3 Power dissipation mA vs. SW[1:0] setting



**Figure 4-4 Illustration of EQ, Gain and Swing setting**

## 5. I2C Programming

### 5.1 Programming registers

#### 5.1.1 I2C address

| A6 | A5 | A4 | A3  | A2  | A1  | A0                 | R/W      |
|----|----|----|-----|-----|-----|--------------------|----------|
| 1  | 1  | 1  | AD3 | AD2 | AD1 | AD0 <sup>(1)</sup> | 1=R, 0=W |

Note:

(1) Address A0 is always "1" tied high for 32-pin package.

#### 5.1.2 Configuration Registers

| BYTE 0 |      |                    |             |                  |                |
|--------|------|--------------------|-------------|------------------|----------------|
| Bit    | Type | Power up condition | Description | Control affected | Comment        |
| 7:0    | R    |                    | Reserved    |                  |                |
| BYTE 1 |      |                    |             |                  |                |
| Bit    | Type | Power up condition | Description | Control affected | Comment        |
| 7:0    | R    |                    | Reserved    |                  |                |
| BYTE 2 |      |                    |             |                  |                |
| Bit    | Type | Power up condition | Description | Control affected | Comment        |
| 7      | R/W  | 0                  |             | A3 Power down    | 1 = Power down |
| 6      | R/W  | 0                  |             | A2 Power down    |                |
| 5      | R/W  | 0                  |             | A1 Power down    |                |
| 4      | R/W  | 0                  |             | A0 Power down    |                |
| 3      | R/W  | 0                  |             | Reserved         |                |
| 2      | R/W  | 0                  |             | Reserved         |                |
| 1      | R/W  | 0                  |             | Reserved         |                |
| 0      | R/W  | 0                  |             | Reserved         |                |

| BYTE 3 |      |                    |                          |                  |           |
|--------|------|--------------------|--------------------------|------------------|-----------|
| Bit    | Type | Power up condition | Description              | Control affected | Comment   |
| 7      | R/W  | 0                  | Channel A0 configuration | EQ3              | Equalizer |
| 6      | R/W  | 0                  |                          | EQ2              |           |
| 5      | R/W  | 0                  |                          | EQ1              |           |
| 4      | R/W  | 0                  |                          | EQ0              |           |
| 3      | R/W  | 0                  |                          | FG1              | Flat gain |
| 2      | R/W  | 0                  |                          | FG0              |           |
| 1      | R/W  | 0                  |                          | SW1              | Swing     |
| 0      | R/W  | 0                  |                          | SW0              |           |

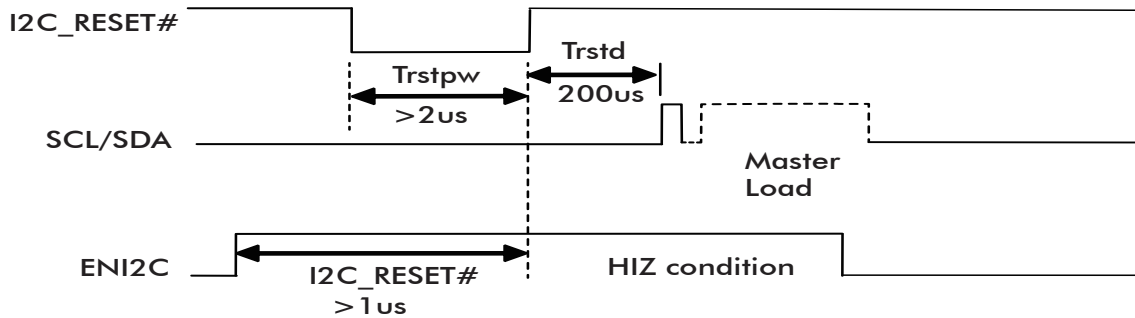


| BYTE 4                   |      |                    |                          |                  |           |
|--------------------------|------|--------------------|--------------------------|------------------|-----------|
| Bit                      | Type | Power up condition | Description              | Control affected | Comment   |
| 7                        | R/W  | 0                  | Channel A1 configuration | EQ3              | Equalizer |
| 6                        | R/W  | 0                  |                          | EQ2              |           |
| 5                        | R/W  | 0                  |                          | EQ1              |           |
| 4                        | R/W  | 0                  |                          | EQ0              |           |
| 3                        | R/W  | 0                  |                          | FG1              | Flat gain |
| 2                        | R/W  | 0                  |                          | FG0              |           |
| 1                        | R/W  | 0                  |                          | SW1              | Swing     |
| 0                        | R/W  | 0                  |                          | SW0              |           |
| BYTE 5                   |      |                    |                          |                  |           |
| Bit                      | Type | Power up condition | Description              | Control affected | Comment   |
| 7                        | R/W  | 0                  | Channel A2 configuration | EQ3              | Equalizer |
| 6                        | R/W  | 0                  |                          | EQ2              |           |
| 5                        | R/W  | 0                  |                          | EQ1              |           |
| 4                        | R/W  | 0                  |                          | EQ0              |           |
| 3                        | R/W  | 0                  |                          | FG1              | Flat gain |
| 2                        | R/W  | 0                  |                          | FG0              |           |
| 1                        | R/W  | 0                  |                          | SW1              | Swing     |
| 0                        | R/W  | 0                  |                          | SW0              |           |
| BYTE 6                   |      |                    |                          |                  |           |
| Bit                      | Type | Power up condition | Description              | Control affected | Comment   |
| 7                        | R/W  | 0                  | Channel A3 configuration | EQ3              | Equalizer |
| 6                        | R/W  | 0                  |                          | EQ2              |           |
| 5                        | R/W  | 0                  |                          | EQ1              |           |
| 4                        | R/W  | 0                  |                          | EQ0              |           |
| 3                        | R/W  | 0                  |                          | FG1              | Flat gain |
| 2                        | R/W  | 0                  |                          | FG0              |           |
| 1                        | R/W  | 0                  |                          | SW1              | Swing     |
| 0                        | R/W  | 0                  |                          | SW0              |           |
| BYTE 7                   |      |                    |                          |                  |           |
| Bit                      | Type | Power up condition | Description              | Control affected | Comment   |
| 7:0                      | R/W  |                    | Reserved                 |                  |           |
| BYTE 8-15                |      |                    |                          |                  |           |
| Bit                      | Type | Power up condition | Description              | Control affected | Comment   |
| power up condition : "0" |      |                    |                          |                  |           |

## 5.2 I2C operation

The integrated I2C interface operates as a slave device mode. Standard I2C mode (100 Kbps) is supported with 7-bit addressing and data byte format 8-bit.

The device supports Read/Write. The bytes must be accessed in sequential order from the lowest to the highest byte with the ability to stop after any complete byte has been transferred. Address bits A3 to A0 are programmable to support multiple chips environment. The Data is loaded until a Stop sequence is issued.



**Figure 5-1 I2C Reset, Enable and SCL/SDA Timing Diagram**

### Transferring Data

Every byte put on the SDA line must be 8-bit long. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see the I2C Data Transfer diagram). It will never hold the clock line SCL LOW to force the master into a wait state.

### Acknowledge

Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, it will pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse as indicated in the I2C Data Transfer diagram. It will generate an acknowledge after each byte has been received.

### Data Transfer

A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, it will watch the next byte of information for a match with its address setting. When a match is found it will respond with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit, except for the last byte of a read cycle which ends with a stop bit. Data is transferred with the most significant bit (MSB) first.

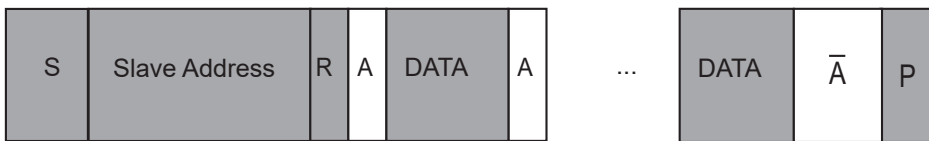
### Start & Stop Conditions

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

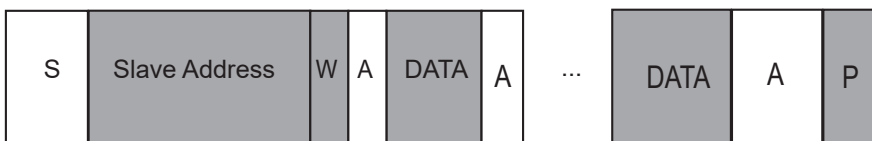
**Table 5-1. I2C Address Setting with 4-bits AD[3:0]**

| I2C address: AD3, AD2, AD1, AD0 | Data starting location |
|---------------------------------|------------------------|
| 0000                            | 00H                    |
| 0001                            | 10H                    |
| 0010                            | 20H                    |
| 0011                            | 30H                    |
| 0100                            | 40H                    |
| 0101                            | 50H                    |
| 0110                            | 60H                    |
| 0111                            | 70H                    |
| 1000                            | 80H                    |
| 1001                            | 90H                    |
| 1010                            | A0H                    |
| 1011                            | B0H                    |
| 1100                            | C0H                    |
| 1101                            | D0H                    |
| 1110                            | E0H                    |
| 1111                            | F0H                    |

**Read Sequence**



**Write Sequence**



From master to slave      A= acknowledge       $\bar{A}$ = not acknowledge  
 From slave to master      S= start condition      P= stop condition

**Figure 5-2 I2C Read / Write Timing Sequence**

## 6. Electrical Specification

### 6.1 Absolute Maximum ratings

|                                    |                            |
|------------------------------------|----------------------------|
| Supply Voltage to Ground Potential | -0.5 V to +4.6 V           |
| DC SIG Voltage                     | -0.5 V to $V_{DD} + 0.5$ V |
| Output Current                     | -25 mA to +25 mA           |
| Power Dissipation Continuous       | 2.1 W                      |
| ESD, HBM                           | -2 kV to +2 kV             |
| Storage Temperature                | -65 °C to +150 °C          |

Note  
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### 6.2 Recommended operating conditions

| Parameter  | Min. | Typ. | Max | Units |
|--|------|------|-----|-------|
| Power supply voltage (VDD to GND) <sup>(1)</sup>   | 3.0  | 3.3  | 3.6 | V     |
| I2C (SDA, SCL)                                     |      |      | 3.6 | V     |
| Supply Noise Tolerance up to 25 MHz <sup>(2)</sup> |      |      | 100 | mVp-p |
| Ambient Temperature                                | -40  | 25   | 85  | °C    |

Note  
(1) Typical parameters are measured at  $V_{CC} = 3.3 \pm 0.3$ V,  $T_A = 25^\circ\text{C}$ . They are for the reference purposes, and are not production-tested  
(2) Allow supply noise (mVp-p sine wave) under typical condition

### 6.3 Electrical characteristics

Over recommend operating supply and temperature range unless otherwise specified.

#### 6.3.1 LVCMOS DC specifications

| Symbol    | Parameter                           | Conditions | Min.             | Typ. | Max              | Unit |
|-----------|-------------------------------------|------------|------------------|------|------------------|------|
| $V_{IH}$  | DC input logic high                 |            | $V_{DD}/2 + 0.7$ |      | $V_{DD} + 0.3$   | V    |
| $V_{IL}$  | DC input logic low                  |            | -0.3             |      | $V_{DD}/2 - 0.7$ | V    |
| $V_{OH}$  | At $I_{OH} = -200\mu\text{A}$       |            | $V_{DD} + 0.2$   |      |                  | V    |
| $V_{OL}$  | At $I_{OL} = -200\mu\text{A}$       |            |                  |      | 0.2              | V    |
| $V_{hys}$ | Hysteresis of Schmitt trigger input |            | 0.8              |      |                  | V    |

#### 6.3.2 Power Dissipation

| Symbol    | Parameter                | Conditions                       | Min. | Typ. | Max. | Unit |
|-----------|--------------------------|----------------------------------|------|------|------|------|
| $I_{DD}$  | Supply current           | PRSENT#=0, SW=1000mVdiff, FG=2.5 |      | 256  | 290  | mA   |
|           |                          | PRSENT#=0, SW=900mVdiff, FG=2.5  |      | 240  |      | mA   |
|           |                          | PRSENT#=0, SW=800mVdiff, FG=2.5  |      | 233  |      | mA   |
| $I_{DDQ}$ | Quiescent supply current | PRSENT#=1, TMDS Output Disable   |      | 2.0  | 4.2  | mA   |

### 6.3.3 Package power ratings

| Package            | Theta Ja(still air)<br>(°C/W) | Theta Jc<br>(°C/W) | Max. Power Dissipation Rating<br>Ta ≤ 70° |
|--------------------|-------------------------------|--------------------|---|
| 32-pin TQFN (ZL32) | 37.05                         | 11.3               | 1.48W                                     |
| 42-pin TQFN (ZH42) | 33.69                         | 15.17              | 1.63W                                     |

### 6.3.4 Switching I/O characteristics

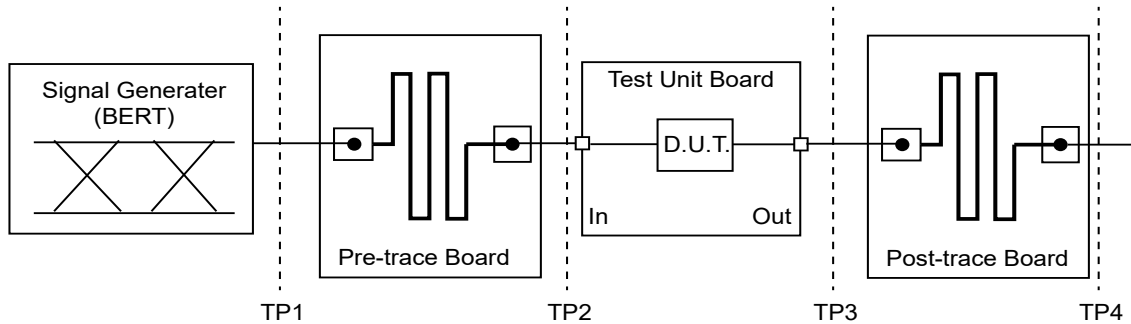
| Symbol                     | Parameter  | Conditions                                   | Min. | Typ. | Max. | Unit             |
|----------------------------|--|--|------|------|------|------------------|
| V <sub>RX-DIF-Fp-p</sub>   | Peak to peak differential input voltage                |  |      | 200  |      | mV               |
| T <sub>R</sub>             | Rise Time  | Input signal with 30ps rise time, 20% to 80% |      | 31   |      | ps               |
| T <sub>F</sub>             | Falling Time   | Input signal with 30ps rise time, 20% to 80% |      | 31   |      | ps               |
| T <sub>PLH</sub>           | Low-to-High Propagation Delay                          |  |      | 65   |      | ps               |
| T <sub>PHL</sub>           | High-to-Low Propagation Delay                          |  |      | 65   |      | ps               |
| T <sub>SK_IN-TRA_IN</sub>  | Input Intra-pair Differential Skew tolerance           |  |      |      | 0.15 | UI               |
| T <sub>SK_IN-TRA_OUT</sub> | Output Intra-pair Differential Skew                    |  |      | 5    | 10   | ps               |
| T <sub>SK_IN-TER_OUT</sub> | Output Inter-pair Differential Skew                    |  |      | 8    |      | ps               |
| R <sub>J</sub>             | Add-in Random Jitter                                   | at 6Gbps                                     |      | 0.57 |      | RMS ps           |
| D <sub>J</sub>             | Add-in Deterministic Jitter                            | at 6Gbps                                     |      | 6.57 |      | ps               |
| T <sub>SX</sub>            | Select to Switch Output                                |  |      |      | 10   | ns               |
| S <sub>22</sub>            | Output return loss                                     | 10 MHz to 6 Gbps differential                |      | 13   |      | dB               |
|                            |  | 2 Gbps to 6 Gbps common mode                 |      | 8    |      |                  |
| R <sub>IN</sub>            | DC single-ended input impedance                        |  |      | 50   |      | Ω                |
|                            | DC Differential Input Impedance                        |  |      | 100  |      |                  |
| R <sub>OUT</sub>           | DC single-ended output impedance                       |  |      | 50   |      | Ω                |
|                            | DC Differential output Impedance                       |  |      | 100  |      |                  |
| Z <sub>RX-HIZ</sub>        | DC input CM input impedance during reset or power down |  |      | 200  |      | kΩ               |
| V <sub>RX-DIFF-PP</sub>    | Differential Input Peak-to-peak Voltage                | Operational                                  |      |      | 1.4  | V <sub>ppd</sub> |

| Symbol                            | Parameter  | Conditions   | Min. | Typ.                         | Max. | Unit              |
|-----------------------------------|--|--|------|------------------------------|------|-------------------|
| V <sub>CM-NOISE</sub>             | Input source common-mode noise   | DC – 200MHz  |      |                              | 150  | mV <sub>pp</sub>  |
| T <sub>TX-IDLE-SET-TO-IDLE</sub>  | Max time to electrical idle after sending an EIOS  |  |      | 4                            | 8    | ns                |
| T <sub>TX-IDLE-TO-DIFF-DATA</sub> | Max time to valid differential signal after leaving electrical idle                            |  |      | 4                            | 8    | ns                |
| T <sub>PD</sub>                   | Latency  | From input to output   |      | 0.5                          |      | ns                |
| G <sub>p</sub>                    | Peaking gain (Compensation at 6Gbps, relative to 100MHz, 100mV <sub>p-p</sub> sine wave input) | EQ<3:0> = 1111   |      | 8.9                          |      | dB                |
|                                   |  | EQ<3:0> = 1000   |      | 6.6                          |      |                   |
|                                   |  | EQ<3:0> = 0000   |      | 3.6                          |      |                   |
|                                   |  | Variation around typical                                     | -3   |                              | +3   | dB                |
| G <sub>F</sub>                    | Flat gain (100MHz, EQ<3:0> = 1000, SW<1:0> = 10)   | FG<1:0> = 11   |      | -3.5                         |      | dB                |
|                                   |  | FG<1:0> = 10   |      | -1.5                         |      |                   |
|                                   |  | FG<1:0> = 01   |      | 0.5                          |      |                   |
|                                   |  | FG<1:0> = 00   |      | 2.5                          |      |                   |
|                                   |  | Variation around typical                                     | -3   |                              | +3   | dB                |
| V <sub>1dB_100M</sub>             | -1dB compression point of output swing (at 100MHz)   | SW<1:0> = 11<br>SW<1:0> = 10<br>SW<1:0> = 01<br>SW<1:0> = 00 |      | 1400<br>1300<br>1200<br>1100 |      | mV <sub>ppd</sub> |
| V <sub>1dB_6G</sub>               | -1dB compression point of output swing (at 6 Gbps)   | SW<1:0> = 11<br>SW<1:0> = 10<br>SW<1:0> = 01<br>SW<1:0> = 00 |      | 1300<br>1200<br>1100<br>1000 |      | mV <sub>ppd</sub> |
| V <sub>Coup</sub>                 | Channel isolation  | 100MHz to 6 Gbps   |      | 40                           |      | dB                |
| V <sub>noise_in-put</sub>         | Input-referred noise <sup>(2)</sup>  | 100MHz to 6 Gbps, FG<1:0> = 11, EQ<3:0> = 0000               |      | 0.5                          |      | mV <sub>RMS</sub> |
|                                   |  | 100MHz to 6 Gbps, FG<1:0> = 11, EQ<3:0> = 1010               |      | 0.4                          |      |                   |
| V <sub>noise_out-put</sub>        | Output-referred noise <sup>(2)</sup>   | 100MHz to 6 Gbps, FG<1:0> = 11, EQ<3:0> = 0000               |      | 0.7                          |      | mV <sub>RMS</sub> |
|                                   |  | 100MHz to 6 Gbps, FG<1:0> = 11, EQ<3:0> = 1010               |      | 0.8                          | 1.6  |                   |

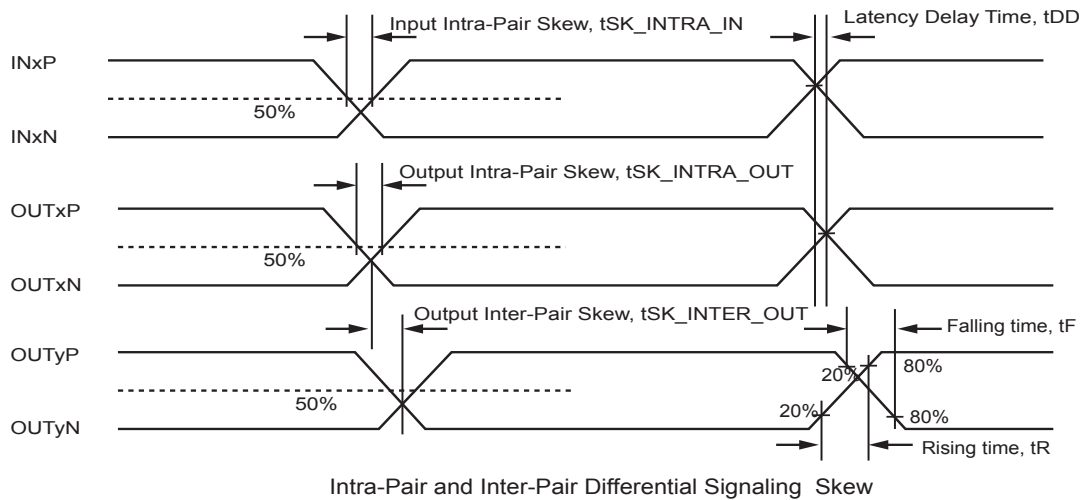
Note

(1) Measured using a vector-network analyzer (VNA) with -15dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.

(2) Guaranteed by design.



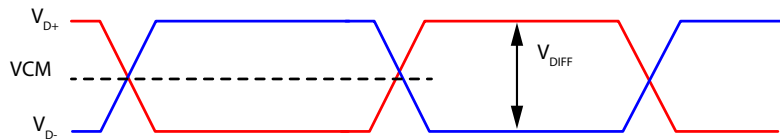
**Figure 6-1 Electrical parameter test setup**



Intra-Pair and Inter-Pair Differential Signaling Skew

**Figure 6-2 Intra and Inter-pair Differential Skew definition**

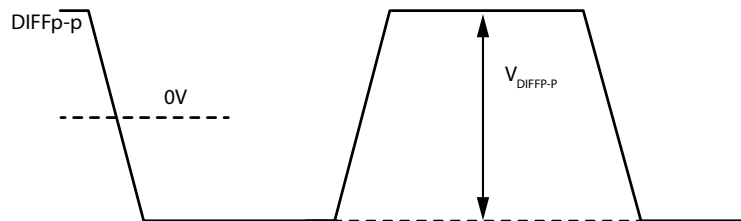
Common Mode Voltage  
 $V_{CM} = (|VD+ + VD-| / 2)$   
 $V_{CMP} = (\max |VD+ + VD-| / 2)$



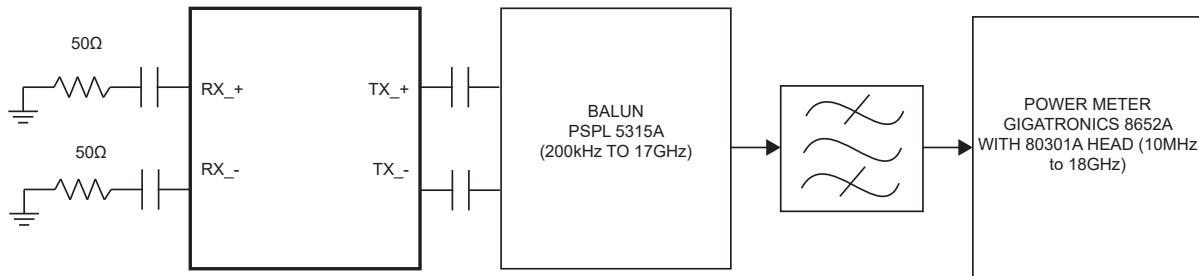
$V_{D+} - V_{D-}$

Symmetric Differential Swing  
 $V_{DIFFP-P} = (2 * \max |V_{D+} - V_{D-}|)$

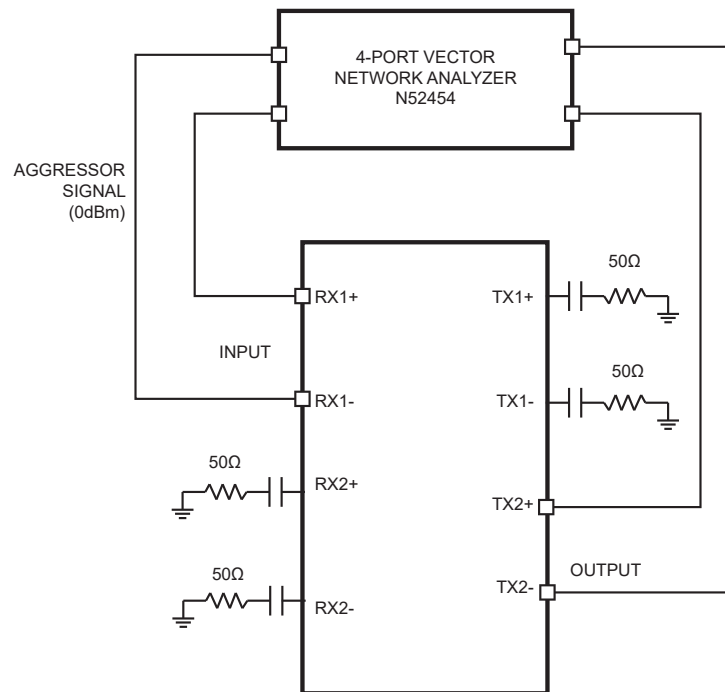
Asymmetric Differential Swing  
 $V_{DIFFD-D} = (\max |V_{D+} - V_{D-}| \{V_{D+} > V_{D-}\})$



**Figure 6-3 Definition of Peak-to-peak Differential voltage**



**Figure 6-4 Noise test configuration**



**Figure 6-5 Channel-isolation test configuration**

Figure 6-6



## 6.4 I2C Interface Bus

| Symbol                | Parameter  | Conditions               | Min.             | Typ. | Max              | Units |
|-----------------------|--|--------------------------|------------------|------|------------------|-------|
| VDD                   | Nominal Bus Voltage  |                          | 3.0              |      | 3.6              | V     |
| Freq                  | Bus Operation Frequency  |                          |                  |      | 400              | kHz   |
| V <sub>IH</sub>       | DC input logic high  |                          | $V_{DD}/2 + 0.7$ |      | $V_{DD} + 0.3$   | V     |
| V <sub>IL</sub>       | DC input logic low   |                          | -0.3             |      | $V_{DD}/2 - 0.7$ | V     |
| V <sub>OL</sub>       | DC output logic low  | I <sub>OL</sub> = 3mA    |                  |      | 0.4              | V     |
| I <sub>pullup</sub>   | Current Through Pull-Up Resistor or Current Source   | High Power specification | 3.0              |      | 3.6              | mA    |
| I <sub>leak-bus</sub> | Input leakage per bus segment  |                          | -200             |      | 200              | uA    |
| I <sub>leak-pin</sub> | Input leakage per device pin   |                          |                  | -15  |                  | uA    |
| CI                    | Capacitance for SDA/SCL  |                          |                  |      | 10               | pF    |
| t <sub>BUF</sub>      | Bus Free Time Between Stop and Start condition   |                          | 1.3              |      |                  | us    |
| t <sub>HD:STA</sub>   | Hold time after (Repeated) Start condition. After this period, the first clock is generated. | At pull-up, Max          | 0.6              |      |                  | us    |
| TSU:STA               | Repeated start condition setup time  |                          | 0.6              |      |                  | us    |
| TSU:STO               | Stop condition setup time  |                          | 0.6              |      |                  | us    |
| THD:DAT               | Data hold time   |                          | 0                |      |                  | ns    |
| TSU:DAT               | Data setup time  |                          | 100              |      |                  | ns    |
| t <sub>LOW</sub>      | Clock low period   |                          | 1.3              |      |                  | us    |
| t <sub>HIGH</sub>     | Clock high period  |                          | 0.6              |      | 50               | us    |
| t <sub>F</sub>        | Clock/Data fall time   |                          |                  |      | 300              | ns    |
| t <sub>R</sub>        | Clock/Data rise time   |                          |                  |      | 300              | ns    |
| t <sub>POR</sub>      | Time in which a device must be operation after power-on reset                                |                          |                  |      | 500              | ms    |

**Note:**

- (1) Recommended maximum capacitance load per bus segment is 400pF.
- (2) Compliant to I2C physical layer specification.
- (3) Ensured by Design. Parameter not tested in production.

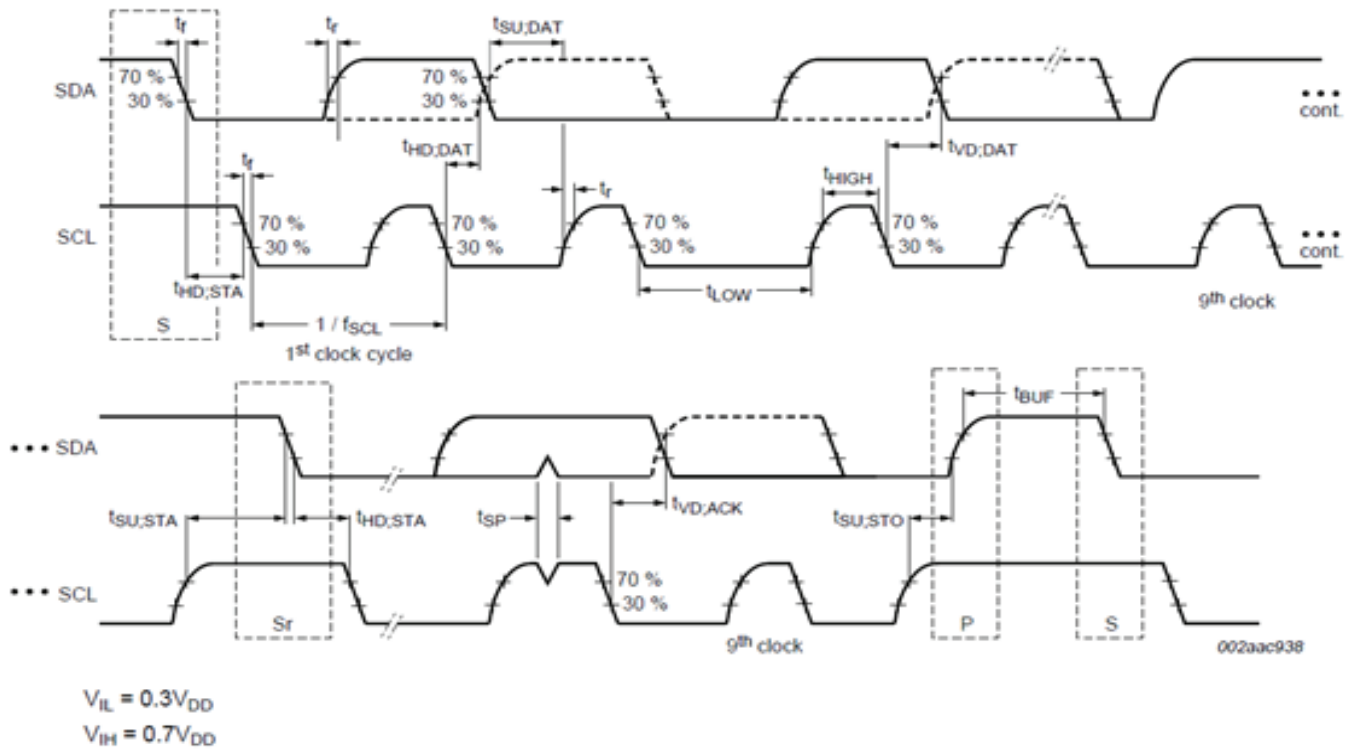
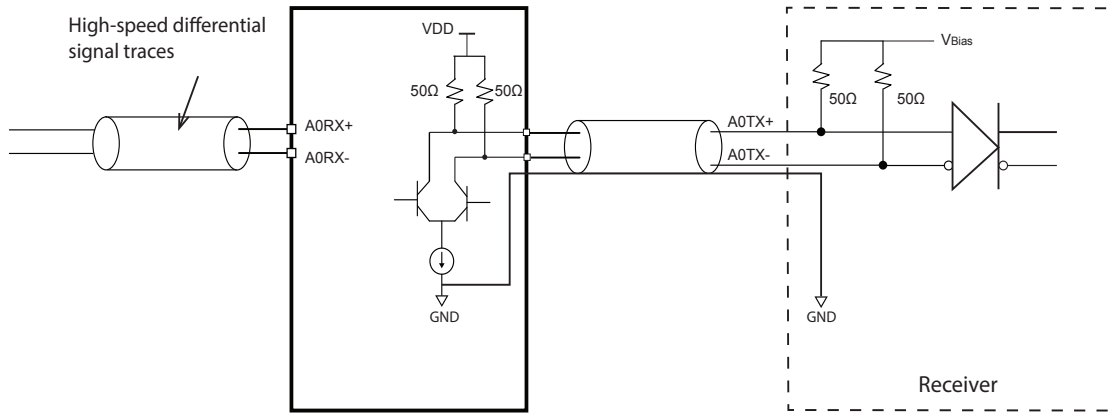


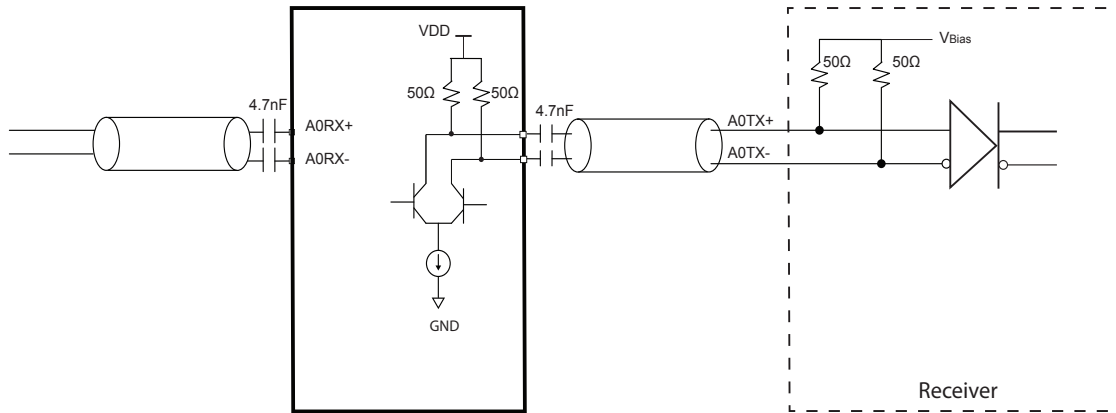
Figure 6-7 I2C Timing definition

## 7. Applications

### 7.1 DC/AC-coupled Application



DC-Coupled Differential Signaling Application Circuits



AC-Coupled Differential Signaling Application Circuits

**Figure 7-1 DC/AC-coupled application diagram**

### 7.2 Sink-side Redriver Application

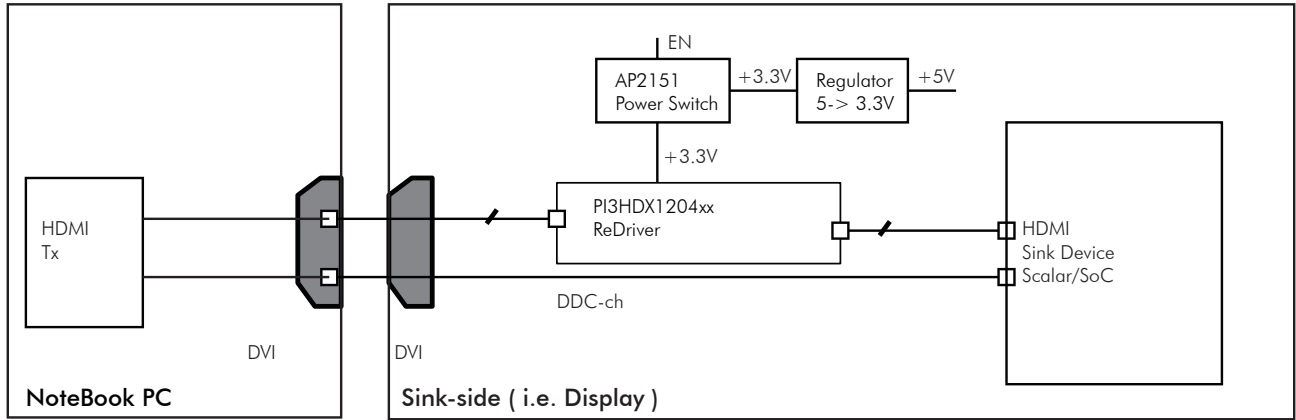


Figure 7-2 HDMI Sink-side application

### 7.3 Channels/Polarity Swap

Linear Redriver does not have built-in internal channel/polarity switch. Transmitter can send swapped polarity signal to the Redriver.

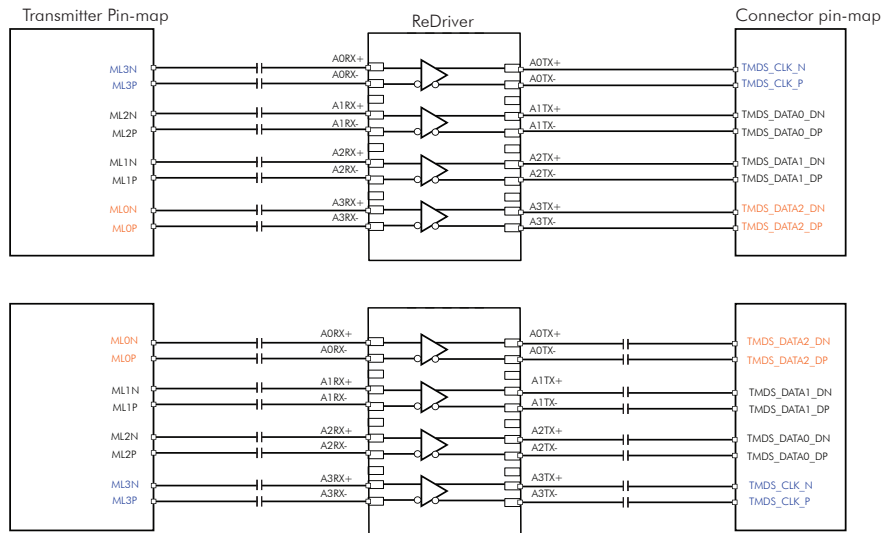


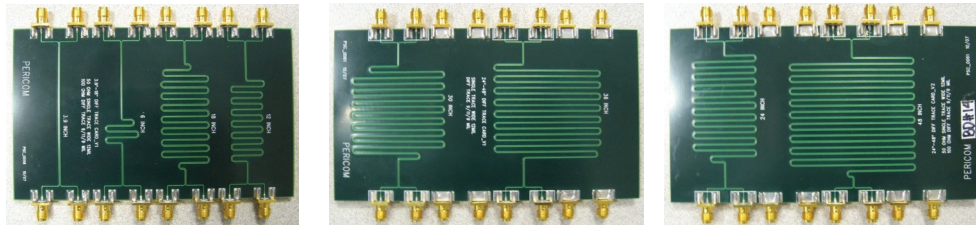
Figure 7-3 Polarity Swap Connection

**7.4 Output Eye Diagram**

**7.4.1 Trace Card Loss Informations**

| Frequency           | 3 GHz  | 6GHz | Units |
|---------------------|--------|------|-------|
| 6 inch Input Trace  | -1.43  | -4   | dB    |
| 12 inch Input Trace | -6.1   | -11  | dB    |
| 18 inch Input Trace | -8.34  | -15  | dB    |
| 30 inch Input Trace | -10.14 | -18  | dB    |
| 36 inch Input Trace | -12.13 | -22  | dB    |
| 48 inch Input Trace | -16.42 | -29  | dB    |

**Table 7-1. Characterization Trace Card dB Loss Information**



**Figure 7-4 Trace board photo**

7.4.2 Output Eye Diagram measurement

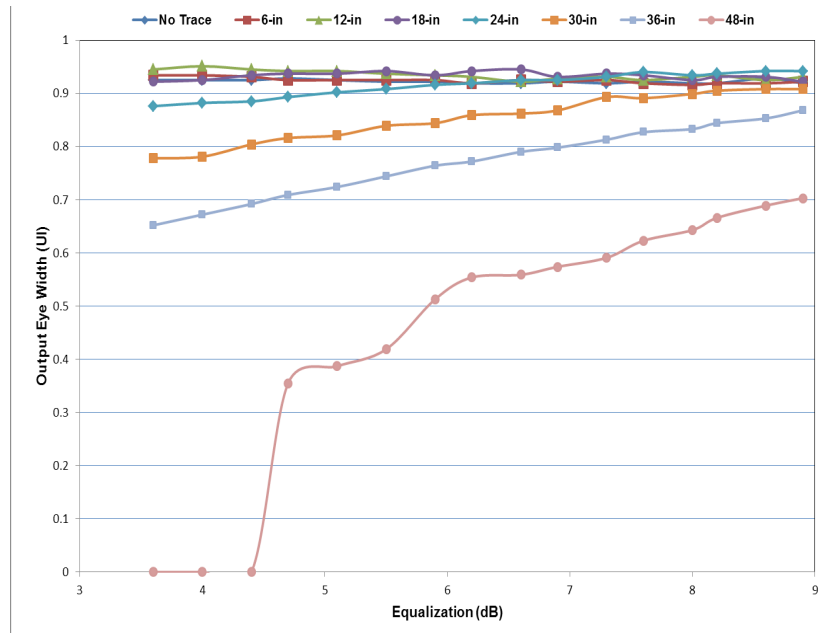


Figure 7-5 Eye Width vs. EQ plots at 6 Gbps, PRBS2<sup>23-1</sup>, FG=11 (Gain +2.5dB)  
Eye Width vs EQ, FG =1000mV, Gain=+2.5dB (Input Swing=800mVd)

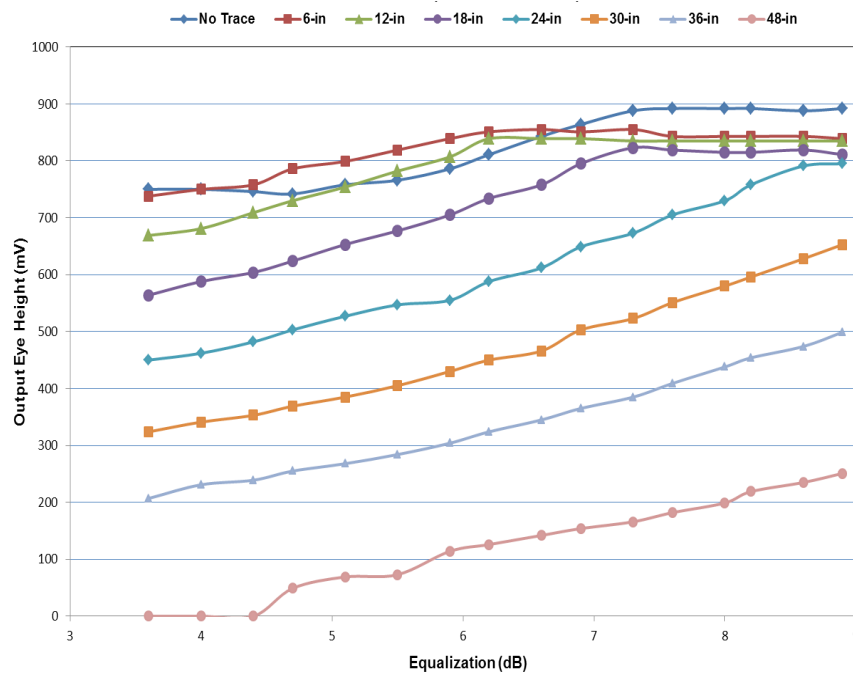
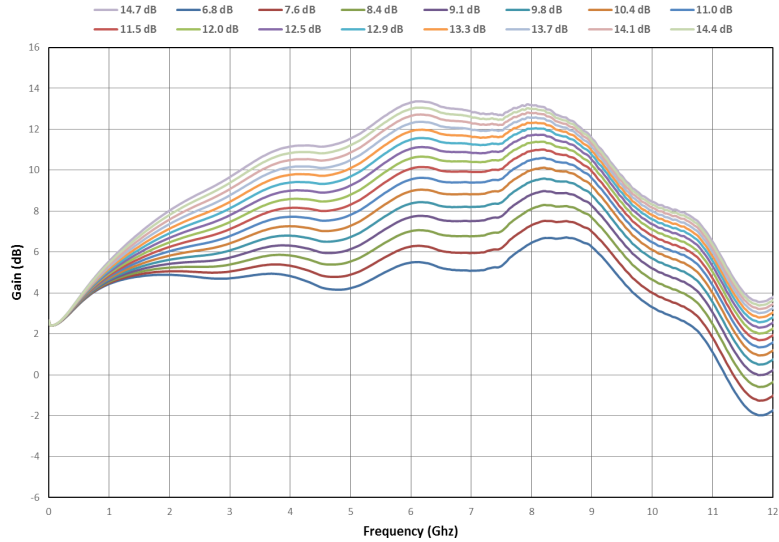


Figure 7-6 Eye Width vs. EQ plots at 6 Gbps, PRBS2<sup>23-1</sup>, FG=10 (Gain +0.5dB)  
Eye Height vs EQ, FG=1000mV, Gain=+2.5dB (input swing=800mVd)

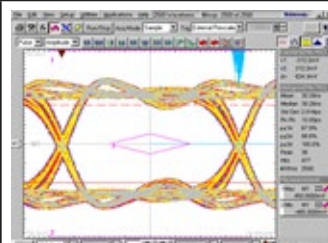
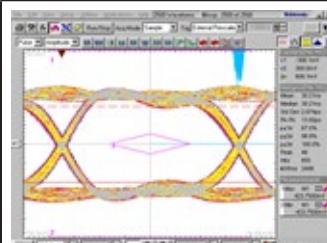
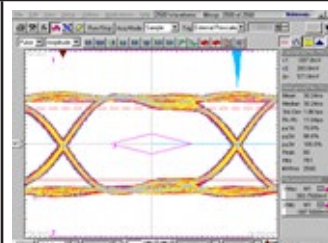
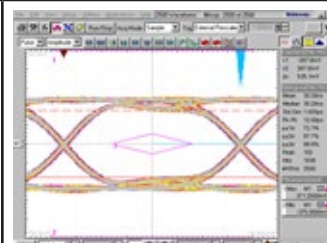
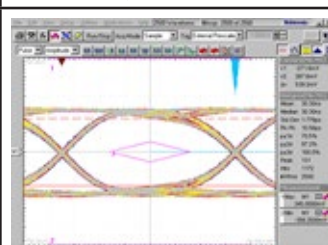
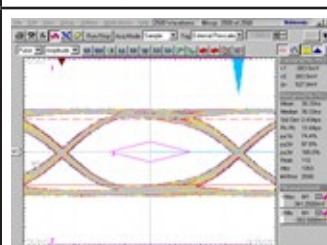
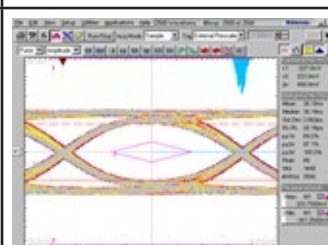
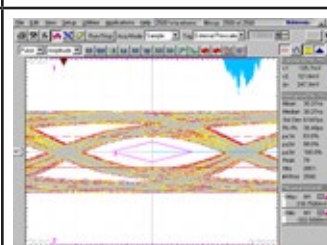


**Figure 7-7 Frequency response vs EQ**  
with FG=11(+2.5dB), Output Swing=1000mV, Vdd=3.0V, 25C, Input Power=-15dBm, No Input Trace

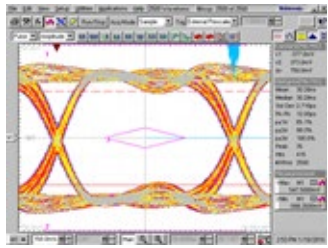
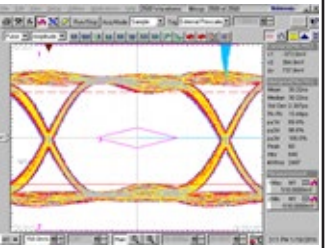
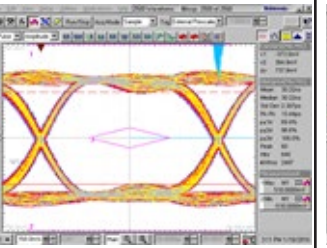
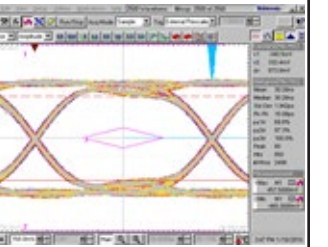
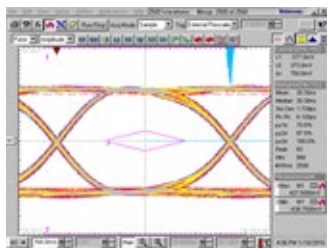
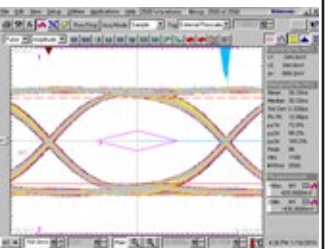
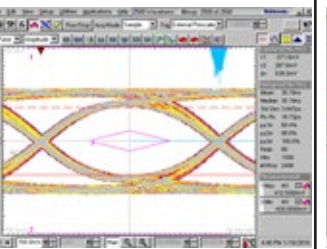
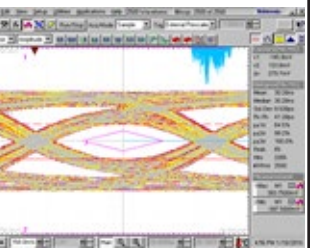
**7.4.3 Output Eye diagram**

Condition: PRBS 2<sup>23</sup>-1 pattern, Input Swing=800mVdiff, Output Swing= 1000mVdiff

**Table 7-2. Output Eye diagram by EQ changes at FG 0.5dB**

| No Trace, FG=0.5dB   | 6-in trace, FG=0.5dB   | 12-in trace, FG=0.5dB   | 18-in trace, FG=0.5dB  |
|--|--|---|--|
| <br>EQ=3dB  | <br>EQ=3dB    | <br>EQ=5dB    | <br>EQ=6dB  |
| <br>EQ=10dB | <br>EQ=13.3dB | <br>EQ=14.5dB | <br>EQ=15dB |

**Table 7-3. Output Eye Diagram by EQ changes at FG 2.5dB**

| No Trace, FG=2.5dB  | 6-in trace, FG=2.5dB  | 12-in trace, FG=2.5dB  | 18-in trace, FG=2.5dB   |
|---|---|--|---|
| <br>EQ=3dB   | <br>EQ=3dB   | <br>EQ=5dB   | <br>EQ=8dB   |
| 24-in trace, FG=2.5dB   | 30-in trace, FG=2.5dB   | 36-in trace, FG=2.5dB  | 48-in trace, FG=2.5dB   |
| <br>EQ=13dB | <br>EQ=15dB | <br>EQ=15dB | <br>EQ=15dB |



## 7.5 Layout Guidelines

As transmission data rate increases rapidly, any flaws and/or mis-matches on PCB layout are amplified in terms of signal integrity. Layout guideline for high-speed transmission is highlighted in this application note.

### 7.5.1 Power and Ground

To provide a clean power supply for high-speed device, few recommendations are listed below:

- Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly without passing through any resistor.
- The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- One low-ESR 0.1uF decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Capacitors of smaller body size, i.e. 0402 package, is more preferable as the insertion loss is lower. The capacitor should be placed next to the VDD pin.
- One capacitor with capacitance in the range of 4.7uF to 10uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- A ferrite bead for isolating the power supply for Pericom high-speed device from the power supplies for other parts on the printed circuit board should be implemented.
- Several thermal ground vias must be required on the thermal pad. 25-mil or less pad size and 14-mil or less finished hole are recommended.

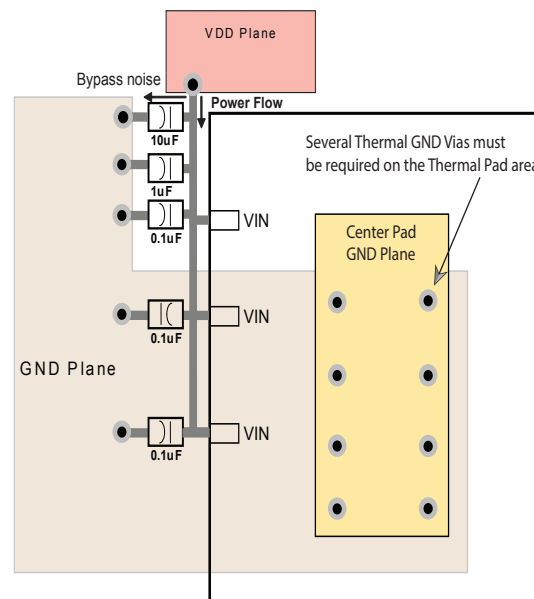
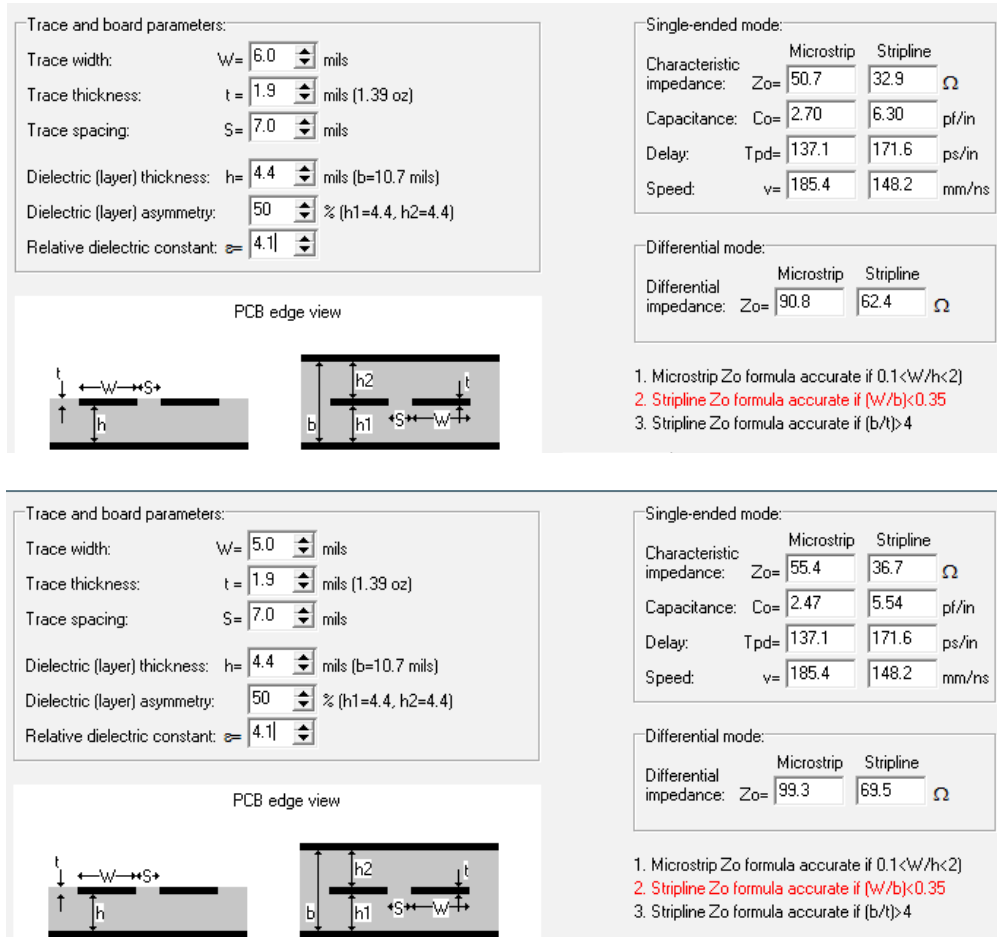


Figure 7-8 Decoupling Capacitor Placement Diagram

### 7.5.2 High-speed signal Routing

Well-designed layout is essential to prevent signal reflection:

- For 90Ω differential impedance, width-spacing-width micro-strip of 6-7-6 mils is recommended; for 100Ω differential impedance, width-spacing-width micro-strip of 5-7-5 mils is recommended.
- Differential impedance tolerance is targeted at ±15%.



**Figure 7-9 Trace Width and Clearance of Micro-strip and Strip-line**

- For micro-strip, using 1/2oz Cu is fine. For strip-line in 6+ PCB layers, 1oz Cu is more preferable.

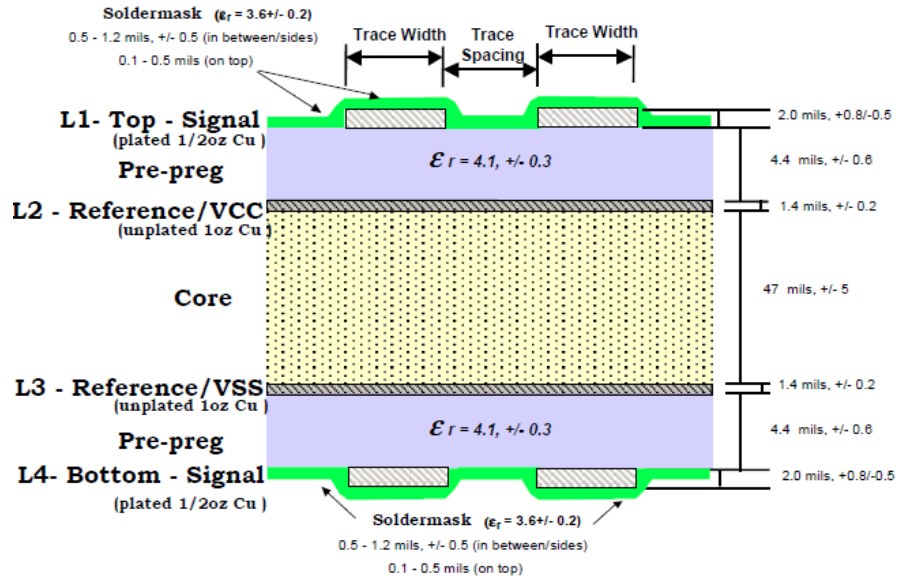


Figure 7-10 4-Layer PCB Stack-up Example

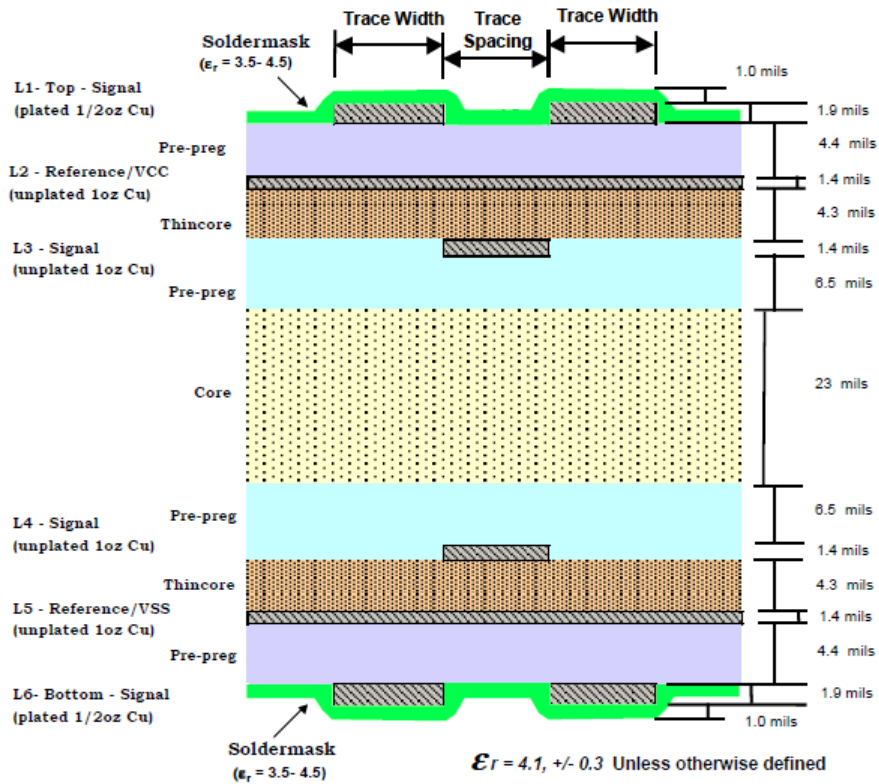
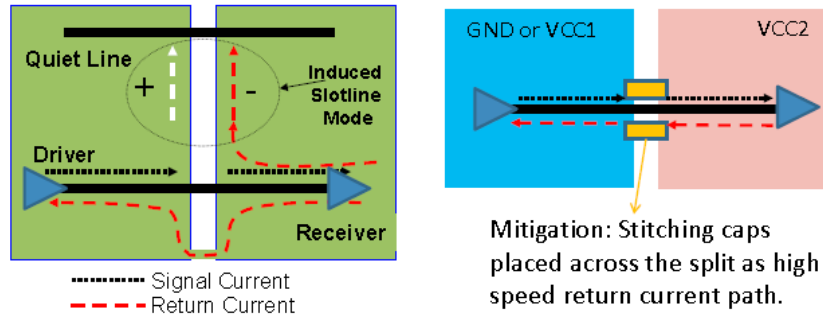


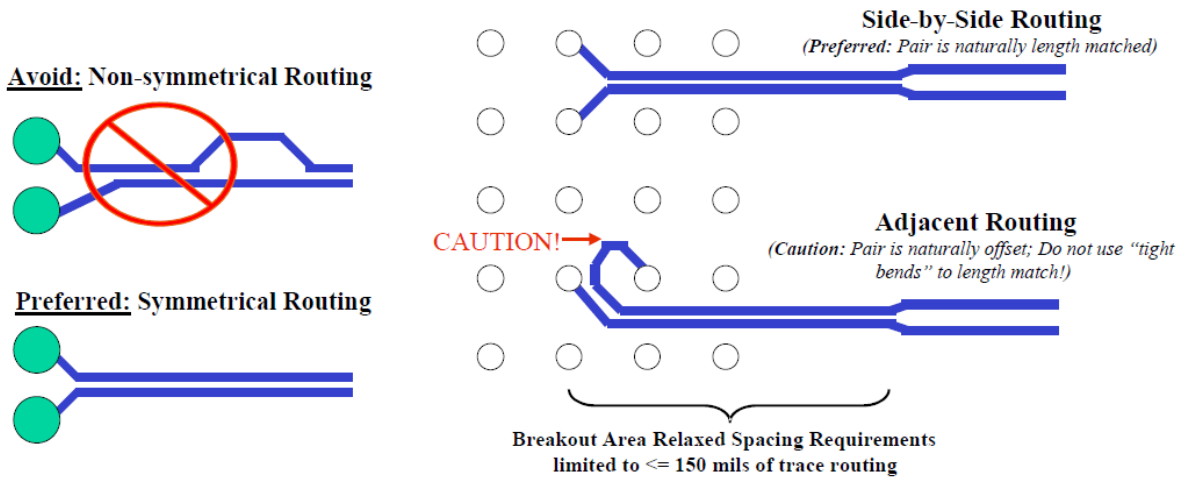
Figure 7-11 6-Layer PCB Stack-up Example

- Ground referencing is highly recommended. If unavoidable, stitching capacitors of 0.1uF should be placed when reference plane is changed.



**Figure 7-12** Stitching Capacitor Placement

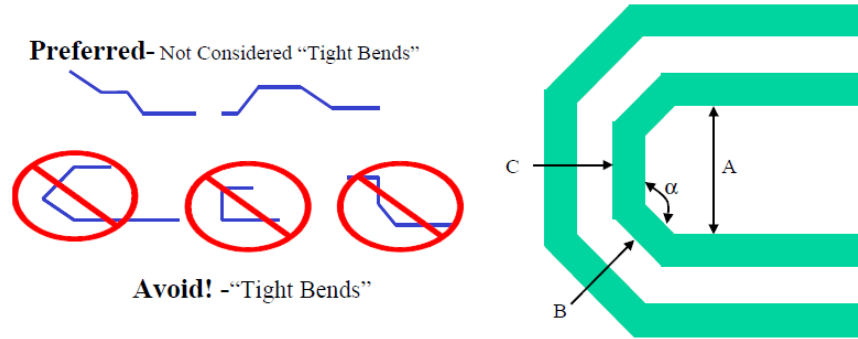
- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.
- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.



**Figure 7-13** Layout Guidance of Matched Differential Pair

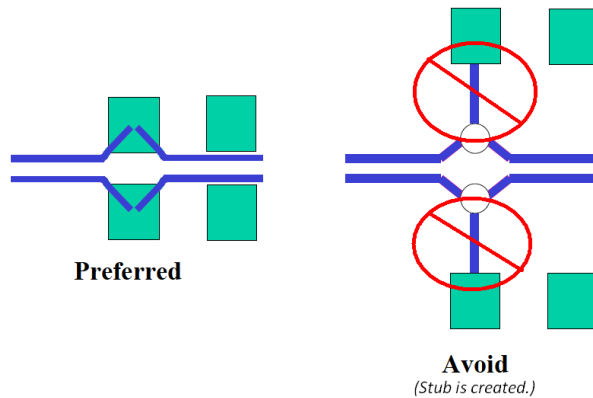
- For minimal crosstalk, inter-pair spacing between two differential micro-strip pairs should be at least 20 mils or 4 times the dielectric thickness of the PCB.
- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.

- To minimize signal loss and jitter, tight bend is not recommended. All angles  $\alpha$  should be at least 135 degrees. The inner air gap A should be at least 4 times the dielectric thickness of the PCB.



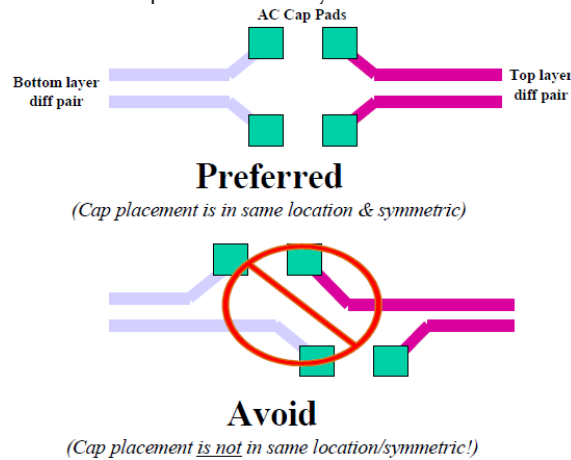
**Figure 7-14 Layout Guidance of Bends**

- Stub creation should be avoided when placing shunt components on a differential pair.



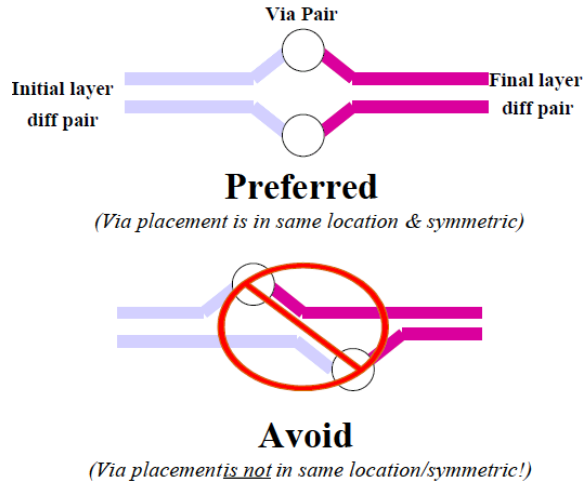
**Figure 7-15 Layout Guidance of Shunt Component**

- Placement of series components on a differential pair should be symmetrical.



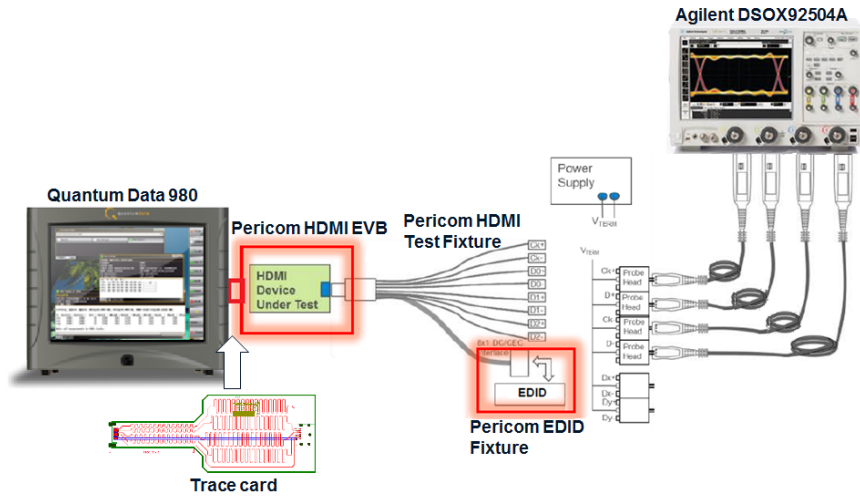
**Figure 7-16 Layout Guidance of Series Component**

- Stitching vias or test points must be used sparingly and placed symmetrically on a differential pair.



**Figure 7-17 Layout Guidance of Stitching Via**

**7.6 HDMI 2.0 Compliance Test**



**Figure 7-18 HDMI 2.0 CTS test setup\***

Note:

**Table 7-4. Application Trace Card Information for CTS test**

| HDMI FR4 trace         | 0 in     | 6 in     | 12 in     | 18 in     | 24 in     | 30 in     | 36 in     |
|------------------------|----------|----------|-----------|-----------|-----------|-----------|-----------|
| Insertion loss @ 6Gbps | -5.91 dB | -9.75 dB | -10.47 dB | -13.05 dB | -15.87 dB | -16.97 dB | -21.20 dB |

# HDMI Test Report

Overall Result: **PASS**

| Test Configuration Details |   |
|----------------------------|---|
| Device Description         |   |
| Device ID                  | Transmitter   |
| Fixture Type               | Other   |
| Probe Connection           | 4 Probes  |
| Probe Head Type            | N5444A  |
| Lane Connection            | 1 Data Lane   |
| HDMI Specification         | 2.0   |
| HDMI Test Type             | TMDS Physical Layer Tests   |
| Test Session Details       |   |
| Infiniium SW Version       | 05.20.0013  |
| Infiniium Model Number     | DSOX92504A  |
| Infiniium Serial Number    | MY54410104  |
| Application SW Version     | 2.11  |
| Debug Mode Used            | No  |
| Probe (Channel 1)          | Model: N2801A<br>Serial: US54094067<br>Head: N5444A<br>Atten: Calibrated (18 FEB 2015 11:16:48), Using Cal Atten (5.7831E+000)<br>Skew: Calibrated (18 FEB 2015 11:16:56), Using Cal Skew |
| Probe (Channel 2)          | Model: N2801A<br>Serial: US54094054<br>Head: N5444A<br>Atten: Calibrated (18 FEB 2015 11:19:29), Using Cal Atten (5.5882E+000)<br>Skew: Calibrated (18 FEB 2015 11:13:57), Using Cal Skew |
| Probe (Channel 3)          | Model: N2801A<br>Serial: US54094059<br>Head: N5444A<br>Atten: Calibrated (18 FEB 2015 11:15:19), Using Cal Atten (5.7320E+000)<br>Skew: Calibrated (18 FEB 2015 11:15:29), Using Cal Skew |
| Probe (Channel 4)          | Model: N2801A<br>Serial: US54094057<br>Head: N5444A<br>Atten: Calibrated (18 FEB 2015 11:11:30), Using Cal Atten (5.5123E+000)<br>Skew: Calibrated (18 FEB 2015 11:12:12), Using Cal Skew |
| Last Test Date             | 2016-01-21 16:43:22 UTC +08:00  |

Figure 7-19 HDMI 2.0 CTS Test Report



## Summary of Results

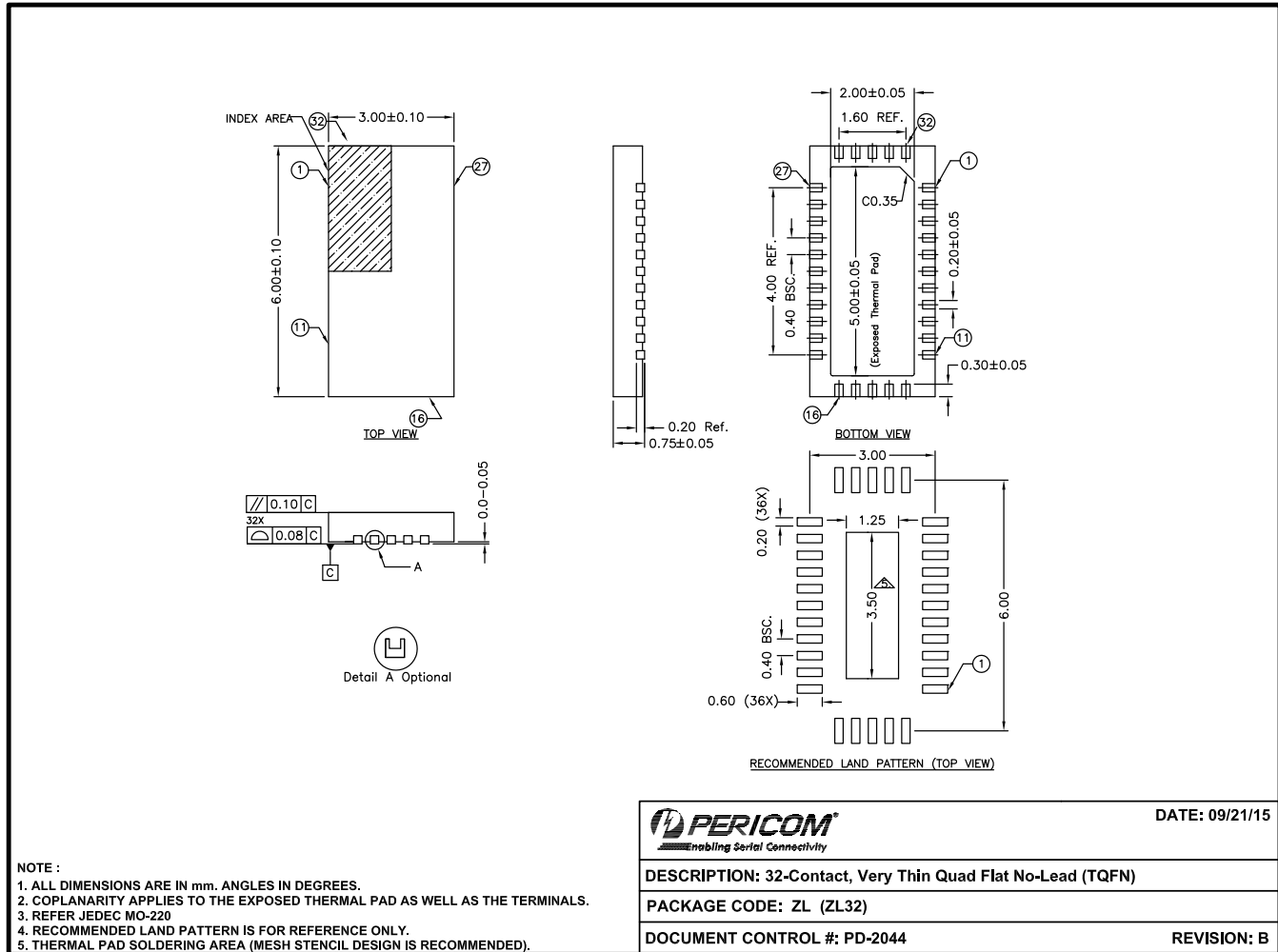
| Test Statistics |    |
|-----------------|----|
| Failed          | 0  |
| Passed          | 24 |
| Total           | 24 |

| Margin Thresholds |       |
|-------------------|-------|
| Warning           | < 2 % |
| Critical          | < 0 % |

| Pass | # Failed | # Trials | Test Name   | Actual Value      | Margin  | Pass Limits                                    |
|------|----------|----------|---|-------------------|---------|--|
| ✓    | 0        | 1        | <u>HF1-2: Clock Rise Time</u>                                     | 151.367 ps        | 101.8 % | VALUE >= 75.000 ps                             |
| ✓    | 0        | 1        | <u>HF1-2: Clock Fall Time</u>                                     | 150.838 ps        | 101.1 % | VALUE >= 75.000 ps                             |
| ✓    | 0        | 1        | <u>HF1-6: Clock Duty Cycle(Minimum)</u>                           | 49.780            | 24.5 %  | >=40%  |
| ✓    | 0        | 1        | <u>HF1-6: Clock Duty Cycle(Maximum)</u>                           | 50.330            | 16.1 %  | <=60%  |
| ✓    | 0        | 1        | <u>HF1-6: Clock Rate</u>  | 148.513500000 MHz | 2.3 %   | 85.000000000 MHz <= VALUE <= 150.000000000 MHz |
| ✓    | 0        | 1        | <u>HF1-7: Differential Clock Voltage Swing, Vs (TP1)</u>          | 997 mV            | 25.4 %  | 400 mV < VALUE < 1.200 V                       |
| ✓    | 0        | 1        | <u>HF1-7: Clock Jitter (TP2 EQ with Worst Case Positive Skew)</u> | 250 mTbit         | 16.7 %  | VALUE <= 300 mTbit                             |
| ✓    | 0        | 1        | <u>HF1-7: Clock Jitter (TP2 EQ with Worst Case Negative Skew)</u> | 225 mTbit         | 25.0 %  | VALUE <= 300 mTbit                             |
| ✓    | 0        | 1        | <u>HF1-5: D0 Maximum Differential Voltage</u>                     | 542 m             | 30.5 %  | VALUE <= 780 m                                 |
| ✓    | 0        | 1        | <u>HF1-5: D0 Minimum Differential Voltage</u>                     | -564 m            | 27.7 %  | VALUE >= -780 m                                |
| ✓    | 0        | 1        | <u>HF1-2: D0 Rise Time</u>  | 135.000 ps        | 217.6 % | VALUE >= 42.500 ps                             |
| ✓    | 0        | 1        | <u>HF1-2: D0 Fall Time</u>  | 134.370 ps        | 216.2 % | VALUE >= 42.500 ps                             |
| ✓    | 0        | 1        | <u>HF1-8: D0 Mask Test (TP2 EQ with Worst Case Positive Skew)</u> | 0.000             | 50.0 %  | No Mask Failures                               |
| ✓    | 0        | 1        | <u>HF1-8: D0 Mask Test (TP2 EQ with Worst Case Negative Skew)</u> | 0.000             | 50.0 %  | No Mask Failures                               |
| ✓    | 0        | 1        | <u>HF1-1: VL Clock +</u>  | 2.684 V           | 48.0 %  | 2.300 V <= VALUE <= 3.100 V                    |
| ✓    | 0        | 1        | <u>HF1-1:Clock + VSwing</u>                                       | 513 mV            | 21.8 %  | 200 mV <= VALUE <= 600 mV                      |
| ✓    | 0        | 1        | <u>HF1-1: VL Clock -</u>  | 2.678 V           | 47.3 %  | 2.300 V <= VALUE <= 3.100 V                    |
| ✓    | 0        | 1        | <u>HF1-1:Clock - VSwing</u>                                       | 513 mV            | 21.8 %  | 200 mV <= VALUE <= 600 mV                      |
| ✓    | 0        | 1        | <u>HF1-4: Intra-Pair Skew - Clock</u>                             | 51 mTbit          | 33.0 %  | -150 mTbit <= VALUE <= 150 mTbit               |
| ✓    | 0        | 1        | <u>HF1-1: VL D0+</u>  | 2.706 V           | 32.3 %  | 2.300 V <= VALUE <= 2.900 V                    |
| ✓    | 0        | 1        | <u>HF1-1: D0+ VSwing</u>  | 459 mV            | 29.5 %  | 400 mV <= VALUE <= 600 mV                      |
| ✓    | 0        | 1        | <u>HF1-1: VL D0-</u>  | 2.718 V           | 30.3 %  | 2.300 V <= VALUE <= 2.900 V                    |
| ✓    | 0        | 1        | <u>HF1-1: D0- VSwing</u>  | 450 mV            | 25.0 %  | 400 mV <= VALUE <= 600 mV                      |
| ✓    | 0        | 1        | <u>HF1-4: Intra-Pair Skew - Data Lane 0</u>                       | 36 mTbit          | 38.0 %  | -150 mTbit <= VALUE <= 150 mTbit               |

## 8. Mechanical/Packaging

### 8.1 Mechanical Outline



15-0222

Figure 8-1 32-pin TQFN package mechanical

**PI3HDX1204E**

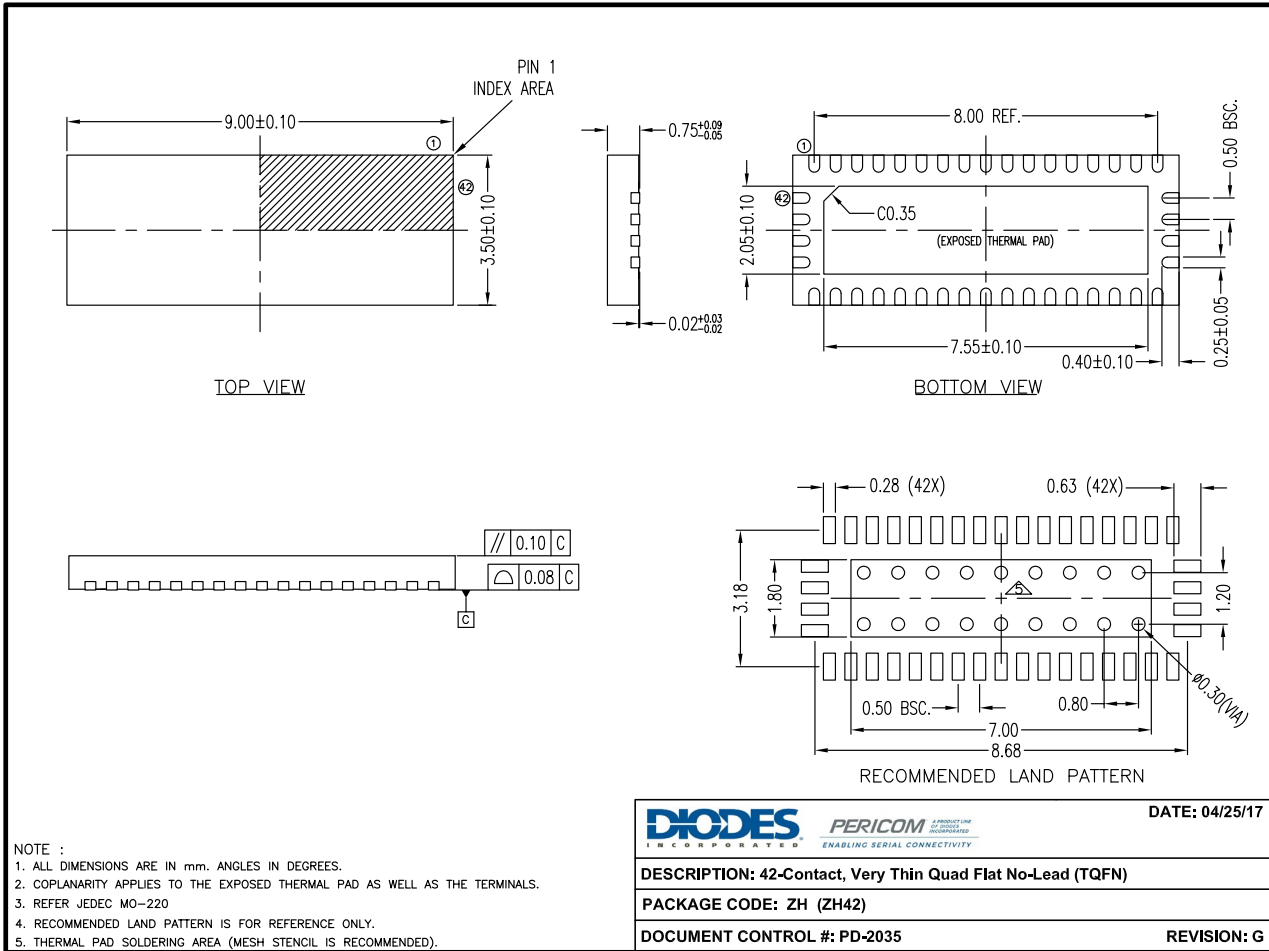
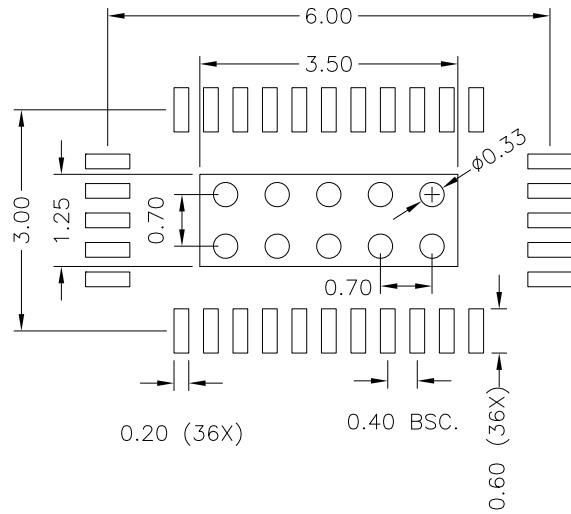


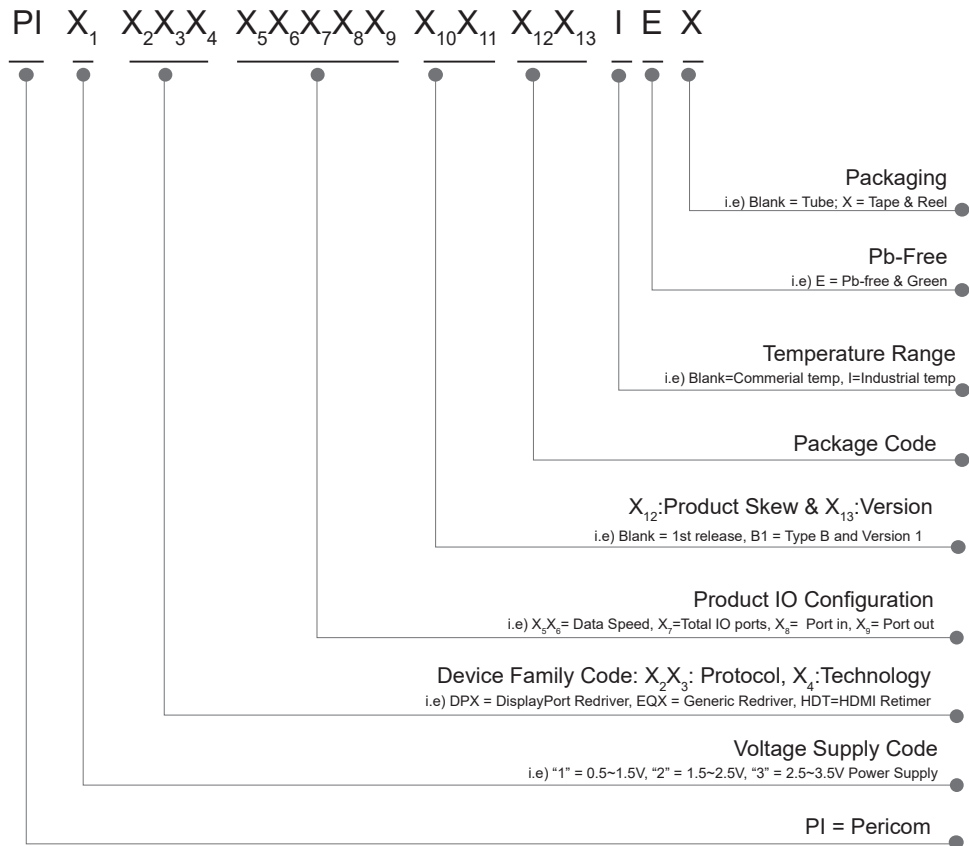
Figure 8-2 42-pin TQFN package mechanical



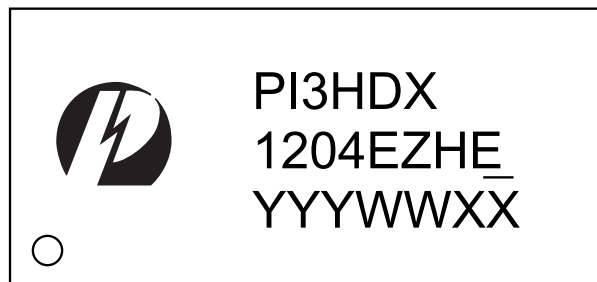
**Figure 8-3 Thermal Via Pad Area: 32-pin**

## 8.2 Part Marking Information

Product marking follows our standard part number ordering information.



**Figure 8-4 Part number information**



1st Y: Die Rev  
YY: Year  
WW: Workweek  
1st X: Assembly Code  
2nd X: Fab Code

**Figure 8-5 Package marketing information**

### 8.3 Tape & Reel Materials and Design

#### 8.3.1 Carrier Tape

The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is  $10^6 \Omega/\text{sq}$ . maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 3 and 4 for carrier tape dimensions.

#### 8.3.2 Cover Tape

Cover tape is made of Anti-static Transparent Polyester film. The surface resistivity is  $10^7 \Omega/\text{Sq}$ . Minimum to  $10^{11} \text{ Ohm sq}$ . maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

#### 8.3.3 Reel

The device loading orientation is in compliance with EIA-481, current version (Figure 2). The loaded carrier tape is wound onto either a 13-inch reel, (Figure 4) or 7-inch reel. The reel is made of Anti-static High-Impact Polystyrene. The surface resistivity  $10^7 \Omega/\text{sq}$ . minimum to  $10^{11} \Omega/\text{sq}$ . max.

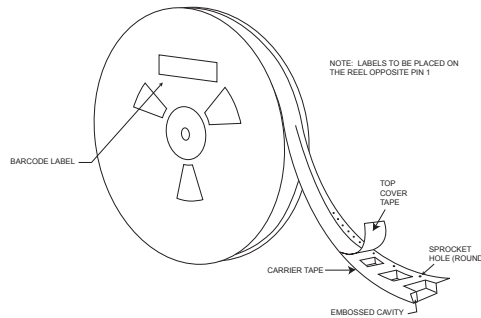


Figure 8-6 Tape & Reel label information

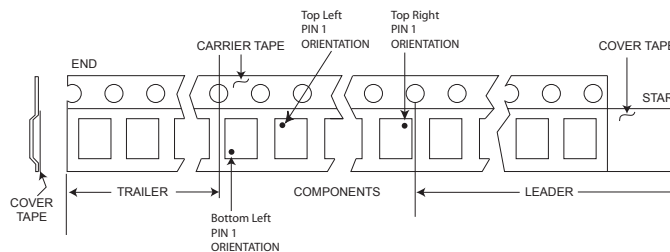
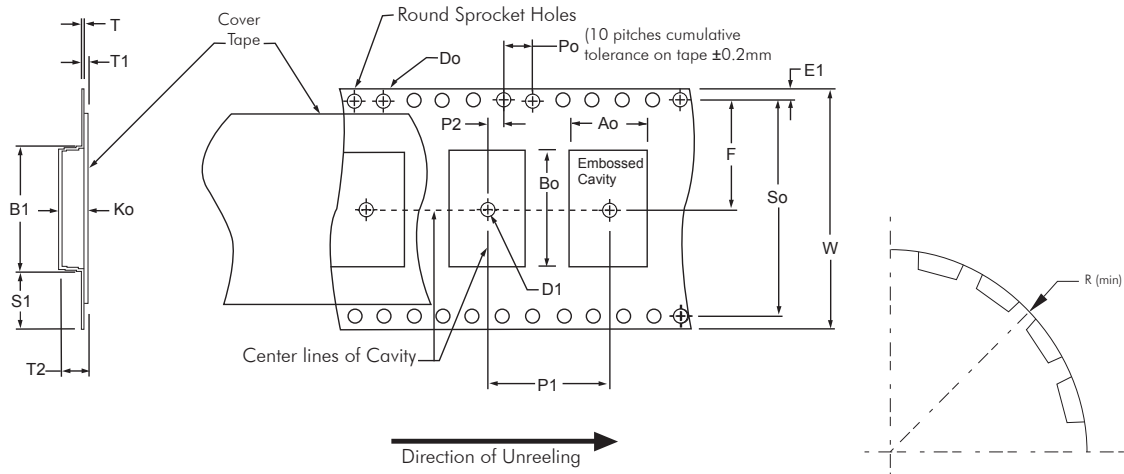


Figure 8-7 Tape leader and trailer pin 1 orientations



**Figure 8-8 Standard embossed carrier tape dimensions**

**Table 8-1. Constant Dimensions**

| Tape Size | D0               | D1 (Min) | E1         | P0        | P2         | R (See Note 2) | S1 (Min)         | T (Max) | T1 (Max) |
|-----------|------------------|----------|------------|-----------|------------|----------------|------------------|---------|----------|
| 8mm       | 1.5 +0.1<br>-0.0 | 1.0      | 1.75 ± 0.1 | 4.0 ± 0.1 | 2.0 ± 0.05 | 25             | 0.6              | 0.6     | 0.1      |
| 12mm      |                  | 1.5      |            |           |            | 2.0 ± 0.1      |                  |         |          |
| 16mm      |                  |          |            |           | 2.0        |                |                  |         |          |
| 24mm      |                  | 2.0      |            |           |            | 50             | N/A (See Note 3) |         |          |
| 32mm      |                  |          |            |           | 2.0        |                | 50               |         |          |
| 44mm      |                  | 2.0      |            |           |            | 50             |                  |         |          |

**Table 8-2. Variable Dimensions**

| Tape Size | P1  | B1 (Max) | E2 (Min) | F           | So               | T2 (Max.) | W (Max) | A0, B0, & K0 |
|-----------|---|----------|----------|-------------|------------------|-----------|---------|--------------|
| 8mm       | Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information) | 4.35     | 6.25     | 3.5 ± 0.05  | N/A (see note 4) | 2.5       | 8.3     | See Note 1   |
| 12mm      |   | 8.2      | 10.25    | 5.5 ± 0.05  |                  | 6.5       | 12.3    |              |
| 16mm      |   | 12.1     | 14.25    | 7.5 ± 0.1   |                  | 8.0       | 16.3    |              |
| 24mm      |   | 20.1     | 22.25    | 11.5 ± 0.1  | 12.0             | 24.3      |         |              |
| 32mm      |   | 23.0     | N/A      | 14.2 ± 0.1  |                  | 32.3      |         |              |
| 44mm      |   | 35.0     | N/A      | 20.2 ± 0.15 | 40.4 ± 0.1       | 16.0      | 44.3    |              |

**NOTES:**

- A0, B0, and K0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16 through 44mm.
- Tape and components will pass around reel with radius "R" without damage.
- S1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where Do≥S1.
- So does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.

**Table 8-3. Reel dimensions by tape size**

| Tape Size | A                          | N (Min)<br>See Note A        | W1                    | W2<br>(Max) | W3  | B (Min) | C                       | D (Min) |
|-----------|----------------------------|------------------------------|-----------------------|-------------|---|---------|-------------------------|---------|
| 8mm       | 178 ±2.0mm or<br>330±2.0mm | 60<br>±2.0mm or<br>100±2.0mm | 8.4 +1.5/-0.0<br>mm   | 14.4 mm     | Shall Ac-<br>commo-<br>date Tape<br>Width<br>Without<br>Interfer-<br>ence | 1.5mm   | 13.0<br>+0.5/-0.2<br>mm | 20.2mm  |
| 12mm      |                            |                              | 12.4 +2.0/-<br>0.0 mm | 18.4 mm     |   |         |                         |         |
| 16mm      | 330 ±2.0mm                 | 100 ±2.0mm                   | 16.4 +2.0/-<br>0.0 mm | 22.4 mm     |   |         |                         |         |
| 24mm      |                            |                              | 24.4 +2.0/-<br>0.0 mm | 30.4 mm     |   |         |                         |         |
| 32mm      |                            |                              | 32.4 +2.0/-0.0<br>mm  | 38.4 mm     |   |         |                         |         |
| 44mm      |                            |                              | 44.4 +2.0/-0.0<br>mm  | 50.4 mm     |   |         |                         |         |

NOTE:

A. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min)) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.



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## 9. Important Notice

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