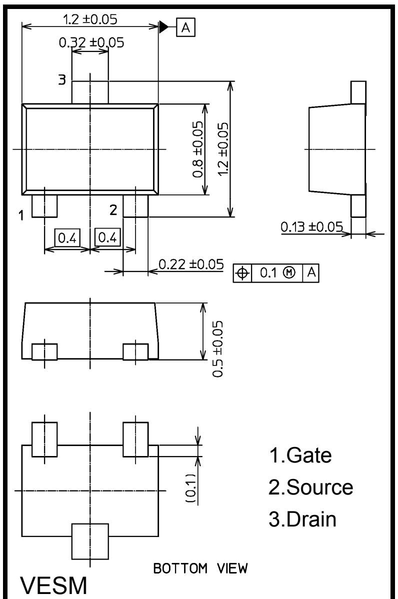
TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type (U-MOSⅥ)

SSM3J56MFV

○ Load Switching Applications

- 1.2 V drive
- Low ON-resistance: $R_{DS(ON)}$ = 390 mΩ (max) (@V_{GS} = -4.5 V)
  $R_{DS(ON)}$ = 480 mΩ (max) (@V_{GS} = -2.5 V)
  $R_{DS(ON)}$ = 660 mΩ (max) (@V_{GS} = -1.8 V)
  $R_{DS(ON)}$ = 900 mΩ (max) (@V_{GS} = -1.5 V)
  $R_{DS(ON)}$ = 4000 mΩ (max) (@V_{GS} = -1.2 V)

Unit: mm



VESM	
JEDEC	—
JEITA	—
TOSHIBA	2-1L1B

Weight: 1.5mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	-20	V
Gate-Source voltage		V_{GSS}	± 8	V
Drain current	DC	I_D (Note 1)	-800	mA
	Pulse	I_{DP} (Note 1)	-1600	
Power dissipation		P_D (Note 2)	150	mW
		P_D (Note 3)	500	
		t < 5s	800	
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

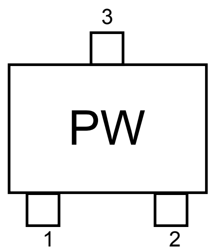
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: The channel temperature should not exceed 150°C during use.

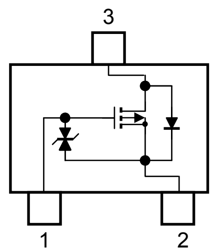
Note 2: Mounted on a FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.585 mm^2)

Note 3: Mounted on a FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

Marking



Equivalent Circuit (top view)



Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance $R_{th\ (ch-a)}$ and Power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration.

Start of commercial production
2011-05

Electrical Characteristics (Ta = 25°C)

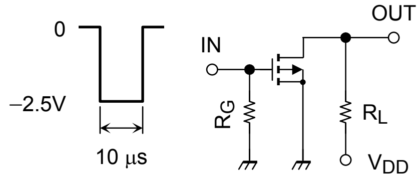
Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	I_D = -1 mA, V_{GS} = 0 V	-20	—	—	V
	$V_{(BR)DSX}$	I_D = -1 mA, V_{GS} = 5 V (Note 5)	-15	—	—	V
Drain cut-off current	I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V	—	—	-1	μA
Gate leakage current	I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0 V	—	—	±1	μA
Gate threshold voltage	V_{th}	V_{DS} = -3 V, I_D = -1 mA	-0.3	—	-1.0	V
Forward transfer admittance	$\|Y_{fs}\|$	V_{DS} = -3 V, I_D = -100 mA (Note 4)	0.5	1.0	—	S
Drain–source ON-resistance	$R_{DS (ON)}$	I_D = -800 mA, V_{GS} = -4.5 V (Note 4)	—	310	390	mΩ
		I_D = -500 mA, V_{GS} = -2.5 V (Note 4)	—	380	480	
		I_D = -200 mA, V_{GS} = -1.8 V (Note 4)	—	470	660	
		I_D = -100 mA, V_{GS} = -1.5 V (Note 4)	—	560	900	
		I_D = -10 mA, V_{GS} = -1.2 V (Note 4)	—	770	4000	
Input capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	—	100	—	pF
Output capacitance	C_{oss}		—	16	—	
Reverse transfer capacitance	C_{rss}		—	10	—	
Switching time: Turn-on time	t_{on}	V_{DD} = -10 V, I_D = -200 mA, V_{GS} = 0 to -2.5 V, R_G = 50 Ω	—	8	—	ns
Switching time: Turn-off time	t_{off}		—	26	—	
Total gate charge	Q_g	V_{DD} = -10 V, I_D = -800 mA, V_{GS} = -4.5 V	—	1.6	—	nC
Gate-source charge	Q_{gs1}		—	0.2	—	
Gate-drain charge	Q_{gd}		—	0.4	—	
Drain-source forward voltage	V_{DSF}	I_D = 800 mA, V_{GS} = 0 V (Note 4)	—	0.9	1.2	V

Note 4: Pulse test

Note 5: If a forward bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

Switching Time Test Circuit

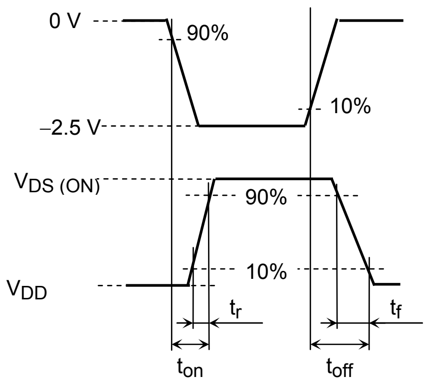
(a) Test Circuit



V_{DD} = -10 V
R_G = 50 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

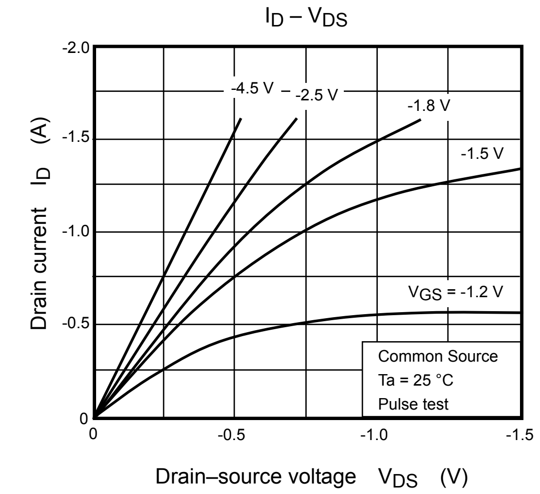
(c) V_{OUT}

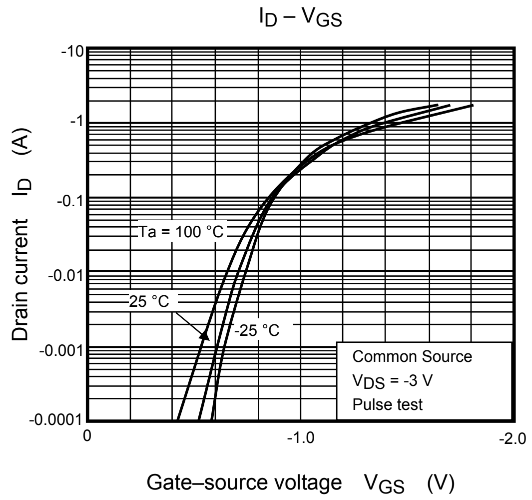


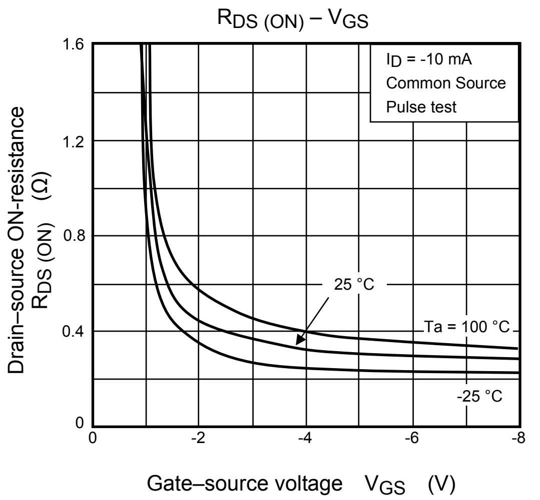
Notice on Usage

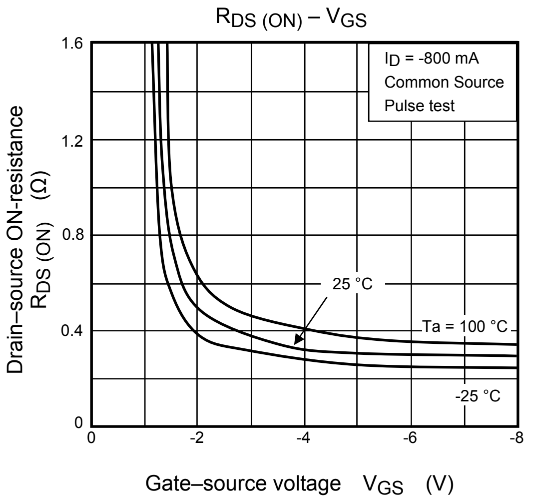
V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D = -1 mA for this product. For normal switching operation, $V_{GS (on)}$ requires a higher voltage than V_{th} and $V_{GS (off)}$ requires a lower voltage than V_{th}. (The relationship can be established as follows: $V_{GS (off)} < V_{th} < V_{GS (on)}$.)

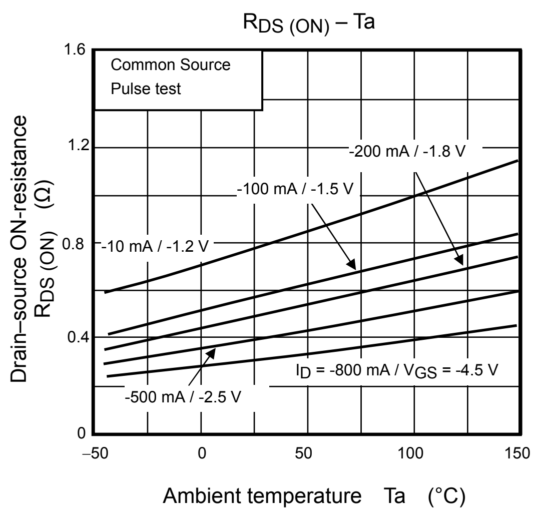
Take this into consideration when using the device.

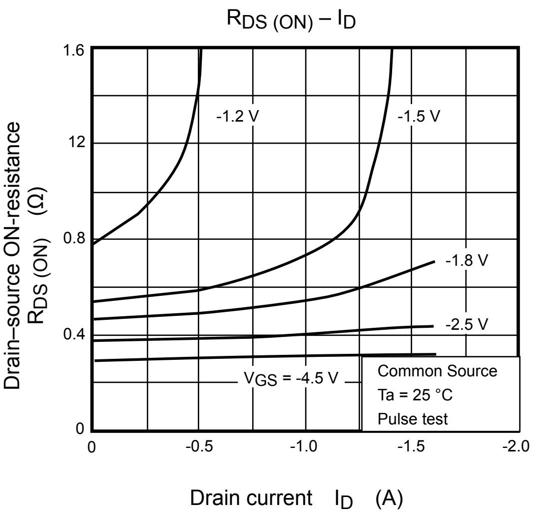

ID – VDS
-2.0
-1.5
-1.0
-0.5
0
Drain current ID (A)
-4.5 V
-2.5 V
-1.8 V
-1.5 V
VGS = -1.2 V
Common Source
Ta = 25 °C
Pulse test
0
-0.5
-1.0
-1.5
Drain–source voltage VDS (V)

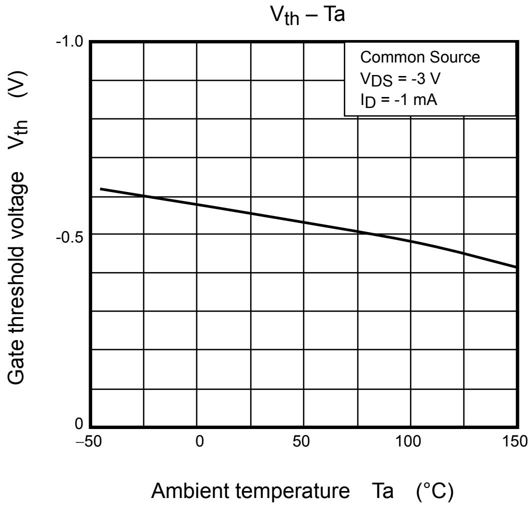

ID – VGS
-10
-1
-0.1
-0.01
-0.001
-0.0001
Drain current ID (A)
Ta = 100 °C
25 °C
-25 °C
Common Source
VDS = -3 V
Pulse test
0
-1.0
-2.0
Gate–source voltage VGS (V)

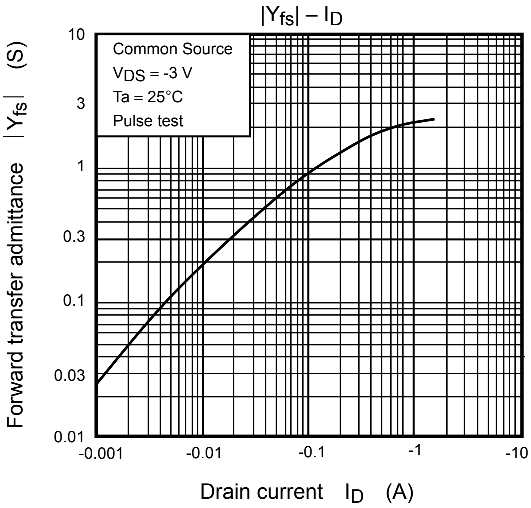

RDS (ON) – VGS
1.6
1.2
0.8
0.4
0
Drain–source ON-resistance RDS (ON) (Ω)
ID = -10 mA
Common Source
Pulse test
25 °C
Ta = 100 °C
-25 °C
0
-2
-4
-6
-8
Gate–source voltage VGS (V)

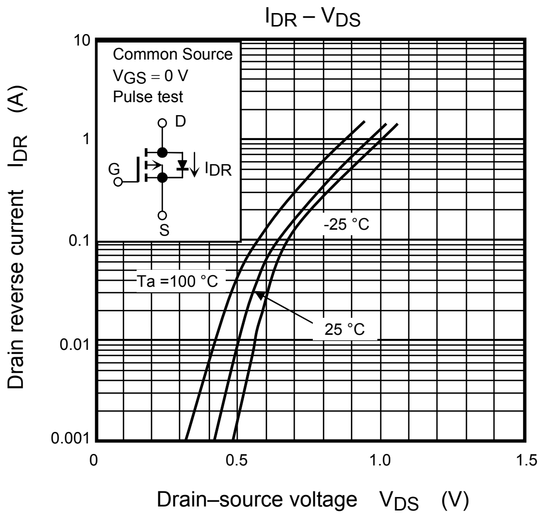

RDS (ON) – VGS
1.6
1.2
0.8
0.4
0
Drain–source ON-resistance RDS (ON) (Ω)
ID = -800 mA
Common Source
Pulse test
25 °C
Ta = 100 °C
-25 °C
0
-2
-4
-6
-8
Gate–source voltage VGS (V)

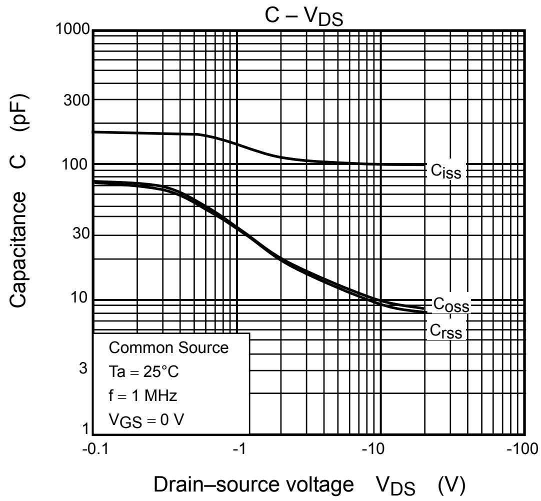

RDS (ON) – Ta
1.6
1.2
0.8
0.4
0
Drain–source ON-resistance RDS (ON) (Ω)
Common Source
Pulse test
-200 mA / -1.8 V
-100 mA / -1.5 V
-10 mA / -1.2 V
ID = -800 mA / VGS = -4.5 V
-500 mA / -2.5 V
–50
0
50
100
150
Ambient temperature Ta (°C)

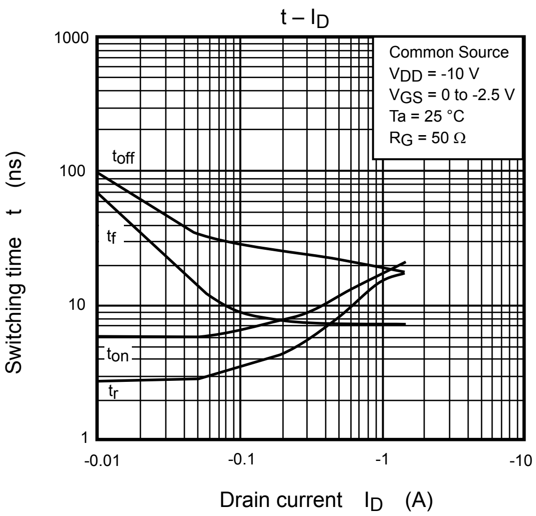

RDS (ON) – ID
1.6
12
0.8
0.4
0
Drain–source ON-resistance RDS (ON) (Ω)
-1.2 V
-1.5 V
-1.8 V
-2.5 V
VGS = -4.5 V
Common Source
Ta = 25 °C
Pulse test
0
-0.5
-1.0
-1.5
-2.0
Drain current ID (A)

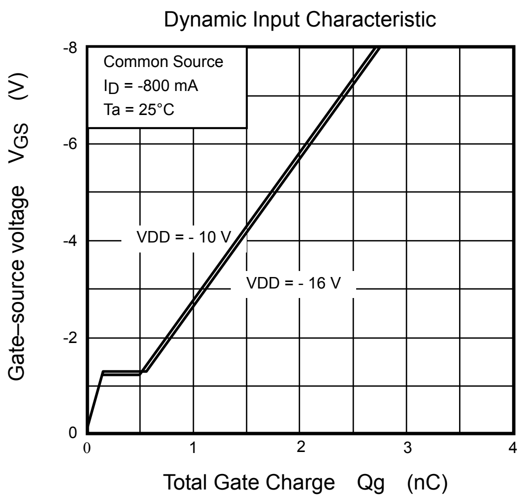

Vth – Ta
Common Source
VDS = -3 V
ID = -1 mA
Gate threshold voltage Vth (V)
-1.0
-0.5
0
–50
0
50
100
150
Ambient temperature Ta (°C)

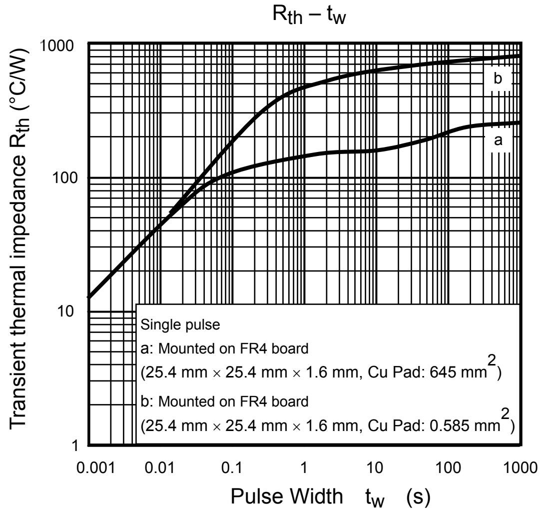

|Yfs| – ID
Common Source
VDS = -3 V
Ta = 25°C
Pulse test
Forward transfer admittance |Yfs| (S)
10
3
1
0.3
0.1
0.03
0.01
-0.001
-0.01
-0.1
-1
-10
Drain current ID (A)

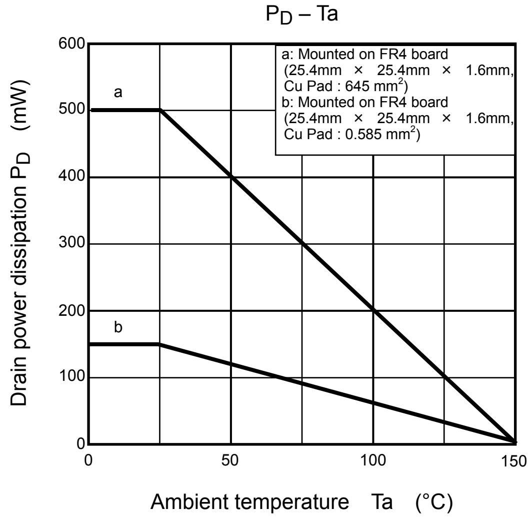

IDR – VDS
Common Source
VGS = 0 V
Pulse test
D
G
IDR
S
-25 °C
Ta =100 °C
25 °C
Drain reverse current IDR (A)
10
1
0.1
0.01
0.001
0
0.5
1.0
1.5
Drain–source voltage VDS (V)


C – VDS
Ciss
Coss
Crss
Common Source
Ta = 25°C
f = 1 MHz
VGS = 0 V
Capacitance C (pF)
1000
300
100
30
10
3
1
-0.1
-1
-10
-100
Drain–source voltage VDS (V)


t – ID
Common Source
VDD = -10 V
VGS = 0 to -2.5 V
Ta = 25 °C
RG = 50 Ω
toff
tf
ton
tr
Switching time t (ns)
1000
100
10
1
-0.01
-0.1
-1
-10
Drain current ID (A)


Dynamic Input Characteristic
Common Source
ID = -800 mA
Ta = 25°C
VDD = - 10 V
VDD = - 16 V
Gate–source voltage VGS (V)
-8
-6
-4
-2
0
0
1
2
3
4
Total Gate Charge Qg (nC)


Rth – tw
Transient thermal impedance Rth (°C/W)
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Pulse Width tw (s)
b
a
Single pulse
a: Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm2)
b: Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.585 mm2)


PD – Ta
Drain power dissipation PD (mW)
600
500
400
300
200
100
0
0
50
100
150
Ambient temperature Ta (°C)
a
b
a: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6mm,
Cu Pad : 645 mm2)
b: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6mm,
Cu Pad : 0.585 mm2)

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