

Features

- Low-voltage operation $V_{DD} = 3.3\text{ V}$
- 1:8 fanout
- Operation to 350 MHz
- Single input configurable for LVDS, LVPECL, or LVTTTL
- 8 pair of LVPECL outputs
- Drives a 50 ohm load
- Low input capacitance
- Low output skew
- Low propagation delay ($t_{pd} = 4\text{ ns}$, typical)
- Commercial and Industrial temperature ranges
- 38-pin TSSOP Package

Description

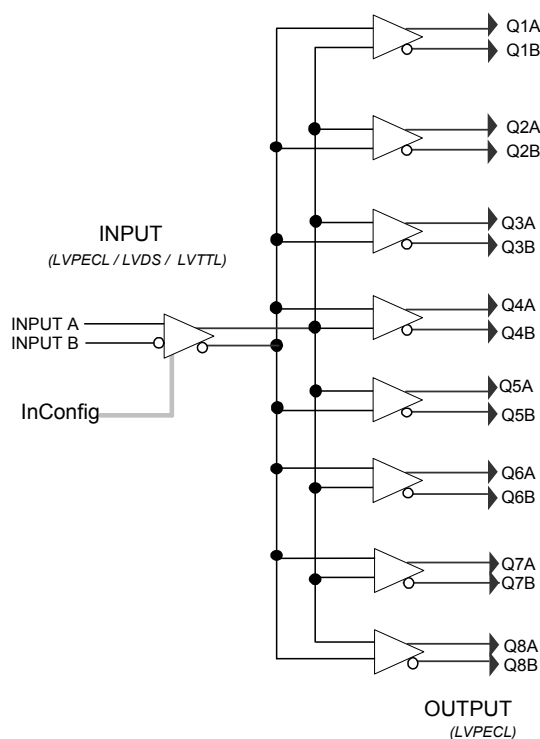
The Cypress CY2DP818 fanout buffer features a single LVDS or a single ended LVTTTL compatible input and eight LVPECL output pairs.

Designed for data-communications clock management applications, the large fanout from a single input reduces loading on the input clock.

The CY2DP818 is ideal for both level translations from single ended to LVPECL and/or for the distribution of LVPECL based clock signals.

The Cypress CY2DP818 has configurable input functions. The input is user configurable via the InConfig pin for single ended or differential input.

Logic Block Diagram

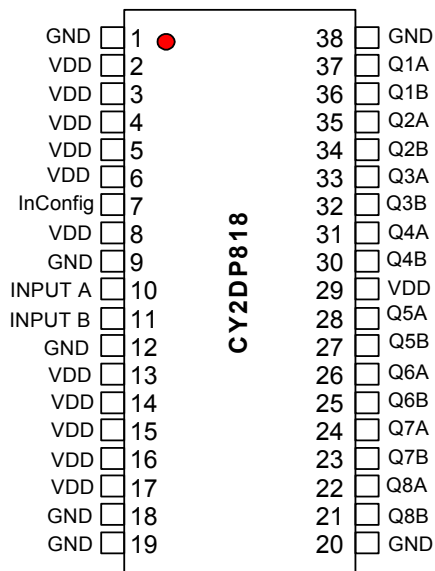


Contents

Pin Configuration	3	Acronyms	11
Pin Description	3	Document Conventions	11
Maximum Ratings	5	Units of Measure	11
DC Electrical Specifications	6	Document History Page	12
AC Switching Characteristics	7	Sales, Solutions, and Legal Information	13
Ordering Information	9	Worldwide Sales and Design Support	13
Ordering Code Definitions	9	Products	13
Package Drawing and Dimensions	10	PSoC Solutions	13

Pin Configuration

Figure 1. 38-pin TSSOP pinout



Pin Description

Pin Number	Pin Name	Type	Description
1, 9, 12, 18, 19, 20, 38	GND	POWER	Ground
2, 3, 4, 5, 6, 8, 13, 14, 15, 16, 17, 29	VDD	POWER	Power Supply
10, 11	Input A, Input B	Default: LVPECL/LDVS Optional: LVTTTL/LVCMOS single pin	Clock Input. Either differential LVPECL/LVDS or single-ended LVTTTL/LVCMOS, as determined by InConfig. See Table 1 and Table 2 for details.
37, 36, 35, 34, 33, 32, 31, 30, 28, 27, 26, 25, 24, 23, 22, 21	Q1(A,B), Q2(A,B), Q3(A,B), Q4(A,B), Q5(A,B), Q6(A,B), Q7(A,B), Q8(A,B)	LVPECL	Differential Output Clocks
7	InConfig	LVTTTL/LVCMOS	Control Input. Selects input type: either differential LVPECL/LVDS or single-ended LVTTTL/LVCMOS. See Table 1 and Table 2 for details.

Table 1. Input Receiver Configuration for Differential or LVTTTL/LVCMOS

InConfig (Pin 7)	Input Receiver Family	Input Receiver Type
1	LVTTTL or LVCMOS	Single ended, non-inverting or inverting, void of bias resistors
0	LVDS or LVPECL	Differential, void of internal termination

Table 2. Single ended LVTTTL/LVCMOS Input Logic (InConfig = 1)

Input A (+) Pin 10	Input B (–) Pin 11	Output Clock QnA Pins
Input	Ground	True
Input	VDD	Invert
Ground	Input	Invert
VDD	Input	True

Maximum Ratings

Exceeding maximum ratings ^[1] may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature: -65 °C to +150 °C

Ambient Temperature: -40 °C to +85 °C

Supply Voltage to Ground Potential

(Inputs and V_{DD} only) -0.3 V to 4.6 V

Supply Voltage to Ground Potential

(Outputs only) -0.3 V to $V_{DD} + 0.3$ V

DC Input Voltage -0.3 V to $V_{DD} + 0.3$ V

DC Output Voltage -0.3 V to $V_{DD} + 0.9$ V

Power Dissipation 0.75 W

Table 3. Power Supply Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I_{CC}	Dynamic Power Supply Current	$V_{DD} = \text{Max}$ Input toggling 50% Duty Cycle, Outputs Open	—	1.5	2.0	mA
I_C	Total Power Supply Current	$V_{DD} = \text{Max}$ Input toggling 50% Duty Cycle, Outputs 50 ohms $f_L = 100$ MHz	—	—	350	mA
$I_{C(\text{Core})}$	Core current when output loads are disabled	$V_{DD} = \text{Max}$ Input toggling 50% Duty Cycle, Outputs not connected to VTT $f_L = 100$ MHz	—	—	50	mA

Note

- Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Specifications

Table 4. LVDS Input, $V_{DD} = 3.3\text{ V} \pm 5\%$, $T_A = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ or $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{ID}	Magnitude of Differential Input Voltage		100	–	600	mV
V_{IC}	Common-mode of Differential Input Voltage $ V_{ID} $ (min and max)		$ V_{ID} /2$	$2.4 - (V_{ID} /2)$		V
V_{IH}	Input High Voltage	Guaranteed Logic High Level	2	–	–	V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level	–	–	0.8	V
I_{IH}	Input High Current	$V_{DD} = \text{Max}$, $V_{IN} = V_{DD}$	–	± 10	± 20	μA
I_{IL}	Input Low Current	$V_{DD} = \text{Max}$, $V_{IN} = V_{SS}$	–	± 10	± 20	μA

Table 5. LVPECL Input, $V_{DD} = 3.3\text{ V} \pm 5\%$, $T_A = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ or $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{ID}	Differential Input Voltage p-p	Guaranteed Logic High Level	400	–	2600	mV
V_{IH}	Input High Voltage	Guaranteed Logic High Level	2.15	–	2.4	V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level	1.5	–	1.8	V
I_{IH}	Input High Current	$V_{DD} = \text{Max}$, $V_{IN} = V_{DD}$	–	± 10	± 20	μA
I_{IL}	Input Low Current	$V_{DD} = \text{Max}$, $V_{IN} = V_{SS}$	–	± 10	± 20	μA
V_{CM}	Common-mode Voltage		–	–	225	mV

Table 6. LVTTTL/LVCMOS Input, $V_{DD} = 3.3\text{ V} \pm 5\%$, $T_A = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ or $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input High Voltage		2	–	–	V
V_{IL}	Input Low Voltage		–	–	0.8	V
I_{IH}	Input High Current	$V_{DD} = \text{Max}$, $V_{IN} = 2.7\text{ V}$	–	–	1	μA
I_{IL}	Input Low Current	$V_{DD} = \text{Max}$, $V_{IN} = 0.5\text{ V}$	–	–	–1	μA
I_I	Input High Current	$V_{DD} = \text{Max}$, $V_{IN} = V_{DD(\text{Max})}$	–	–	20	μA
V_{IK}	Clamp Diode Voltage	$V_{DD} = \text{Min}$, $I_{IN} = -18\text{ mA}$	–	–0.7	–1.2	V
V_H	Input Hysteresis		–	80	–	mV

Table 7. LVPECL Output, $V_{DD} = 3.3 \text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C or -40°C to 85°C

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OD}	Driver Differential Output voltage p-p	$V_{DD} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL} , $R_L = 50 \Omega$	1000	—	3600	mV
V_{OC}	Driver common-mode p-p	$V_{DD} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL} , $R_L = 50 \Omega$	—	—	300	mV
t_R	Rise Time	Differential 20% to 80%, $C_L = 10 \text{ pF}$ to GND, $R_L = 50 \Omega$ to GND	300	—	1200	ps
t_F	Fall Time					
V_{OH}	Output High Voltage	$V_{DD} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OH} = -12 \text{ mA}$	2.1	—	3.0	V
$V_{OL}^{[2]}$	Output Low Voltage	$V_{DD} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL}	0.8	—	1.3	V
I_{OS}	Short Circuit Current	$V_{DD} = \text{Max}$, $V_{OUT} = \text{GND}$	-125	—	-150	mA

AC Switching Characteristics

Table 8. $V_{DD} = 3.3 \text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C or -40°C to 85°C

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay – Low to High	$V_{ID} = 100 \text{ mV}$	3	4	5	ns
t_{PHL}	Propagation Delay – High to Low	$V_{ID} = 100 \text{ mV}$	3	4	5	ns
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)		—	—	0.2	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} - t_{PLH}$)		—	0.2	—	ns
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. Same input signal level and output load.	$V_{ID} = 100 \text{ mV}$	—	—	1	ns

Table 9. High frequency Parametrics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Fmax	Maximum frequency $V_{DD} = 3.3 \text{ V}$	45%–55% duty cycle Standard load circuit	—	—	350	MHz

Note

2. V_{OL} levels are dependent on the termination voltage V_{TT} and termination resistance R_{TT} . Changing either of these values will affect V_{OL} .

Figure 2. Driver Design

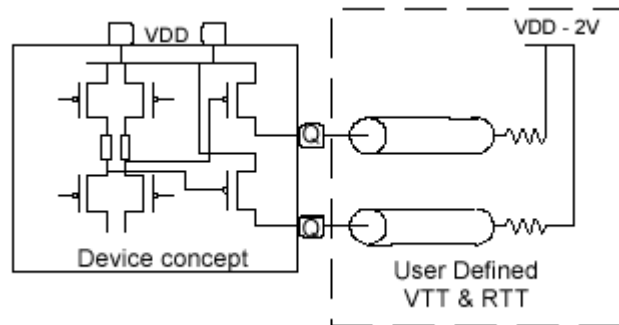


Figure 3. Standard Termination

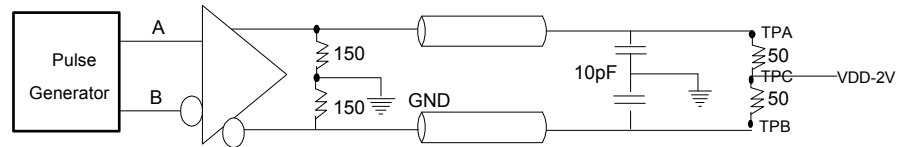


Figure 4. Differential Receiver to Driver Propagation Delay and Driver Transition Time [3,4,5,6]

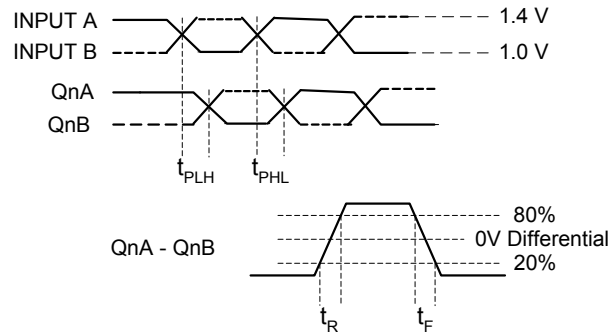
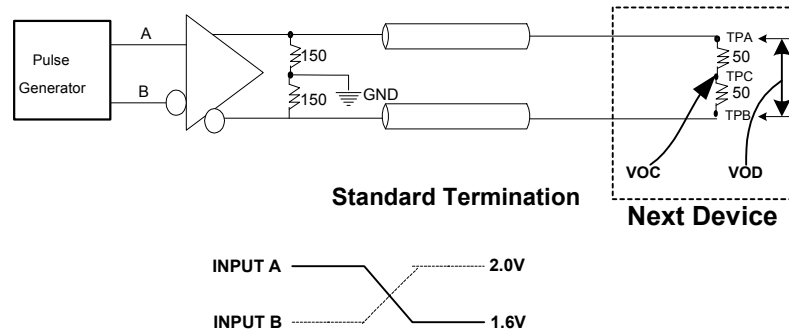


Figure 5. Test Circuit and Voltage Definitions for the Driver Common Mode Output Voltage [3, 4, 5, 6]



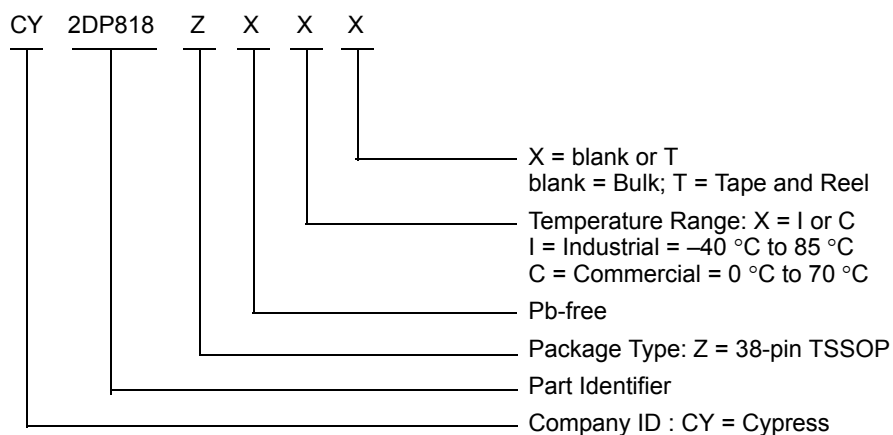
Notes

3. All input pulses are supplied by a frequency generator with the following characteristics: t_R and $t_F \leq 1$ ns; pulse rate = 50 Mpps; pulse width = 10 ± 0.2 ns.
4. $R_L = 50 \text{ ohm} \pm 1\%$; $Z_{line} = 50 \text{ ohm}$ 6".
5. CL includes instrumentation and fixture capacitance within 6 mm of the UT.
6. TPA and B are used for prop delay and Rise/Fall measurements. TPC is used for VOC measurements only and is otherwise connected to $V_{DD} - 2V$.

Ordering Information

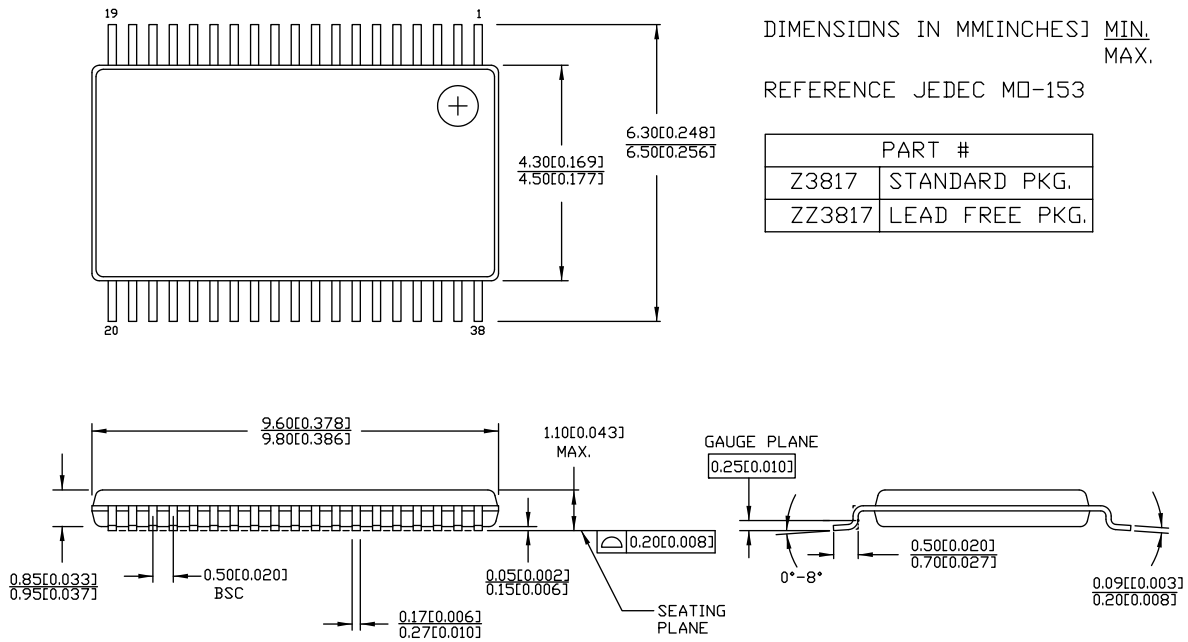
Part Number	Package Type	Product Flow
Pb-free		
CY2DP818ZXI	38-pin TSSOP	Industrial, -40 °C to 85 °C
CY2DP818ZXC	38-pin TSSOP	Commercial, 0 °C to 70 °C

Ordering Code Definitions



Package Drawing and Dimensions

Figure 6. 38-pin TSSOP (9.7 × 4.4 × 1.1 mm) Z3817 / ZZ3817 Package Outline, 51-85151



51-85151 °C

Acronyms

Acronym	Description
LVC MOS	low-voltage complementary metal oxide semiconductor
LVDS	low-voltage differential signaling
LVPECL	low-voltage pseudo (positive) emitter-coupled logic
LVTTTL	low-voltage transistor-transistor logic
TSSOP	thin shrink small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY2DP818, 1:8 Clock Fanout Buffer Document Number: 38-07061				
Rev.	ECN	Orig. of Change	Submission Date	Description of Change
**	107086	06/07/01	IKA	New Data Sheet
*A	115913	07/11/02	CTK	IC, VCM, VOC, Rise/Fall Time Fmax (20)
*B	2748606	08/05/09	KVM	Deleted references to ComLink Minor edits to page 1 text Instances of VCC changed to VDD Changed table sequence to be more logical Edited Table 1 on page 4 and reformatted Table 2 on page 4 for clarity Added voltage and temperature specs to heading of all DC and AC tables Added commercial temp range to DC and AC table headings Clarified wording for IC Core Removed duplicate I_I (input high current) parameter from LVPECL & LVDS Removed T_{PE} and T_{PD} parameters from AC table Cleaned up waveform drawings Removed figures showing inputs for different InConfig values because Table 1 on page 4 and Table 2 on page 4 are more complete Updated Ordering Information (Added part numbers CY2DP818ZXC, CY2DP818ZXCT, CY2DP818ZXI and CY2DP818ZXIT to the ordering information table). Updated Package Drawing and Dimensions .
*C	2899846	KVM	03/26/10	Updated Ordering Information (Removed inactive parts in ordering information table). Updated Package Drawing and Dimensions .
*D	3717888	PURU	08/20/2012	Added Ordering Code Definitions . Updated Package Drawing and Dimensions (spec 51-85151 (Changed revision from *B to *C)). Added Acronyms and Units of Measure . Updated in new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

[psoc.cypress.com/solutions](#)

[PSoC 1](#) | [PSoC 3](#) | [PSoC 5](#)

© Cypress Semiconductor Corporation, 2001-2012. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели,
кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А