



# BUK6Y57-60P

60 V, P-channel Trench MOSFET

5 July 2018

Product data sheet

## 1. General description

P-channel enhancement mode MOSFET in an LFPAK56 (Power SO8) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

This product has been designed and qualified to AEC-Q101 standard for use in high-performance automotive applications such as reverse battery protection.

## 2. Features and benefits

- High thermal power dissipation capability
- Suitable for thermally demanding environments due to 175 °C rating
- Trench MOSFET technology
- AEC-Q101 qualified

## 3. Applications

- Reverse battery protection
- Power management
- High-side loadswitch
- Motor drive

## 4. Quick reference data

Table 1. Quick reference data

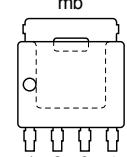
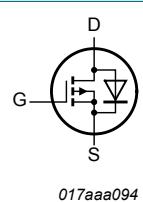
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$		-	-	-60	V
$V_{GS}$	gate-source voltage		[1]	-20	-	20	V
$I_D$	drain current	$V_{GS} = -10 \text{ V}; T_{mb} = 25 \text{ }^\circ\text{C}$		-	-	-23	A
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$		-	-	66	W
<b>Static characteristics</b>							
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10 \text{ V}; I_D = -4.8 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$		-	45	57	$\text{m}\Omega$

[1]  $V_{GS} = -20 \text{ V}/+5 \text{ V}$  according AEC-Q101 at  $T_j = 175 \text{ }^\circ\text{C}$ ;  $V_{GS} = -20 \text{ V}/+20 \text{ V}$  according AEC-Q101 at  $T_j = 150 \text{ }^\circ\text{C}$

**nexperia**

## 5. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BUK6Y57-60P	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

## 7. Marking

**Table 4. Marking codes**

Type number	Marking code
BUK6Y57-60P	6Y5760P

## 8. Limiting values

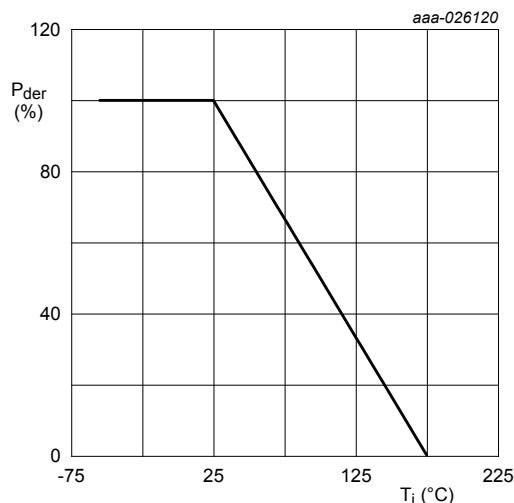
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25^\circ\text{C}$		-	-60	V
$V_{GS}$	gate-source voltage		[1]	-20	20	V
$I_D$	drain current	$V_{GS} = -10\text{ V}; T_{mb} = 25^\circ\text{C}$		-	-23	A
		$V_{GS} = -10\text{ V}; T_{mb} = 100^\circ\text{C}$		-	-16	A
$I_{DM}$	peak drain current	single pulse; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25^\circ\text{C}$		-	-91	A
$P_{tot}$	total power dissipation	$T_{mb} = 25^\circ\text{C}$		-	66	W
$T_j$	junction temperature			-55	175	$^\circ\text{C}$
$T_{amb}$	ambient temperature			-55	175	$^\circ\text{C}$
$T_{stg}$	storage temperature			-65	175	$^\circ\text{C}$
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25^\circ\text{C}$		-	-23	A
$I_{SM}$	peak source current	single pulse; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25^\circ\text{C}$		-	-91	A
<b>ESD maximum rating</b>						
$V_{ESD}$	electrostatic discharge voltage	HBM	[2]	-	1000	V
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{sup} \leq -60\text{ V}; V_{GS} = -10\text{ V}; T_{j(init)} = 25^\circ\text{C}; I_D = -4.8\text{ A}; \text{DUT in avalanche (unclamped)}$		-	3.9	mJ

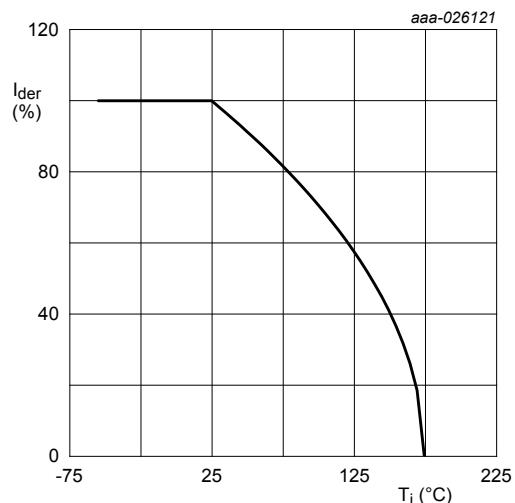
[1]  $V_{GS} = -20\text{ V}/+5\text{ V}$  according AEC-Q101 at  $T_j = 175^\circ\text{C}$ ;  $V_{GS} = -20\text{ V}/+20\text{ V}$  according AEC-Q101 at  $T_j = 150^\circ\text{C}$

[2] Measured between all pins.



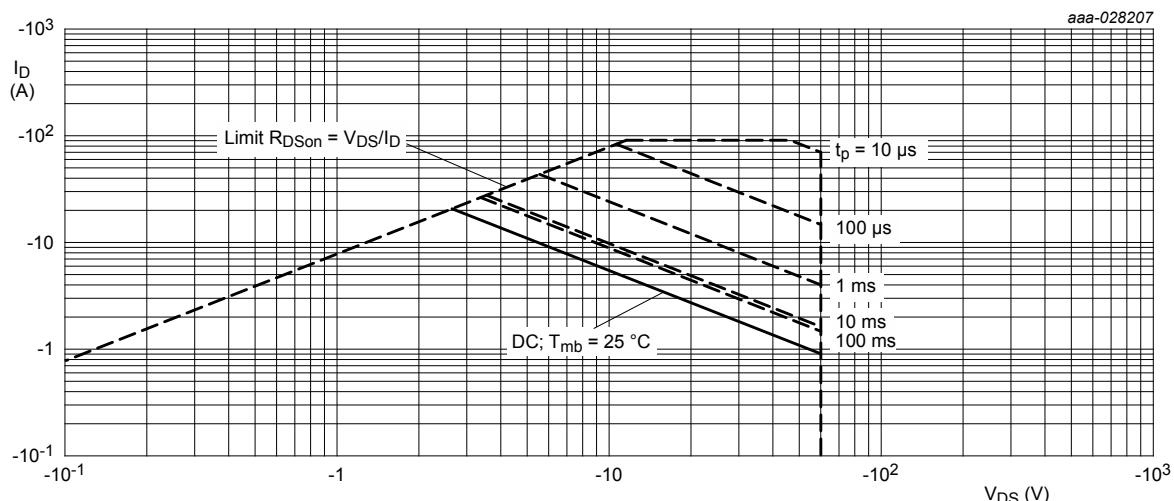
$$P_{der} = \frac{P_{tot}}{P_{tot}(25^\circ\text{C})} \times 100 \text{ \%}$$

**Fig. 1. Normalized total power dissipation as a function of junction temperature**



$$I_{der} = \frac{I_D}{I_D(25^\circ\text{C})} \times 100 \text{ \%}$$

**Fig. 2. Normalized continuous drain current as a function of junction temperature**



**Fig. 3. Safe operating area; junction to mounting base; continuous and peak drain currents as a function of drain-source voltage**

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base			-	1.8	2.3	K/W

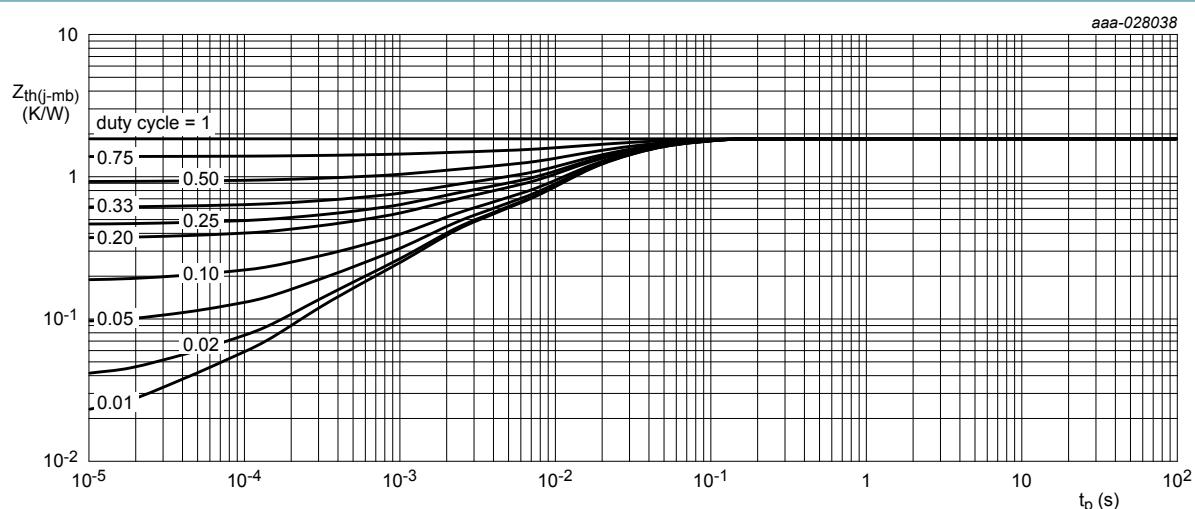


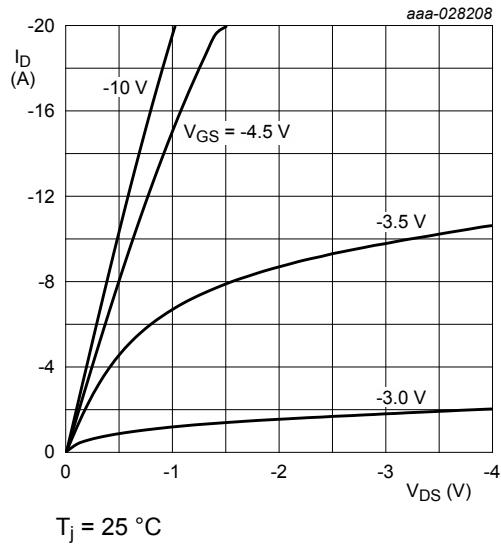
Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

## 10. Characteristics

**Table 7. Characteristics**

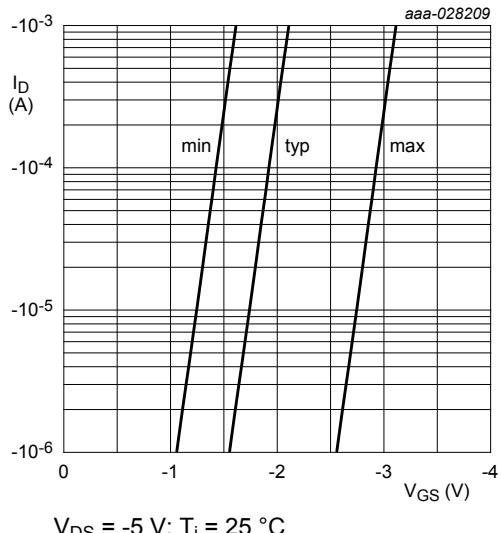
$T_j = 25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Static characteristics</b>							
$V_{(\text{BR})\text{DSS}}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}; V_{GS} = 0 \text{ V}$		-60	-	-	V
$V_{\text{GSTh}}$	gate-source threshold voltage	$I_D = -250 \mu\text{A}; V_{DS}=V_{GS}; T_j = 25^\circ\text{C}$		-1.5	-2	-3	V
$I_{\text{DSS}}$	drain leakage current	$V_{DS} = -60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25^\circ\text{C}$		-	-	-1	$\mu\text{A}$
		$V_{DS} = -60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175^\circ\text{C}$		-	-	-100	$\mu\text{A}$
$I_{\text{GSS}}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25^\circ\text{C}$		-	-	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25^\circ\text{C}$		-	-	-100	nA
$R_{\text{DSon}}$	drain-source on-state resistance	$V_{GS} = -10 \text{ V}; I_D = -4.8 \text{ A}; T_j = 25^\circ\text{C}$		-	45	57	$\text{m}\Omega$
		$V_{GS} = -10 \text{ V}; I_D = -4.8 \text{ A}; T_j = 175^\circ\text{C}$		-	100	127	$\text{m}\Omega$
		$V_{GS} = -4.5 \text{ V}; I_D = -3.9 \text{ A}$		-	58	87	$\text{m}\Omega$
$g_{\text{fs}}$	forward transconductance	$V_{DS} = -10 \text{ V}; I_D = -2 \text{ A}; T_j = 25^\circ\text{C}$		-	65	-	s
$R_G$	gate resistance	$f = 1 \text{ MHz}$		-	7	-	$\Omega$
<b>Dynamic characteristics</b>							
$Q_{\text{G(tot)}}$	total gate charge	$V_{DS} = -30 \text{ V}; I_D = -5.3 \text{ A}; V_{GS} = -10 \text{ V}$		-	21	24	nC
$Q_{\text{GS}}$	gate-source charge			-	3.7	-	nC
$Q_{\text{GD}}$	gate-drain charge			-	4.6	-	nC
$C_{\text{iss}}$	input capacitance	$V_{DS} = -30 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$		-	1200	-	pF
$C_{\text{oss}}$	output capacitance			-	105	-	pF
$C_{\text{rss}}$	reverse transfer capacitance			-	56	-	pF
$t_{\text{d(on)}}$	turn-on delay time	$V_{DS} = -30 \text{ V}; I_D = -4.8 \text{ A}; V_{GS} = -10 \text{ V}; R_{\text{G(ext)}} = 6 \Omega$		-	6	-	ns
$t_r$	rise time			-	12	-	ns
$t_{\text{d(off)}}$	turn-off delay time			-	39	-	ns
$t_f$	fall time			-	16	-	ns
<b>Source-drain diode</b>							
$V_{\text{SD}}$	source-drain voltage	$I_S = -22.7 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25^\circ\text{C}$		-	-0.7	-1.2	V
$t_{\text{rr}}$	reverse recovery time	$I_S = -4.8 \text{ A}; dI_S/dt = 100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = -30 \text{ V}; T_j = 25^\circ\text{C}$		-	30	-	ns
$Q_r$	recovered charge			-	36	-	nC



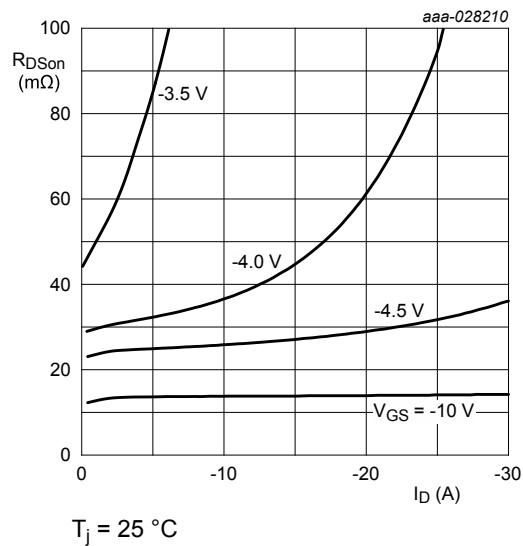
$T_j = 25^\circ\text{C}$

**Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



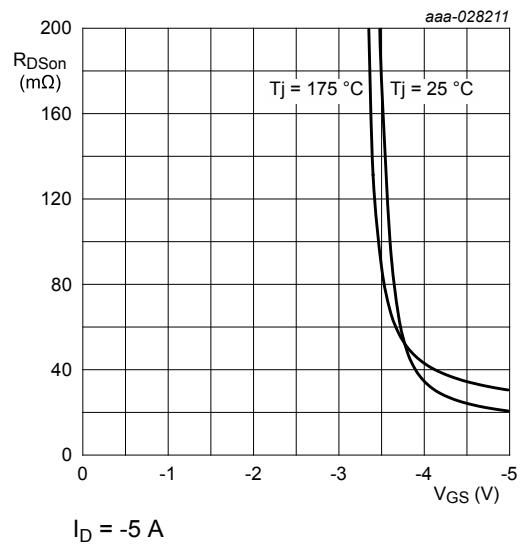
$V_{DS} = -5\text{ V}; T_j = 25^\circ\text{C}$

**Fig. 6. Sub-threshold drain current as a function of gate-source voltage**



$T_j = 25^\circ\text{C}$

**Fig. 7. Drain-source on-state resistance as a function of drain current; typical values**



$I_D = -5\text{ A}$

**Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values**

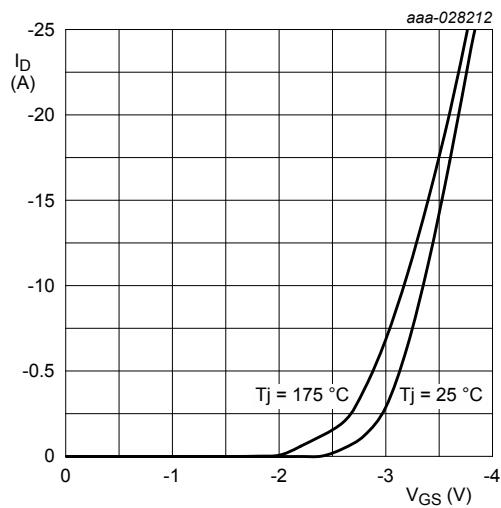


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

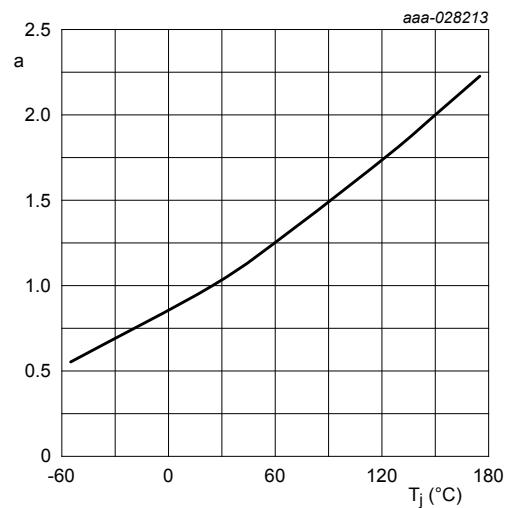


Fig. 10. Normalized drain-source on-state resistance as a function of junction temperature; typical values

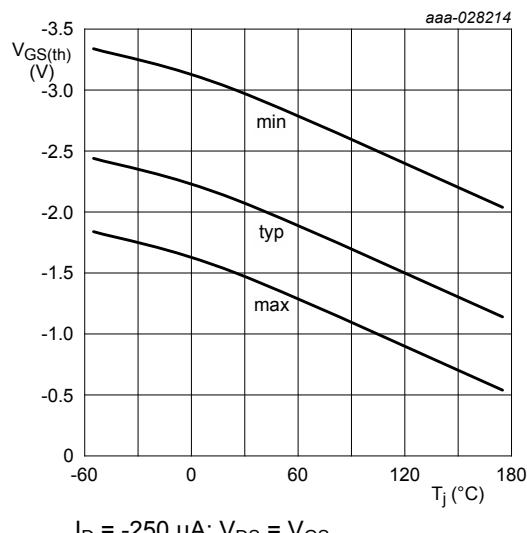


Fig. 11. Gate-source threshold voltage as a function of junction temperature

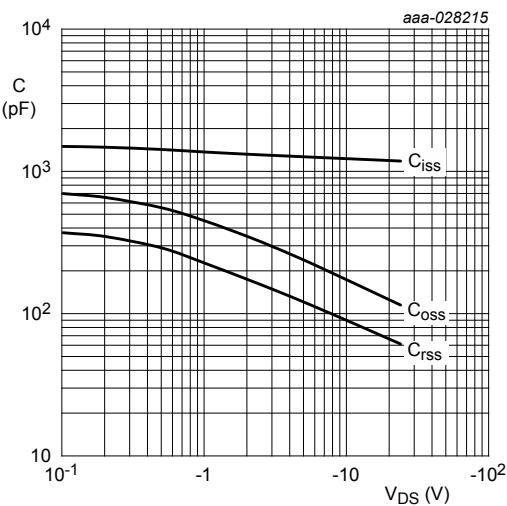


Fig. 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

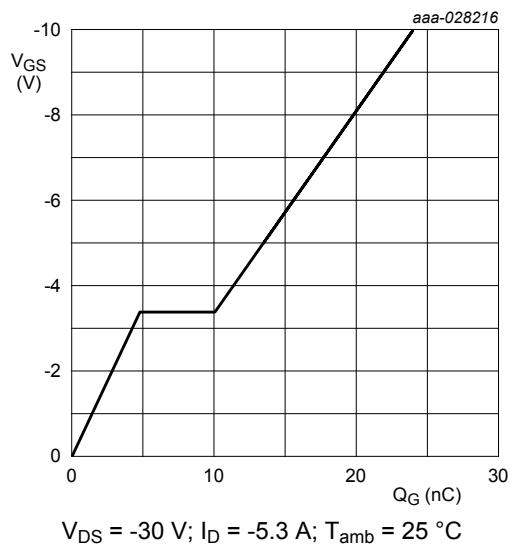


Fig. 13. Gate-source voltage as a function of gate charge; typical values

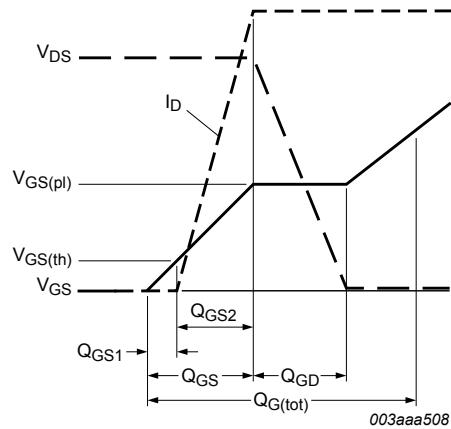


Fig. 14. Gate charge waveform definitions

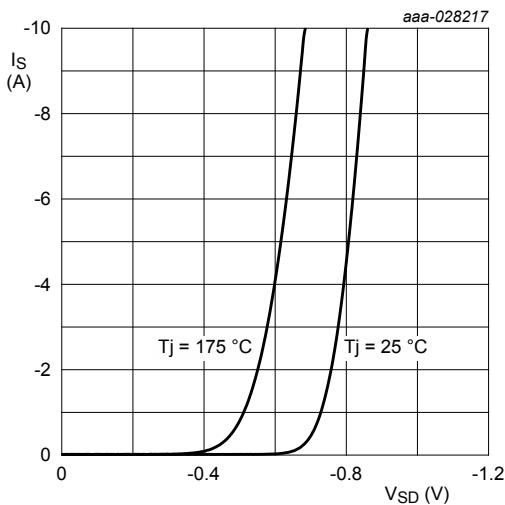


Fig. 15. Source current as a function of source-drain voltage; typical values

## 11. Test information

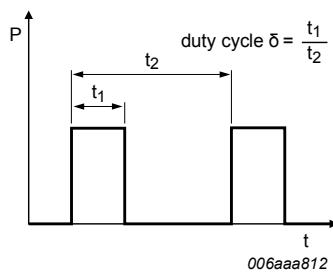


Fig. 16. Duty cycle definition

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

## 12. Package outline

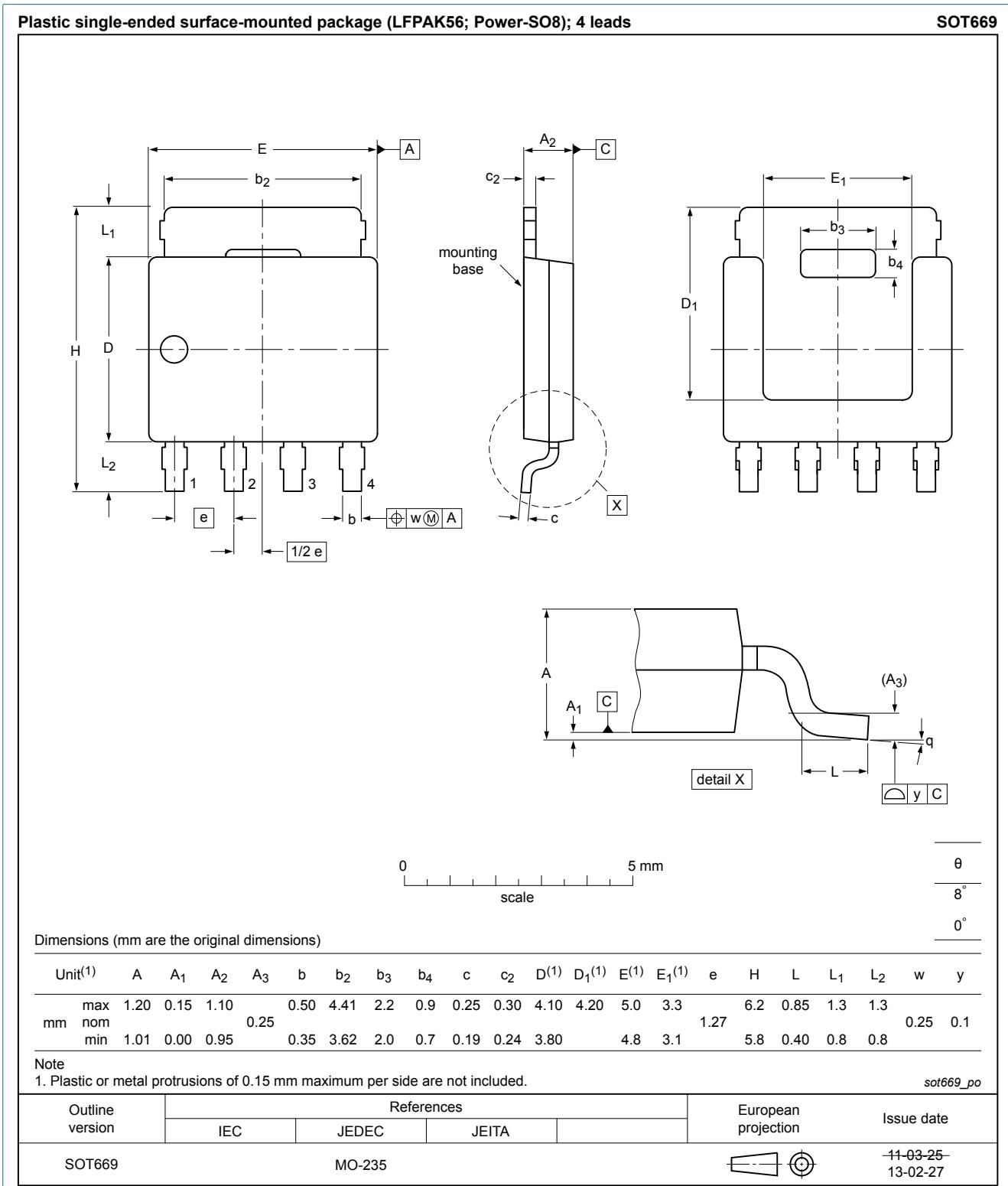


Fig. 17. Package outline LFPAK56; Power-SO8 (SOT669)

## 13. Revision history

**Table 8. Revision history**

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK6Y57-60P v.3	20180705	Product data sheet	-	BUK6Y57-60P v.2
Modifications:	<ul style="list-style-type: none"><li>Characteristics: Fig. 5 updated.</li></ul>			
BUK6Y57-60P v.2	20180606	Product data sheet	-	BUK6Y57-60P v.1
BUK6Y57-60P v.1	20180309	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Date of release: 5 July 2018



# OCEAN CHIPS

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