

Data Sheet

FEATURES

4 channels of low noise amplifiers (LNAs) followed by programmable gain amplifiers (PGAs) Minimum -3 dB bandwidth of 5 MHz Typical -3 dB bandwidth of 42.3 MHz Typical slew rate of 28 V/µs Differential input and output Gain of 18 dB to 36 dB in 6 dB steps Selectable low noise and low power modes Input referred noise of 4.5 nV/√Hz at 18.3 mW per channel Input referred noise of 3.8 nV/√Hz at 26.5 mW per channel Input referred noise of 3.6 nV/√Hz at 34.8 mW per channel Input referred noise of 3.4 nV/√Hz at 54.8 mW per channel Channel to channel gain matching of ±0.25 dB Absolute gain error of ±0.5 dB SPI programmable Power-down mode (SPI selectable) 3.1 V p-p differential output swing when using a 3.3 V supply 32-lead, 5 mm × 5 mm LFCSP package Specified from -40°C to +125°C Qualified for automotive applications

APPLICATIONS

Automotive radar Adaptive cruise control Collision avoidance Blind spot detection Self parking Electronic bumpers GENERAL DESCRIPTION

The ADA8282 is designed for applications that require low cost, low power, compact size, and flexibility. The ADA8282 has four parallel channels, each including an LNA and a PGA. The LNA and PGA combine to form a signal chain that features a gain range of 18 dB to 36 dB in 6 dB increments with a guaranteed minimum bandwidth of 5 MHz.

Using the highest power settings, the combined input referred voltage noise of the combined LNA and PGA channel is $3.4 \text{ nV}/\sqrt{\text{Hz}}$ at maximum gain.

Radar Receive Path AFE: 4-Channel LNA and PGA

ADA8282

FUNCTIONAL BLOCK DIAGRAM



The ADA8282 can be configured in four power modes that trade off power and noise performance to optimize the overall performance according to the end application.

Fabricated in an advanced complementary metal-oxide semiconductor (CMOS) process, the ADA8282 is available in a 5 mm \times 5 mm, RoHS-compliant, 32-lead LFCSP. It is specified over the automotive temperature range of -40°C to +125°C.

Rev. 0

Document Feedback

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REVISION HISTORY

7/15—Revision 0: Initial Version

SPECIFICATIONS

AVDD = 3.3 V, LNA + PGA gain = 36 dB (LNA gain = 24 dB, PGA gain = 12 dB), $T_A = -40^{\circ}$ C to +125°C, PGA_BIAS_SEL = b'10, LNA_BIAS_SEL = b'10, unless otherwise noted.

Table 1.					
Parameter	Test Conditions/Comments	Min	Тур	Max	Unit
ANALOG CHANNEL CHARACTERISTICS					
Gain			18/24/30/36		dB
Gain Range			18		dB
Gain Error				±0.5	dB
–3 dB Bandwidth	V _{OUT} = 100 mV p-p, gain = 36 dB				
	PGA_BIAS_SEL = b'00, LNA_BIAS_SEL = b'00	5	20.5		MHz
	PGA_BIAS_SEL = b'01, LNA_BIAS_SEL = b'01	5	34.2		MHz
	PGA_BIAS_SEL = b'01, LNA_BIAS_SEL = b'10	5	42.3		MHz
	PGA_BIAS_SEL = b'11, LNA_BIAS_SEL = b'11	5	52.3		MHz
Channel to Channel Gain Matching	Frequencies up to 5 MHz		0.1	±0.25	dB
Channel to Channel Phase Matching ¹	Frequencies up to 5 MHz		0.1	±1	Degrees
Slew Rate			28		V/µs
Input Referred Noise	Gain = 36 dB at 2 MHz				
	PGA_BIAS_SEL = b'00, LNA_BIAS_SEL = b'00		4.5		nV/√Hz
	PGA_BIAS_SEL = b'01, LNA_BIAS_SEL = b'01		3.8		nV/√Hz
	PGA_BIAS_SEL = b'01, LNA_BIAS_SEL = b'10		3.6		nV/√Hz
	PGA_BIAS_SEL = b'11, LNA_BIAS_SEL = b'11		3.4		nV/√Hz
	50Ω impedance used for voltage to power conversion		-156		dBm/Hz
Output Referred Noise	Gain = 18 dB		36		nV/√Hz
	Gain = 24 dB		61		nV/√Hz
	Gain = 30 dB		115		nV/√Hz
	Gain = 36 dB		218		nV/√Hz
Offset Voltage					
Referred to Input	Gain = 36 dB		±0.8	±3	mV
Referred to Output	Gain = 36 dB		±50	±200	mV
SPI Offset Adjustment Resolution (Relative to Input)	LNA_BIAS_SEL = b'00		113		μV
	LNA_BIAS_SEL = b'01		186		μV
	$LNA_BIAS_SEL = b'10$		250		μV
	$LNA_BIAS_SEL = b'11$		440		μV
SPI Offset Adjustment Range (Relative to Input)	LNA_BIAS_SEL = b'00		±4		mV
	LNA_BIAS_SEL = b'01		±б		mV
	LNA_BIAS_SEL = b'10		±8		mV
	LNA BIAS SEL = $b'11$		±14		mV
Harmonic Distortion					
Second Harmonic (HD2)	$V_{OUT} = 2 V p - p, f_{IN} = 100 \text{ kHz}$		-70		dBc
	$V_{OUT} = 100 \text{ mV p-p}, f_{IN} = 2 \text{ MHz}$		-85		dBc
Third Harmonic (HD3)	$V_{OUT} = 2 V p - p, f_{IN} = 100 \text{ kHz}$		-85		dBc
	$V_{OUT} = 100 \text{ mV p-p}, f_{IN} = 2 \text{ MHz}$		-95		dBc
Intermodulation Distortion	V _{OUT} = 2 V p-p, f _{IN1} = 100 kHz, f _{IN2} = 150 kHz		-72		dBc
	$V_{OUT} = 100 \text{ mV p-p}, f_{IN1} = 2 \text{ MHz}, f_{IN2} = 2.1 \text{ MHz}$		-83		dBc
Common-Mode Rejection Ratio (CMRR)			-80		dB
Crosstalk			-105		dBc

	1	T			
Parameter	Test Conditions/Comments	Min	Тур	Мах	Unit
POWER SUPPLY					
Total Power Dissipation					
	PGA_BIAS_SEL = b'00, LNA_BIAS_SEL = b'00			73	mW
	PGA_BIAS_SEL = b'01, LNA_BIAS_SEL = b'01			106	mW
	PGA_BIAS_SEL = b'01, LNA_BIAS_SEL = b'10			139	mW
	PGA_BIAS_SEL = b'11, LNA_BIAS_SEL = b'11			219	mW
Power Dissipation per Channel			31		mW
AVDD		3.0		3.6	V
VIO		1.8		3.6	V
lavdd	Four channels active				
	PGA_BIAS_SEL = b'00, LNA_BIAS_SEL = b'00		19.6	22	mA
	PGA_BIAS_SEL = b'01, LNA_BIAS_SEL = b'01		29	32	mA
	PGA_BIAS_SEL = b'01, LNA_BIAS_SEL = b'10		37.7	42	mA
	PGA_BIAS_SEL = b'11, LNA_BIAS_SEL = b'11		60	66.3	mA
	One channel active		9.8	11	mA
lvio			10	12	μA
Power-Down Current	I _{AVDD} and I _{VIO}		20	100	μA
Power-Down Dissipation			0.07	0.33	mW
Power-Up Time	Time to operational after chip is enabled		5		μs
Power Supply Rejection Ratio (PSRR)	At dc	-80			dB
	At 1 MHz		-80		dB
INPUT					
Input Resistance					
Differential Input Resistance		1.45	1.57	1.7	kΩ
Common-Mode Input Resistance		0.37	0.39	0.42	kΩ
Differential Input Capacitance		10.8	12	13.2	pF
OUTPUT					
Output Voltage Swing	+OUTx (–OUTx), gain = 18 dB	3.1			V р-р
	+OUTx (-OUTx), gain = 24 dB, 30 dB, or 36 dB	6.3			Vp-p
Output Balance	$f_{IN} = 100 \text{ kHz}$	1	-70		dB
Short-Circuit Current	Per output at 25°C	1	205		mA
Capacitive Load	20% overshoot		30		pF

 $^{\rm 1}$ Normalized to 0° phase matching at 25°C; see the Theory of Operation section for details.

DIGITAL SPECIFICATIONS

AVDD = 3.3 V, $T_A = -40^{\circ}$ C to +125°C, unless otherwise noted.

Parameter	Temperature	Min	Тур	Max	Unit
LOGIC INPUT (CS)					
Logic 1 Voltage	Full	1.2		VIO + 0.3	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		15		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUTS (SDI, SCLK, RESET)					
Logic 1 Voltage	Full	1.2		VIO + 0.3	V
Logic 0 Voltage	Full	0		0.3	V
Input Resistance	25°C		2.5		kΩ
Input Capacitance	25°C		2		pF
Maximum SCLK Frequency				10	MHz
LOGIC OUTPUT (SDO)					
Logic 1 Voltage ($I_{OH} = 800 \ \mu A$)	Full	VIO – 0.3			V
Logic 0 Voltage ($I_{OL} = 50 \mu A$)	Full			0.3	V

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Electrical	
AVDD to EPAD	–0.3 V to +3.9 V
+INx, –INx, SCLK, SDI, SDO, CS, VIO, RESET,	-0.3V to AVDD +
–OUTx, +OUTx to EPAD	0.3 V
ESD Ratings	
Human Body Model (HBM)	±4000 V
Charged Device Model (CDM)	±2000 V
Environmental	
Operating Temperature Range (Ambient)	-40°C to +125°C
Storage Temperature Range (Ambient)	–65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

 θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ」Α	θıc	Unit
32-Lead, 5 mm × 5 mm LFCSP	33.51	4.1	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

0FADExposed Pad. Tie the exposed pad on the bottom side of the package to the analog/digital ground plane.1+INAPositive LNA Analog Input for Channel A.3+INBNegative LNA Analog Input for Channel B.3+INBPositive LNA Analog Input for Channel B.4-INCNegative LNA Analog Input for Channel B.5+INCPositive LNA Analog Input for Channel C.6-INCNegative LNA Analog Input for Channel C.7+INDNegative LNA Analog Input for Channel D.8-INDPositive LNA Analog Input for Channel D.8-INDNo Internal Connection. Leave this pin floating.10NICNo Internal Connection. Leave this pin floating.11NICNo Internal Connection. Leave this pin floating.12NICNo Internal Connection. Leave this pin floating.13NICNo Internal Connection. Leave this pin floating.14NICNo Internal Connection. Leave this pin floating.15NICNo Internal Connection. Leave this pin floating.16AVDD3.3 V Analog Output for Channel D.17-OUTDNegative Analog Output for Channel D.18+OUTDPositive Analog Output for Channel B.20-OUTCNegative Analog Output for Channel B.21-OUTBNegative Analog Output for Channel B.22-OUTBNegative Analog Output for Channel C.23-OUTCNegative Analog Output for Channel B.24+OUTAPositive Analog Output for Channel A	Pin No.	Mnemonic	Description
1+INAPositive LNA Analog Input for Channel A.2-INANegative LNA Analog Input for Channel A.3+INBPositive LNA Analog Input for Channel B.4-INBNegative LNA Analog Input for Channel C.5+INCPositive LNA Analog Input for Channel C.6-INCNegative LNA Analog Input for Channel D.7+INDPositive LNA Analog Input for Channel D.8-INDNegative LNA Analog Input for Channel D.9AVDD3.3 V Analog Supply.10NICNo Internal Connection. Leave this pin floating.11NICNo Internal Connection. Leave this pin floating.12NICNo Internal Connection. Leave this pin floating.13NICNo Internal Connection. Leave this pin floating.14NICNo Internal Connection. Leave this pin floating.15NICNo Internal Connection. Leave this pin floating.16AVDD3.3 V Analog Supply.17-OUTDNegative Analog Output for Channel D.18+OUTDPositive Analog Output for Channel D.19-OUTCNegative Analog Output for Channel C.20+OUTDPositive Analog Output for Channel A.21+OUTBNegative Analog Output for Channel A.22+OUTBNegative Analog Output for Channel A.23-OUTANegative Analog Output for Channel A.24+OUTBNegative Analog Output for Channel A.25AVDD3.3 V Analog Output for Channel A.26 <t< td=""><td>0</td><td>EPAD</td><td>Exposed Pad. Tie the exposed pad on the bottom side of the package to the analog/digital ground plane.</td></t<>	0	EPAD	Exposed Pad. Tie the exposed pad on the bottom side of the package to the analog/digital ground plane.
2-INANegative LNA Analog Input for Channel A.3+INBPositive LNA Analog Input for Channel B.5+INCNegative LNA Analog Input for Channel B.5+INCPositive LNA Analog Input for Channel C.6-INCNegative LNA Analog Input for Channel C.7+INDPositive LNA Analog Input for Channel D.8-INDNegative LNA Analog Input for Channel D.9AVDD3.3 V Analog Supply.10NICNo Internal Connection. Leave this pin floating.11NICNo Internal Connection. Leave this pin floating.12NICNo Internal Connection. Leave this pin floating.13NICNo Internal Connection. Leave this pin floating.14NICNo Internal Connection. Leave this pin floating.15NICNo Internal Connection. Leave this pin floating.16AVDD3.3 V Analog Supply.17-OUTDNegative Analog Output for Channel D.18+OUTDPositive Analog Output for Channel D.19-OUTCNegative Analog Output for Channel D.19-OUTCNegative Analog Output for Channel C.20+OUTDPositive Analog Output for Channel B.21-OUTBNegative Analog Output for Channel B.22+OUTBPositive Analog Output for Channel B.23-OUTANegative Analog Output for Channel A.24+OUTBPositive Analog Output for Channel A.25AVDD3.3 V Analog Supply.26VIOS	1	+INA	Positive LNA Analog Input for Channel A.
3+INBPositive LNA Analog Input for Channel B.4-INBNegative LNA Analog Input for Channel B.5+INCPositive LNA Analog Input for Channel C.6-INCNegative LNA Analog Input for Channel C.7+INDPositive LNA Analog Input for Channel D.8-INDNegative LNA Analog Input for Channel D.9AVDD3.3 V Analog Supply.10NICNo Internal Connection. Leave this pin floating.11NICNo Internal Connection. Leave this pin floating.12NICNo Internal Connection. Leave this pin floating.13NICNo Internal Connection. Leave this pin floating.14NICNo Internal Connection. Leave this pin floating.15NICNo Internal Connection. Leave this pin floating.16AVDD3.3 V Analog Supply.17-OUTDNegative Analog Output for Channel D.18+OUTDPositive Analog Output for Channel D.19-OUTCNegative Analog Output for Channel D.20+OUTDPositive Analog Output for Channel C.21+OUTBNegative Analog Output for Channel C.22+OUTBNegative Analog Output for Channel B.23-OUTANegative Analog Output for Channel A.24+OUTBPositive Analog Output for Channel A.25YOD3.3 V Analog Supply.26VIODigitive Analog Output for Channel A.27Positive Analog Output for Channel A.28AVDD3.3 V Analog Suppl	2	–INA	Negative LNA Analog Input for Channel A.
4-INBNegative LNA Analog Input for Channel B.5+INCPositive LNA Analog Input for Channel C.6-INCNegative LNA Analog Input for Channel D.7+INDPositive LNA Analog Input for Channel D.8-INDNegative LNA Analog Input for Channel D.9AVDD3.3 V Analog Supply.10NICNo Internal Connection. Leave this pin floating.11NICNo Internal Connection. Leave this pin floating.12NICNo Internal Connection. Leave this pin floating.13NICNo Internal Connection. Leave this pin floating.14NICNo Internal Connection. Leave this pin floating.15NICNo Internal Connection. Leave this pin floating.16AVDD3.3 V Analog Supply.17-OUTDNegative Analog Output for Channel D.18+OUTDPositive Analog Output for Channel D.19-OUTCNegative Analog Output for Channel D.20+OUTCPositive Analog Output for Channel C.21-OUTBNegative Analog Output for Channel C.22+OUTBPositive Analog Output for Channel B.23-OUTANegative Analog Output for Channel B.24+OUTAPositive Analog Output for Channel A.25AVDD3.3 V Analog Supply.26VIODigital Level Select for SPI and RESET. This pin can accept 1.8 V to 3.3 V.27RESTReset Input. REST overrides the SPI and powers down the device and returns all settings back to default. RESET is pulled to gr	3	+INB	Positive LNA Analog Input for Channel B.
5+INCPositive LNA Analog Input for Channel C.6-INDNegative LNA Analog Input for Channel D.7+INDPositive LNA Analog Input for Channel D.8-INDNegative LNA Analog Input for Channel D.9AVDD3.3 V Analog Supply.10NICNo Internal Connection. Leave this pin floating.11NICNo Internal Connection. Leave this pin floating.12NICNo Internal Connection. Leave this pin floating.13NICNo Internal Connection. Leave this pin floating.14NICNo Internal Connection. Leave this pin floating.15NICNo Internal Connection. Leave this pin floating.16AVDD3.3 V Analog Supply.17-OUTDNegative Analog Output for Channel D.18+OUTDPositive Analog Output for Channel D.19-OUTCNegative Analog Output for Channel D.19-OUTCNegative Analog Output for Channel C.21+OUTCPositive Analog Output for Channel C.22+OUTBNegative Analog Output for Channel B.23-OUTANegative Analog Output for Channel B.24+OUTAPositive Analog Output for Channel A.25AVDD3.3 V Analog Supply.26VIODigital Level Select for SPI and RESET. This pin can accept 1.8 V to 3.3 V.27RESETReset Input. RESET overrides the SPI and powers down the device and returns all settings back to default. RESET is pulled to ground by default. A logic high triggers the reset.28S	4	–INB	Negative LNA Analog Input for Channel B.
66-INCNegative LNA Analog Input for Channel C.7+INDPositive LNA Analog Input for Channel D.8-INDNegative LNA Analog Input for Channel D.9AVDD3.3 V Analog Supply.10NICNo Internal Connection. Leave this pin floating.11NICNo Internal Connection. Leave this pin floating.12NICNo Internal Connection. Leave this pin floating.13NICNo Internal Connection. Leave this pin floating.14NICNo Internal Connection. Leave this pin floating.15NICNo Internal Connection. Leave this pin floating.16AVDD3.3 V Analog Supply.17-OUTDNegative Analog Output for Channel D.18+OUTDPositive Analog Output for Channel D.19-OUTCNegative Analog Output for Channel D.20+OUTCPositive Analog Output for Channel C.21+OUTDPositive Analog Output for Channel B.22+OUTBPositive Analog Output for Channel B.23+OUTANegative Analog Output for Channel B.24+OUTAPositive Analog Output for Channel A.25AVDD3.3 V Analog Supply.26VIODigital Level Select for SPI and RESET. This pin can accept 1.8 V to 3.3 V.27Reset Input.RESET or SPI and Powers down the device and returns all settings back to default. RESET is pulled to ground by default. A logic high triggers the reset.28SCLKSerial Clock.29CSChip Select Bar. <t< td=""><td>5</td><td>+INC</td><td>Positive LNA Analog Input for Channel C.</td></t<>	5	+INC	Positive LNA Analog Input for Channel C.
7+INDPositive LNA Analog Input for Channel D.8-INDNegative LNA Analog Input for Channel D.9AVDD3.3 V Analog Supply.9NICNo Internal Connection. Leave this pin floating.11NICNo Internal Connection. Leave this pin floating.12NICNo Internal Connection. Leave this pin floating.13NICNo Internal Connection. Leave this pin floating.14NICNo Internal Connection. Leave this pin floating.15NICNo Internal Connection. Leave this pin floating.16AVDD3.3 V Analog Supply.17-OUTDNegative Analog Output for Channel D.18+OUTDPositive Analog Output for Channel D.19-OUTCNegative Analog Output for Channel C.20+OUTCPositive Analog Output for Channel C.21-OUTBNegative Analog Output for Channel C.22+OUTBPositive Analog Output for Channel B.23-OUTANegative Analog Output for Channel B.24+OUTAPositive Analog Output for Channel A.25AVDD3.3 V Analog Supply.26VIODigital Level Select for SPI and RESET. This pin can accept 1.8 V to 3.3 V.27RESETReset Input. RESET overrides the SPI and powers down the device and returns all settings back to default. RESET is pulled to ground by default. A logic high triggers the reset.28SCLKSerial Clock.29GSChip Select Bar.31SDOSerial Data Output. <td>6</td> <td>–INC</td> <td>Negative LNA Analog Input for Channel C.</td>	6	–INC	Negative LNA Analog Input for Channel C.
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14NICNo Internal Connection. Leave this pin floating.15NICNo Internal Connection. Leave this pin floating.16AVDD3.3 V Analog Supply.17-OUTDNegative Analog Output for Channel D.18+OUTDPositive Analog Output for Channel D.19-OUTCNegative Analog Output for Channel C.20+OUTCPositive Analog Output for Channel C.21-OUTBNegative Analog Output for Channel B.22+OUTBPositive Analog Output for Channel B.23-OUTANegative Analog Output for Channel A.24+OUTAPositive Analog Output for Channel A.25AVDD3.3 V Analog Supply.26VIODigital Level Select for SPI and RESET. This pin can accept 1.8 V to 3.3 V.27RESETReset Input. RESET overrides the SPI and powers down the device and returns all settings back to default. RESET is pulled to ground by default. A logic high triggers the reset.28SCLKSerial Clock.29CSChip Select Bar.31SDOSerial Data Output.	13	NIC	No Internal Connection. Leave this pin floating.
15NICNo Internal Connection. Leave this pin floating.16AVDD3.3 V Analog Supply.17-OUTDNegative Analog Output for Channel D.18+OUTDPositive Analog Output for Channel D.19-OUTCNegative Analog Output for Channel C.20+OUTCPositive Analog Output for Channel C.21-OUTBNegative Analog Output for Channel B.22+OUTBPositive Analog Output for Channel B.23-OUTANegative Analog Output for Channel A.24+OUTAPositive Analog Output for Channel A.25AVDD3.3 V Analog Supply.26VIODigital Level Select for SPI and RESET. This pin can accept 1.8 V to 3.3 V.27RESETReset Input. RESET overrides the SPI and powers down the device and returns all settings back to default. RESET is pulled to ground by default. A logic high triggers the reset.28SCLKSerial Clock.29CSChip Select Bar.30SDISerial Data Input.31SDOSerial Data Output.	14	NIC	No Internal Connection. Leave this pin floating.
16AVDD3.3 V Analog Supply.17-OUTDNegative Analog Output for Channel D.18+OUTDPositive Analog Output for Channel D.19-OUTCNegative Analog Output for Channel C.20+OUTCPositive Analog Output for Channel C.21-OUTBNegative Analog Output for Channel B.22+OUTBPositive Analog Output for Channel B.23-OUTANegative Analog Output for Channel A.24+OUTAPositive Analog Output for Channel A.25AVDD3.3 V Analog Supply.26VIODigital Level Select for SPI and RESET. This pin can accept 1.8 V to 3.3 V.27RESETReset Input. RESET overrides the SPI and powers down the device and returns all settings back to default. RESET is pulled to ground by default. A logic high triggers the reset.28SCLKSerial Clock.29CSChip Select Bar.30SDISerial Data Input.31SDOSerial Data Output.	15	NIC	No Internal Connection. Leave this pin floating.
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18+OUTDPositive Analog Output for Channel D.19-OUTCNegative Analog Output for Channel C.20+OUTCPositive Analog Output for Channel C.21-OUTBNegative Analog Output for Channel B.22+OUTBPositive Analog Output for Channel B.23-OUTANegative Analog Output for Channel A.24+OUTAPositive Analog Output for Channel A.25AVDD3.3 V Analog Supply.26VIODigital Level Select for SPI and RESET. This pin can accept 1.8 V to 3.3 V.27RESETReset Input. RESET overrides the SPI and powers down the device and returns all settings back to default. RESET is pulled to ground by default. A logic high triggers the reset.28SCLKSerial Clock.29CSChip Select Bar.30SDISerial Data Input.31SDOSerial Data Output.	17	-OUTD	Negative Analog Output for Channel D.
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20+OUTCPositive Analog Output for Channel C.21-OUTBNegative Analog Output for Channel B.22+OUTBPositive Analog Output for Channel B.23-OUTANegative Analog Output for Channel A.24+OUTAPositive Analog Output for Channel A.25AVDD3.3 V Analog Supply.26VIODigital Level Select for SPI and RESET. This pin can accept 1.8 V to 3.3 V.27RESETReset Input. RESET overrides the SPI and powers down the device and returns all settings back to default. RESET is pulled to ground by default. A logic high triggers the reset.28SCLKSerial Clock.29CSChip Select Bar.30SDISerial Data Input.31SDOSerial Data Output.	19	-OUTC	Negative Analog Output for Channel C.
21-OUTBNegative Analog Output for Channel B.22+OUTBPositive Analog Output for Channel B.23-OUTANegative Analog Output for Channel A.24+OUTAPositive Analog Output for Channel A.25AVDD3.3 V Analog Supply.26VIODigital Level Select for SPI and RESET. This pin can accept 1.8 V to 3.3 V.27RESETReset Input. RESET overrides the SPI and powers down the device and returns all settings back to default. RESET is pulled to ground by default. A logic high triggers the reset.28SCLKSerial Clock.29CSChip Select Bar.30SDISerial Data Input.31SDOSerial Data Output.	20	+OUTC	Positive Analog Output for Channel C.
22+OUTBPositive Analog Output for Channel B.23-OUTANegative Analog Output for Channel A.24+OUTAPositive Analog Output for Channel A.25AVDD3.3 V Analog Supply.26VIODigital Level Select for SPI and RESET. This pin can accept 1.8 V to 3.3 V.27RESETReset Input. RESET overrides the SPI and powers down the device and returns all settings back to default. RESET is pulled to ground by default. A logic high triggers the reset.28SCLKSerial Clock.29CSChip Select Bar.30SDISerial Data Input.31SDOSerial Data Output.	21	-OUTB	Negative Analog Output for Channel B.
23-OUTANegative Analog Output for Channel A.24+OUTAPositive Analog Output for Channel A.25AVDD3.3 V Analog Supply.26VIODigital Level Select for SPI and RESET. This pin can accept 1.8 V to 3.3 V.27RESETReset Input. RESET overrides the SPI and powers down the device and returns all settings back to default. RESET is pulled to ground by default. A logic high triggers the reset.28SCLKSerial Clock.29CSChip Select Bar.30SDISerial Data Input.31SDOSerial Data Output.	22	+OUTB	Positive Analog Output for Channel B.
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25AVDD3.3 V Analog Supply.26VIODigital Level Select for SPI and RESET. This pin can accept 1.8 V to 3.3 V.27RESETReset Input. RESET overrides the SPI and powers down the device and returns all settings back to default. RESET is pulled to ground by default. A logic high triggers the reset.28SCLKSerial Clock.29CSChip Select Bar.30SDISerial Data Input.31SDOSerial Data Output.	24	+OUTA	Positive Analog Output for Channel A.
26VIODigital Level Select for SPI and RESET. This pin can accept 1.8 V to 3.3 V.27RESETReset Input. RESET overrides the SPI and powers down the device and returns all settings back to default. RESET is pulled to ground by default. A logic high triggers the reset.28SCLKSerial Clock.29CSChip Select Bar.30SDISerial Data Input.31SDOSerial Data Output.	25	AVDD	3.3 V Analog Supply.
27RESETReset Input. RESET overrides the SPI and powers down the device and returns all settings back to default. RESET is pulled to ground by default. A logic high triggers the reset.28SCLKSerial Clock.29CSChip Select Bar.30SDISerial Data Input.31SDOSerial Data Output.	26	VIO	Digital Level Select for SPI and RESET. This pin can accept 1.8 V to 3.3 V.
28SCLKSerial Clock.29CSChip Select Bar.30SDISerial Data Input.31SDOSerial Data Output.	27	RESET	Reset Input. RESET overrides the SPI and powers down the device and returns all settings back to default. RESET is pulled to ground by default. A logic high triggers the reset.
29 CS Chip Select Bar. 30 SDI Serial Data Input. 31 SDO Serial Data Output.	28	SCLK	Serial Clock.
30SDISerial Data Input.31SDOSerial Data Output.	29	CS	Chip Select Bar.
31 SDO Serial Data Output.	30	SDI	Serial Data Input.
	31	SDO	Serial Data Output.
32 AVDD 3.3 V Analog Supply.	32	AVDD	3.3 V Analog Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 3.3 V, LNA + PGA gain = 36 dB (LNA gain = 24 dB, PGA gain = 12 dB), $T_A = 25^{\circ}C$, $PGA_BIAS_SEL = b'10$, $LNA_BIAS_SEL = b'10$, $LNA_SEL = b'10$,











Figure 5. Distribution of Channel to Channel Gain Matching



Figure 6. Distribution of Channel to Channel Phase Matching



Figure 7. Total Harmonic Distortion (THD) vs. Frequency for Various Gains, $V_{OUT} = -10 \, dBm$



Figure 8. Input Impedance vs. Frequency

Data Sheet



Figure 9. Gain Step Transient Response





Figure 12. Frequency Response at All Gains (Bias Mode 0)





Data Sheet



Figure 15. Pulse Response at Various Output Capacitive Loads



Figure 16. Large Signal Pulse Response for Various LNA and PGA Bias Modes











Figure 20. Differential Output Voltage Swing vs. Output Load Resistance

ADA8282

Data Sheet



THEORY OF OPERATION RADAR RECEIVE PATH AFE

The primary application for the ADA8282 is a high speed ramp, frequency modulated, continuous wave radar (HSR-FMCW radar). Figure 25 shows a simplified block diagram of an HSR-FMCW radar system. The signal chain requires multiple channels, each including an LNA and a PGA. The ADA8282 provides these key components in a single 5 mm × 5 mm LFCSP.

The performance of each component is designed to meet the demands of an HSR-FMCW radar system. Some examples of these performance metrics are the LNA noise, PGA gain range, and signal chain bandwidth and power. The ADA8282 also has adjustable power modes to adjust the power and performance level to accommodate a wide variety of applications.

The ADA8282 is programmable via the SPI. Channel gain, power mode, and offset voltage can be adjusted using the SPI port.

DEFAULT SPI SETTINGS

When initially powered, the ADA8282 defaults to a setting of 0x00 in Register 0x17, which disables all channels. The device is enabled by writing 0x0F to Register 0x17.

INPUT IMPEDANCE

The input impedance to the ADA8282 is set by an internal 785 Ω resistance at each input, biased to midsupply by an internal voltage buffer. Both the positive and negative inputs are biased with the same network, creating a differential input impedance of 1.57 k Ω .

The input to the ADA8282 is typically ac-coupled. The ac coupling capacitors operate with the input impedance of the ADA8282 to create a high-pass filter with a pole at $1/(2\pi 2RC)$, where R = 785 Ω with a typical tolerance of ±15%.

POWER MODES

The ADA8282 has four power modes that can be controlled through Register 0x14 (BIAS_SEL). The power modes allow a user to adjust the power and performance tradeoffs to suit the end application. Use the low power mode when power savings are in demand, and use the high power mode in applications that require increased bandwidth and low noise.

Table 6 shows the power performance trade-offs of the various SPI settings.

Table 6.	Power	Mode	Trade-	Offs
----------	-------	------	--------	------

Mode Setting	Power per Channel (mW)	Input Referred Noise at 2 MHz (nV/√Hz)	Typical Bandwidth (MHz), Gain = 36 dB
b′00	18.3	4.5	20.5
b'01	26.5	3.8	34.2
b'10	34.8	3.6	42.3
b′11	54.8	3.4	52.3



Figure 25. Typical Signal Chain Overview

The ADA8282 has a programmable gain to allow adjusting of the output amplitudes of signals to accommodate a variety of applications. The gain of the ADA8282 is programmable in 6 dB increments from 18 dB to 36 dB. The gain is controlled using Register 0x15. The same register controls all four channels, but each channel can be independently controlled by utilizing the appropriate bits in the register. Channel A is controlled with the two LSBs of Register 0x15 (Bits[1:0]), Channel B uses Bits[3:2], Channel C uses Bits[5:4], and Channel D uses the two MSBs, Bits[7:6].

The gain setting and gains are listed in Table 7.

Table 7. Gain Settings

Register 0x15 Setting	Gain (dB)	Gain (V/V)
b'00	18	7.9
b'01	24	15.9
b'10	30	31.6
b'11	36	63.1

OUTPUT SWING VARIATION WITH GAIN

The ADA8282 gain is implemented using two internal gain stages. The first stage is an LNA with a gain of 24 dB, and the second stage is a PGA with a gain that varies from -6 dB to +12 dB. The output of the LNA has a fixed output swing range, and is the limiting factor when the channel gain is 18 dB. Because of the limitations of the LNA swing range, the ADA8282 has an output swing that is dependent on gain, as shown in Table 8.

Table 8. Output Swing at Various Gains

1 0	
Gain (dB)	Output Swing (V p-p)
18	3.1
24	6.3
30	6.3
36	6.3

OFFSET VOLTAGE ADJUSTMENTS

Register 0x10 through Register 0x13 adjust the dc offset voltage of each channel. The default value of 0x20 is intended to be the setting for the offset closest to 0 V, but adjustments can be made as required by the application.

The default setting (0x20) applies a zero offset, 0x00 applies the maximum negative offset, and 0x3F applies the maximum positive offset.

The range and resolution of the LNA_OFFSETx adjustments are dependent on the LNA bias mode as described in Table 9.

Table 9. Offset	Voltage	Adjustments
-----------------	---------	-------------

LNA_BIAS_SEL Setting	Referred to Input (RTI) Offset Resolution (μV)	RTI Offset Range (mV)						
b'00	113	±4						
b'01	186	±б						
b'10	250	±8						
b'11	440	±14						

VIO Pin

The VIO pin sets the voltage levels used by the SPI interface. If the VIO pin is tied to the 3.3 V supply, the SPI port functions on 3.3 V logic.

SINGLE-ENDED OR DIFFERENTIAL INPUT

The ADA8282 operates with either a differential or single-ended signal source. The maximum input voltage swing is the same in either configuration. When using a single-ended signal source, connect the unused input to ground with a capacitor. Matching the ac coupling capacitor to the ac grounding capacitor optimizes CMRR performance.

SHORT-CIRCUIT CURRENTS

The ADA8282 typically has a 205 mA short-circuit current per output pin. The thermal implications of this current during unintended shorting of these outputs must be taken into account when designing boards with this device.

SPI INTERFACE

The ADA8282 SPI interface uses a 4-wire interface to deliver a 16-bit instruction header, followed by 8 bits of data. The first bit is a read/write bit. W1 and W0 determine how many bytes are transferred, and must both be zeros for the ADA8282 to write to a single register. Then, a 13-bit address and an 8-bit data byte follow.

The SPI port operates at SCLK frequencies of up to 10 MHz. For additional SPI timing information, see the AN-877 Application Note.



CHANNEL TO CHANNEL PHASE MATCHING

In a multichannel radar application, matching the ac performance between channels improves the distance and angle resolution of a detected object, particularly the phase matching in the band of interest for the application. The ADA8282 layout and design are optimized to increase phase matching. The ADA8282 also has sufficient bandwidth to minimize any channel to channel phase variation for up to 5 MHz input signals.

The phase mismatch between channels can be calibrated at a single temperature. However, any variation in phase matching over temperature can still degrade system performance. The ADA8282 is characterized to capture the maximum channel to channel phase mismatch as the temperature varies from a calibration temperature of 25°C.

Figure 27 shows a distribution of channel to channel phase mismatch for signal frequencies up to 5 MHz. When the initial phase mismatch between channels is normalized to 0° at +25°C, the 6σ mismatch is 0.43° at -40°C and 0.6° at +125°C.



Igure 27. Channel to Channel Phase Mismatch, Normalized to 0° at 25°C LNA_BIAS_SEL = PGA_BIAS_SEL = b'00, PGA_GAIN = b'11

The amount of channel to channel phase mismatch varies with the power mode. Table 10 shows the 6σ phase mismatch up to 5 MHz over the full temperature range for all gain settings in different power modes, when normalized to 0° at 25°C in each power mode.

Table 10. Maximum Channel to Channel Phase Mismatch over Temperature After 25°C Calibration

PGA_BIAS_SEL	LNA_BIAS_SEL	6σ Channel to Channel Phase Mismatch over Temperature (Degrees)	Maximum Channel to Channel Phase Mismatch (Degrees)
b'00	b'00	0.60	±1
b'01	b'01	0.41	±1
b'10	b'10	0.33	±1
b'11	b'11	0.60	±1

APPLICATIONS INFORMATION

INCREASED GAIN USING TWO ADA8282 DEVICES IN SERIES

For applications that require gains greater than 36 dB, two ADA8282 devices can be used in series with each other. To optimize the signal swing for the path, increment the gains according to Table 11.

Total Gain (dB)	A1 (Input Side ADA8282) Gain (dB)	A2 (Output Side ADA8282) Gain (dB)
36	18	18
42	18	24
48	24	24
54	30	24
60	30	30
66	36	30
72	36	36



Table 11. Gain Settings for Two Devices in Series

MULTIPLEXING INPUTS USING MULTIPLE ADA8282 DEVICES

It is possible to multiplex eight differential inputs down to four differential outputs by using two ADA8282 devices. The devices can be connected such that the outputs are connected (see

Figure 29) as long as only one device is enabled at a time. When an ADA8282 is disabled, the outputs present a 6 k Ω load on the output bus.



Figure 29. Multiplexing by Connecting Two ADA8282 Outputs to One Output Bus

BASIC CONNECTIONS FOR A TYPICAL APPLICATION

The ADA8282 is typically configured to operate with a nominal 3.3 V power supply, using the EPAD as the analog ground connection. Place the bypass capacitors as close as possible to the power supply pins to minimize the length of metal traces in

series with the bypassing paths. AC couple the inputs and outputs for each channel as shown in Figure 30. Pull the RESET pin low with a 10 k Ω resistor and drive it with 3.3 V GPIO logic. The SPI pins can be directly connected to the SPI bus.



Figure 30. Typical Component Connections

REGISTER MAP

REGISTER SUMMARY

Table 12. Register Summary

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	INTF_CONFA	[7:0]	INTF_C	ONFA2	LSBFIRST1	_SBFIRST1 INTF_CONFA1 LSBFIRST0 INTF_CONFA0				0x00	RW	
0x01	SOFT_RESET	[7:0]				Unuse	d			SOFT_RESET	0x00	R
0x04	CHIP_ID1	[7:0]				C	HIP_IDLOW				0x82	R
0x05	CHIP_ID2	[7:0]		CHIP_IDHI						0x82	R	
0x06	Revision	[7:0]		Revision						0x00	R	
0x10	LNA_OFFSET0	[7:0]	Սու	ised			LN	A_OFFSET0			0x20	RW
0x11	LNA_OFFSET1	[7:0]	Unu	ised			LN	A_OFFSET1			0x20	RW
0x12	LNA_OFFSET2	[7:0]	Unu	ised			LN	A_OFFSET2			0x20	RW
0x13	LNA_OFFSET3	[7:0]	Unu	ised			LN	A_OFFSET3			0x20	RW
0x14	BIAS_SEL	[7:0]		Un	nused		PGA_E	BIAS_SEL	LNA_E	BIAS_SEL	0x0A	RW
0x15	PGA_GAIN	[7:0]	PGA_	GAIN3	PGA_	GAIN2	PGA_	GAIN1	PGA_	_GAIN0	0x00	RW
0x17	EN_CHAN	[7:0]		Unused EN_			EN_ CHANNEL0	0x00	RW			
0x18	EN_BIAS_GEN	[7:0]				Unuse	d			EN_BIAS_GEN	0x00	RW
0x1D	SPAREWRO	[7:0]		Unused GPIO_WRITE GPIO_WR_ MODE				GPIO_WR_ MODE	0x00	RW		
0x1E	SPARERD0	[7:0]				Unuse	d			GPIO_READ	0x00	R

REGISTER DETAILS

Register 0x00: Interface Configuration Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTF_CONFA2		LSBFIRST1	INTF_C	ONFA1	LSBFIRSTO	INTF_0	CONFA0

The INTF_CONFA configuration register is symmetric, as it is the first register written and sets the data direction (LSB first or MSB first).

Table 13. INTF_CONFA Configuration Register Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	INTF_CONFA2	INTF_CONFA2 must remain b'00.	0x00	RW
5	LSBFIRST1	LSBFIRST1 must be set to b'1 for LSB first operation and to b'0 for MSB first operation.	0x00	RW
[4:3]	INTF_CONFA1	INTF_CONFA1 must remain b'00.	0x00	RW
2	LSBFIRST0	LSBFIRST0 must be set to b'1 for LSB first operation and to b'0 for MSB first operation.	0x00	RW
[1:0]	INTF_CONFA0	INTF_CONFA0 must remain b'00.	0x00	RW

Register 0x01: Soft Reset Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Unused							SOFT_RESET	

Table 14. SOFT_RESET Configuration Register Bit Descriptions

Bits	Bit Name	Description	Reset	Access
0	SOFT_RESET	The SOFT_RESET bit resets all registers to their default values when SOFT_RESET is set to b'1.	0x00	RW

Register 0x04: Chip ID Low Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
	CHIP IDLOW								

Table 15. CHIP_IDLOW Configuration Register Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	CHIP_IDLOW	The CHIP_ID1 and CHIP_ID2 registers identify the ADA8282.	0x82	R

Register 0x05: Chip ID High Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				CHIP_IDHI			

Table 16. CHIP_IDHI Configuration Register Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	CHIP_IDHI	The CHIP_ID1 and CHIP_ID2 registers identify the ADA8282.	0x82	R

Register 0x06: Revision Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Revision							

Table 17. Revision Configuration Register Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:0]	Revision	The revision register identifies the silicon revision of the current die.	0x00	R

Register 0x10: LNA Offset 0 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unu	sed			LN	NA_OFFSET0		

Table 18. LNA_OFFSET0 Configuration Register Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[5:0]	LNA_OFFSET0	LNA_OFFSET0 controls the offset of Channel A. The default setting (0x20) applies the minimum offset, 0x00 applies the maximum negative offset, and 0x3F applies the maximum positive offset.	0x20	RW
		The resolution of the offset varies with the LNA bias mode as follows:		
		LNA Bias Mode 0: 113 μ V RTI offset resolution, ±4 mV range.		
		LNA Bias Mode 1: 186 μ V RTI offset resolution, ±6 mV range.		
		LNA Bias Mode 2: 250 μ V RTI offset resolution, ±8 mV range.		
		LNA Bias Mode 3: 440 μ V RTI offset resolution, ±14 mV range.		

Register 0x11: LNA Offset 1 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unu	sed			LN	IA_OFFSET1		

Table 19. LNA_OFFSET1 Configuration Register Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[5:0]	LNA_OFFSET1	LNA_OFFSET0 controls the offset of Channel B. The default setting (0x20) applies the minimum offset, 0x00 applies the maximum negative offset, and 0x3F applies the maximum positive offset.	0x20	RW
		The resolution of the offset varies with the LNA bias mode as follows:		
		LNA Bias Mode 0: 113 μ V RTI offset resolution, ±4 mV range.		
		LNA Bias Mode 1: 186 μ V RTI offset resolution, ±6 mV range.		
		LNA Bias Mode 2: 250 μ V RTI offset resolution, ±8 mV range.		
		LNA Bias Mode 3: 440 μ V RTI offset resolution, ±14 mV range.		

Register 0x12: LNA Offset 2 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unu	sed			LN	IA_OFFSET2		

Bits	Bit Name	Description	Reset	Access
[5:0]	LNA_OFFSET2	LNA_OFFSET0 controls the offset of Channel C. The default setting (0x20) applies the minimum offset 0x00 applies the maximum negative offset	0x20	RW
		The resolution of the offset varies with the LNA bias mode as follows:		
		LNA Bias Mode 0: 113 μ V RTI offset resolution, ±4 mV range.		
		LNA Bias Mode 1: 186 μ V RTI offset resolution, ±6 mV range.		
		LNA Bias Mode 2: 250 μ V RTI offset resolution, ±8 mV range.		
		LNA Bias Mode 3: 440 μ V RTI offset resolution, ±14 mV range.		

Table 20. LNA_OFFSET2 Configuration Register Bit Descriptions

Register 0x13: LNA Offset 3 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unu	sed			LN	IA_OFFSET3		

Table 21. LNA_OFFSET3 Configuration Register Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[5:0]	LNA_OFFSET3	LNA_OFFSET0 controls the offset of Channel D. The default setting (0x20) applies the minimum offset, 0x00 applies the maximum negative offset, and 0x3F applies the maximum positive offset.	0x20	RW
		The resolution of the offset varies with the LNA bias mode as follows:		
		LNA Bias Mode 0: 113 μ V RTI offset resolution, ±4 mV range.		
		LNA Bias Mode 1: 186 μ V RTI offset resolution, ±6 mV range.		
		LNA Bias Mode 2: 250 μ V RTI offset resolution, ±8 mV range.		
		LNA Bias Mode 3: 440 μ V RTI offset resolution, ±14 mV range.		

Register 0x14: PGA Bias Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused			PGA_B	IAS_SEL	LNA_B	BIAS_SEL	

The PGA bias select register allows the user to trade off power and performance (for example, bandwidth and noise).

Table 22. BIAS_SEL Configuration Register Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[3:2]	PGA_BIAS_SEL	Set PGA_BIAS_SEL to b'00 for the minimum PGA bias and to b'11 for the maximum PGA bias.	0x00	RW
[1:0]	LNA_BIAS_SEL	Set LNA_BIAS_SEL to b'00 for the minimum LNA bias and to b'11 for the maximum LNA bias.	0x00	RW

Register 0x15: PGA Gain Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PGA_C	GAIN3	PGA_0	GAIN2	PGA_	GAIN1	PGA_	_GAIN0

The PGA gain register allows independent gain settings for each channel.

Table 23. PGA_GAIN Configuration Register Bit Descriptions

Bits	Bit Name	Description	Reset	Access
[7:6]	PGA_GAIN3	Set PGA_GAIN3 to b'00 for 18 dB gain, to b'01 for 24 dB gain, to b'10 for 30 dB gain, and to b'11 for 36 dB gain for Channel D	0x00	RW
[5:4]	PGA_GAIN2	Set PGA_GAIN2 to b'00 for 18 dB gain, to b'01 for 24 dB gain, to b'10 for 30 dB gain, and to b'11 for 36 dB gain for Channel C	0x00	RW
[3:2]	PGA_GAIN1	Set PGA_GAIN1 to b'00 for 18 dB gain, to b'01 for 24 dB gain, to b'10 for 30 dB gain, and to b'11 for 36 dB gain for Channel B	0x00	RW
[1:0]	PGA_GAIN0	Set PGA_GAIN0 to b'00 for 18 dB gain, to b'01 for 24 dB gain, to b'10 for 30 dB gain, and to b'11 for 36 dB gain for Channel A	0x00	RW

Register 0x17: Enable Channel Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused			EN_CHANNEL3	EN_CHANNEL2	EN_CHANNEL1	EN_CHANNEL0	

The enable channel register allows individual channels to be enabled or disabled. The default mode for the channel is disabled. Write 0x0F to the EN_CHAN register to enable all channels.

When a channel is disabled but the bias generator is still enabled, the channel's current consumption is $<100 \mu$ A. When a channel is disabled, its output pins are high-Z. The enable channel register resets at AVDD power-on to 0x00 to avoid inrush current for fast supply ramps.

Table 24. EN_CHAN Register Bit Descriptions

Bits	Bit Name	Description	Reset	Access
3	EN_CHANNEL3	Set to b'1 to enable Channel D, and set to b'0 to disable Channel D	0x00	RW
2	EN_CHANNEL2	Set to b'1 to enable Channel C, and set to b'0 to disable Channel C	0x00	RW
1	EN_CHANNEL1	Set to b'1 to enable Channel B, and set to b'0 to disable Channel B	0x00	RW
0	EN_CHANNEL0	Set to b'1 to enable Channel A, and set to b'0 to disable Channel A	0x00	RW

Register 0x18: Enable Bias Generator Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			Unused				EN_BIAS_GEN

When any channel is enabled, the bias generator is automatically enabled. The EN_BIAS_GEN register controls whether the bias generator stays active, even when all channels are disabled. Leaving the bias generator active decreases the enable time of the device.

Table 25. EN_BIAS_GEN Register Bit Descriptions

Bits	Bit Name	Description	Reset	Access
0	EN_BIAS_GEN	Setting EN_BIAS_GEN to 1 keeps the bias generator active, providing a faster enable time (~2 μ s).	0x00	RW

Register 0x1D: GPIO Write Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		L	Inused			GPIO_WRITE	GPIO_WR_MODE

The GPIO_WR_MODE bit reconfigures the SDO pin to a general-purpose input/output (GPIO) port that can be written by the GPIO_WRITE register or read by the GPIO_READ register.

Table 26. SPAREWR0 Configuration Register Bit Descriptions

Bits	Bit Name	Description	Reset	Access
1	GPIO_WRITE	Data bit is put onto the SDO pin when GPIO write mode is active.	0x00	RW
0	GPIO_WR_MODE	Write b'1 to this register to activate GPIO write mode.	0x00	RW

Register 0x1E: GPIO Read Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			Unused				GPIO_READ

Table 27. SPARERD0 Configuration Register Bit Descriptions

Bits	Bit Name	Description	Reset	Access
0	GPIO_READ	This register reflects the logic level placed on SDO when a b'0 is written to GPIO_WR_MODE.	0x00	R

OUTLINE DIMENSIONS



(CP-32-11) Dimensions shown in millimeters

ORDERING GUIDE

Model ^{1, 2}	Temperature Range	Package Description	Package Option
ADA8282WBCPZ-R7	-40°C to +125°C	32-Lead LFCSP_WQ, 7" Tape and Reel	CP-32-11
ADA8282WBCPZ	-40°C to +125°C	32-Lead LFCSP_WQ	CP-32-11
ADA8282CP-EBZ		Evaluation Board	

¹ Z = RoHS Compliant Part.

 2 W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADA8282W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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Телефон: 8 (812) 309-75-97 (многоканальный) Факс: 8 (812) 320-03-32 Электронная почта: ocean@oceanchips.ru Web: http://oceanchips.ru/ Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А