

NB3N3002

3.3V, Crystal-to-HCSL Clock Generator

Description

The NB3N3002 is a high precision, low phase noise clock generator that supports PCI-Express and Ethernet requirements. The device takes a 25 MHz fundamental mode parallel resonant crystal and generates differential HCSL output at 25 MHz, 100 MHz, 125 MHz or 200 MHz clock frequencies. Outputs can interface with LVDS with proper termination (See Figure 5).

This device is housed in 5.0 mm x 4.4 mm narrow body TSSOP 16 pin package.

Features

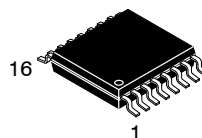
- Uses 25 MHz Fundamental Mode Parallel Resonant Crystal
- External Loop Filter is Not Required
- HCSL Differential Output or LVDS with Proper Termination
- Typical TIE RMS jitter of 2.5 ps
- Jitter or Low Phase Noise:

| Offset | Noise Power |
|---------|-------------|
| 100 Hz | -103 dBc |
| 1 kHz | -118 dBc |
| 10 kHz | -122 dBc |
| 100 kHz | -130 dBc |
| 1 MHz | -132 dBc |
| 10 MHz | -149 dBc |
- Operating Range 3.3 V $\pm 5\%$
- Industrial Temperature Range -40°C to $+85^{\circ}\text{C}$
- These are Pb-Free Devices



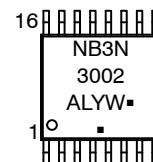
ON Semiconductor®

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TSSOP-16
DT SUFFIX
CASE 948F

MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

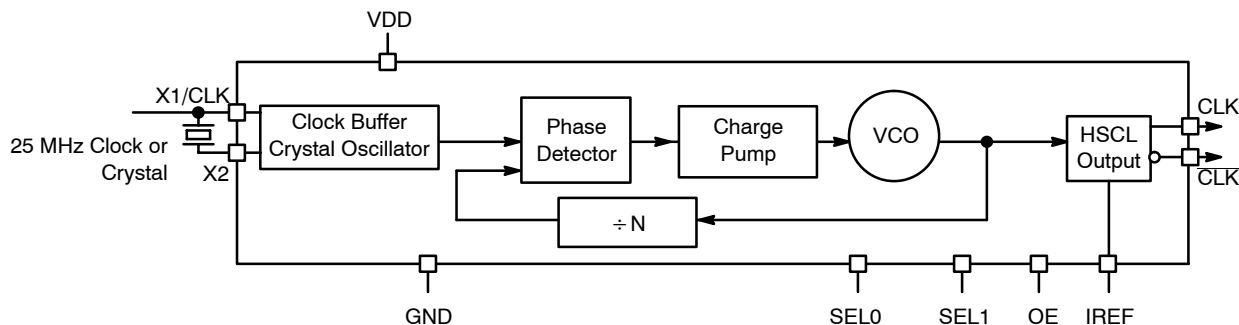


Figure 1. NB3N3002 Simplified Logic Diagram

NB3N3002

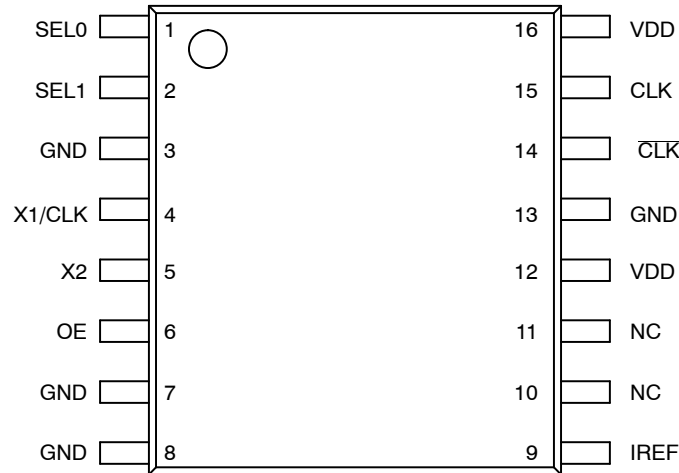


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

| Pin | Symbol | I/O | Description |
|-------------|-------------------------|---------------------|---|
| 1 | Sel0 | Input | LVTTL/LVCMOS frequency select input 0. Internal pullup resistor to V_{DD} . See output select table 2 for details. |
| 2 | Sel1 | Input | LVTTL/LVCMOS frequency select input 1. Internal pullup resistor to V_{DD} . See output select Table 2 for details. |
| 12, 16 | V_{DD} | Power Supply | Positive supply voltage pins are connected to +3.3 V supply voltage. |
| 4 | X1/CLK | Input | Crystal or Clock input. Connect to 25 MHz crystal source or single-ended clock. |
| 5 | X2 | Input | Crystal input. Connect to a 25 MHz crystal or leave unconnected for clock input. |
| 6 | OE | Input | Output enable tri-states output when connected to GND. Internal pullup resistor to V_{DD} . |
| 3, 7, 8, 13 | GND | Power Supply | Ground 0 V. These pins provide GND return path for the devices. |
| 9 | I_{REF} | Output | Output current reference pin. Precision resistor (typ. 475 Ω) is connected from pin 9 to GND to set the output current. |
| 15 | CLK | HCSL or LVDS Output | Noninverted clock output. (For LVDS levels see Figure 5) |
| 14 | $\overline{\text{CLK}}$ | HCSL or LVDS Output | Inverted clock output. (For LVDS levels see Figure 5) |
| 10,11 | NC | | Do not connect |

Table 2. OUTPUT FREQUENCY SELECT TABLE

| Sel1 | Sel0 | f_{CLKout} (MHz) |
|------|------|--------------------|
| L | L | 25 |
| L | H | 100 |
| H | L | 125 |
| H | H | 200 |

Recommended Crystal Parameters

| | |
|------------------------------|--------------------|
| Crystal | Fundamental AT-Cut |
| Frequency | 25 MHz |
| Load Capacitance | 16–20 pF |
| Shunt Capacitance, C_0 | 7 pF Max |
| Equivalent Series Resistance | 35 Ω Max |
| Initial Accuracy at 25 °C | ± 20 ppm |
| Temperature Stability | ± 30 ppm |
| Aging | ± 20 ppm |
| C_0/C_1 Ratio | 250 Max |

NB3N3002

Table 3. ATTRIBUTES

| Characteristic | Value |
|--|----------------------|
| ESD Protection Human Body Model | > 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1) | Level 1 |
| Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | 7623 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 2)

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|------------------|--|--------------------|--|----------------------------------|--------------|
| V _{DD} | Positive Power Supply | GND = 0 V | | 4.6 | V |
| V _I | Input Voltage (V _{IN}) | GND = 0 V | GND ≤ V _I ≤ V _{DD} | -0.5 V to V _{DD} +0.5 V | V |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | TSSOP-16 TSSOP-16 | 138 108 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | (Note 3) | TSSOP-16 | 33 to 36 | °C/W |
| T _{sol} | Wave Solder | | | 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 5. DC CHARACTERISTICS (V_{DD} = 3.3 V ±5%, GND = 0 V, T_A = -40°C to +85°C)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---------------------|---|-----------------------|-----|-----------------------|------|
| I _{DD} | Power Supply Current (Note 4) | 65 | | 95 | mA |
| I _{DDOE} | Power Supply Current when OE is Set Low | 35 | | 65 | mA |
| V _{IH} | Input HIGH Voltage (X1/CLK, Sel0, Sel1, and OE) | 0.7 * V _{DD} | | V _{DD} + 300 | mV |
| V _{IL} | Input LOW Voltage (X1/CLK, Sel0, Sel1, and OE) | GND - 300 | | 0.3 * V _{DD} | mV |
| V _{OH} | Output HIGH Voltage (See Figure 4) | 660 | 700 | 850 | mV |
| V _{OL} | Output LOW Voltage (See Figure 4) | -150 | 0 | 150 | mV |
| V _{cross} | Crossing Voltage Magnitude (Absolute) | 250 | | 400 | mV |
| ΔV _{cross} | Change in Magnitude of V _{cross} | | | 150 | mV |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. NB3N circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
5. Measurement taken with outputs terminated with R_S = 33.2 Ω, R_L = 49.9 Ω, with load capacitance of 2 pF and current biasing resistor, R_{REF} from I_{REF} (Pin 9) to GND of 475 Ω. See Figure 3.

NB3N3002

Table 6. Table 5. AC CHARACTERISTICS ($V_{DD} = 3.3\text{ V} \pm 5\%$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; Note 7)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|-------------------|--|-----|------|-----|---------------|
| f_{CLKIN} | Clock/Crystal Input Frequency | | 25 | | MHz |
| f_{CLKOUT} | Output Clock Frequency | 25 | | 200 | MHz |
| Ω_{NOISE} | Phase-Noise Performance | | | | dBc/Hz |
| | $f_{CLKout} = 200\text{ MHz}$ | | | | |
| | @ 100 Hz offset from carrier | | -103 | | |
| | @ 1 kHz offset from carrier | | -118 | | |
| | @ 10 kHz offset from carrier | | -122 | | |
| | @ 100 kHz offset from carrier | | -130 | | |
| Tjitter (TIE) | TIE RMS Jitter (Note 8) | | 2.5 | | ps |
| | $f_{CLKout} = 200\text{ MHz}$ | | | | |
| | Cycle-to-Cycle RMS Jitter (Note 9) | | 2 | 5 | |
| | $f_{CLKout} = 200\text{ MHz}$ | | | | |
| | Cycle-to-Cycle Peak to Peak Jitter (Note 9) | | 20 | 35 | |
| OE | Output Enable/Disable Time | | | 1.0 | μs |
| | $f_{CLKout} = 200\text{ MHz}$ | | | | |
| t_{DUTY_CYCLE} | Output Clock Duty Cycle (Measured at cross point) | 45 | 50 | 55 | % |
| t_R | Output Risetime (Measured from 175 mV to 525 mV, Figure 4) | 175 | 340 | 700 | ps |
| t_F | Output Falltime (Measured from 525 mV to 175 mV, Figure 4) | 175 | 340 | 700 | ps |
| Δt_R | Output Risetime Variation (Single-Ended) | | | 125 | ps |
| Δt_F | Output Falltime Variation (Single-Ended) | | | 125 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. NB3N circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.
7. Measurement taken from differential output on single-ended channel terminated with $R_S = 33.2\ \Omega$, $R_L = 49.9\ \Omega$, with load capacitance of 2 pF and current biasing resistor, R_{REF} from I_{REF} (Pin 9) to GND of 475 Ω . See Figures 3 and 4.
8. Sampled with 20000 cycles to capture jitter component down to 100 kHz.
9. Sampled with 20000 cycles.

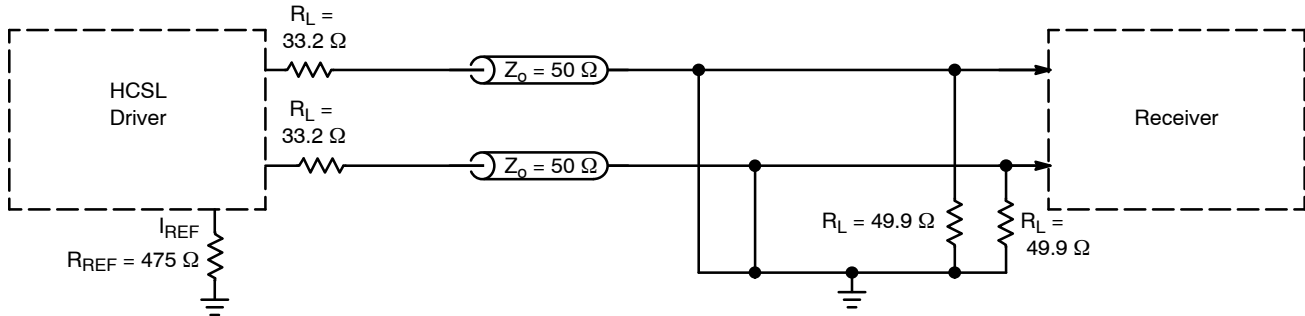


Figure 3. Typical Termination for Output Driver and Device Evaluation

NB3N3002

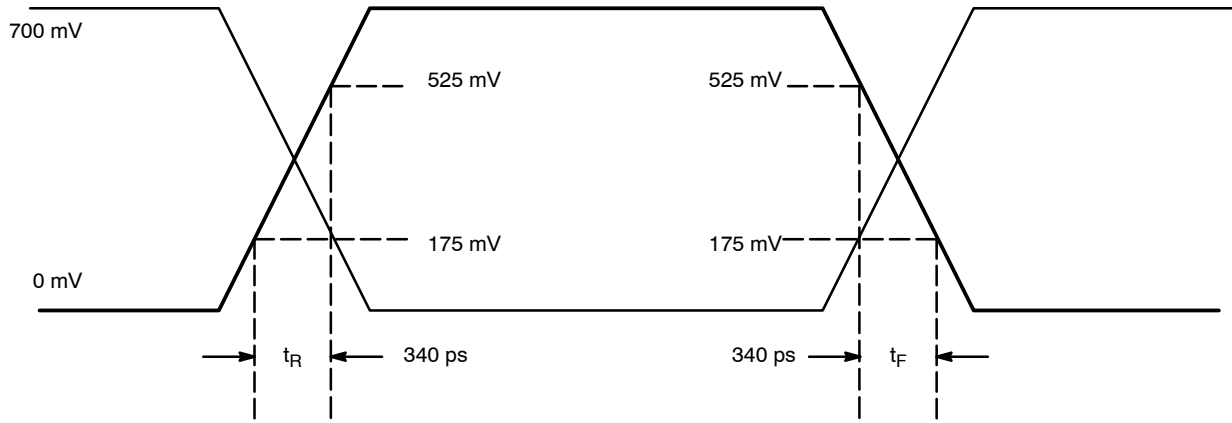


Figure 4. HCSL Output Parameter Characteristics

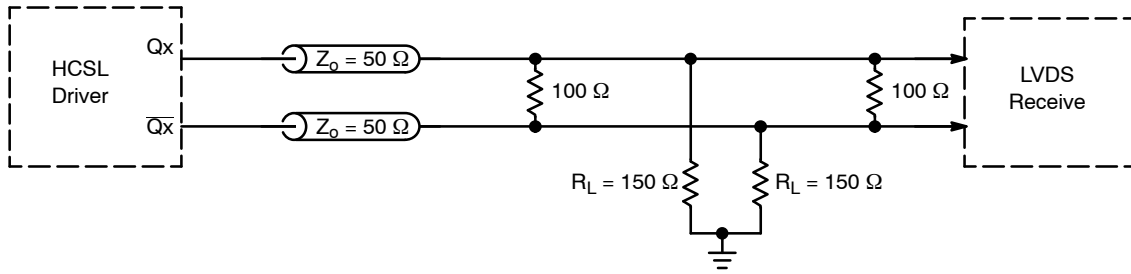


Figure 5. HCSL Interface Termination to LVDS

ORDERING INFORMATION

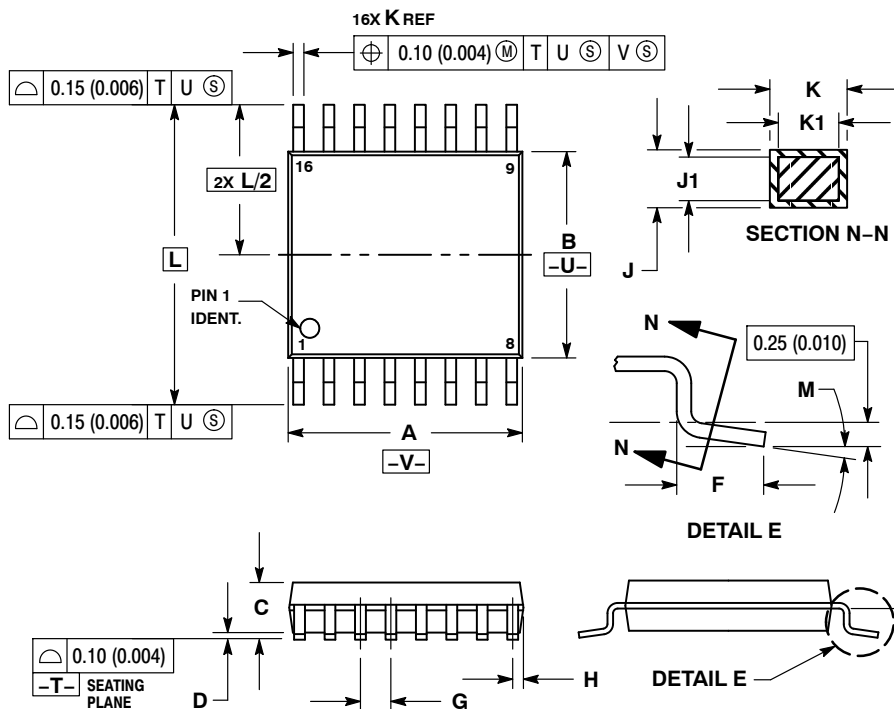
| Device | Package | Shipping† |
|---------------|-----------------------|--------------------|
| NB3N3002DTG | TSSOP-16 (Pb-Free) | 96 Units / Rail |
| NB3N3002DTR2G | TSSOP-16 (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB3N3002

PACKAGE DIMENSIONS

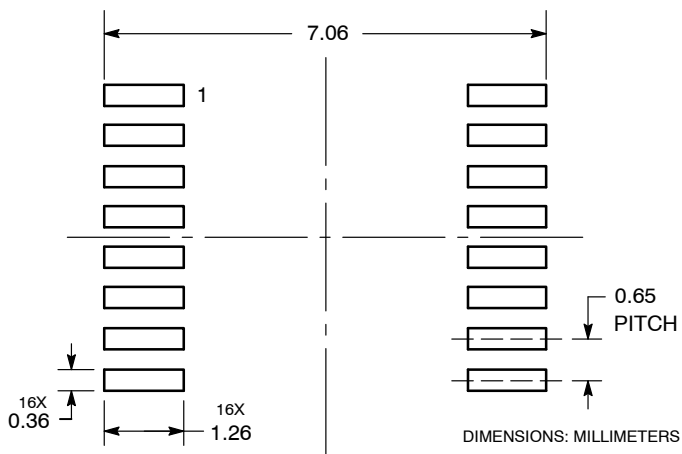
TSSOP-16
CASE 948F-01
ISSUE B




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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Телефон: 8 (812) 309-75-97 (многоканальный)

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Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А