

N-channel 60 V, 21 mΩ typ., 7 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 2x2 package

Datasheet - production data

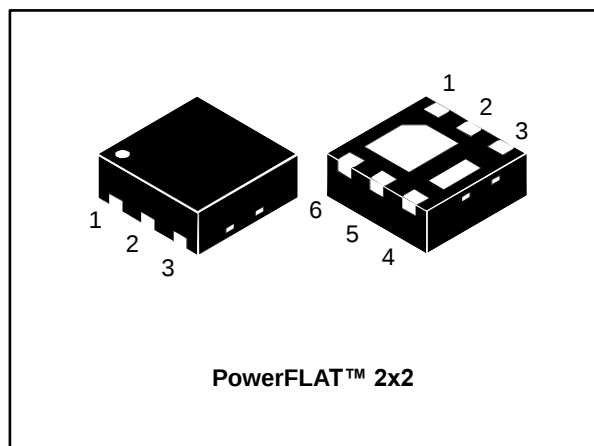


Figure 1: Internal schematic diagram

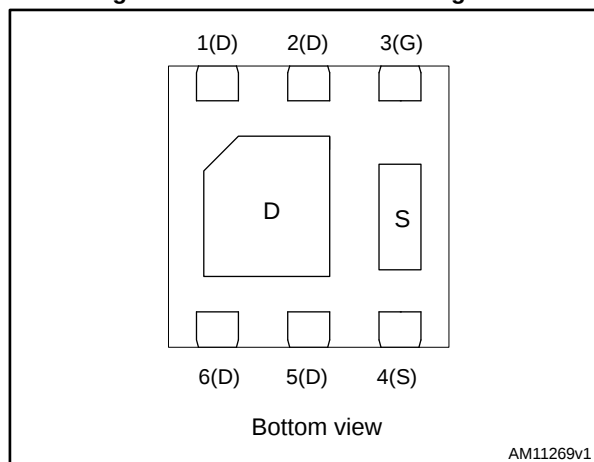


Table 1: Device summary

Order code	Marking	Package	Packing
STL7N6F7	ST7N	PowerFLAT™ 2x2	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STL7N6F7	60 V	25 mΩ	7 A

- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	7	A
I_D	Drain current (continuous) at $T_{pcb} = 100\text{ }^{\circ}\text{C}$	4.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	28	A
P_{TOT}	Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	2.4	W
T_J	Operating junction temperature range	-55 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		

Notes:

⁽¹⁾Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	52	$^{\circ}\text{C/W}$

Notes:

⁽¹⁾When mounted on FR-4 board of 1 inch², 2oz Cu, $t < 10\text{ s}$.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	60			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 60 V			1	μA
I _{GSS}	Gate-body leakage current	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 3.5A		21	25	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 30 V, f = 1 MHz, V _{GS} = 0 V	-	420	-	pF
C _{oss}	Output capacitance		-	215	-	pF
C _{rss}	Reverse transfer capacitance		-	16	-	pF
Q _g	Total gate charge	V _{DD} = 30 V, I _D = 7 A V _{GS} = 0 to 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	8	-	nC
Q _{gs}	Gate-source charge		-	2.3	-	nC
Q _{gd}	Gate-drain charge		-	2.1	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 30 V, I _D = 3.5A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	7.85	-	ns
t _r	Rise time		-	3.25	-	ns
t _{d(off)}	Turn-off delay time		-	12.1	-	ns
t _f	Fall time		-	3.95	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 7\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_D = 7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 48\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	17.1		ns
Q_{rr}	Reverse recovery charge		-	6.67		nC
I_{RRM}	Reverse recovery current		-	0.8		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

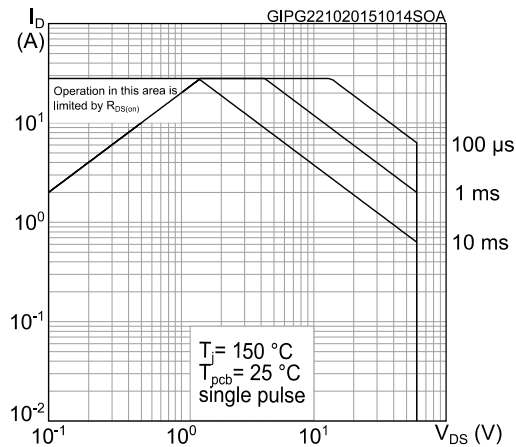


Figure 3: Thermal impedance

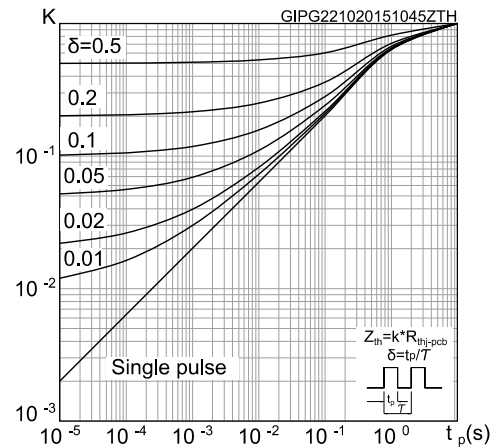


Figure 4: Output characteristics

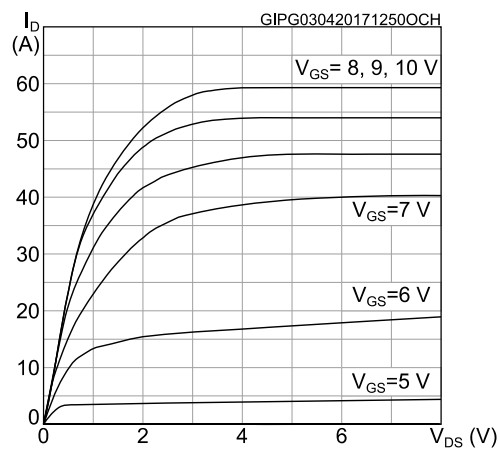


Figure 5: Transfer characteristics

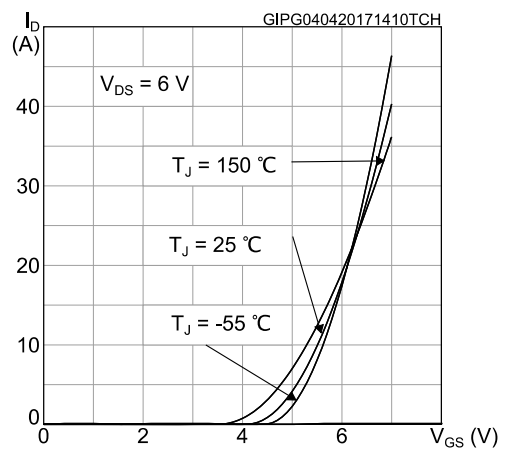


Figure 6: Gate charge vs gate-source voltage

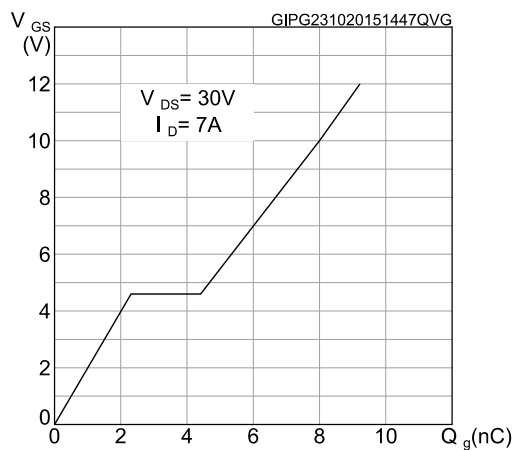


Figure 7: Static drain-source on-resistance

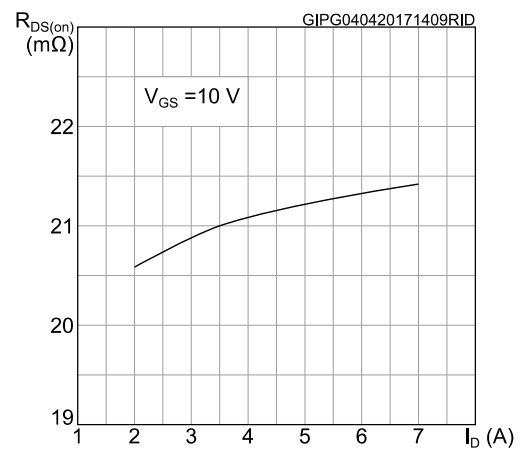


Figure 8: Capacitance variations

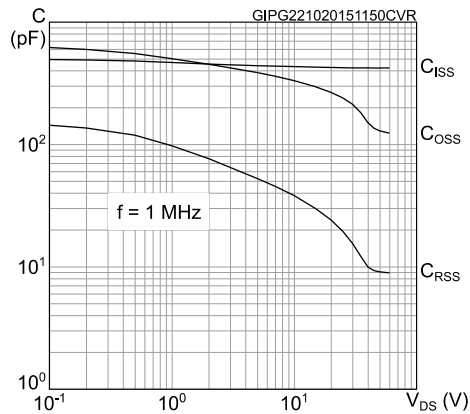


Figure 9: Normalized gate threshold voltage vs temperature

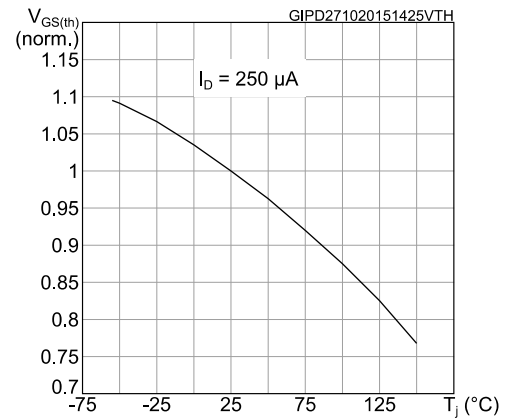


Figure 10: Normalized on-resistance vs temperature

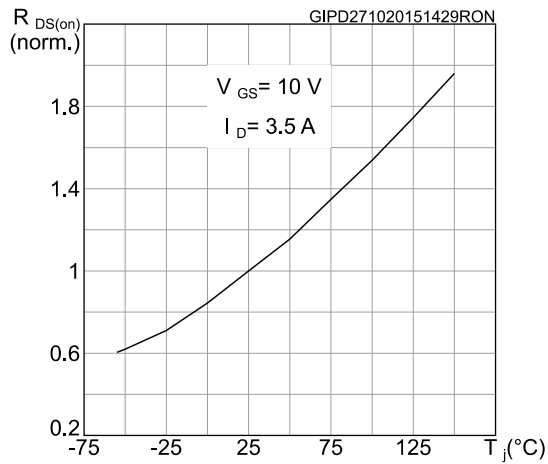
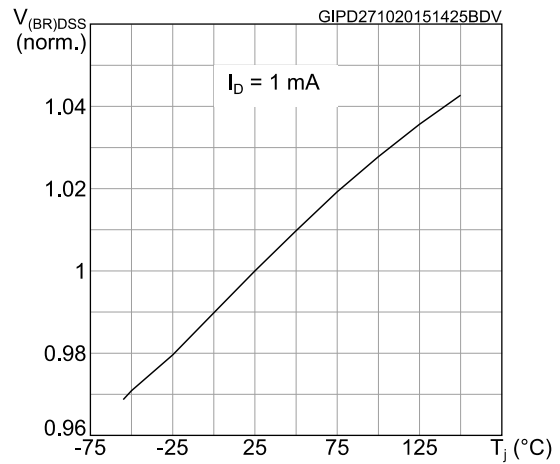
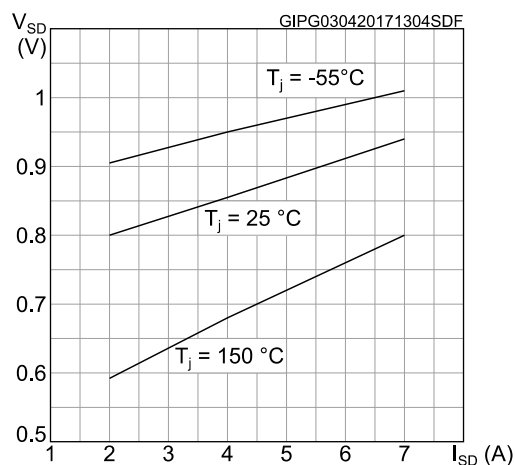
Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

Figure 12: Source-drain diode forward characteristics



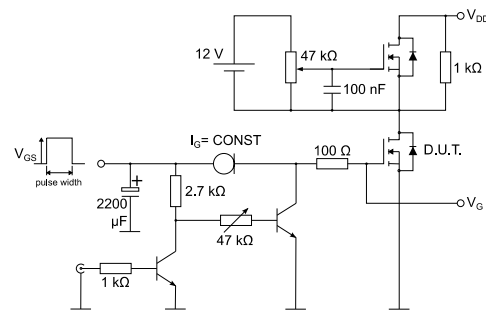
3 Test circuits

Figure 13: Test circuit for resistive load switching times



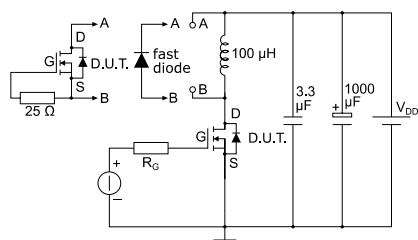
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Figure 14: Test circuit for gate charge behavior



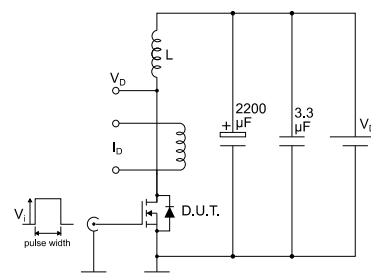
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Figure 15: Test circuit for inductive load switching and diode recovery times



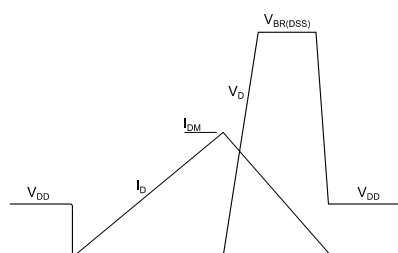
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Figure 16: Unclamped inductive load test circuit



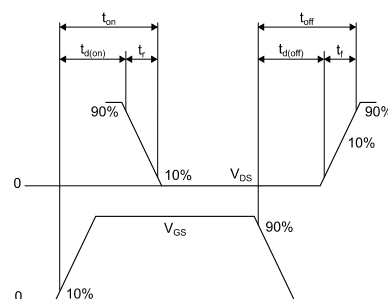
AM01471v1

Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 PowerFLAT 2x2 package information

Figure 19: PowerFLAT™ 2x2 package outline

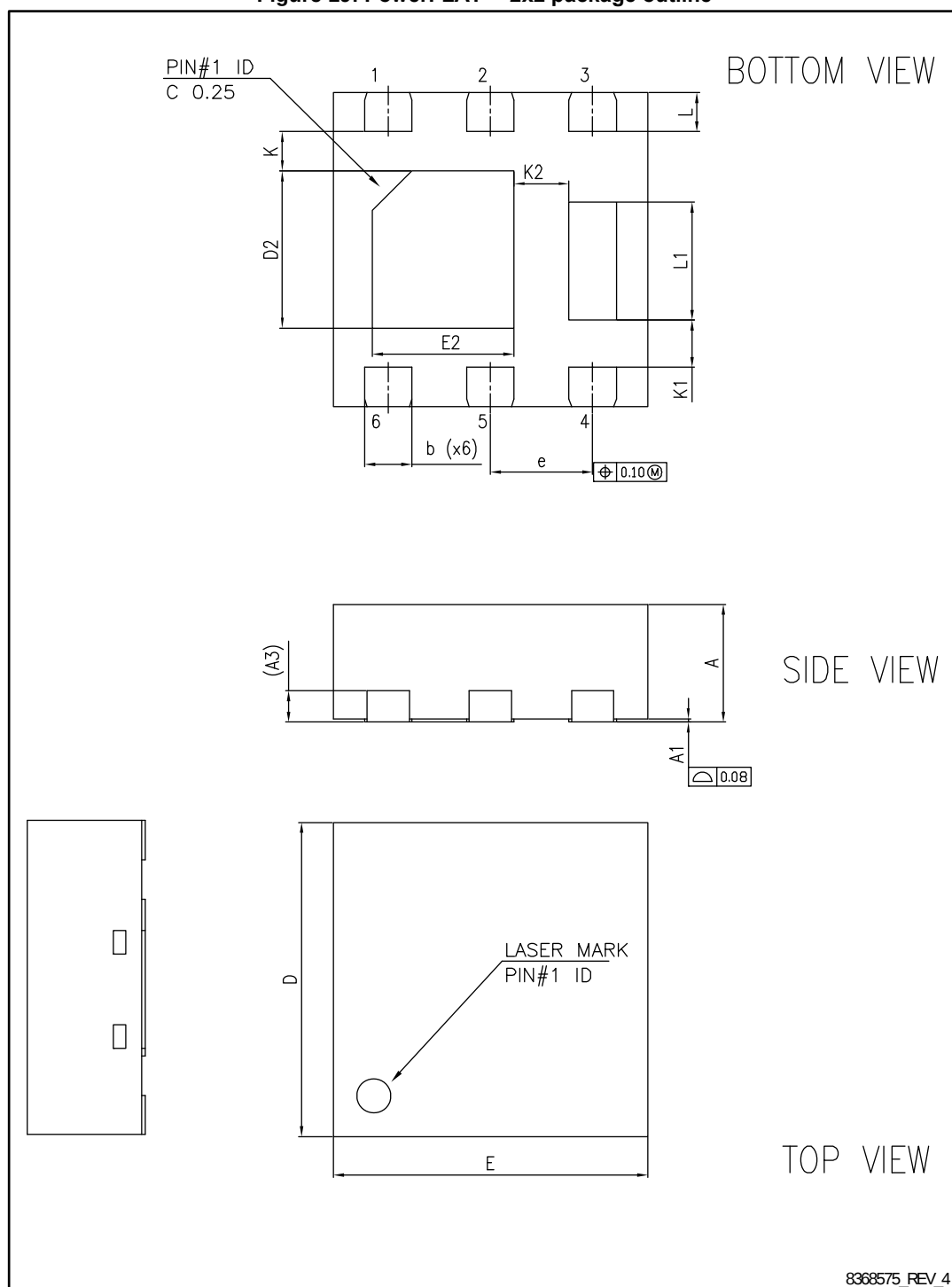
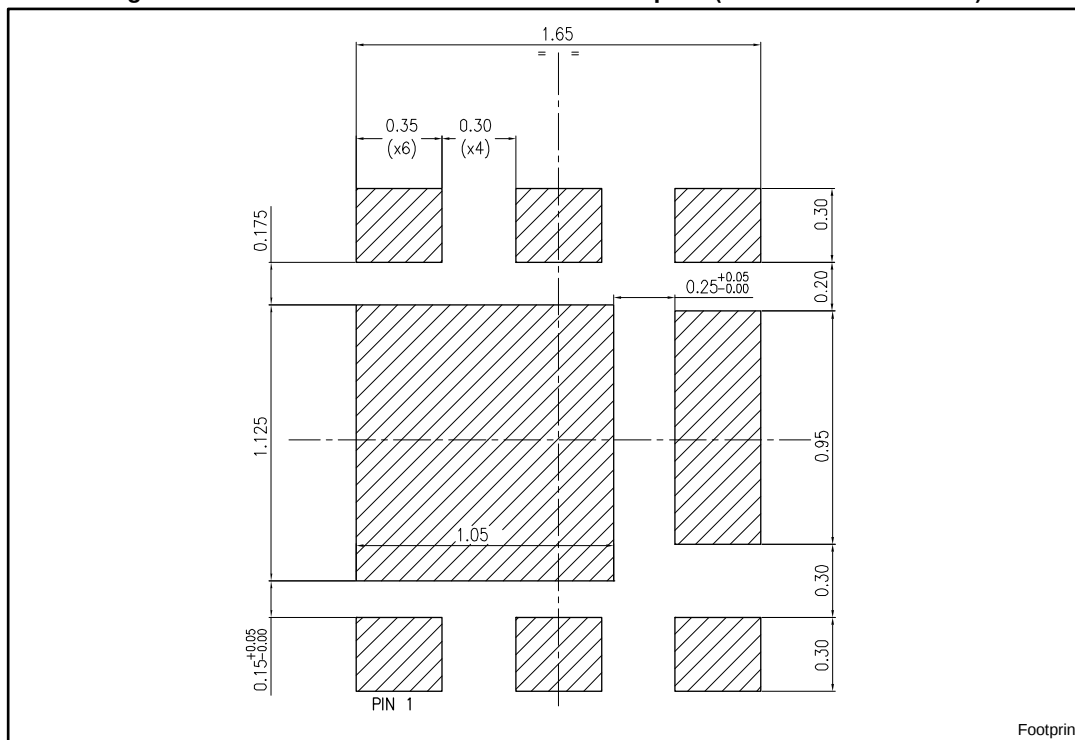


Table 8: PowerFLAT™ 2x2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	0.80	0.90	1.00
e	0.55	0.65	0.75
K	0.15	0.25	0.35
K1	0.20	0.30	0.40
K2	0.25	0.35	0.45
L	0.20	0.25	0.30
L1	0.65	0.75	0.85

Figure 20: PowerFLAT™ 2x2 recommended footprint (dimensions are in mm)



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
27-Aug-2015	1	First release.
22-Oct-2015	2	Updated title and features in cover page Updated Table 4: "On /off states", Table 5: "Dynamic" and Table 6: "Switching times". Added Section 4.1: "Electrical characteristics (curves)"
03-Apr-2017	3	Modified title and features table on cover page Modified <i>Table 4: "On /off states"</i> Modified <i>Figure 4: "Output characteristics"</i> , <i>Figure 5: "Transfer characteristics"</i> , <i>Figure 7: "Static drain-source on-resistance"</i> and <i>Figure 12: "Source-drain diode forward characteristics"</i> Minor text changes.

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