



10-Bit, Low-Power, Dual, Voltage-Output DAC with Serial Interface

MAX5721

General Description

The MAX5721 dual 10-bit, low-power, buffered voltage-output, digital-to-analog converter (DAC) is packaged in a space-saving 8-pin μ MAX[®] package (5mm x 3mm). The wide supply voltage range of +2.7V to +5.5V and 112 μ A supply current accommodate low-power and low-voltage applications. DAC outputs employ on-chip precision output amplifiers that swing rail-to-rail. The MAX5721's reference input accepts a voltage range from 0 to V_{DD} . In power-down the reference input is high impedance, further reducing the system's total power consumption.

The 20MHz, 3-wire SPI[™], QSPI[™], MICROWIRE[™] and DSP-compatible serial interface saves board space and reduces the complexity of opto- and transformer-isolated applications. The MAX5721 on-chip power-on reset (POR) circuit resets the DAC outputs to zero and loads the output with a 100k Ω resistor to ground. This provides additional safety for applications that drive valves or other transducers that need to be off on power-up. The MAX5721's software-controlled power-down reduces supply current to less than 0.3 μ A and provides software-selectable output loads (1k Ω , 100k Ω , or high impedance) while in power-down. The MAX5721 is specified over the -40°C to +125°C automotive temperature range.

Applications

Automatic Tuning
Gain and Offset Adjustment
Power Amplifier Control
Process Control I/O Boards
Battery-Powered Instruments
VCO Control

Functional Diagram appears at end of data sheet.

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SPI and QSPI are trademarks of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor, Corp.

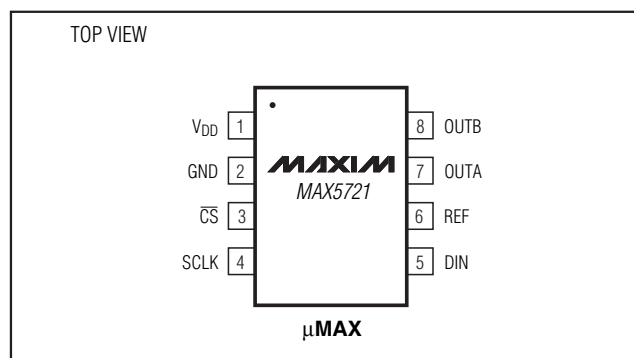
Features

- ◆ **Ultra-Low Power Consumption**
112 μ A at $V_{DD} = +3.6V$
135 μ A at $V_{DD} = +5.5V$
- ◆ **Wide +2.7V to +5.5V Single-Supply Range**
- ◆ **Tiny 8-Pin μ MAX Package**
- ◆ **0.3 μ A Power-Down Current**
- ◆ **Guaranteed 10-Bit Monotonicity (± 1 LSB DNL)**
- ◆ **Safe Power-Up Reset to Zero Volts at DAC Output**
- ◆ **Three Software Selectable Power-Down Impedances (100k Ω , 1k Ω , Hi-Z)**
- ◆ **Fast 20MHz, 3-Wire SPI, QSPI, and MICROWIRE-Compatible Serial Interface**
- ◆ **Rail-to-Rail Output Buffer Amplifiers**
- ◆ **Schmitt-Triggered Logic Inputs for Direct Interface to Optocouplers**
- ◆ **Wide -40°C to +125°C Operating Temperature Range**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5721EUA	-40°C to +85°C	8 μ MAX
MAX5721AUA	-40°C to +125°C	8 μ MAX

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND-0.3V to +6V
 OUT₊, SCLK, DIN, CS, REF to GND.....-0.3 to (V_{DD}+0.3V)
 Maximum Continuous Current Into Any Pin.....±50mA
 Continuous Power Dissipation (T_A = +70°C)
 8-Pin μ MAX (derate 4.6 mW/°C above +70°C)362mW

Operating Temperature Range-40°C to +125°C
 Junction Temperature+150°C
 Storage Temperature Range-65°C to +150°C
 Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V, GND = 0, V_{REF} = V_{DD}, R_L = 5k Ω , C_L = 200pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are V_{DD} = +5V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY (Note 1)						
Resolution	N		10			Bits
Integral Nonlinearity Error	INL	(Note 2)		±0.5	±4	LSB
Differential Nonlinearity Error	DNL	Guaranteed monotonic (Note 2)			±1	LSB
Zero-Code Error	OE	Code = 000		0.4	1.5	% of FS
Zero-Code Error Tempco				2.3		ppm/°C
Gain Error	GE	Code = 3FF hex			±3	% of FS
Gain-Error Tempco				0.26		ppm/°C
Power-Supply Rejection Ratio	PSRR	Code = 3FF hex, Δ V _{DD} = ±10%		58.8		dB
REFERENCE INPUT						
Reference Input Voltage Range	V _{REF}		0		V _{DD}	V
Reference Input Impedance	R _{REF}	In operation	64	90	126	k Ω
		In power-down mode		2		M Ω
Reference-Down Reference Current		In power-down mode (Note 3)		1	10	μ A
DAC OUTPUT						
Output Voltage Range		No load (Note 4)	0		V _{DD}	V
DC Output Impedance		Code = 200 hex		0.8		Ω
Short-Circuit Current		V _{DD} = +3V		15		mA
		V _{DD} = +5V		48		
Wake-Up Time		V _{DD} = +3V		8		μ s
		V _{DD} = +5V		8		
Output Leakage Current		Power-down mode = output high impedance		±18		nA

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +2.7V$ to $+5.5V$, $GND = 0$, $V_{REF} = V_{DD}$, $R_L = 5k\Omega$, $C_L = 200pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are $V_{DD} = +5V$, $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$)						
Input High Voltage	V_{IH}	$V_{DD} = +3V, +5V$	0.7 x V_{DD}			V
Input Low Voltage	V_{IL}	$V_{DD} = +3V, +5V$			0.3 x V_{DD}	V
Input Leakage Current	I_{IN}	Digital inputs = 0 or V_{DD}	± 0.1		± 1	μA
Input Capacitance			5			pF
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR		0.5			V/ μs
Voltage-Output Settling Time		100 hex to 300 hex (Note 5)	4		10	μs
Digital Feedthrough		All digital inputs from 0 to V_{DD}	0.1			nV-s
Digital-Analog Glitch Impulse		Major carry transition (code 1FF hex to code 200 hex)	12			nV-s
DAC-to-DAC Crosstalk						nV-s
POWER REQUIREMENTS						
Supply Voltage Range	V_{DD}		2.7		5.5	V
Supply Current with No Load	I_{DD}	All digital inputs at 0 or $V_{DD} = 3.6V$	112		205	μA
		All digital inputs at 0 or $V_{DD} = 5.5V$	135		215	
Power-Down Supply Current	I_{DDPD}	All digital inputs at 0 or $V_{DD} = 5.5V$	0.29		1	μA

TIMING CHARACTERISTICS

($V_{DD} = 2.7V$ to $5.5V$, $GND = 0$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Frequency	f_{SCLK}		0		20	MHz
SCLK Pulse Width High	t_{CH}		25			ns
SCLK Pulse Width Low	t_{CL}		25			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		10			ns
SCLK Fall to $\overline{CS}$ Rise Setup Time	t_{CSH}		10			ns
DIN to SCLK Fall Setup Time	t_{DS}		15			ns
DIN to SCLK Fall Hold Time	t_{DH}		0			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		80			ns

Note 1: DC specifications are tested without output loads.

Note 2: Linearity guaranteed from code 29 to code 995.

Note 3: Limited with test conditions.

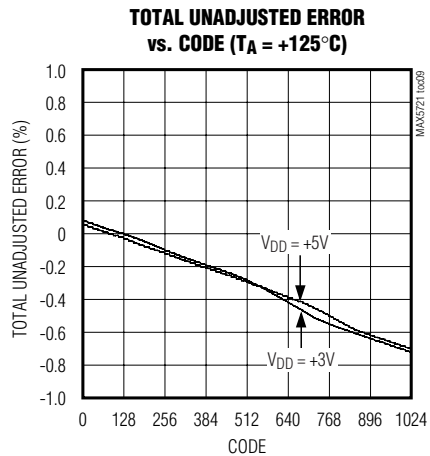
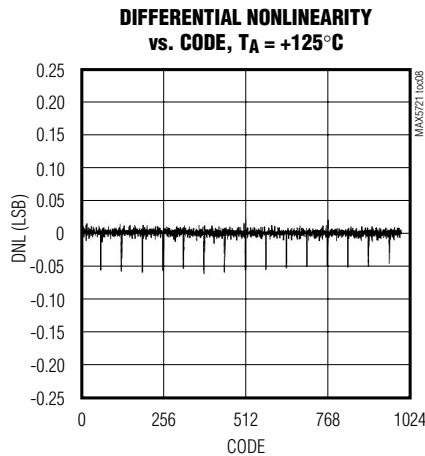
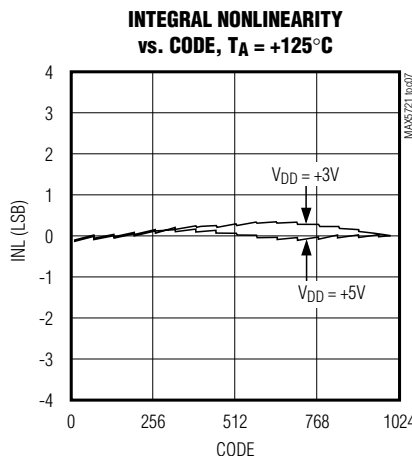
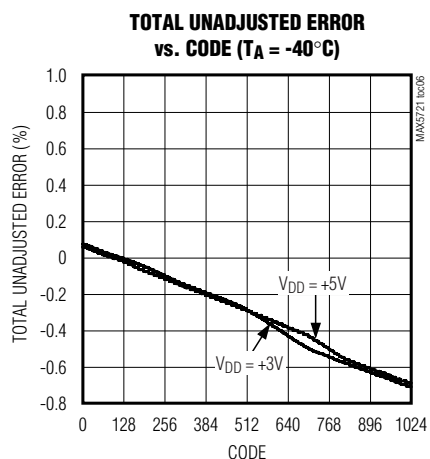
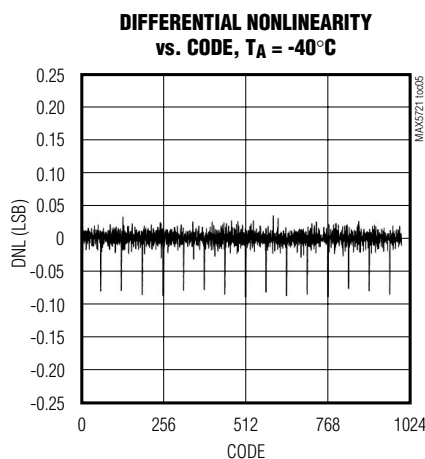
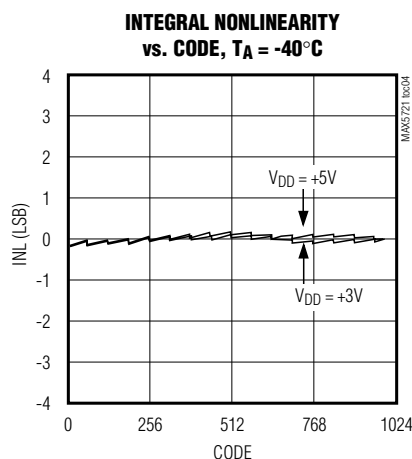
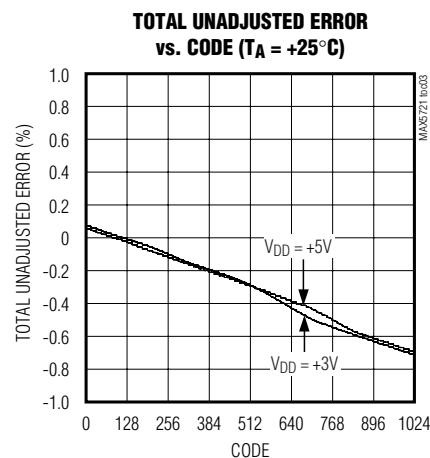
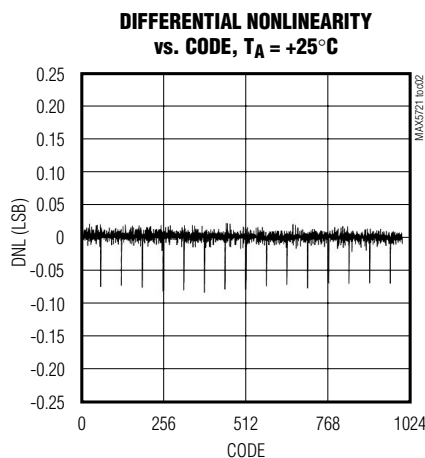
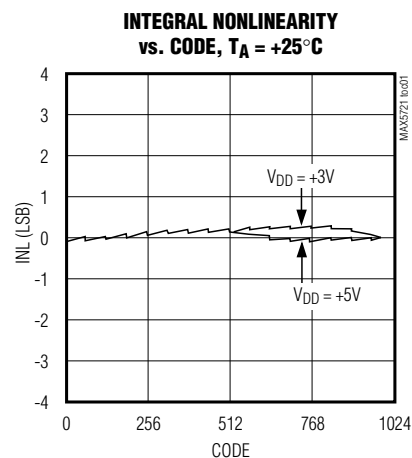
Note 4: Offset and gain error limit the FSR.

Note 5: Guaranteed by design.

10-Bit, Low-Power, Dual, Voltage-Output DAC with Serial Interface

Typical Operating Characteristics

($V_{REF} = V_{DD}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

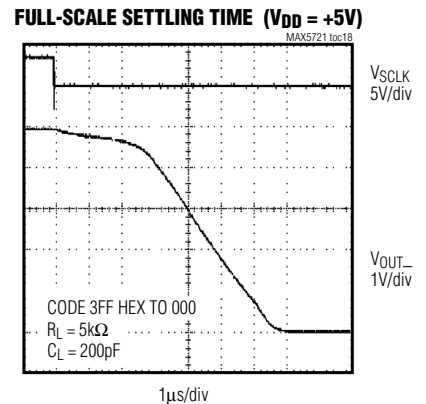
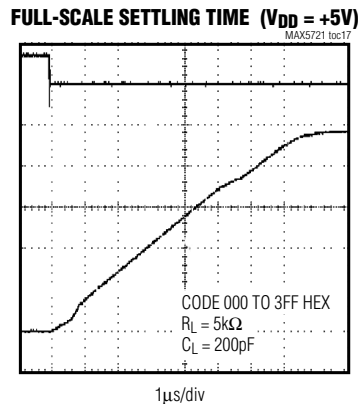
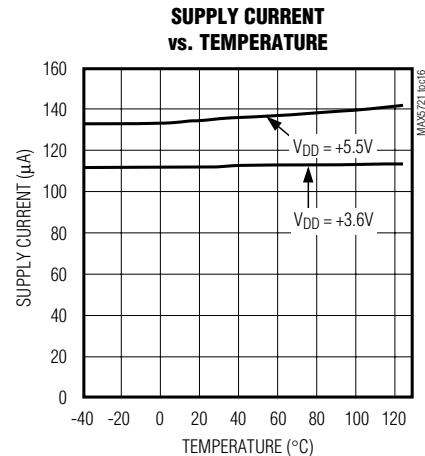
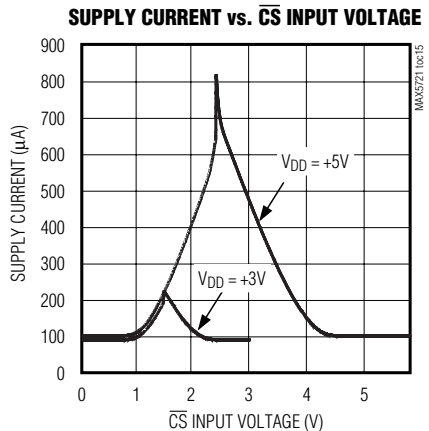
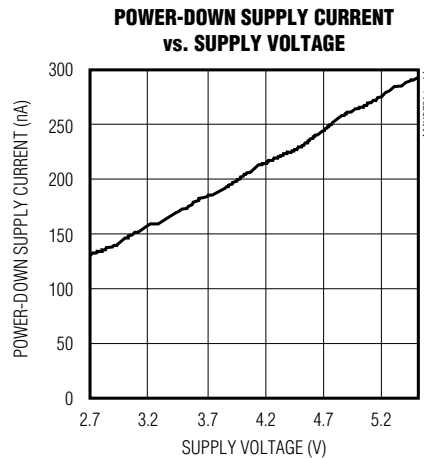
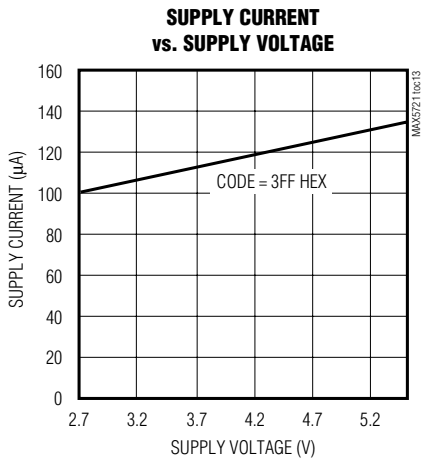
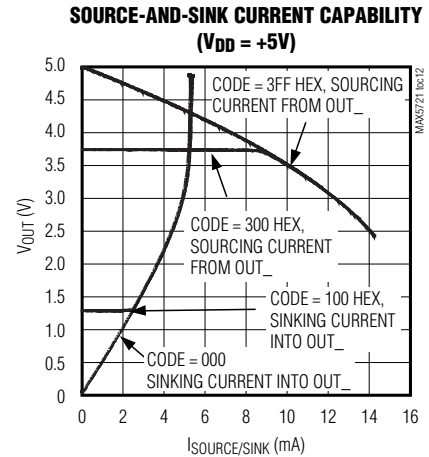
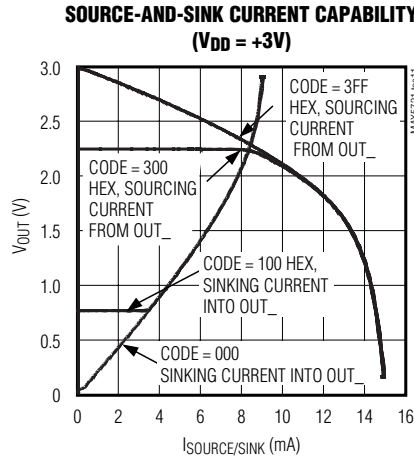
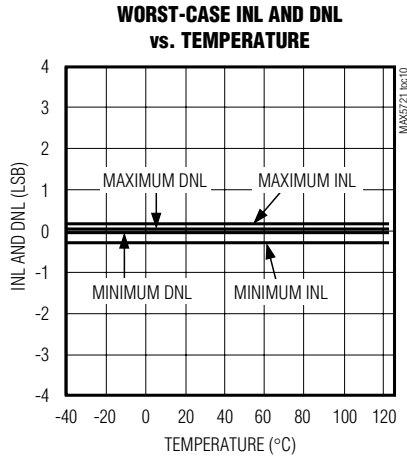


10-Bit, Low-Power, Dual, Voltage-Output DAC with Serial Interface

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Typical Operating Characteristics (continued)

($V_{REF} = V_{DD}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

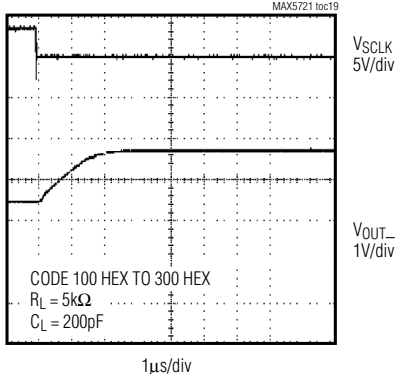


10-Bit, Low-Power, Dual, Voltage-Output DAC with Serial Interface

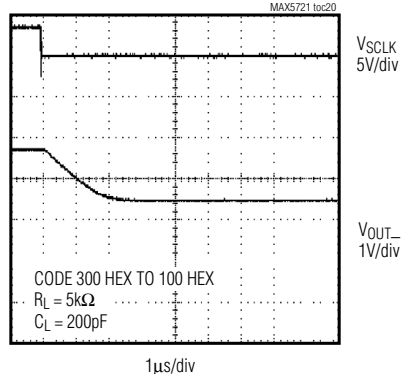
Typical Operating Characteristics (continued)

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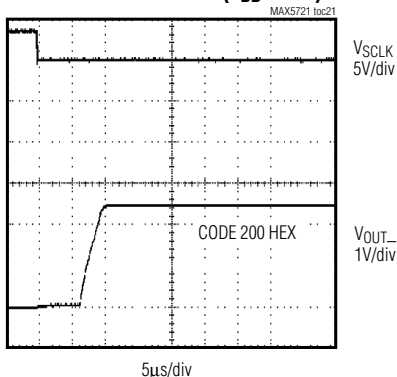
HALF-SCALE SETTLING TIME ($V_{DD} = +3\text{V}$)



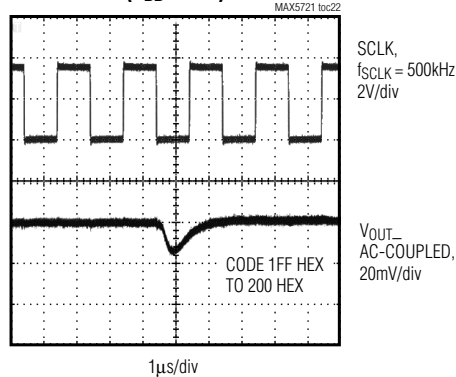
HALF-SCALE SETTLING TIME ($V_{DD} = +3\text{V}$)



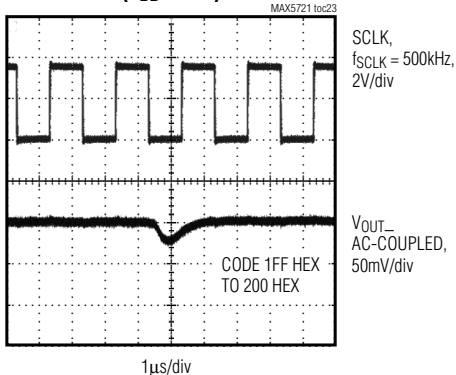
EXITING POWER-DOWN ($V_{DD} = +5\text{V}$)



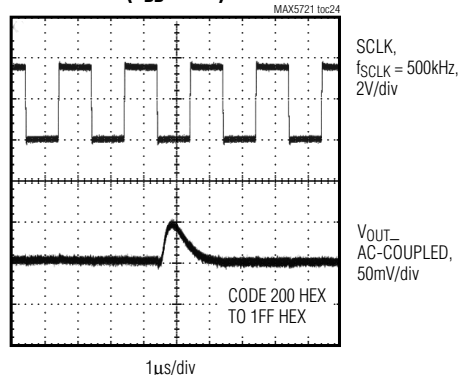
DIGITAL-TO-ANALOG GLITCH IMPULSE ($V_{DD} = +5\text{V}$)



DIGITAL-TO-ANALOG GLITCH IMPULSE ($V_{DD} = +3\text{V}$)



DIGITAL-TO-ANALOG GLITCH IMPULSE ($V_{DD} = +5\text{V}$)



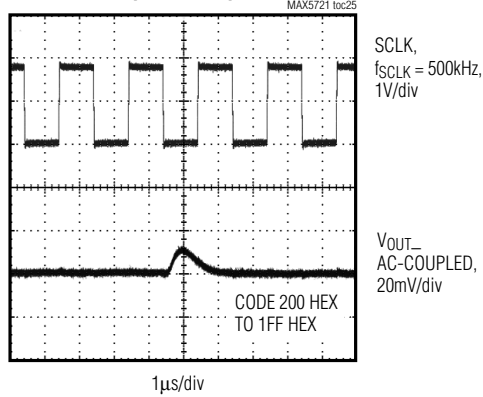
10-Bit, Low-Power, Dual, Voltage-Output DAC with Serial Interface

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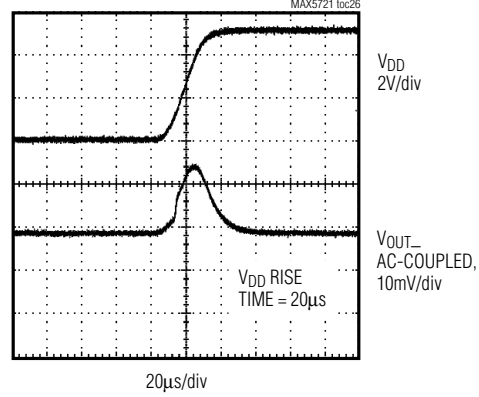
Typical Operating Characteristics (continued)

($V_{REF} = V_{DD}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

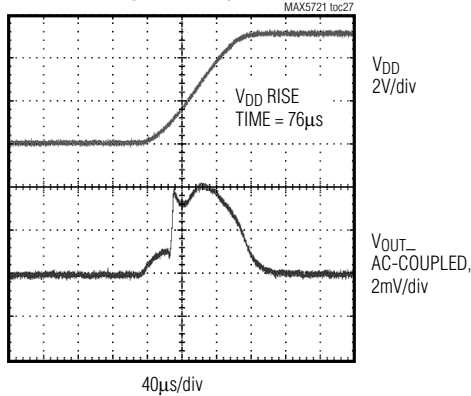
DIGITAL-TO-ANALOG GLITCH IMPULSE
($V_{DD} = +3\text{V}$)



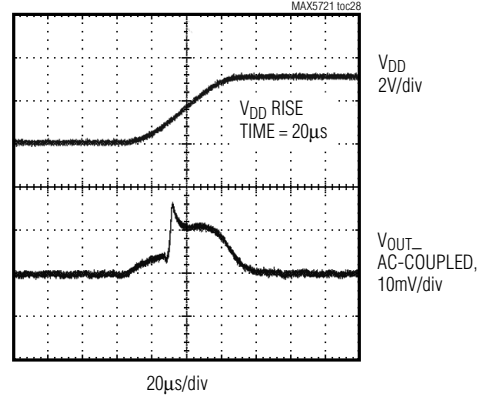
POWER-ON RESET, FAST RISE TIME
($V_{DD} = +5\text{V}$)



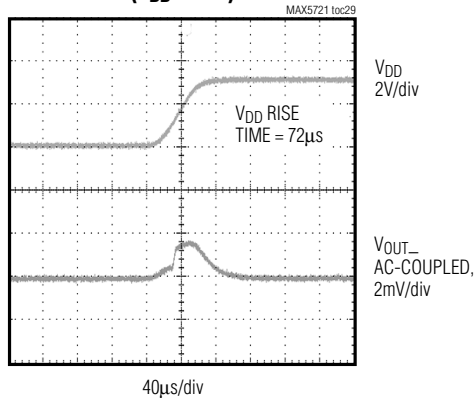
POWER-ON RESET, SLOW RISE TIME
($V_{DD} = +5\text{V}$)



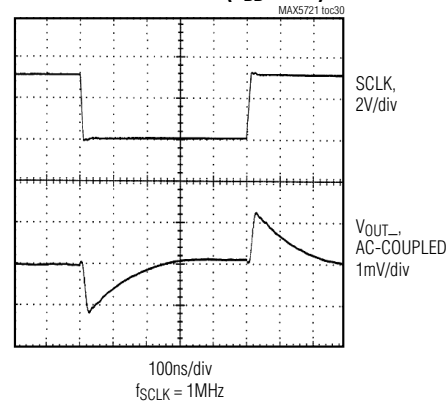
POWER-ON RESET, FAST RISE TIME
($V_{DD} = +3\text{V}$)



POWER-ON RESET, SLOW RISE TIME
($V_{DD} = +3\text{V}$)



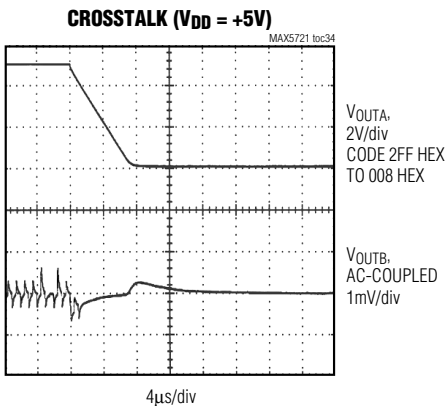
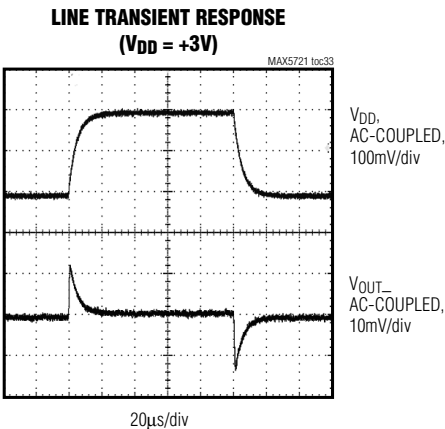
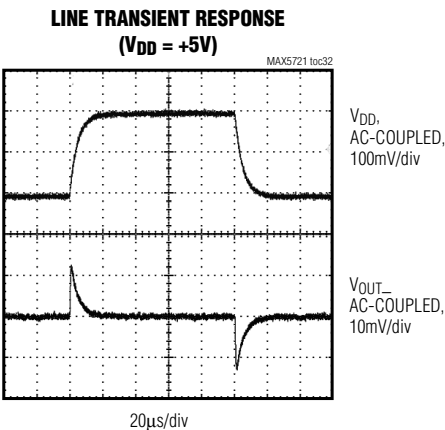
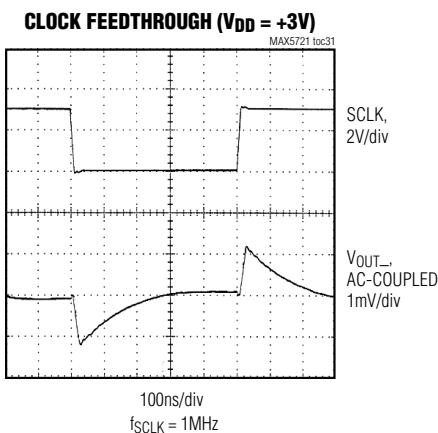
CLOCK FEEDTHROUGH ($V_{DD} = +5\text{V}$)



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Typical Operating Characteristics (continued)

($V_{REF} = V_{DD}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Power-Supply Input
2	GND	Ground
3	$\overline{CS}$	Chip-Select Input
4	SCLK	Serial Clock Input
5	DIN	Serial Data Input
6	REF	External Reference Voltage Input
7, 8	OUTA, OUTB	DAC Voltage Outputs. Power-on reset sets DAC registers to zero, and internally connects OUT to GND with 100k Ω resistor.

10-Bit, Low-Power, Dual, Voltage-Output DAC with Serial Interface

Detailed Description

The MAX5721 contains two 10-bit, voltage-output, low-power digital-to-analog converters (DACs). Each DAC employs a resistor string architecture that converts a 10-bit digital input word to an equivalent analog output voltage proportional to the applied reference voltage. The MAX5721 shares one reference input (REF) between both DACs. The MAX5721 includes rail-to-rail output buffer amplifiers for each DAC, and input logic for simple microprocessor (μ P), and CMOS interfaces. The power-supply range is from +2.7V to +5.5V (*Functional Diagram*). The MAX5721's reference input accepts a voltage range from 0 to V_{DD} . In power-down mode the reference input is high impedance. The MAX5721 is compatible with the 3-wire SPI, QSPI, MICROWIRE, and DSP serial interface with Schmitt-triggered logic inputs.

Reference Input and DAC Output Range

The reference input accepts positive DC and AC signals. The voltage at REF sets the full-scale output voltage of both DACs. The reference input voltage range is 0 to V_{DD} . The impedance at REF is 90k Ω . The voltage at REF can vary from GND to V_{DD} . The output voltages ($V_{OUT_}$) are represented by a digitally programmable voltage source as:

$$V_{OUT_} = (V_{REF} \times D) / 2^{10}$$

where D is the decimal equivalent of binary DAC input code ranging from 0 to 1023. V_{REF} is the voltage at REF.

Output Buffer Amplifiers

All DACs are internally buffered at the output. The buffer amplifiers have both rail-to-rail common mode and (GND to V_{REF}) output voltage range. The buffers are unity-gain stable with $C_L = 200$ pF and $R_L = 5$ k Ω . Buffer amplifiers are disabled during power-up and individual DAC outputs are shorted to GND through a 100k Ω resistor. Buffer amplifiers can individually or altogether be powered-down by programming the input register control bits. During power down, contents of the input and DAC registers remain the same. On wake-up all DAC outputs are restored to their pre-power-down voltage values.

Power-Down Mode

In power-down mode, the DAC outputs are programmed to one of three output states, 1k Ω , 100k Ω , or floating (Table 1). The REF input is high impedance (2M Ω typ) to conserve current drain from the system reference; therefore, the system reference does not have to be powered-down. The DAC outputs return to the values contained in the registers when brought out of power-down. The recovery time, from total power-

down to power-up, is 8 μ s. This extra time is needed to allow the internal bias to wake-up. Power-down mode reduces current consumption to 0.5 μ A.

3-Wire Serial Interface

The MAX5721 digital interface is a standard 3-wire connection compatible with SPI/QSPI/MICROWIRE/DSP interfaces. The chip-select input ($\overline{CS}$) frames the serial data loading at DIN. Immediately following $\overline{CS}$ high-to-low transition, the data is shifted synchronously and latched into the input register on the falling edge of the serial clock input (SCLK). After 16 bits have been loaded into the serial input register, it transfers its contents to the DAC latch. $\overline{CS}$ may then either be held low or brought high. $\overline{CS}$ must be brought high for a minimum of 80ns before the next write sequence, since a write sequence is initiated on a falling edge of $\overline{CS}$. Not keeping $\overline{CS}$ low during the first 15 SCLK cycles discards input data. The serial clock (SCLK) can idle either high or low between transitions.

The MAX5721 has two internal registers per DAC, the input register and the DAC register. The input register holds the data that is waiting to be shifted to the DAC register. Both input registers can be loaded without updating the output. This function is useful when both outputs need to be updated at the same time. The input register can be made transparent. When the input register is transparent, the data written into DIN loads directly to the DAC register and the output is updated. The DAC output is not updated until data is written to the DAC register. See Table 2 for a list of serial-interface programming commands.

Power-On Reset (POR)

The MAX5721 has an internal POR circuit. At power-up all DACs are powered-down and OUT_{-} is terminated to GND through 100k Ω resistors. Contents of input and DAC registers are cleared to all zero. An 8 μ s recovery time after issuing a wake-up command is needed before writing to the DAC registers. Power-down mode control commands can be applied immediately with no recovery time.

C3-C0 are control bits. The data bits D9 to D0 are in straight binary format. Set bits S1 and S0 to zero. All zeros correspond to zero scale and all ones correspond to full scale.

Digital Inputs

The digital inputs are compatible with CMOS logic. In order to save power and reduce input to output coupling, SCLK and DIN input buffers are powered down immediately after completion of shifting 16 bits into the input shift register. A high to low transition at $\overline{CS}$ powers up SCLK and DIN input buffers.

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Table 1. Power-Down Mode Control

EXTENDED CONTROL				DATA BITS						DESCRIPTION	FUNCTION
C3	C2	C1	C0	D9–D3	D2	D1	D0	S1	S0		
1	1	1	1	X	0	0	0	0	0	DAC A	DAC O/P, wake-up
1	1	1	1	X	0	0	0	0	1	DAC A	Floating output
1	1	1	1	X	0	0	0	1	0	DAC A	Output is terminated with 1k Ω
1	1	1	1	X	0	0	0	1	1	DAC A	Output is terminated with 100k Ω
1	1	1	1	X	0	0	1	0	0	DAC B	DAC O/P, wake-up
1	1	1	1	X	0	0	1	0	1	DAC B	Floating output
1	1	1	1	X	0	0	1	1	0	DAC B	Output is terminated with 1k Ω
1	1	1	1	X	0	0	1	1	1	DAC B	Output is terminated with 100k Ω
1	1	1	1	X	1	0	0	0	0	DAC A-B	DAC O/P, wake-up
1	1	1	1	X	1	0	0	0	1	DAC A-B	Floating output
1	1	1	1	X	1	0	0	1	0	DAC A-B	Output is terminated with 1k Ω
1	1	1	1	X	1	0	0	1	1	DAC A-B	Output is terminated with 100k Ω

X = Don't Care

CONTENTS OF INPUT SHIFT REGISTER															
D15 (MSB)															D0 (LSB)
C3	C2	C1	C0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	S1	S0

Figure 1. 16-Bit Input Word

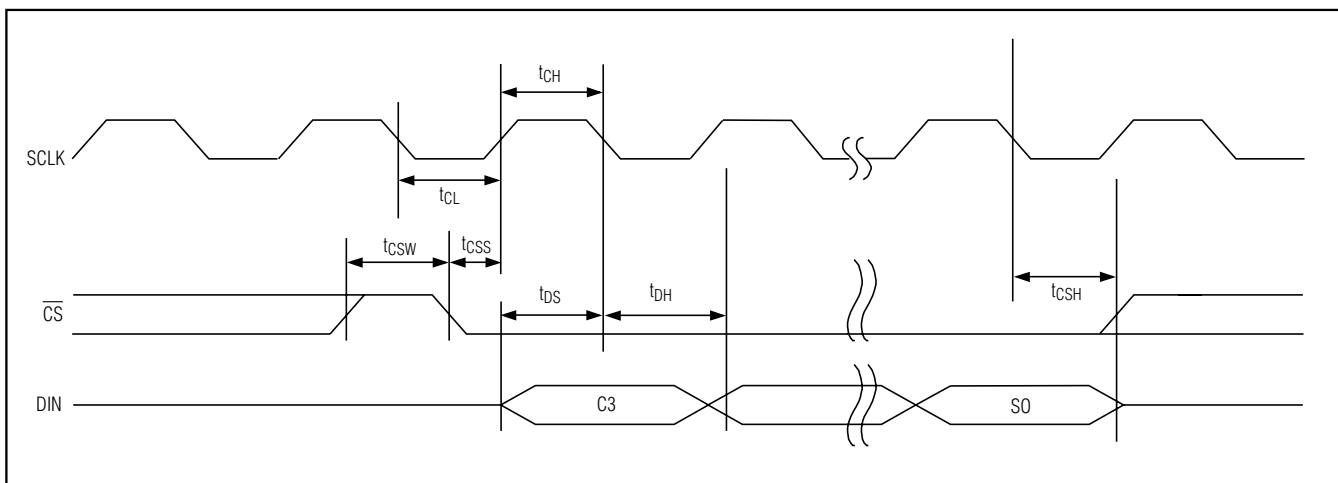


Figure 2. Timing Diagram

MAX5721

CONTROL				DATA BITS		DAC	FUNCTION
C3	C2	C1	C0	D9–D0	S1–S0		
0	0	0	0	X	X	A	Input register transparent, data shifted directly to DAC register, OUTA updated
0	0	0	1	X	X	B	Input register transparent, data shifted directly to DAC register, OUTB updated
0	1	0	0	X	X	A	Data shifted to input register, OUTA unchanged
0	1	0	1	X	X	B	Data shifted to input register, OUTB unchanged
1	0	0	0	X	X	A	Shift data from input register to DAC register, OUTA updated
1	0	0	1	X	X	B	Shift data from input register to DAC register, OUTB updated
1	1	0	0	X	X	A-B	Input registers transparent, data shifted directly to DAC registers, OUTA and OUTB updated
1	1	0	1	X	X	A-B	Data shifted to input registers, OUTA and OUTB unchanged
1	1	1	0	X	X	A-B	Shift data from input registers to DAC registers, OUTA and OUTB updated

Applications Information

The typical application circuit (Figure 3) shows the MAX5721 configured for a unipolar output, where the output voltages and the reference inputs have the same polarity. Table 3 lists the unipolar output codes.

Careful PC board layout is important for optimal system performance. To reduce noise injection and digital feed-through, keep analog and digital signals separate. Ensure that the return path from GND to the supply ground is short and low impedance. Use a ground plane. Bypass V_{DD} to GND with a $0.1\mu\text{F}$ capacitor as close as possible to V_{DD} .

The diagram shows the MAX5721 DAC chip with its internal DAC_ and OUT_ blocks. The REF pin is connected to a voltage divider consisting of resistors R1 and R2. The input to the divider is labeled "+2.7V to +5.5V". The output of the divider, which is the midpoint between R1 and R2, is connected to the non-inverting input (+) of an external op-amp. The op-amp is configured as a voltage follower (buffer), with its output VOUT connected back to its inverting input (-). The op-amp's supply pins are labeled V+ and V-. The MAX5721 chip's VDD pin is connected to the same input voltage source as R1, and its GND pin is connected to ground. The output of the DAC_ block is connected to the OUT_ block. The text "MAXIM MAX5721" is printed on the chip symbol. Below the diagram, the text "R1 = R2" is specified.

Figure 4. Bipolar Output Circuit

10-Bit, Low-Power, Dual, Voltage-Output DAC with Serial Interface

Table 3. Unipolar Code Table

DAC CONTENTS	ANALOG OUTPUT
1111 1111 1100	$+V_{REF}\left(\frac{1023}{1024}\right)$
1000 0000 0100	$+V_{REF}\left(\frac{513}{1024}\right)$
1000 0000 0000	$+ \frac{V_{REF}}{2}$
0111 1111 1100	$+V_{REF}\left(\frac{511}{1024}\right)$
0000 0000 0100	$+V_{REF}\left(\frac{1}{1024}\right)$
0000 0000 0000	0

Table 4. Bipolar Code Table

DAC CONTENTS	ANALOG OUTPUT
1111 1111 1100	$+V_{REF}\left(\frac{511}{512}\right)$
1000 0000 01000	$+V_{REF}\left(\frac{1}{512}\right)$
1000 0000 0000	0
0111 1111 11100	$-V_{REF}\left(\frac{1}{512}\right)$
0000 0000 0100	$-V_{REF}\left(\frac{511}{512}\right)$
0000 0000 0000	$-V_{REF}$

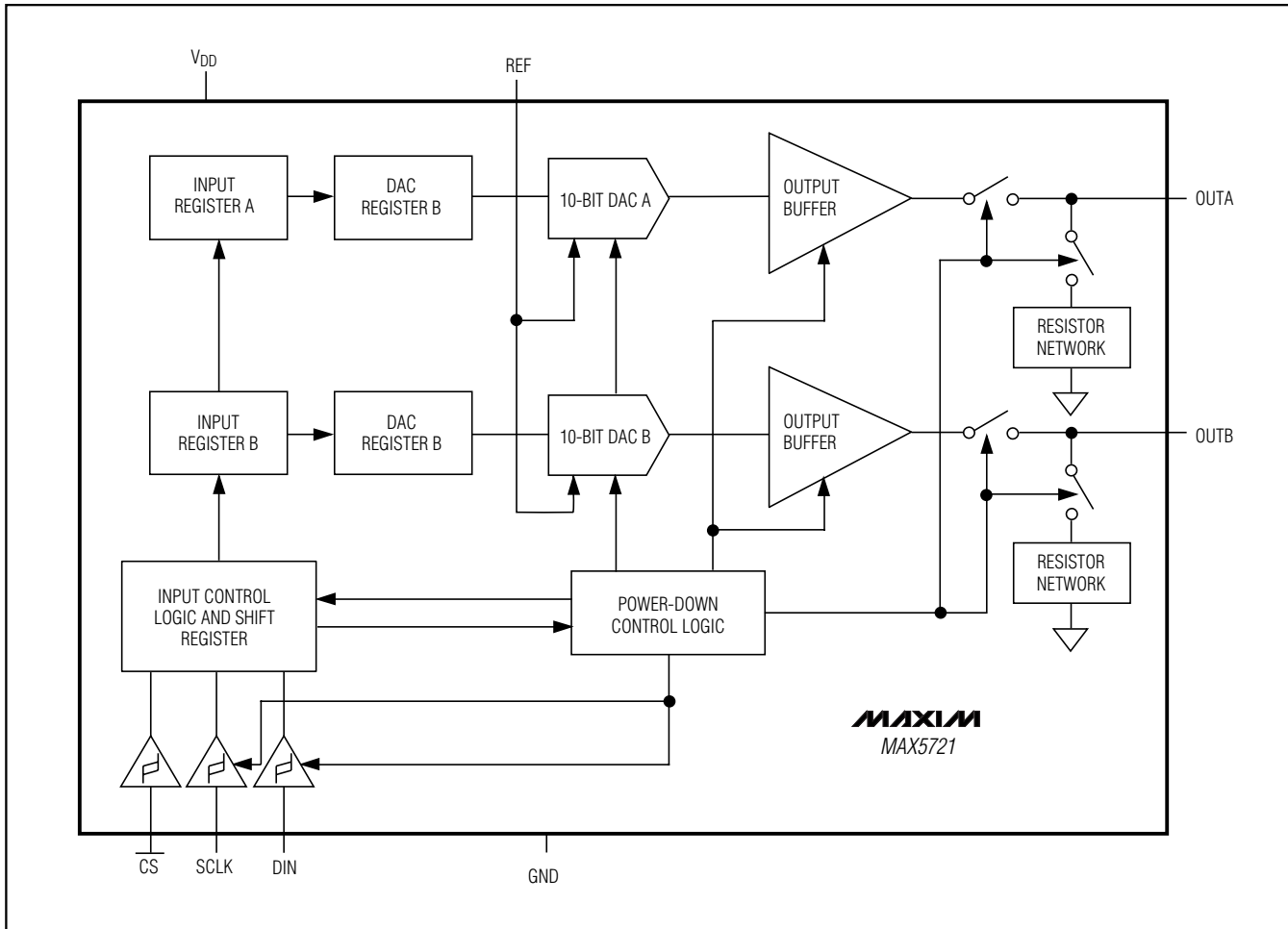
Chip Information

TRANSISTOR COUNT: 7737
PROCESS: BiCMOS

10-Bit, Low-Power, Dual, Voltage-Output DAC with Serial Interface

Functional Diagram

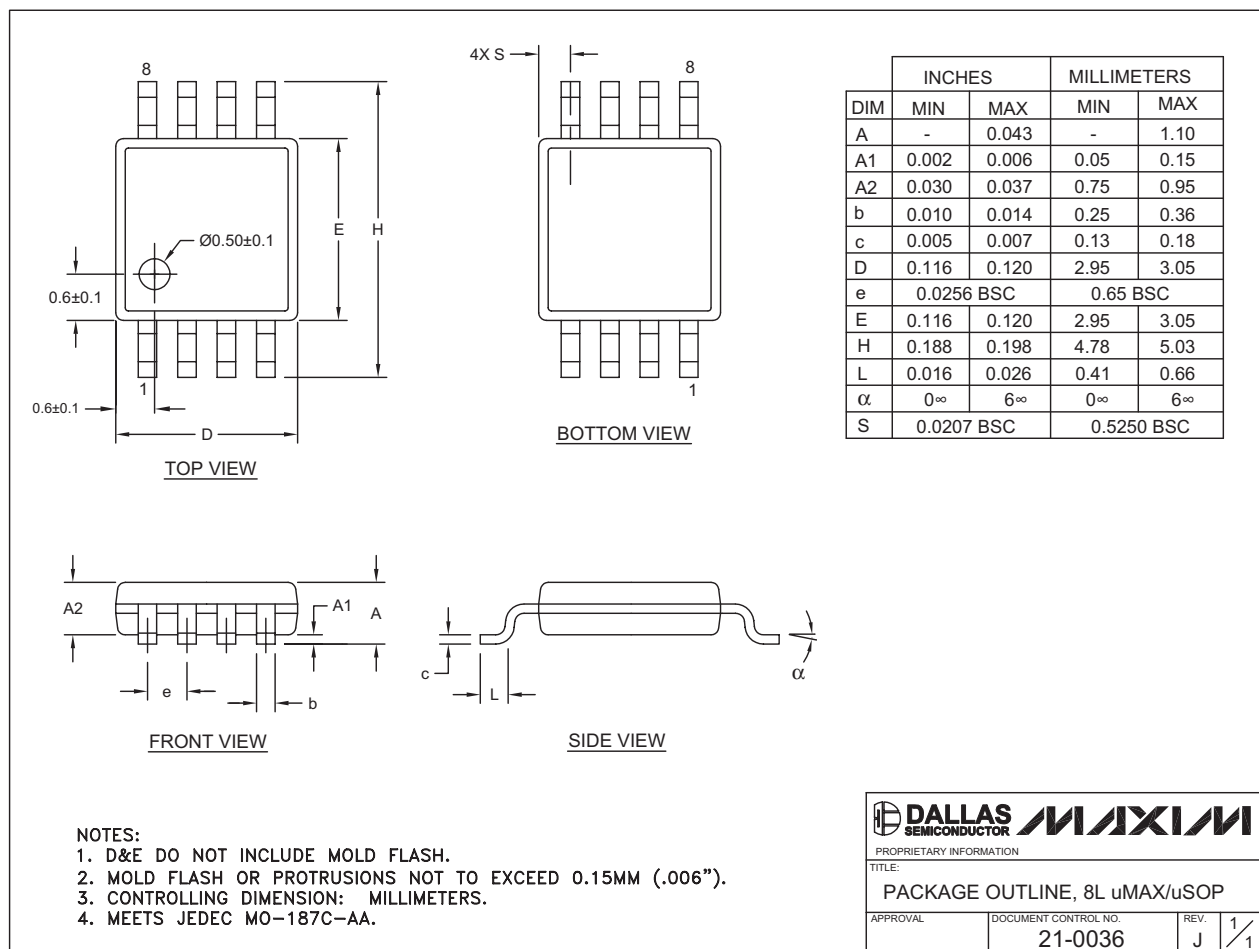
MAX5721



10-Bit, Low-Power, Dual, Voltage-Output DAC with Serial Interface

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



MAX5721

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