

## Product Summary

$V_{(BR)DSS}$	$R_{DS(on) \max}$	$I_D$ $T_A = +25^\circ\text{C}$
100V	220m $\Omega$ @ $V_{GS} = 10\text{V}$	1.6A
	250m $\Omega$ @ $V_{GS} = 4.5\text{V}$	1.3A

## Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

## Description

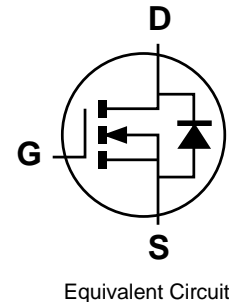
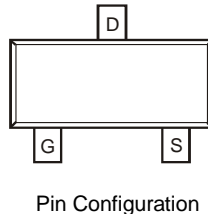
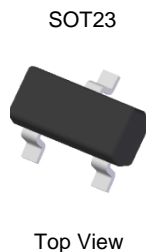
This new generation MOSFET is designed to minimize the on-state resistance ( $R_{DS(on)}$ ) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

## Applications

- Load Switch

## Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic, "Green" Molding Compound
- UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish—Matte Tin Annealed Over Copper Leadframe. Solderable per MIL-STD-202, Method 208 **e3**
- Weight: 0.0072 grams (Approximate)



## Ordering Information (Note 4)

Part Number	Compliance	Case	Packaging
DMN10H220L-7	Standard	SOT23	3000/Tape & Reel
DMN10H220L-13	Standard	SOT23	10,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

## Marking Information



N1H = Marking Code  
 YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)  
 ȲM = Date Code Marking for CAT (Chengdu Assembly/ Test site)  
 Y or Ȳ = Year (ex: A = 2013)  
 M = Month (ex: 9 = September)

### Date Code Key

Year	2013	2014	2015	2016	2017	2018	2019
Code	A	B	C	D	E	F	G

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V <sub>DSS</sub>	100	V
Gate-Source Voltage	V <sub>GSS</sub>	±16	V
Continuous Drain Current (Note 5) V <sub>GS</sub> = 10V	(Note 6) T <sub>A</sub> = +25°C T <sub>A</sub> = +70°C	1.6 1.3	A
	(Note 5) T <sub>A</sub> = +25°C T <sub>A</sub> = +70°C	1.4 1.1	A
Maximum Continuous Body Diode Forward Current (Note 6)	I <sub>S</sub>	0.6	A
Pulsed Drain Current (10μs Pulse, Duty Cycle = 1%)	I <sub>DM</sub>	8	A

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 6)	P <sub>D</sub>	T <sub>A</sub> = +25°C	1.3
		T <sub>A</sub> = +70°C	0.8
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	(Note 6)	94
		(Note 5)	177
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	1	μA	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±16V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	1	—	2.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	—	220	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 1.6A
			—	250		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 1.3A
Diode Forward Voltage	V <sub>SD</sub>	—	0.7	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 1.1A
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>ISS</sub>	—	401	—	pF	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V f = 1MHz
Output Capacitance	C <sub>OSS</sub>	—	22	—		
Reverse Transfer Capacitance	C <sub>RSS</sub>	—	17	—		
Gate Resistance	R <sub>G</sub>	—	2.1	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (V <sub>GS</sub> = 4.5V)	Q <sub>g</sub>	—	4.1	—	nC	V <sub>DS</sub> = 50V, I <sub>D</sub> = 1.6A
Total Gate Charge (V <sub>GS</sub> = 10V)	Q <sub>g</sub>	—	8.3	—		
Gate-Source Charge	Q <sub>GS</sub>	—	1.5	—		
Gate-Drain Charge	Q <sub>GD</sub>	—	2	—		
Turn-On Delay Time	t <sub>D(on)</sub>	—	6.8	—	ns	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 4.5V, R <sub>G</sub> = 6.8Ω, I <sub>D</sub> = 1A
Turn-On Rise Time	t <sub>r</sub>	—	8.2	—		
Turn-Off Delay Time	t <sub>D(off)</sub>	—	7.9	—		
Turn-Off Fall Time	t <sub>f</sub>	—	3.6	—		
Reverse Recovery Time	t <sub>rr</sub>	—	17	—	ns	I <sub>F</sub> = 1.1A, di/dt = 100A/μs
Reverse Recovery Charge	Q <sub>rr</sub>	—	9.8	—	nC	

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
  - Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate.
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to production testing.

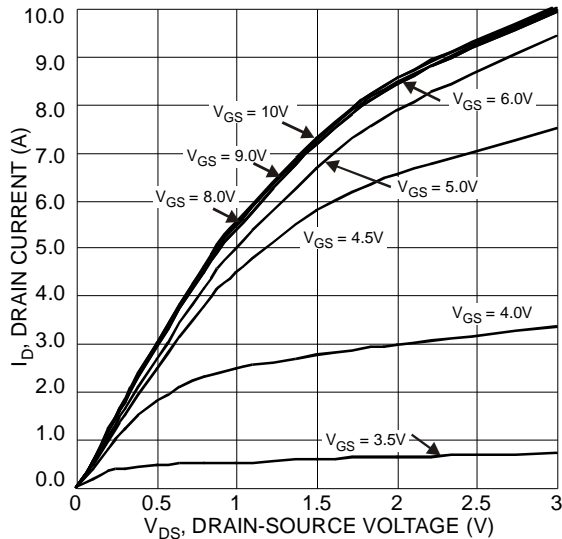


Figure 1 Typical Output Characteristic

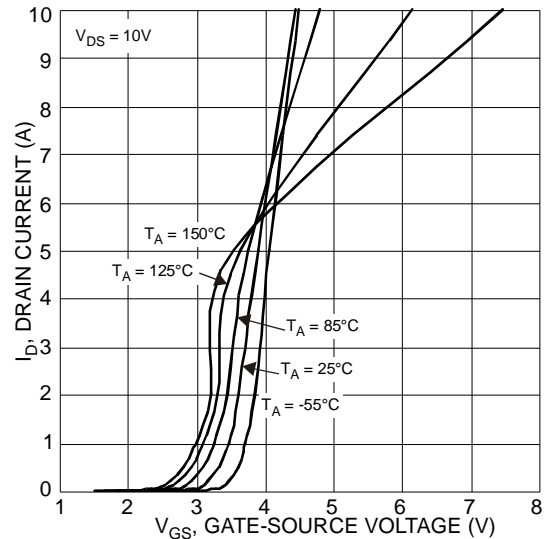


Figure 2 Typical Transfer Characteristics

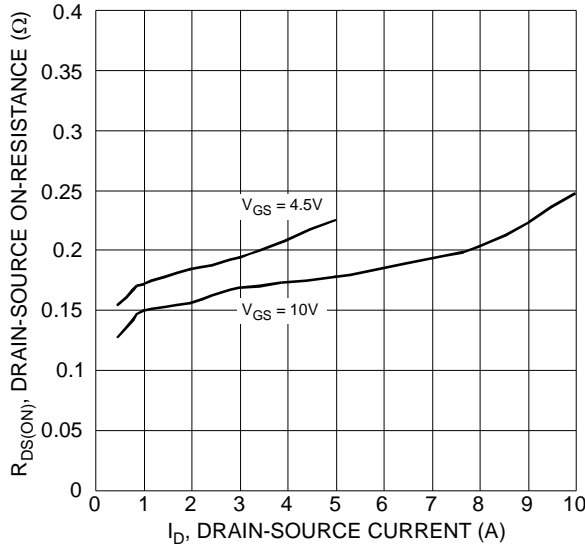


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

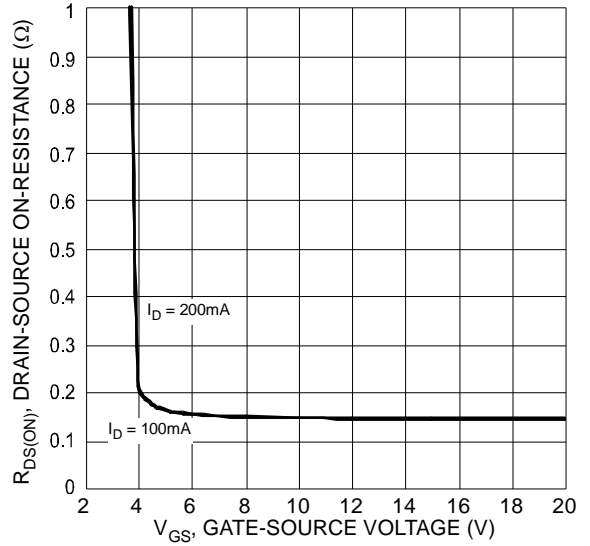


Figure 4 Typical Transfer Characteristic

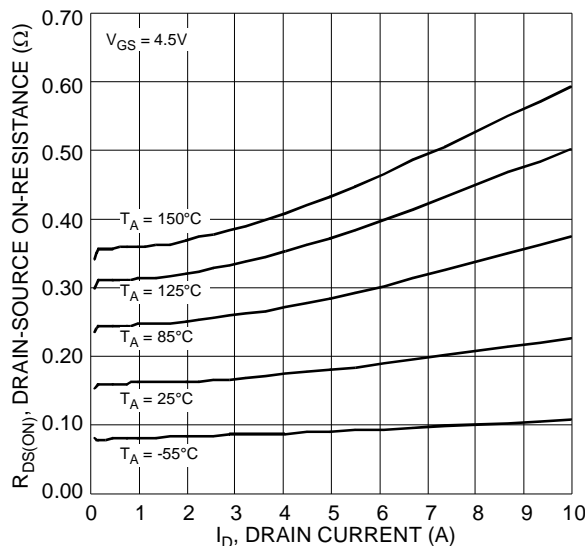


Figure 5 Typical On-Resistance vs. Drain Current and Temperature

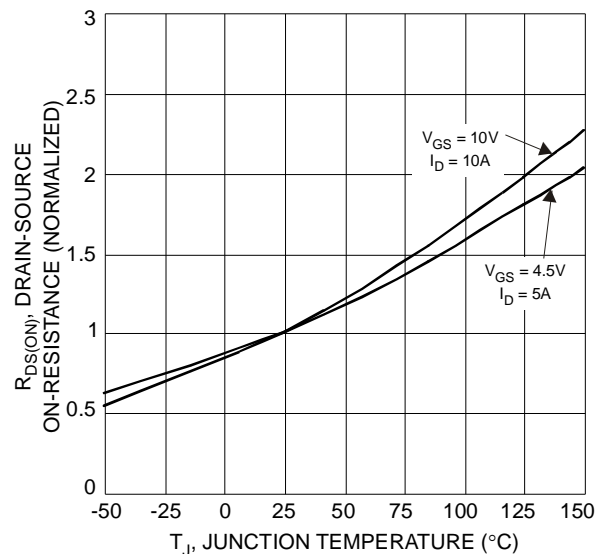


Figure 6 On-Resistance Variation with Temperature

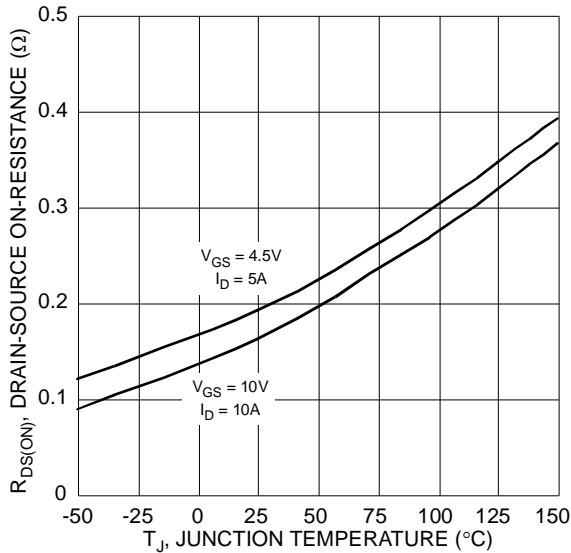


Figure 7 On-Resistance Variation with Temperature

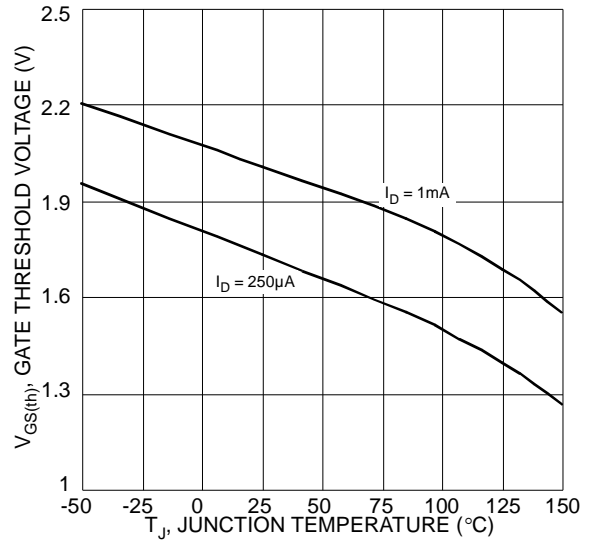


Figure 8 Gate Threshold Variation vs. Ambient Temperature

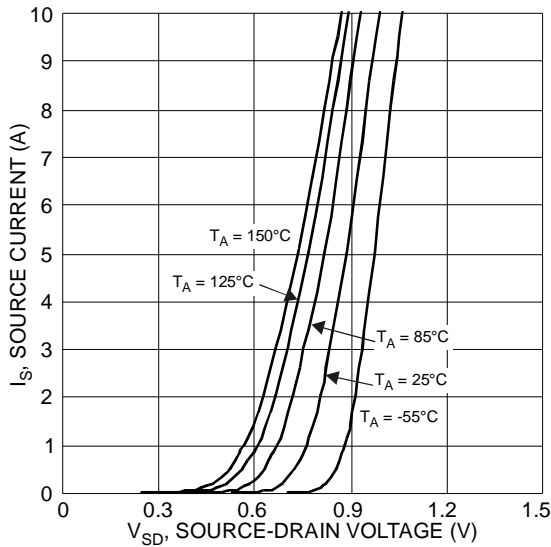


Figure 9 Diode Forward Voltage vs. Current

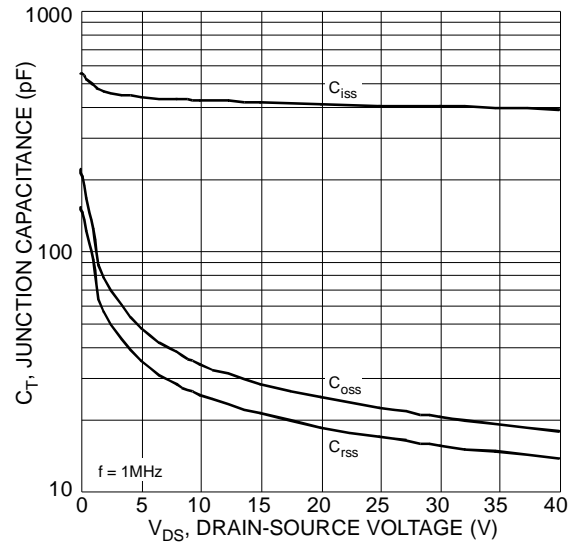


Figure 10 Typical Junction Capacitance

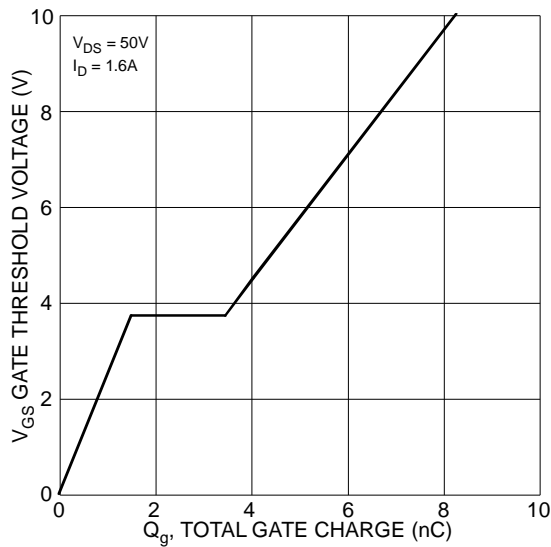


Figure 11 Gate Charge

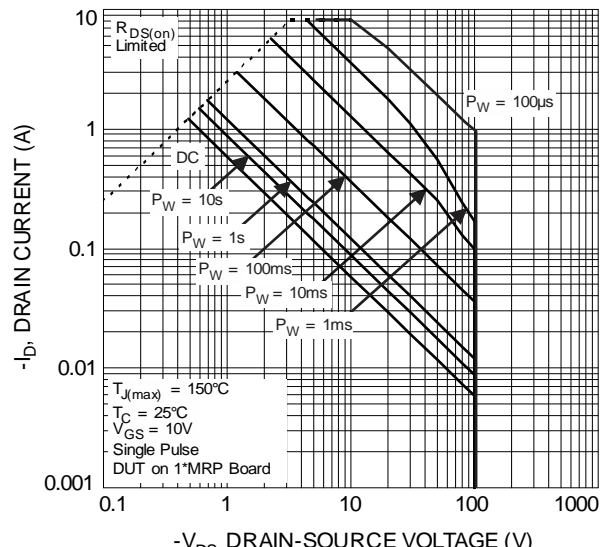
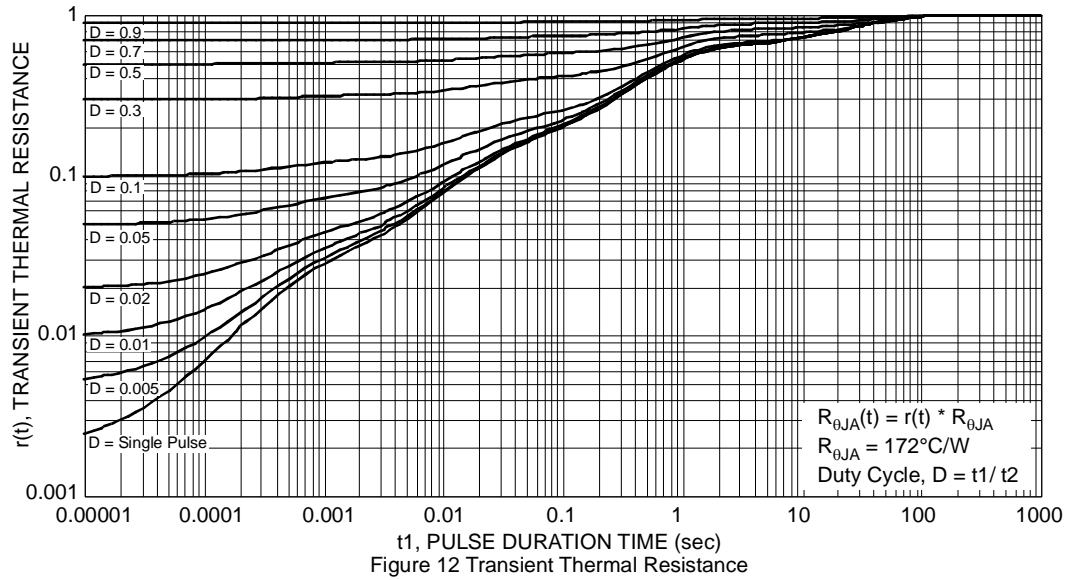
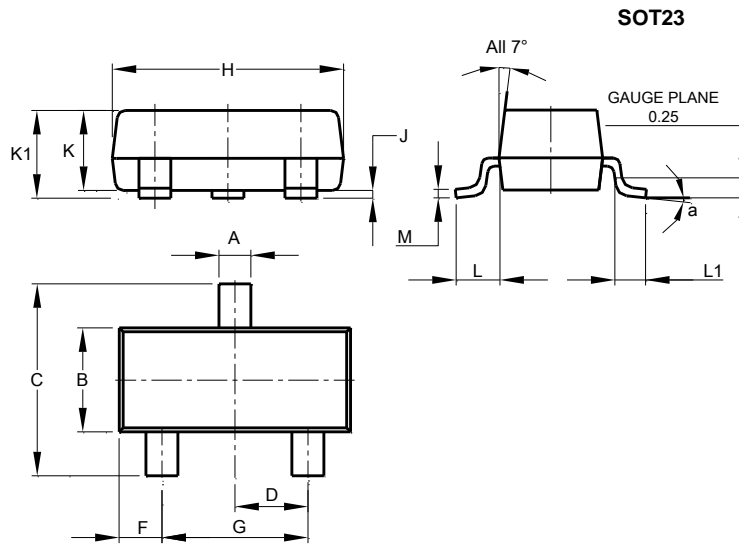


Figure 12 SOA, Safe Operation Area



**Package Outline Dimensions**

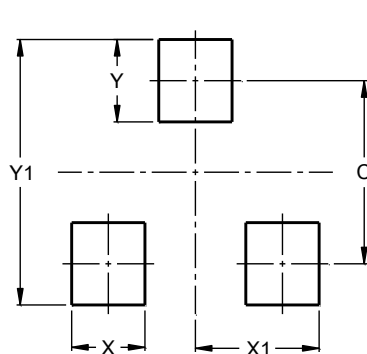
Please see <http://www.diodes.com/package-outlines.html> for the latest version.



SOT23			
Dim	Min	Max	Typ
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
a	0°	8°	--
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.



Dimensions	Value (in mm)
C	2.0
X	0.8
X1	1.35
Y	0.9
Y1	2.9

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