XMCxxxxSC

Wireless Power Controller Series
for Commercial and
Industrial Applications

XMC1000 Family

ARM® Cortex®-M0
32-bit processor core

Data Sheet

V1.3, 2019-05

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About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMCXXXXSC series devices.

The document describes the characteristics of a superset of the XMCXXXXSC series devices. For simplicity, the various device types are referred to by the collective term XMCXXXXSC throughout this document.

XMC1000 Family User Documentation

The set of user documentation includes:

- **Data Sheets**
  - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **API Interface Document**
  - list details regarding API interface and registers.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc1000** to get access to the latest versions of those documents.

1 Summary of Features

The XMCXXXXSC devices are members of the XMC1000 Family of microcontrollers based on the ARM Cortex-M0 processor core. The XMCXXXXSC series addresses the real-time control needs of wireless power systems.

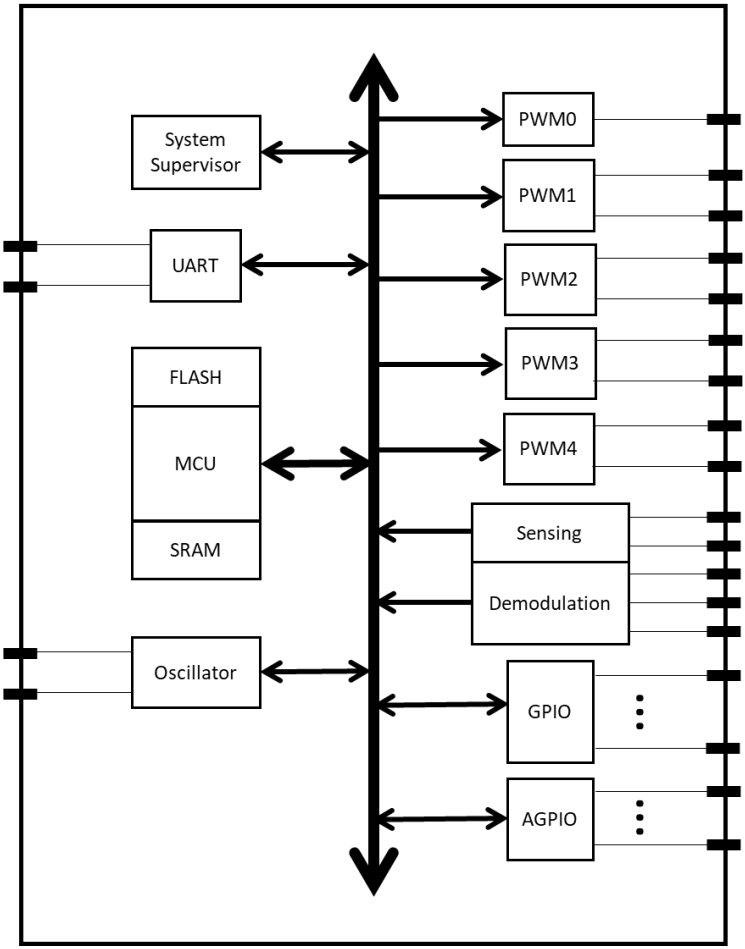

Figure 1 Block Diagram

Features

CPU subsystem

- 32-bit ARM Cortex-M0 CPU Core
- MATH coprocessor

On-Chip Memories

- SRAM (with parity)
- Flash (with ECC)

Supply, Reset and Clock

- 3.3 V or 5 V supply with power on reset and brownout detector
- On-chip clock monitor
- External crystal oscillator support (8 to 20 MHz)

System Control

- Window watchdog
- Real time clock module
- Pseudo random number generator

Communication Peripherals

- Four USIC channels, usable as
  - UART (115.2 kb/s)
  - IIC (up to 400 kb/s)

Analog Frontend Peripherals

- A/D converters for voltage and current sensing
- Temperature Sensor

Industrial Control Peripherals

- 2 PWM channels for full bridge coil driver
- 1 PWM channel for step-up or step-down bridge supply control

Up to 13 Input/Output Ports

- 3.3 V or 5 V capable

Programming Support

- Secure bootloader

Packages

- VQFN-40 (5×5 mm^2)

Tools

- Easy to use GUI for programming and debugging

1.1 Device Overview

The following table lists the available features per device type for the XMCXXXXSC series.

Table 1 Features of XMCXXXXSC Device Types

Features	
Operating temperature (ambient)	-40 to 105 °C
Operating voltage	3.3 V or 5.5 V
GPIOs	27
GPIs	8
Packages	VQFN-40

1.2 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC<DDDD>SC-<Z><PPP><T>” identifies:

- <DDDD> the derivatives function set
- <Z> the package variant
  – Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  – X: -40°C to 105°C

For ordering codes for the XMCXXXXSC please contact your sales representative or local distributor.

This document describes several derivatives of the XMCXXXXSC series, some descriptions may not apply to a specific product. Please see **Table 2**.

For simplicity the term **XMCXXXXSC** is used for all derivatives throughout this document.

1.3 Device Types

These device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 2 Synopsis of XMCXXXXSC Device Types

Derivative	Description
XMC0001SC-Q040X	Evaluation device to be programmed by the customer
XMC6521SC-Q040X	Qi single coil 15W inductive MP-A11 desktop transmitter
XMC6511SC-Q040X	Qi single coil 10W sub-surface infrastructure transmitter
XMC7501SC-Q040X	Single coil low power inductive transmitter
XMC7531SC-Q040X	Single coil 30W Telecom and Security transmitter
XMC7541SC-Q040X	Single coil 80W high power inductive transmitter
XMC8511SC-Q040X	Low power resonant multi-device transmitter
XMC8531SC-Q040X	30W resonant transmitter

2 General Device Information

This section summarizes the package pin configurations with a detailed list of the functional I/O mapping.

2.1 Pin Configuration and Definition

The following figures summarize all pins, showing their locations.

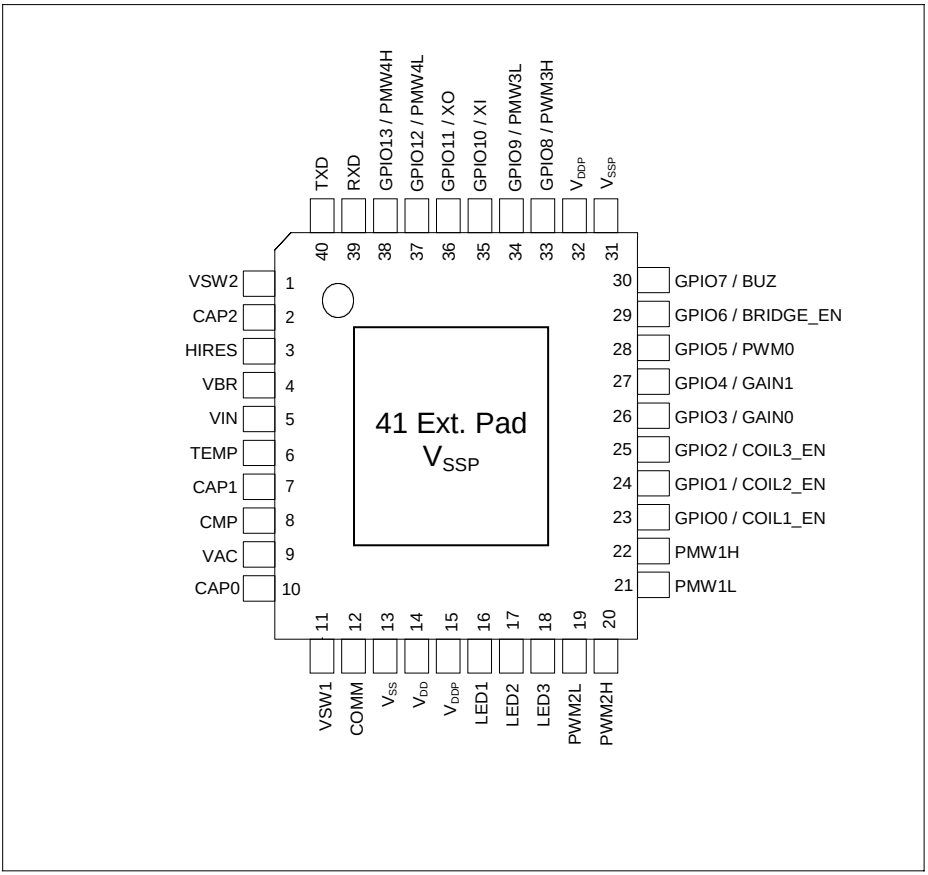

Figure 7 XMCXXXXSC PG-VQFN-40-17 Pin Configuration (top view)

2.1.1 Package Pin Summary

The following columns list the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type:

- STD_INOUT (standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- STD_INOUT/clock (standard bi-directional pads with oscillator function)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameter chapter.

Table 5 Package Pin Mapping

Function	VQFN 40	Pad Type	Notes
GPIO0	23	STD_INOUT	GPIO0 or COIL1_EN (coil #1 enable)
GPIO1	24	STD_INOUT	GPIO1 or COIL2_EN (coil #2 enable)
GPIO2	25	STD_INOUT	GPIO2 or COIL3_EN (coil #3 enable)
GPIO3	26	STD_INOUT	GPIO3 or GAIN0 (measurement gain control)
GPIO4	27	STD_INOUT	GPIO4 or GAIN1 (measurement gain control)
GPIO5	28	STD_INOUT	GPIO5 or PWM0 (bridge supply PWM)
GPIO6	29	STD_INOUT	GPIO6 or BRIDGE_EN (bridge enable)
GPIO7	30	STD_INOUT	GPIO7 or BUZ (buzzer)
GPIO8	33	STD_INOUT	GPIO8 or PWM3H (PWM channel #3)
GPIO9	34	STD_INOUT	GPIO9 or PWM3L (PWM channel #3)
GPIO10	35	STD_INOUT /clock_IN	GPIO10 or XI (crystal input)
GPIO11	36	STD_INOUT /clock_O	GPIO11 or XO (crystal output)
GPIO12	37	STD_INOUT	GPIO12 or PWM4L (PWM channel #4)
GPIO13	38	STD_INOUT	GPIO13 or PWM4H (PWM channel #4)

Table 5 Package Pin Mapping (cont'd)

Function	VQFN 40	Pad Type	Notes
RXD	39	STD_INOUT	UART receive
TXD	40	STD_INOUT	UART transmit
PWM1H	22	High Current	PWM channel #1
PWM1L	21	High Current	PWM channel #1
PWM2H	20	High Current	PWM channel #2
PWM2L	19	High Current	PWM channel #2
LED3	18	High Current	LED control
LED2	17	High Current	LED control
LED1	16	High Current	LED control
VSW2	1	STD_INOUT /AN	PWM channel #2 switch node voltage
CAP2	2	STD_INOUT /AN	High Resolution PWM capacitor
HIRES	3	STD_IN/AN	High Resolution PWM input
VBR	4	STD_IN/AN	Bridge voltage measurement
VIN	5	STD_IN/AN	Input voltage measurement
TEMP	6	STD_IN/AN	Coil thermistor (optional)
CAP1	7	STD_IN/AN	BIAS/Peak Capacitor
CMP	8	STD_IN/AN	Current sense/Peak detector

Table 5 Package Pin Mapping (cont'd)

Function	VQFN 40	Pad Type	Notes
VAC	9	STD_IN/AN	Coil AC measurement
CAP0	10	STD_IN/AN	Communication demodulator input B
VSW1	11	STD_INOUT /AN	PWM channel #1 switch node voltage
COMM	12	STD_INOUT /AN	Communication demodulator input
VSS	13	Power	Supply GND, ADC reference GND
VDD	14	Power	Supply VDD, ADC reference voltage/ ORC reference voltage
VDDP	15	Power	When VDD is supplied, VDDP has to be supplied with the same voltage.
VDDP	32	Power	I/O port supply
VSSP	31	Power	I/O port ground
VSSP	Exp. Pad	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package and Reliability chapter.

3 Electrical Parameter

This section provides the electrical parameter which are implementation-specific for the XMCXXXXSC.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMCXXXXSC and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMCXXXXSC and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMCXXXXSC is designed in.

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 11 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Junction temperature	T_J	SR	-40	–	115	°C	–
Storage temperature	T_{ST}	SR	-40	–	125	°C	–
Voltage on power supply pin with respect to V_{SSP}	V_{DDP}	SR	-0.3	–	6	V	–
Voltage on digital pins with respect to V_{SSP} [1]	V_{IN}	SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	whichever is lower
Voltage on analog input pins with respect to V_{SSP} [2]	V_{INP2}	SR	-0.3	–	V_{DDP} + 0.3	V	–
Voltage on analog input pins with respect to V_{SSP}	V_{AIN} V_{AREF}	SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	whichever is lower
Input current on any pin during overload condition	I_{IN}	SR	-10	–	10	mA	–
Absolute maximum sum of all input currents during overload condition	ΣI_{IN}	SR	-50	–	+50	mA	–

1) Excluding pins CAP2, HIRES, CAP1, CMP, VAC, CAP0, COMM.

1) Applicable to pins CAP2, HIRES, CAP1, CMP, VAC, CAP0, COMM.

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 12 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels (V_{DDP})
  - temperature

If a pin current is outside of the **Operating Conditions** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 12 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	25	mA	

Figure 11 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

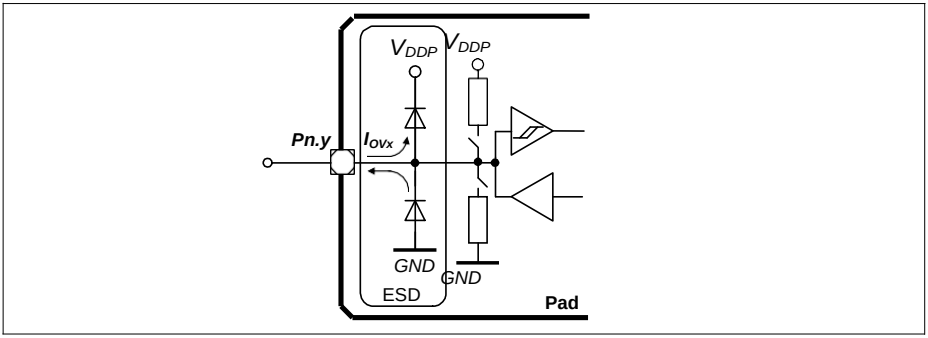

Figure 11 Input Overload Current via ESD structures

Table 13 and **Table 14** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

Table 13 PN-Junction Characteristics for positive Overload

Pad Type	I_{OV} =5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{DDP} + 0.5$ V $V_{AIN} = V_{DDP} + 0.5$ V $V_{AREF} = V_{DDP} + 0.5$ V
CAP2, HIRES, CAP1, CMP, VAC, CAP0, COMM	$V_{INP2} = V_{DDP} + 0.3$ V

Table 14 PN-Junction Characteristics for negative Overload

Pad Type	I_{OV} =5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{SS} - 0.5$ V $V_{AIN} = V_{SS} - 0.5$ V $V_{AREF} = V_{SS} - 0.5$ V
CAP2, HIRES, CAP1, CMP, VAC, CAP0, COMM	$V_{INP2} = V_{SS} - 0.3$ V

3.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMCXXXXSC. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 15 Operating Conditions Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Ambient Temperature	T_A	SR	-40	–	105	°C	Temp. Range X
Digital supply voltage[1)]	V_{DDP}	SR	3.3	–	5.5	V	
Short circuit current of digital outputs	I_{SC}	SR	-5	–	5	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D}	SR	–	–	25	mA	

1) See also the Supply Monitoring thresholds, **Chapter 3.3.2**.

3.2 DC Parameters

3.2.1 Input/Output Characteristics

Table 16 provides the characteristics of the input/output pins of the XMCXXXXSC.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.

Table 16 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Output low voltage on port pins (with standard pads)	V_{OLP} CC	–	1.0	V	I_{OL} = 11 mA (5 V) I_{OL} = 7 mA (3.3 V)
		–	0.4	V	I_{OL} = 5 mA (5 V) I_{OL} = 3.5 mA (3.3 V)
Output low voltage on high current pads	V_{OLP1} CC	–	1.0	V	I_{OL} = 50 mA (5 V) I_{OL} = 25 mA (3.3 V)
		–	0.32	V	I_{OL} = 10 mA (5 V)
		–	0.4	V	I_{OL} = 5 mA (3.3 V)
Output high voltage on port pins (with standard pads)	V_{OHP} CC	V_{DDP} - 1.0	–	V	I_{OH} = -10 mA (5 V) I_{OH} = -7 mA (3.3 V)
		V_{DDP} - 0.4	–	V	I_{OH} = -4.5 mA (5 V) I_{OH} = -2.5 mA (3.3 V)
Output high voltage on high current pads	V_{OHP1} CC	V_{DDP} - 0.32	–	V	I_{OH} = -6 mA (5 V)
		V_{DDP} - 1.0	–	V	I_{OH} = -8 mA (3.3 V)
		V_{DDP} - 0.4	–	V	I_{OH} = -4 mA (3.3 V)
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS} SR	–	0.19 × V_{DDP}	V	CMOS Mode (5 V, 3.3 V)
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS} SR	0.7 × V_{DDP}	–	V	CMOS Mode (5 V, 3.3 V)

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Input low voltage on port pins (Large Hysteresis)	V_{ILPL} SR	–	$0.08 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V)
Input high voltage on port pins (Large Hysteresis)	V_{IHPL} SR	$0.85 \times V_{DDP}$	–	V	CMOS Mode (5 V, 3.3 V)
Rise/fall time on High Current Pad[1)]	t_{HCPR}, CC t_{HCPF}	–	9	ns	50 pF @ 5 V[2)]
		–	12	ns	50 pF @ 3.3 V[3)]
Rise/fall time on Standard Pad[1)]	t_R, t_F CC	–	12	ns	50 pF @ 5 V[5)]
		–	15	ns	50 pF @ 3.3 V[6)].
Input Hysteresis on port pin except VBR, VIN, TEMP, CAP1, CMP, VAC, CAP0[8)]	HYS CC	$0.08 \times V_{DDP}$	–	V	CMOS Mode (5 V), Standard Hysteresis
		$0.03 \times V_{DDP}$	–	V	CMOS Mode (3.3 V), Standard Hysteresis
		$0.5 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode(5 V), Large Hysteresis
		$0.4 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode(3.3 V), Large Hysteresis

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input Hysteresis on port pin VBR, VIN, TEMP, CAP1, CMP, VAC, CAP0[8]	$HYS\_$ P2	CC	0.08 × V_{DDP}	–	V	CMOS Mode (5 V), Standard Hysteresis
			0.03 × V_{DDP}	–	V	CMOS Mode (3.3 V), Standard Hysteresis
			0.35 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(5 V), Large Hysteresis
			0.25 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(3.3 V), Large Hysteresis
Pin capacitance (digital inputs/outputs)	C_{IO}	CC	–	10	pF	
Pull-up current on port pins	I_{PUP}	CC	–	-80	µA	$V_{IH,min}$ (5 V)
			-95	–	µA	$V_{IL,max}$ (5 V)
			–	-50	µA	$V_{IH,min}$ (3.3 V)
			-65	–	µA	$V_{IL,max}$ (3.3 V)
Pull-down current on port pins	I_{PDP}	CC	–	40	µA	$V_{IL,max}$ (5 V)
			95	–	µA	$V_{IH,min}$ (5 V)
			–	30	µA	$V_{IL,max}$ (3.3 V)
			60	–	µA	$V_{IH,min}$ (3.3 V)
Input leakage current except GPIO11[9]	I_{OZP}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105$ °C
Input leakage current for GPIO11[9]	I_{OZP1}	CC	-10	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105$ °C
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	[10]
Maximum current per pin (excluding high current pins, V_{DDP} and V_{SS})	I_{MP}	SR	-10	11	mA	–
Maximum current per high current pins	I_{MP1A}	SR	-10	50	mA	–

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Maximum current into V_{DDP} (VQFN40)	I_{MVDD3} SR	–	260	mA	
Maximum current out of V_{SS} (VQFN40)	I_{MVSS3} SR	–	260	mA	

1) Rise/Fall time parameters are taken with 10% - 90% of supply.
2) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.150 ns/pF at 5 V supply voltage.
3) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.205 ns/pF at 3.3 V supply voltage.
4) .
5) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.225 ns/pF at 5 V supply voltage.
6) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.288 ns/pF at 3.3 V supply voltage.
7) .
8) Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
9) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.
10) However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

3.2.2 Oscillator Pins

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The oscillator pins can be operated with an external crystal/resonator (see **Figure 15**) or in direct input mode (see **Figure 16**).

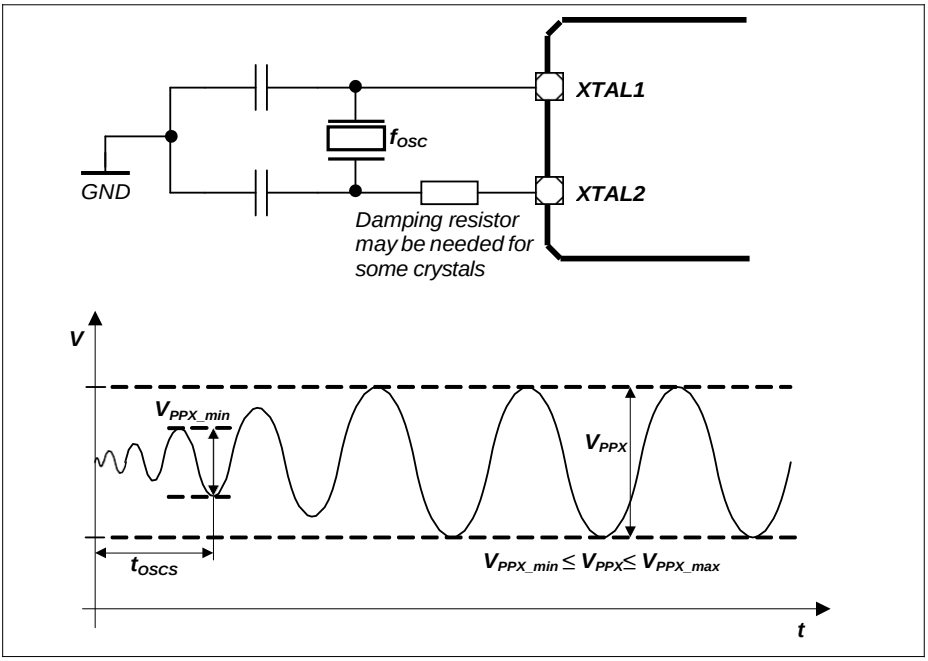

Figure 15 Oscillator in Crystal Mode

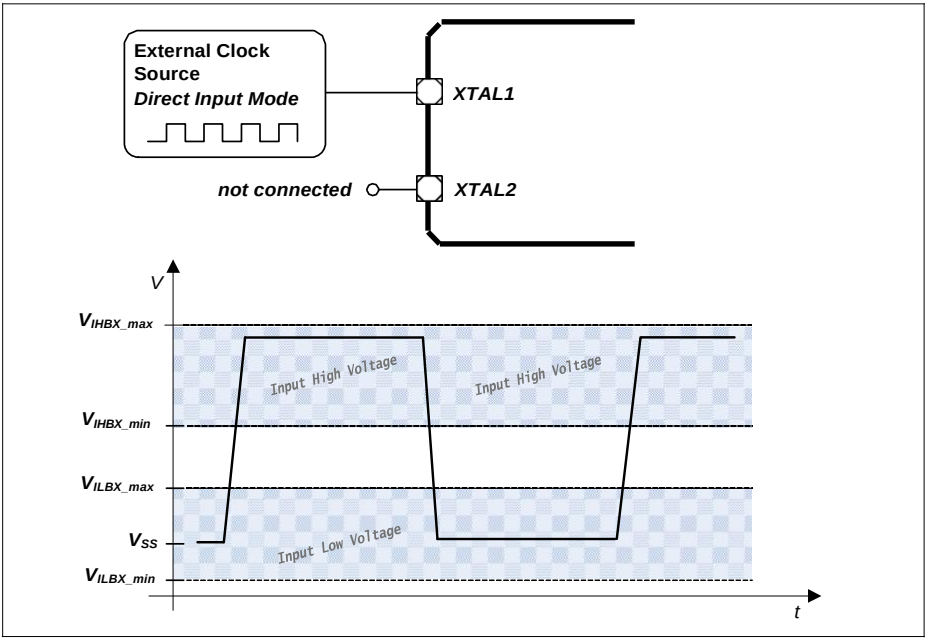

Figure 16 Oscillator in Direct Input Mode

Table 21 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	4	–	48	MHz	Direct Input Mode
		4	–	20	MHz	External Crystal Mode
Oscillator start-up time[1)2)]	t_{OSCS} CC	–	–	10	ms	
Input voltage at GPIO10	V_{IX} SR	-0.3	–	1.5	V	External Crystal Mode
		-0.3	–	5.5	V	Direct Input Mode
Input amplitude (peak-to-peak) at GPIO10[2)3)]	V_{PPX} SR	0.6	–	1.7	V	External Crystal Mode

1) t_{OSCS} is defined from the moment the oscillator is enabled wih SCU_ANAOSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of 0.9 * V_{PPX}.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) If the shaper unit is enabled and not bypassed.

3.2.3 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 23 Power Supply parameter table; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[1]	Max.		
Active mode current Peripherals enabled[2]	I_{DDPAE} CC	–	14.1	20	mA	48 / 96

Table 23 Power Supply parameter table; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[1]	Max.		
Sleep mode current Peripherals clock disabled Flash powered down[6]	I_{DDPSR} CC	–	1.1	–	mA	1 / 1
Deep Sleep mode current[7]	I_{DDPDS} CC	–	0.27	–	mA	
Wake-up time from Sleep to Active mode[8]	t_{SSA} CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode[9]	t_{DSA} CC	–	290	–	µsec	

1) The typical values are measured at T_A = + 25 °C and V_{DDP} = 5 V.

2) CPU and all peripherals clock enabled, Flash is in active mode.

3) .

4) .

5) .

6) CPU in sleep, Flash is powered down and code executed from RAM after wake-up.

7) CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.

8) CPU in sleep, Flash is in active mode during sleep mode.

9) CPU in sleep, Flash is in powered down mode during deep sleep mode.

3.3 AC Parameters

3.3.1 Testing Waveforms

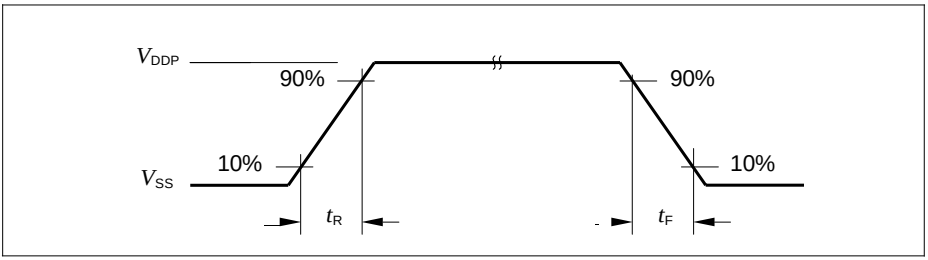

Figure 20 Rise/Fall Time Parameters

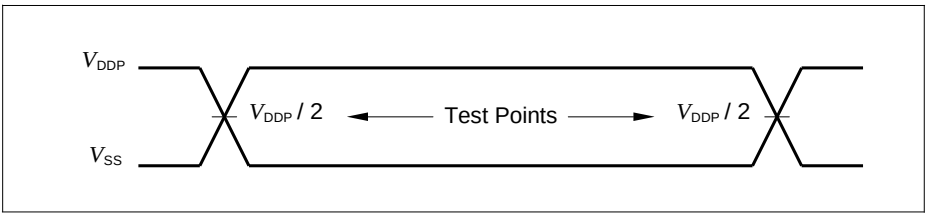

Figure 21 Testing Waveform, Output Delay

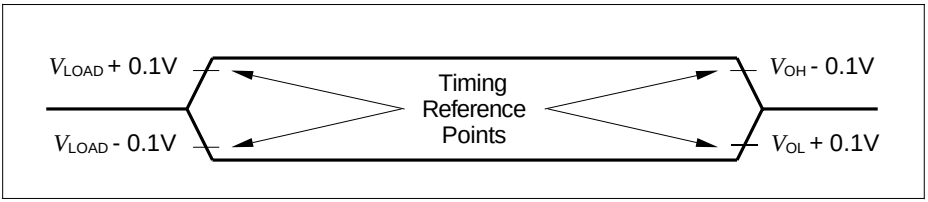

Figure 22 Testing Waveform, Output High Impedance

3.3.2 Power-Up and Supply Threshold Characteristics

Table 26 provides the characteristics of the supply threshold in XMCXXXXSC.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DDP} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 26 Power-Up and Supply Threshold Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	V_{DDP}/ $S_{VDDPrise}$	–	10^{7}	µs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	V/µs	Slope during normal operation
	S_{VDDP10} SR	0	–	10	V/µs	Slope during fast transient within +/-10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}$ [1] SR	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits[2]
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00_B

Table 26 Power-Up and Supply Threshold Parameters (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} brownout reset voltage	V_{DDPBO} CC	1.55	1.62	1.75	V	calibrated, before user code starts running
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
Start-up time from power-on reset	t_{SSW} SR	–	260	–	µs	Time to the first user code instruction[3]

1) A capacitor of at least 100 nF has to be added between V_{DDP} and V_{SSP} to fulfill the requirement as stated for this parameter.

2) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.

3) This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 48 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

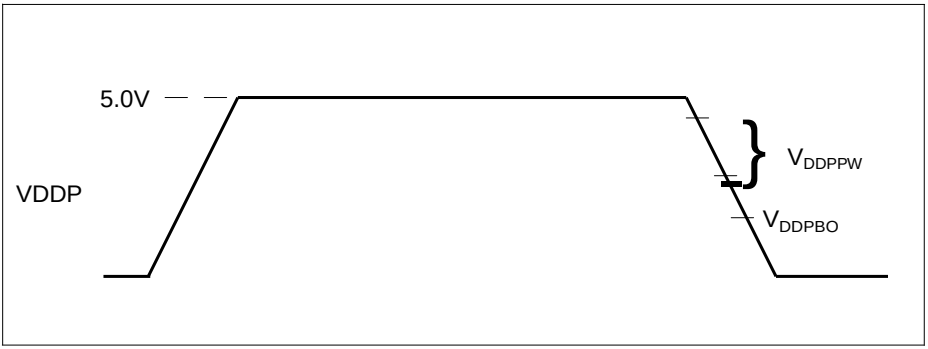

Figure 23 Supply Threshold Parameters

3.3.3 Peripheral Timings

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.3.1 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 33 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

Table 34 USIC IIC Fast Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

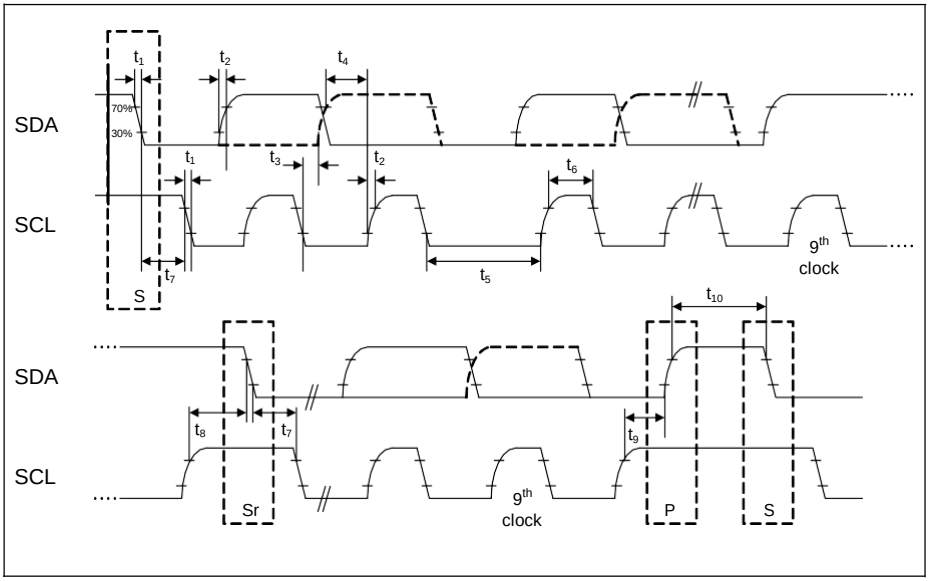

Figure 26 USIC IIC Timing

4 Package and Reliability

The XMCXXXXSC is a member of the XMC1000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 37 provides the thermal characteristics of the packages used in XMCXXXXSC.

Table 37 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	3.7 × 3.7	mm	PG-VQFN-40-17
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	45.3	K/W	PG-VQFN-40-17[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMCXXXXSC in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

The difference between junction temperature and ambient temperature is determined by $\otimes T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as

$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as

$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

4.2 Package Outlines

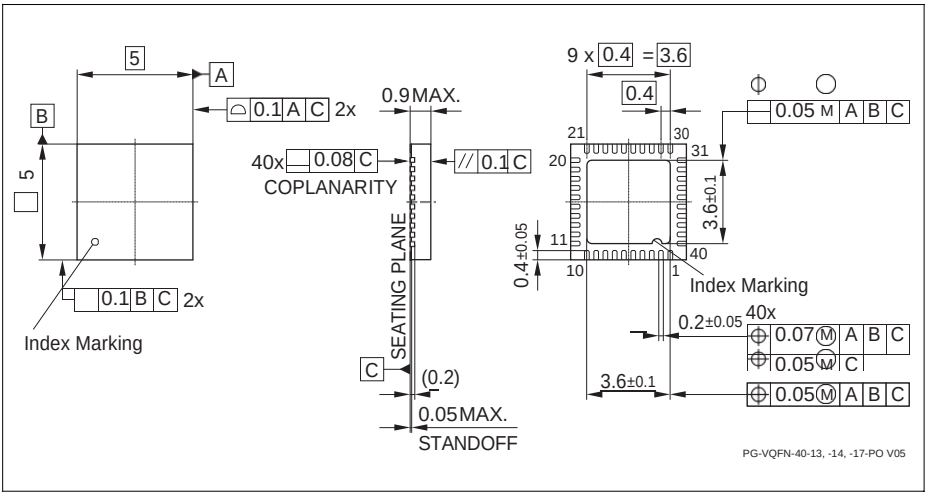

Figure 30 PG-VQFN-40-17

All dimensions in mm.

5 Quality Declaration

Table 38 shows the characteristics of the quality parameters in the XMCXXXXSC.

Table 38 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	-	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	-	3	-	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	-	260	°C	Profile according to JEDEC J-STD-020D

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