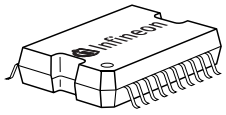
1 Overview



P-DSO-20-10, -12, -16

1.1 Features

- 5 V, 800 mA linear regulator
- Undervoltage/overvoltage reset
- Undervoltage and overvoltage logout
- Digital watchdog supervision for 2 Microcontrollers
- (motor) relay driver
- (valve) relay driver
- Inverted or non inverted lamp relay driver
- Enable output
- Overtemperature and overcurrent protection

Type	Ordering code	Package/Shipment
TLE 6210 C	on request	Bare dice
TLE 6210 G	on request	P-DSO-20-12, Tape and Reel
TLE 6211 G	on request	P-DSO-20-12, Tape and Reel

1.2 Functional Description

The TLE 6210 and TLE 6211 are integrated circuit consisting of a 5 V voltage regulator with 800 mA current capability, different relay driver outputs and supervision logic. The supervision logic watches the input voltage and the regulator output voltage both for over-voltage and under-voltage. In addition two window watchdogs supervise the correct operation of 2 independent watchdog signals, e.g. from two Microcontrollers.

The TLE 6210 and TLE 6211 are designed especially for the severe conditions of ABS/ ASR applications in an automotive environment.

1.3 Block Diagram

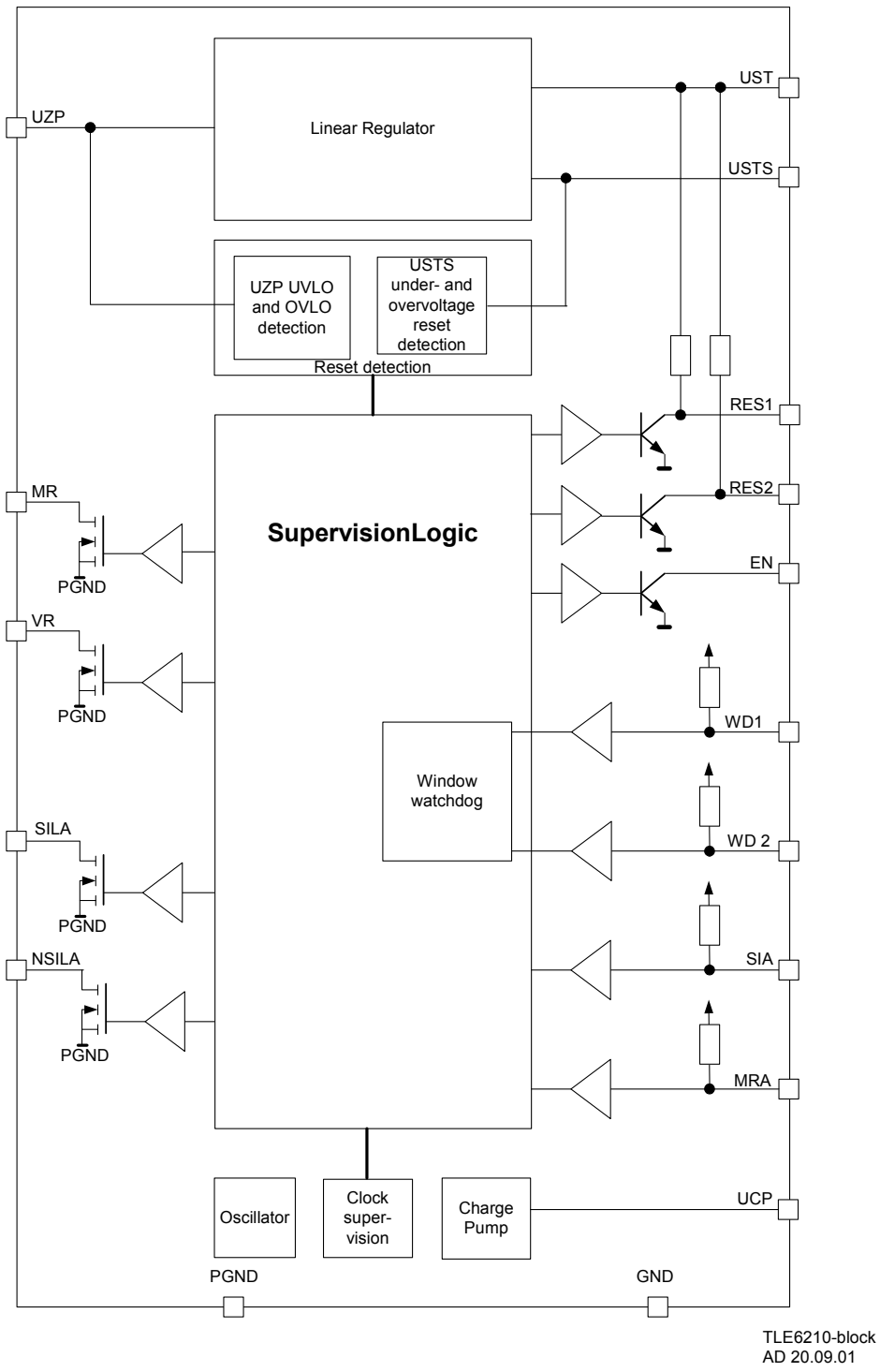


Figure 1 Block Diagram

2 Pin / Pad Configuration

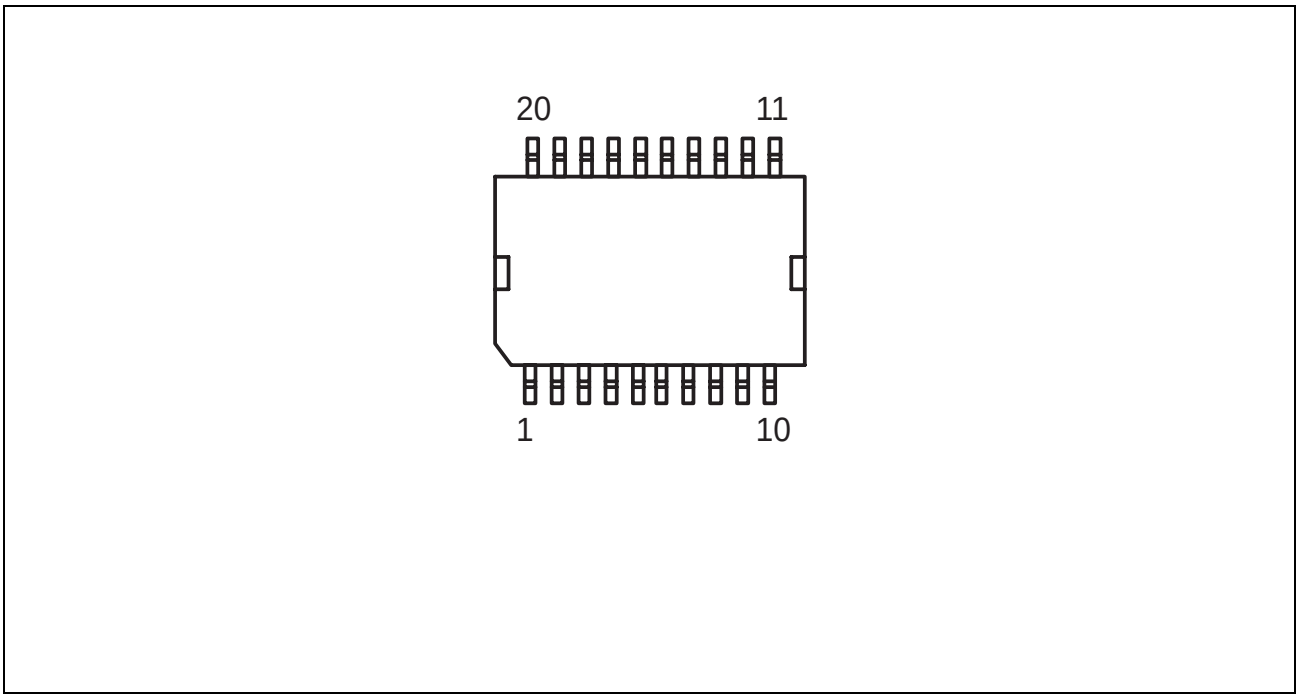


Figure 2 Pin Configuration P-DSO-20-12

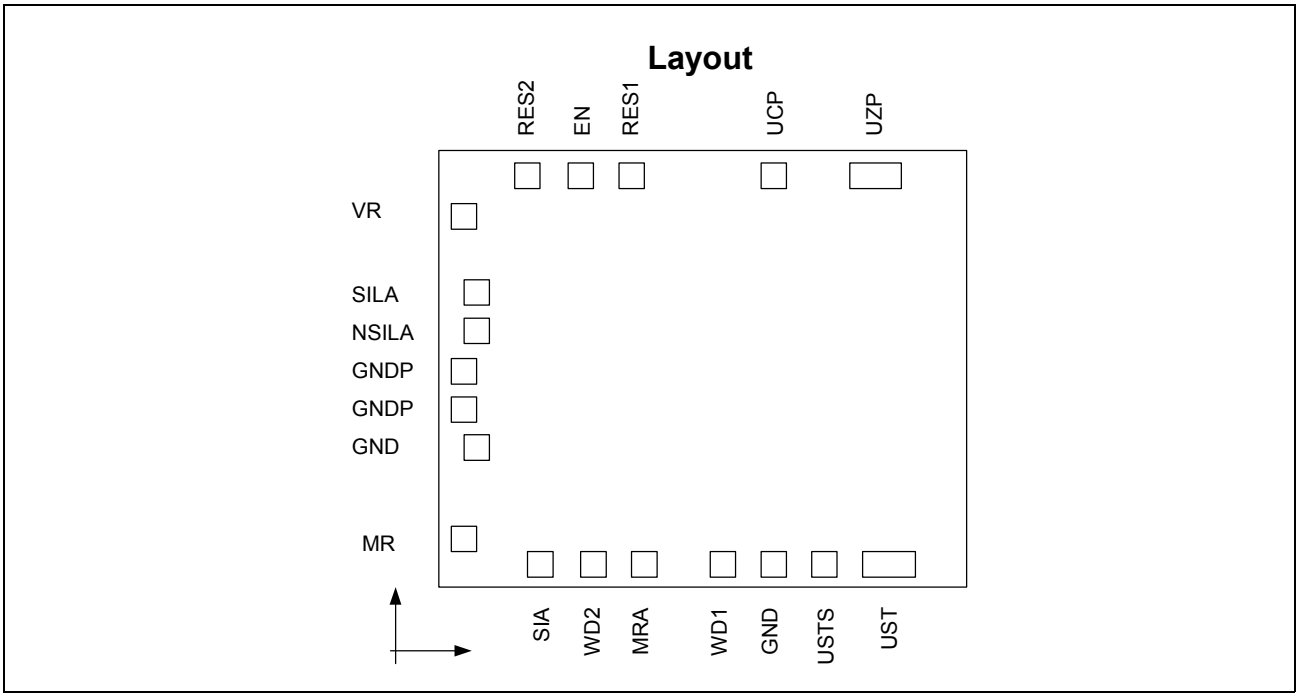


Figure 3 Chip-Layout

Pin / Pad Definitions and Functions

Pin Number		Symbol / Pad Name	Function
TLE 6210 G	TLE 6211G		
1	1	GND	**Power GND** connection
2	2	N.C.	**Not Connected**
3	3	U_{ZP}	**Supply Voltage**; reverse protection diode is required
4	4	U_{CP}	**Charge Pump Capacitor** pin; An external capacitor is the energy storage for the charge pump
5	5	RES1	**Reset Output 1**; open collector output with integrated pull-up resistor. A high indicates normal operation; function identical to RES2
6	6	EN	**Enable Output**; open collector; low indicates an error condition
7	7	RES2	**Reset Output 2**; open collector output with integrated pull-up resistor. A high indicates normal operation; function identical to RES1
8	8	VR	**Valve Relay Output**; open drain output
9	–	SILA	**Lamp Output**; open drain output; For TLE 6210 CW only
–	9	NSILA	**Inverted Lamp Output**; open drain output; For TLE 6211 CW only
10	10	GND	**Power Ground** connection
11	11	GND	**Power Ground** connection
12	12	MR	**Motor Relay Output**; open drain output
13	13	SIA	**Lamp Control Signal Input**; controls SILA/NSILA; a logic high switches SILA off and NSILA on
14	14	WD2	**Watchdog Input 2**
15	15	MRA	**Motor Relay Control Input**; A logic High switches MR on
16	16	WD1	**Watchdog Input 1**
17	17	GND	**Logic Ground**
18	18	U_{STS}	**Sense input** for U_{ST} supervision
19	19	U_{ST}	**5 V Linear Regulator Output**
20	20	GND	**Ground Connection**
Backside metallization		GND	The lead frame connects the pins 1, 10, 11 and 20 to the backside metallization.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

-40 °C ≤ T_j ≤ 150 °C

#	Parameter	Symbol	Limit Values		Unit	Conditions
			min.	max.		
M1	Supply Voltage	U_{ZP}	0	20	V	–
			0	26.5	V	0 < t_p ≤ 5 min.; -40 °C ≤ 80 °C
			0	35	V	0 < t_p ≤ 200 ms; f < 0.067 Hz; n ≤ 360 cycles
			0	35	V	0 < t_p ≤ 50 ms; 0 < f_p ≤ 1 Hz; n ≤ 36000 cycles
			-1.5	–	V	t_p = 2 s
M2	Supply Voltage variation	dU_{ZP}/dt	–	|10|	V/µs	–
M3	Output voltage at VR, MR	U_{VR}, U_{MR}	–	60	V	VR, MR-DMOS off
M4	Output voltage at SILA	U_{SILA}	–	42	V	SILA-DMOS off
M5	Output voltage at NSILA	U_{NSILA}	–	42	V	NSILA-DMOS off
M6	Output voltage at RES1, RES2	U_{RES1} U_{RES2}	-0.5	7	V	–
M7	Output voltage at EN	U_{EN}	-0.5	7	V	–
M8	Input Voltage at WD1, WD2, MRA, SIA	U_{WD1}, U_{WD2} U_{MRA}, U_{SIA}	-0.5	7	V	–
M9	Voltage U_{CP}	U_{CP}	-0.5	20	V	–
M10	Storage Temperature	T_{stg}	-55	150	°C	–
M11	Junction Temperature	T_j	-40	150 175	°C °C	continuos short term (< 50 h over lifetime)

3.1 Absolute Maximum Ratings (cont'd)

-40 °C ≤ T_j ≤ 150 °C

#	Parameter	Symbol	Limit Values		Unit	Conditions
			min.	max.		
M12	ESD	–				according to EIA/JESD 22-A 114B
			±4000	–	V	U_{ZP}, MR, EN, VR, SILA,
			±2000	–	V	all other pins
M13	Life Time	t_b	10000	–	h	ambient temperature range: -40°C 2% -20°C 10% 25°C 24% 60°C 34% 80°C 24% 100°C 5% >120°C 1%

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 Functional Range

#	Parameter	Sym-bol	Limit Values			Unit	Conditions
			min.	typ.	max.		
F1	Supply voltage	U_{ZP}	4.5	14.0	18	V	–
			–	–	26.5	V	t < 5 min.
			–	–	4.5	V	$U_{ST} \leq 0.3$ V; Reset = Low; Enable = Low; VR and MR off
F2	Input capacitor	C_{UZP}	0.33	3.3	–	µF	T_U = 20 °C U_N = 63 V Typ. = MKT
F3	Case Temperature	T_C	-40	–	125	°C	P-DSO-20-12
F4	Junction Temperature	T_j	-40 –	– –	150 175	°C °C	life time short time[1)]
F5	Thermal resistance junction-ambient	R_{thja}	–	40	–	K/W	P-DSO-20-12 minimum footprint
F6	Thermal resistance junction-case	R_{thjc}	–	–	2.4	K/W	P-DSO-20-12

1) Parameter may deviate in the temperature range T_j = 150 °C … 175 °C
Total operation time max. 50 h for temperature range T_j > 150 °C

Within the functional range the device works according to the functional description. However parameters may exceed the values given in the Characteristics.

4 Block Description and Electrical Characteristics

4.1 General

Characteristics
6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Sym-bol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.1.1	Power consumption regulator	I_{UZP}	–	7	15	mA	U_{ZP} = 16 V, I_{UST} = 800 mA, VR on, SILA on, EN, RES1, RES2 = High
4.1.2	Overtemperature protection threshold	T_{ab}	150	–	–	°C	T_j > T_{ab}

4.2 Oscillator

A 16 kHz oscillator is used as time base for the 1 kHz clock. An independent clock supervision circuit supervises the oscillator. If the oscillator clock is missing the error flag is set.

Characteristics Internal Oscillator
6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Sym-bol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.2.1	Frequency	f_{OSZ}	14.4 13.6	16 –	17.6 18.4	kHz kHZ	U_{ZP} ≥ 6 V 4.7 V ≤ U_{ZP} < 6 V
4.2.2	Clock supervision	t_{CLUE}	–	120	–	µs	error if t_{Low} or t_{High} > t_{CLUE}
4.2.3	Logic time base	t_{CLK}	0.9	1	1.1	ms	Period

4.3 Charge Pump

The integrated charge pump requires an external capacitor at pin U_{CP}. The charge pump voltage is typically 15 V. It is internally used for the voltage regulator only. It is only intended for internal function and may not be used for any external loads. The output voltage is short circuit protected against the supply voltage.

Characteristics Charge Pump

6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Sym-bol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.3.1	Power up time	t_{CP}	–	10	–	ms	U_{ZP} = 6 V; C_{CP} = 68 nF; Load capacitor to U = 0.9 × U_{CPmax}
4.3.2	Charge pump voltage	U_{CP}	–	15	22	V	Regulator on
4.3.3	Frequency	f_{CP}	1.4	3.2	–	MHz	–

4.4 Voltage Regulator

The 5 V low drop linear regulator can supply up to 800 mA current. The regulator requires an output capacitor. The linear regulator is equipped with overcurrent protection and its own overtemperature protection. The linear element consists of 2 anti-serial DMOS transistors. In case of low input supply voltage this avoids discharging of the output capacitor.

The output voltage U_{ST} is supervised for over- and undervoltage. U_{ST} output has to be connected externally to the sense input U_{STS}. If over- or undervoltage condition is detected the Reset outputs RES1 and RES2 are logical low. For a detailed description of the reset logic please see **Chapter 4.9**.

Characteristics Voltage Regulator

6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Sym-bol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.4.1	Nominal output voltage	U_{ST}	 4.95 4.925	 5.00 5.00	 5.05 5.075	 V V	U_{ZP} = 14 V; I_{ST} = 400 mA; Output capacitor as defined in **4.4.11**; on wafer level T_j = 25 °C P-DSO-20-12
4.4.2	U_{ST} load current	I_{ST}	–	–	800	mA	–
4.4.3	Line variation	ΔU_{ST}	–	–	|50|	mV	T_j **= 25 °C**; 6.0 V ≤ U_{ZP} ≤ 18 V; I_{ST} = 600 mA; capacitor as defined in **4.4.11**; dU_Z/dt < 1 V/µs

Characteristics Voltage Regulator (cont'd)
6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Sym-bol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.4.4	Load variation	ΔU_{ST}	–	–	|50|	mV	**T_j = 25 °C**; U_{ZP} = 14 V; 0 mA ≤ I_{ST} ≤ 800 mA; capacitor as defined in **4.4.11**; dI_{ST}/dt ≤ 1 mA/µs
4.4.5	Temperature variation	ΔU_{ST}	–	|50|	|100|	mV	U_{ZP} = 14 V; I_{ST} = I_{STmax}; -40 °C ≤ T_j ≤ 150 °C; capacitor as defined in **4.4.11**; for die mounted in a hybrid: dT_U/dt ≤ 10 K/s for P-DSO-20-12: dT_G/dt ≤ 5 K/min.
4.4.6	Long time drift	ΔU_{ST}	–	–	|50|	mV	U_{ZP} ≤ $U_{ZPmax.}$; 0 mA ≤ I_{ST} ≤ $I_{STmax.}$; -40 °C ≤ T_j ≤ 150 °C; t_b = 10000 h, see conditions M13.
4.4.7	Overall output voltage tolerance	U_{ST}	4.75	5.00	5.25	V	all parameters from **4.4.1** to **4.4.6**
4.4.8	Power Supply ripple rejection	ΔU_{STss}	–	–	|25|	mV	0 Hz ≤ f_{UST} ≤ 10 kHz; capacitor as defined in **4.4.11**; 7 V ≤ U_{ZP} ≤ 24 V
4.4.9	Series Resistor	R_{DSon}	– –	– –	1.7 2.7	Ω Ω	T_j = 25 °C T_j = 150 °C U_{CP} > 15 V; U_{ZP} = 6 V; I_{ST} = 800 mA
4.4.10	Maximum output current (output shorted)	I_K	0.8	–	1.6	A	U_{CP} > 15 V; U_{ST} = 0 V; 4.5 V ≤ U_{ZP} ≤ 18 V
4.4.11	Load capacitor at output U_{ST}	C_{UST}	3.3	–	150	µF	T_U = 20 °C; U_N = 25 V; Type ETQW Roederstein
		Z	–	4	–	Ω	f = 100 kHz; T_U = 20 °C
4.4.12	U_{ST} off voltage	U_{STRest}	–	–	400	mV	I_{ST} = 0 mA
4.4.13	Clamping voltage	U_{ZST}	5.5	–	7	V	clamping voltage at I = 100 mA

4.5 Enable-Output EN

The open collector enable output EN informs the system about any error condition. Any error except a detected supply under-voltage will set the EN output Low. Of cause for long under-voltage at the supply line, soon the U_{ST} output capacitor will be discharged and this will cause U_{ST} under-voltage and therefore EN Low. The time depends on the load and the output capacitor. The EN is an open collector output. It is short circuit protected to U_{ST}.

After power up when the first watchdog edges at WD1 a WD2 are detected the Enable output is switched into High state.

Characteristics EN Output

6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.5.1	Output Low voltage	U_L	– –	– –	0.4 0.2	V V	I_L ≤ 10 mA I_L ≤ 1 mA
4.5.2	Reverse current	I_R	–	–	5	µA	U_{EN} = 5 V

Power Driver

The TLE 6210/TLE 6211 includes 3 open drain outputs for loads up to 0.5 A: The two drivers VR and MR are intended for (valve and motor) relays, while the SILA/NSILA output is designed for a lamp.

In the TLE 6210 GW the SILA output is available. The output goes low if the supply voltage U_{ZP} is no longer available – the DMOS is switched on automatically. In the TLE 6211 GW the NSILA has the inverted polarity related to SILA. In bare dice both outputs SILA and NSILA can be used.

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4.6 Valve Relay Output VR

The valve relay output VR is switched On after the power up reset and valid watchdog signals. The driver has an open drain configuration and can supply up to 500 mA. The output is protected against overtemperature and overcurrent. The output is short circuit protected to U_Z. The output stage is equipped with its own overtemperature protection. In case of overvoltage at the supply U_{ZP} the output is switched off. However the output is not protected against overvoltages caused by switching inductive loads. Therefore externally a free wheeling diode is required as shown in the application diagram.

The valve relay output VR is controlled by the internal supervision logic. If any watchdog errors or supply over-voltage is detected or the 5 V regulator is out of range, the VR is switched off (please see also **Table 1** on **Page 19** and **Table 2** on **Page 28**).

Characteristics Relay Driver Output VR

6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Sym-bol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.6.1	Saturation Voltage	U_{DS}	–	–	1.2	V	R_{last} ≥ 35 Ω; I_L ≤ 0.5 A; 6 V ≤ U_{ZP} ≤ 16 V
4.6.2	On state resistance	R_{DSon}	–	–	2.4	Ω	T_j = 150 °C; I_L = 0.5 A; U_{ZP} = 6 V
4.6.3	Overload detection current	I_K	500	–	–	mA	–
4.6.4	Output leakage current	I_R	– –	– –	0.5 2	mA mA	U_A ≤ 16 V 16 V < U_A ≤ 60 V
4.6.5	Overtemperature shutdown threshold	T_K	150	–	–	°C	–

4.7 Motor Relay Driver

The motor relay driver MR is controlled by the MRA input signal and the internal control logic. A logic High at the MRA input switches the MR low side switch on, a logic Low signal switches it off. However the supervision logic overrules the MRA input condition. Please see also **Table 1** on **Page 19** and **Table 2** on **Page 28**.

The output is an open collector output and can sink up to 500 mA. It is protected against overtemperature and overcurrent and short circuit prove to U_Z. Even the output is switched off by the supervision logic at U_{ZP} overvoltage externally a free wheeling diode is required to protect the output against switching off inductive loads.

Characteristics Relay Driver Output MR

6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Sym-bol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.7.1	Saturation Voltage	U_{DS}	–	–	1.2	V	R_{last} ≥ 35 Ω; I_L ≤ 0.5 A; 6 V ≤ U_{ZP} ≤ 16 V
4.7.2	On state resistance	R_{DSon}	–	–	2.4	Ω	T_j = 150 °C; I_L = 0.5 A; U_{ZP} = 6 V
4.7.3	Overload detection current	I_K	500	–	–	mA	–
4.7.4	Output leakage current	I_R	– –	– –	0.5 2	mA mA	U_A ≤ 16 V 16 V < U_A ≤ 60 V
4.7.5	Overtemperature shutdown threshold	T_K	150	–	–	°C	–

4.7.1 Control Input MRA

The logic inputs MRA expect TTL-type signals from a µ-controller with 5 V I/Os. An integrated pull-up resistor ensures that an open input is read High.

Characteristics Control Inputs MRA

6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Sym-bol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.7.6	Internal pull-up resistor to U_{ST}	R_{WD}	10	20	40	kΩ	0 V ≤ U_E ≤ U_{ST} + 0.3 V
4.7.7	Input voltage Low	U_L	-0.3	–	1.0	V	–
4.7.8	Input voltage High	U_H	2.0	–	U_{ST} + 1.0	V	–
4.7.9	Input current	I_H	–	–	|5|	µA	U_E = U_{ST}
			–	–	1.0	mA	U_{ST} < U_E ≤ U_{ST} + 1 V

4.8 Error Lamp Output SILA and Lamp Relay Output NSILA

The SILA output is a 300 mA open collector output. It is available in the TLE 6210 G. SILA is a self-on output: It is switched on if the supply voltage is missing. The TLE 6211 G is equipped with the logically inverted NSILA output. NSILA is a 30 mA open collector output. It is intended to drive the lamp relay. In the dice version TLE 6211 C both outputs can be used.

Both SILA and NSILA are intended to control a warning lamp. The output is controlled by the internal supervision logic and control signal at the SIA pin.

A logic High at the SIA input switches SILA off and NSILA on.

The supervision logic will switch on SILA if a watchdog timing violation is detected or the output voltage U_{ST} is out of range. **Table 1** on **Page 19** and **Table 2** on **Page 28** give an overview on the different errors.

The SILA output is equipped with its own overtemperature protection.

Characteristics Lamp Driver Output SILA

6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Sym-bol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.8.1	Saturation voltage	U_{SILA}	– –	– –	2.5 2.5	V	I = 300 mA; U_{ZP} ≥ 6 V I = 300 mA; U_{ZP} = 0 V
4.8.2	Overload detection current	I_K	300	–	–	mA	–
4.8.3	Output leakage current	I_R	– –	– –	0.1 4	mA mA	U_{SILA} ≤ 16 V 16 V < U_{SILA} < 42 V
4.8.4	Threshold voltage for automatic ON	U_{ZP}	1	–	4.7	V	U_{SILA} ≤ 2.5 V; I = 300 mA
4.8.5	Overtemperature shutdown threshold	T_K	150	–	–	°C	U_{ZP} ≥ 6 V

Characteristics Lamp-Relay Driver Output NSILA

6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Sym-bol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.8.6	On state resistance	R_{DSon}	–	–	33	Ω	T_j = 150 °C; I = 30 mA; U_{ZP} ≥ 7 V
4.8.7	Overload detection current	I_K	30	–	–	mA	–
4.8.8	Output leakage current	I_R	–	–	10	µA	U_{NSILA} ≤ 42 V

4.8.1 Control Input SIA

The logic inputs SIA expect TTL-type signals from a µ-controller with 5 V I/Os. An integrated pull-up resistor ensures that an open input is read High.

Characteristics Control Inputs SIA

6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Sym-bol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.8.9	Internal pull-up resistor to U_{ST}	R_{WD}	10	20	40	kΩ	0 V ≤ U_E ≤ U_{ST} + 0.3 V
4.8.10	Input voltage Low	U_L	-0.3	–	1.0	V	–
4.8.11	Input voltage High	U_H	2.0	–	U_{ST} + 1.0	V	–
4.8.12	Input current	I_H	–	–	|5|	µA	U_E = U_{ST}
			–	–	1.0	mA	U_{ST} < U_E ≤ U_{ST} + 1 V

Supervision

The TLE 6210 and TLE 6211 are equipped with a complex supervision logic. The input voltage and the regulator output voltage is supervised. In addition two µ-controller are supervised by independent watchdog circuits.

4.9 Overvoltage and Undervoltage

Both the supply voltage U_{ZP} and the output voltage U_{ST} are supervised for over- and undervoltage.

In case any undervoltage or overvoltage condition at U_{ST} or U_{ZP} is detected, the reset outputs RES1 and RES2 are switched to low state. RES1 and RES2 are not controlled by the watchdog logic.

To supervise the output voltage U_{ST} an independent bandgap from the reference bandgap is used.

The reset outputs RES1 and RES2 are together controlled by the U_{ST} reset logic and the supply undervoltage lockout (UVLO) and overvoltage lockout (OVLO).

A logic High at the RES1 and RES2 indicates normal operation. The outputs are open collector type outputs with integrated pull-up resistors to U_{ST}. Even when the U_{ST} voltage drops, the reset outputs RES1 and RES2 remain low (< 0.4 V).

Both undervoltage and overvoltage detection of U_{ST} and U_{ZP} use a voltage hysteresis to avoid any reset toggling.

Undervoltage and Overvoltage Detection U_{ST}

The U_{ST} output voltage has to be externally connected to the U_{STS} sense input.

To be able to detect also wrong output voltages causes by a malfunction of the related bandgap reference for supervision an independent bandgap is used.

As soon as any reset condition is detected the RES1 and RES2 go low.

4.9.1 Undervoltage Lockout (UVLO) and Overvoltage Lockout (OVLO)

The supply voltage U_{ZP} is supervised as well. If the voltage rises above the upper threshold value of 19.5 V reset is asserted. When an undervoltage occurs, after some time the output voltage will drop below the reset threshold and a reset is asserted. The undervoltage lockout is only valid during power up.

Both the OVLO and the UVLO threshold use a hysteresis to avoid reset glitches. In addition the OVLO is digitally filtered. Overvoltage below 2 to 3 clock cycles (equals typical 2 µs or 3 µs) are neglected to avoid resetting the system when any inductive load is switched off.

When the undervoltage condition at U_{ST} or U_{ZP} is no longer detected a reset reaction time of typical 52 ms (52 clock cycles) is started. After this time the reset signal is set high.

Table 1 Truth Table Overvoltage and Undervoltage Supervision

The table assumes that no other error is detected, especially no watchdog failure and no clock failure.

Supply voltage U_{ZP}	**Regulator Voltage U_{ST}**	**SILA**	**NSILA**	**MR**	**VR**	**EN**	**RES 1 RES 2**	**Regulator**
ok	ok	= SIA	= not SIA	= not MRA	L	Z	H	ON
ok	under-voltage	L	Z	Z	Z	L	L	ON
normal	over-voltage	L	Z	Z	Z	L	H	ON
under-voltage	under-voltage	L	Z	Z	Z	Z*	L	OFF
under-voltage	ok	= SIA	= not SIA	not MRA	L	H	H	ON
over-voltage	x	= L	Z	Z	Z	Z*	L	OFF

Z: high impedance

* In the application the voltage is undefined as regulator is off

4.9.2 Under- and Overvoltage Reset Behavior

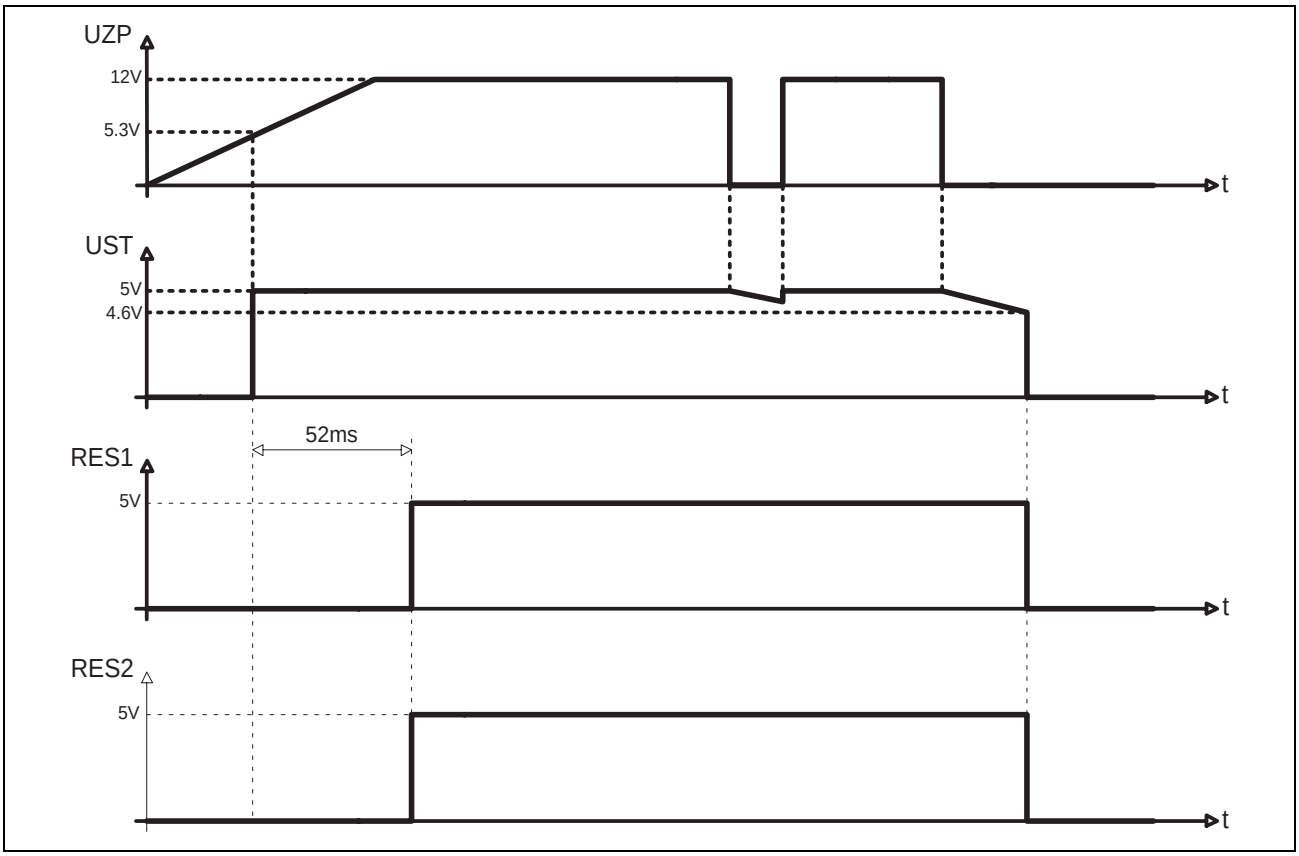


Figure 4

Characteristics Supervision of U_{ZP}, U_{ST}

6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
U_{ZP}-Undervoltage							
4.9.1	U_{ZP} undervoltage threshold	U_{ZPU}	5.2	5.3	5.4	V	U_{ST} off
4.9.2	U_{ZP} undervoltage hysteresis	U_H	20	–	50	mV	$U_{ZPU(ON)}$ = $U_{ZPU(OFF)}$ + U_H [1)]
U_{ZP}-Overvoltage							
4.9.3	U_{ZP} overvoltage threshold	U_{ZUE}	18.75	19.5	20.25	V	Outputs NSILA, VR, MR, U_{ST} off

Characteristics Supervision of U_{ZP}, U_{ST} (cont'd)
6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.9.4	U_{ZP} overvoltage hysteresis	U_H	0.5	–	1.0	V	U_H = $U_{ZUE(on)}$ - $U_{ZUE(off)}$
4.9.5	U_{ZP} overvoltage filter	t_{on}	2 1.8	– –	3 3.4	× t_{CLK} ms	U_{ZP} ≥ overvoltage threshold
		t_{off}	2 1.8	– –	3 3.4	× t_{CLK} ms	U_{ZP} < overvoltage threshold
U_{ST}-Undervoltage							
4.9.6	U_{ST} undervoltage threshold	U_{STU}	4.5	4.6	4.7	V	RES1, RES2 = low
4.9.7	U_{ST} undervoltage hysteresis	U_H	20	–	50	mV	$U_{STU(on)}$ = $U_{STU(off)}$ + U_H [1]
U_{ST}-Overvoltage							
4.9.8	U_{ST} overvoltage threshold	U_{STUE}	5.3	5.4	5.5	V	Error flag is set
4.9.9	U_{ST} overvoltage hysteresis	U_H	20	–	50	mV	$U_{STUE(ON)}$ = $U_{STUE\ (off)}$ - U_H [1]
4.9.10	U_{STS} input current	I_{STS}	0.94	1.5	2.2	mA	U_{STS} = 6 V
Reset timing							
4.9.11	Reset delay time	t_{RH}	– 46.35	52 52	– 58.85	× t_{CLK} ms	U_{ZP} ≥ 5.4 V U_{ST} ≥ 4.75 V

[1] Hysteresis guaranteed by design.

4.10 Reset Outputs RES1, RES2

The two reset outputs RES1 and RES2 are open collector outputs with integrated pull-up resistor of typical 10 kΩ to U_{ST}. Both outputs are protected against short circuits to U_{ST}.

Characteristics RES1 and RES2

6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.10.1	Output low voltage	U_L	– –	– –	0.4 0.4	V V	I_L = 0.8 mA; U_{ST} = 1.8 V I_L = 2 mA; U_{ST} = 4.5 V 1.8 V ≤ U_{ST} ≤ 4.5 V
4.10.2	Output high voltage	U_H	U_{ST} - 0.1	–	U_{ST}	V	R_L ≥ 10 MΩ
4.10.3	Internal pull-up resistor to U_{ST}	R_{RES}	5	10	20	kΩ	0 V ≤ U_A ≤ U_{ST} + 0.3 V

4.11 Watchdog

To supervise the operation of 2 µ-processors watchdog logic for two input signals is integrated. The logic expects at each WD1 and WD2 rectangular signals with 10 ms high and 10 ms low time. Deviations from the expected time are counted as errors and influence the output signals.

A digital filter suppresses noise or pulses below 3 clock cycles (typ. 3 ms).

The detection ciruit is described in **Figure 12**.

After power up and 1or 2 valid watchdog edges the WD logic enables the output Drivers.

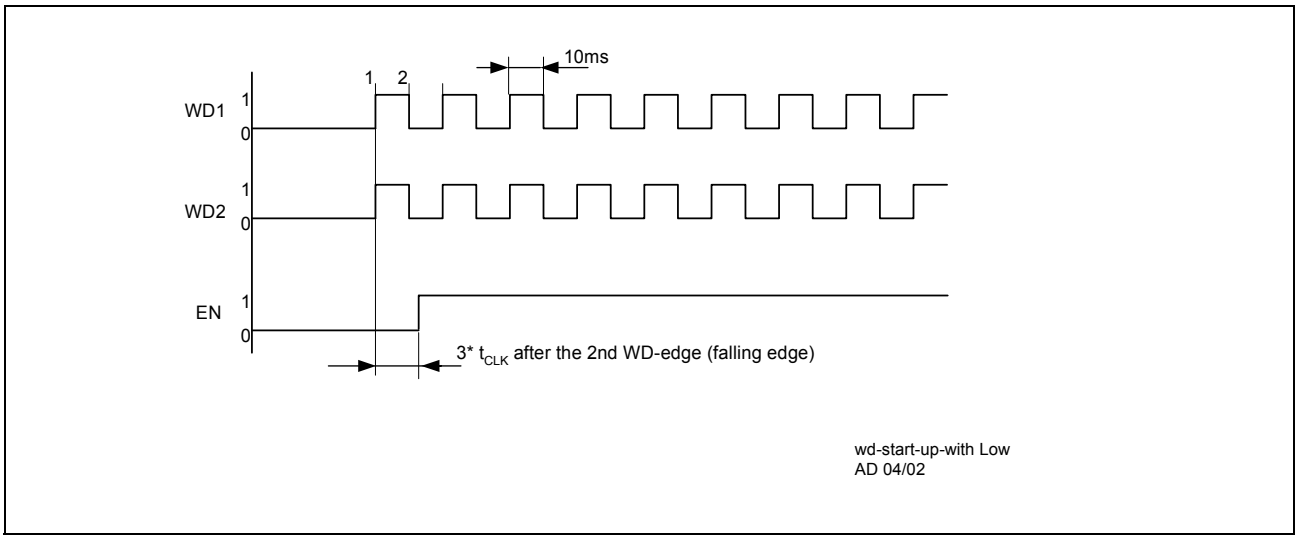


Figure 5 Enable output EN after correct watchdog signals at WD1 and WD2 are present; WD1 and WD2 start with logic Low

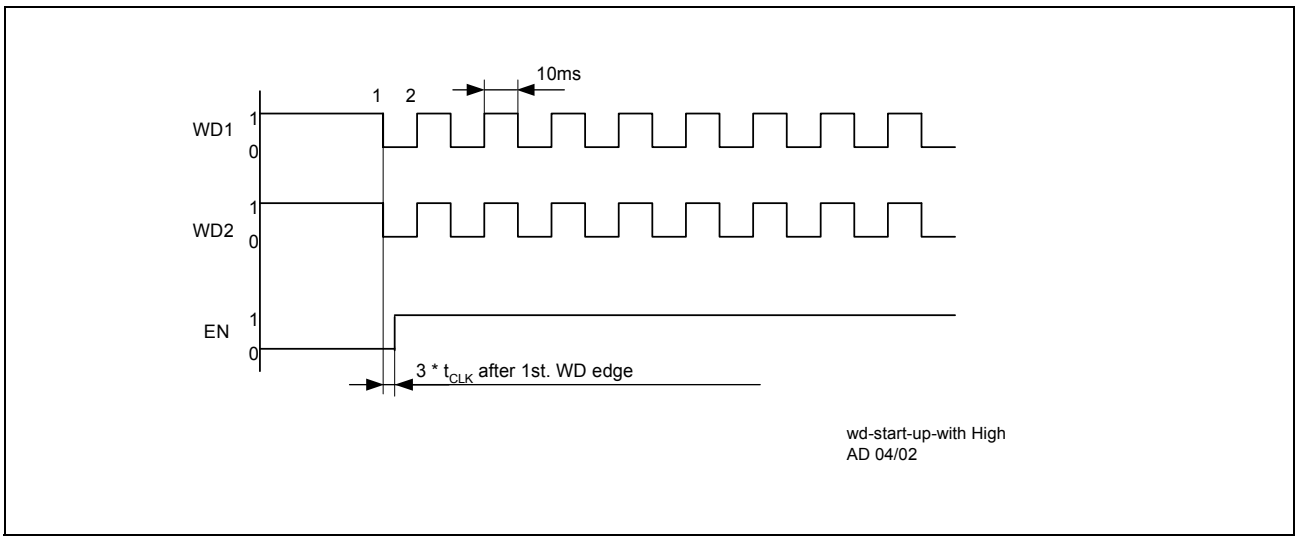


Figure 6 Enable output EN after correct watchdog signals at WD1 and WD2 are present; WD1 and WD2 start with logic High

The logic expects the time between two clock edges between 3 and 15 clock-cycles. If this window is not met, the outputs VR, MR and NSILA are switched off, SILA is switched on and the enable output goes low.

An internal counter (see**Figure 12**) includes a 4 bit counter. Each time the value 15 is reached a dominant counter reset signal is generated at the output "=15". This pulse is generated continuously at

$t = (15+3)\ T1 + n * (16*T1)$

after the last valid watchdog pulse was detected.

When internal resets and watchdog edges occur at the same time, the internal reset is dominant.

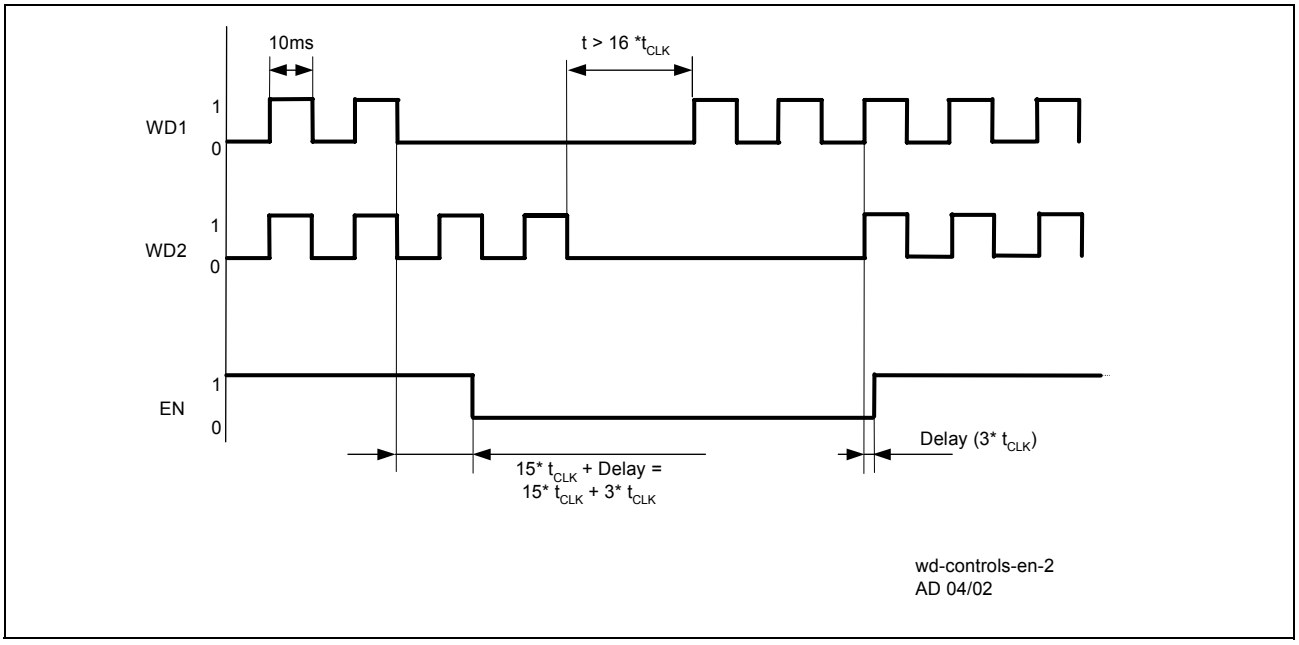


Figure 7 Missing watchdog signals cause EN low

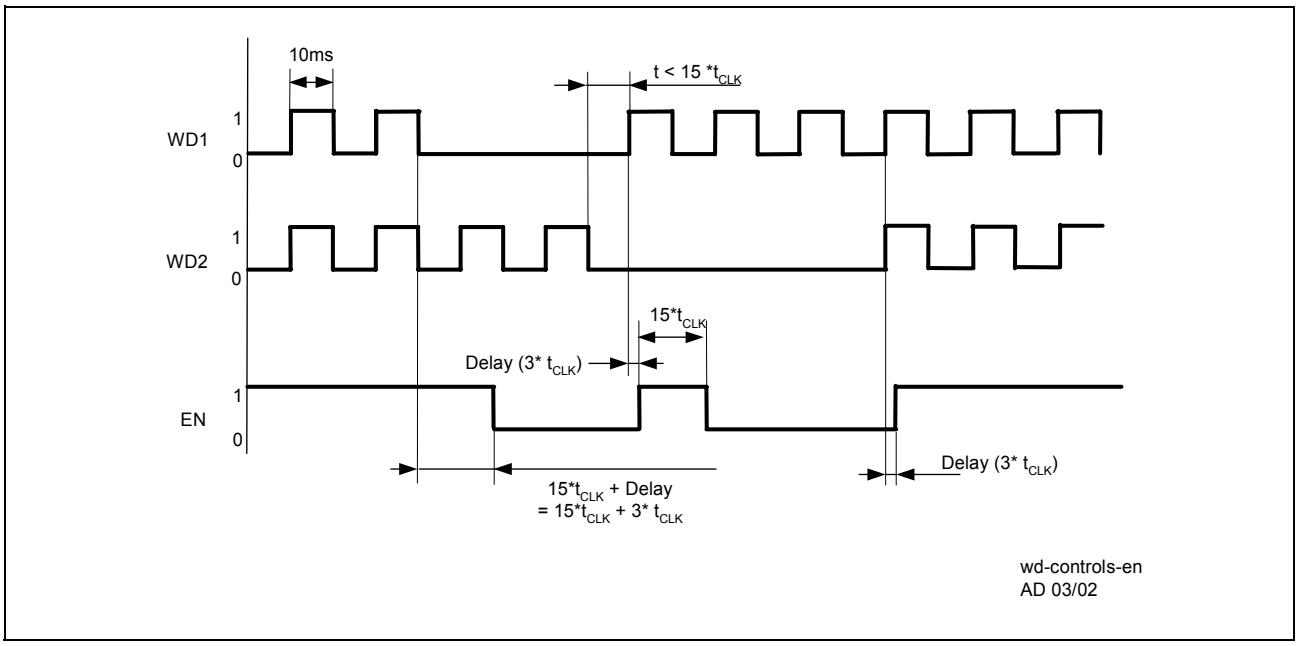


Figure 8 Missing watchdog signals cause EN low

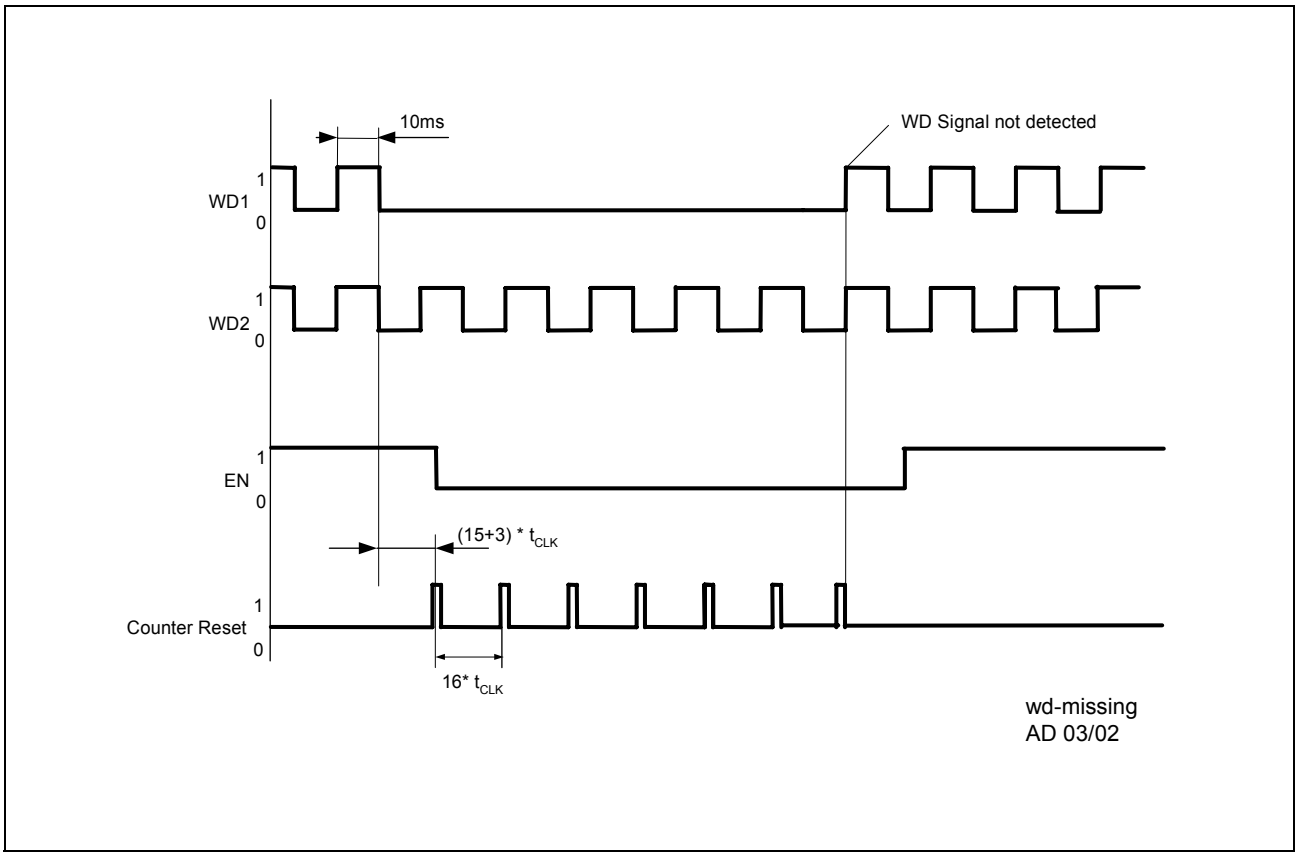


Figure 9 Timing diagram - any watchdog signal missing causes a High signal at the output "=15" (Counter reset). This signal sets back the logic

Any watchdog high or low time above 15 ms influences the enable (EN) and the VR output.If the time after the last watchdog edge exceeds 120 clock cycles - typical 120 ms- an error flag is set. This flag can only be removed by powering down the IC.

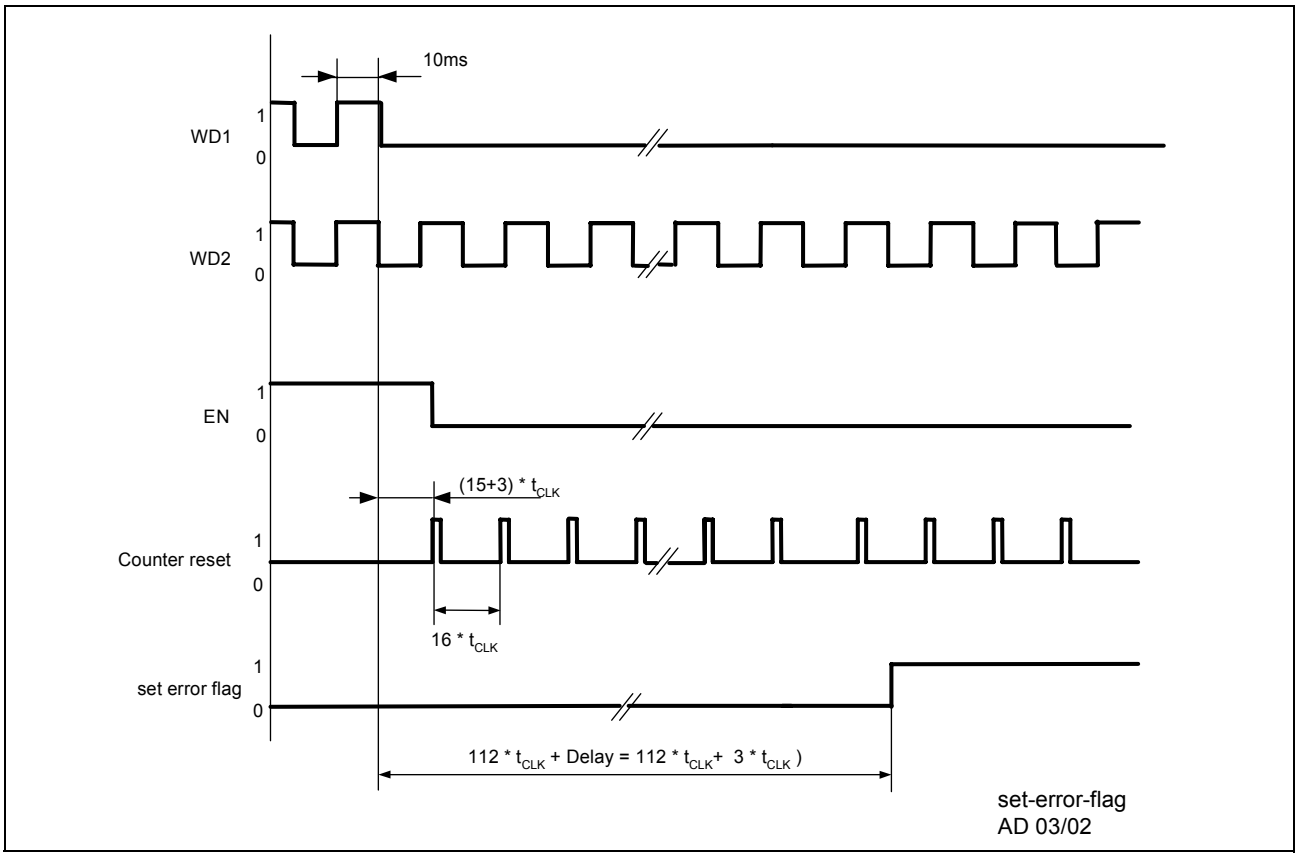


Figure 10 Missing watchdog signals for more than 120 * t_{CLK} (typ. 120ms) sets the failure register

An integrated pull-up resistor to U_{ST} in the WD1 and WD2 inputs ensures to detect a permanent logic High in case the input is open.

Characteristics WD1, WD2

6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Sym-bol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.11.1	Internal pullup resistor to U_{ST}	R_{WD}	10	20	40	kΩ	0 V ≤ U_E ≤ U_{ST} + 0.3 V
4.11.2	Input voltage Low	U_L	-0.3	–	1.0	V	–
4.11.3	Input voltage High	U_H	2.0	–	U_{ST} + 1.0	V	–
4.11.4	Input current	I_H	–	–	|5|	µA	U_E = U_{ST}
			–	–	1.0	mA	U_{ST} < U_E ≤ U_{ST} + 1 V

Characteristics Watchdog

6 V ≤ U_{ZP} ≤ 18 V, -40 °C ≤ T_j ≤ +150 °C, if not otherwise specified

#	Parameter	Sym-bol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.11.5	Release reaction time	t_{ON}	1	–	2	× t_{CLK}	Number of valid Watchdog input clock edges
4.11.6	Closed window time	t_{pulse}	– 2.25 1.8	3 3 3	– 3.3 3.3	× t_{CLK} ms ms	The distance between clock edges is at least t_{pulse} equals: periodically pulse
4.11.7	Open window time	t_{VR}	– 13.5	15 15	– 17.6	× t_{CLK} ms	if the edge distance $\Delta t > t_{VR}$, VR is switched off equals
4.11.8	Error flag detection	t_{FSP}	– 108	120 120	– 132	× t_{CLK} ms	if $\Delta t > t_{FSP}$, the error flag is set. equals

4.11.1 Watchdog Logic

Table 2 and Figure 11 show the watchdog logic. figure 12 shows the logic implementation

Watchdog WD1, WD2 Time between Edges	Clock	SILA	NSILA	MR	VR	EN	RES1/2	Error Flag
ok	ok	= SIA	= not SIA	= not MRA	L	Z	H	L
< 3 * t_{CLK}	ok	L	Z	Z	Z	L	H	L
> 15 * t_{CLK}	ok	L	Z	Z	Z	L	H	L
> 120 * t_{CLK}	ok	L	Z	Z	Z	L	H	H
ok	error	L	Z	Z	Z	L	H	H

Table 2 Watchdog and Clock Supervision Truth Table

The table assumes that no other error is detected, especially no undervoltage or overvoltage at the supply and regulator output.

Z: High impedance

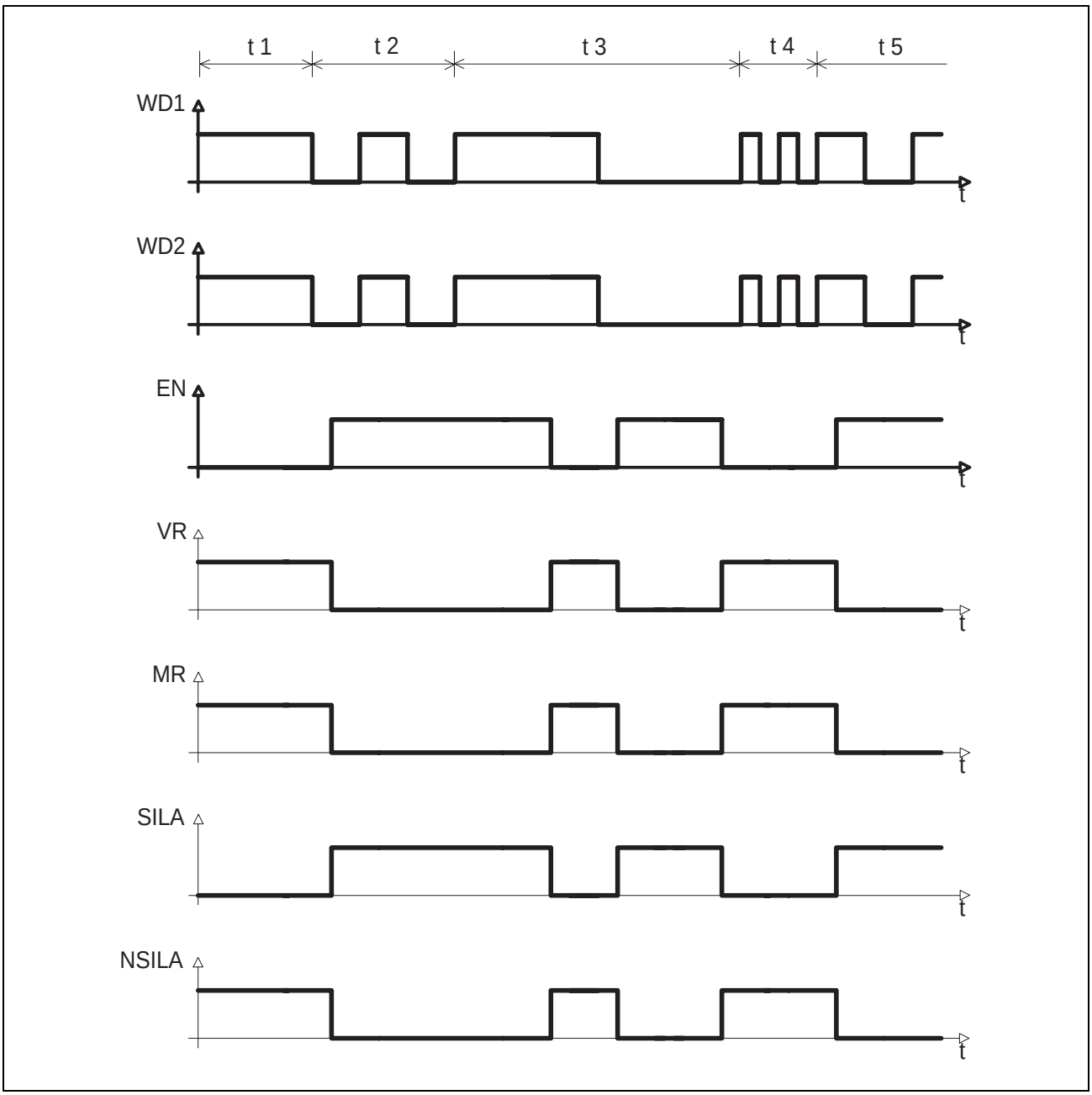


Figure 11 Watchdog Violation Reaction

t_1: No watchdog signals at WD1 or WD2

t_2: Normal operation. EN is going high after the first watchdog edges at WD1 and WD2 are detected.

t_3: Watchdog open window time exceeded: but below 120 *$t_{CLK\ (typ.}$ 120 ms). Error Flag is not set.

t_4: Watchdog time too short (below closed window time)

t_5: Normal operation

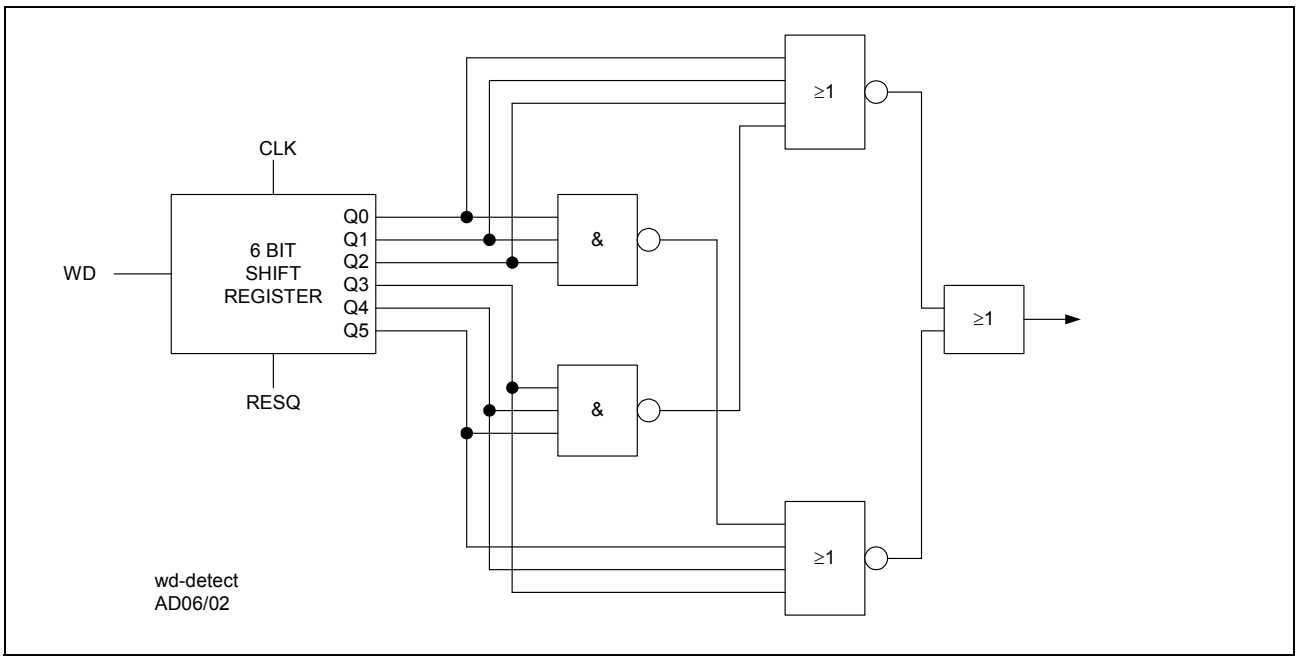


Figure 12 Logic Diagram: Detection of Watchdog Edges.

The watchog signal is clocked through the shiftregister. The output condition of the edge detection circuit above is true for register state 111000 and 000111. 3 clks after the rising edge or falling edge of WDx the logic below will get a pulse of 1 clk length.

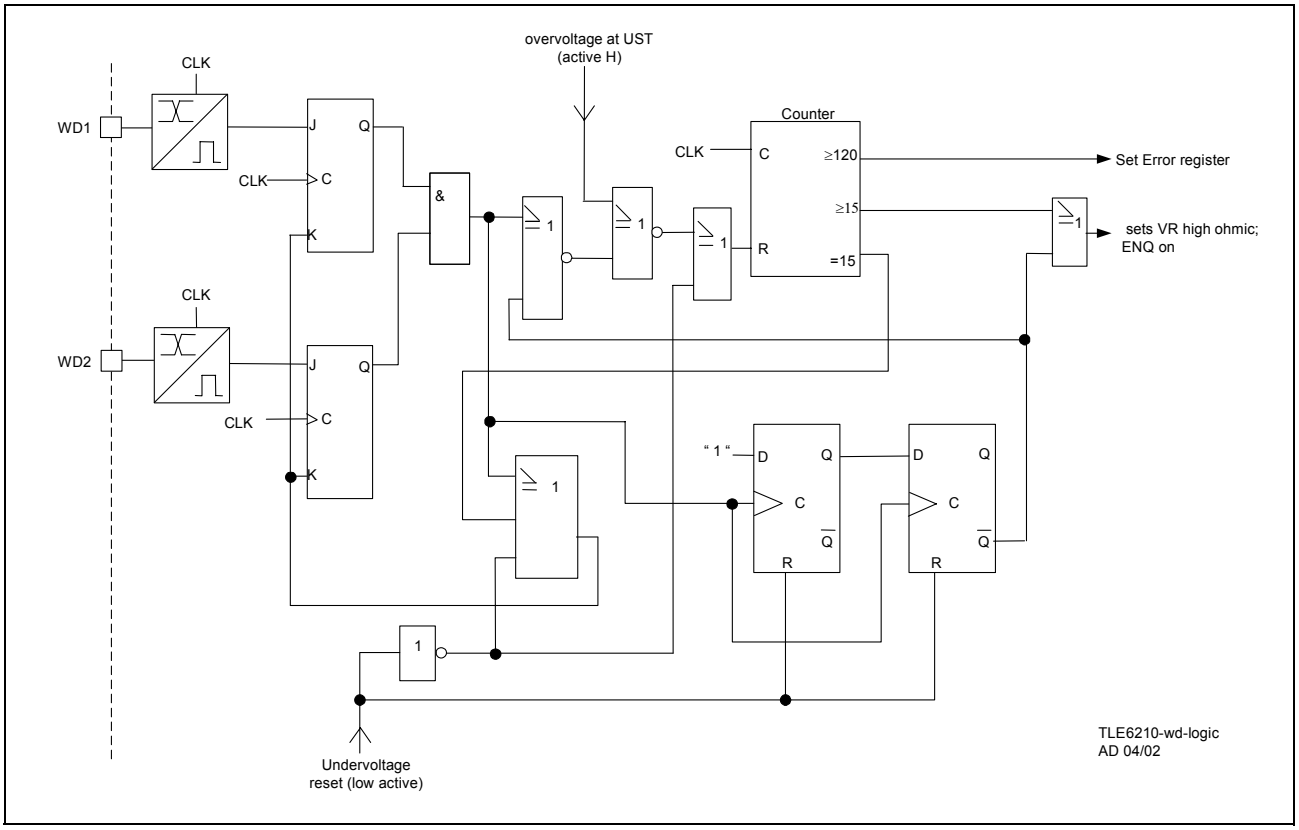


Figure 13 Block Diagram Watchdog Logic

5 Application Diagram

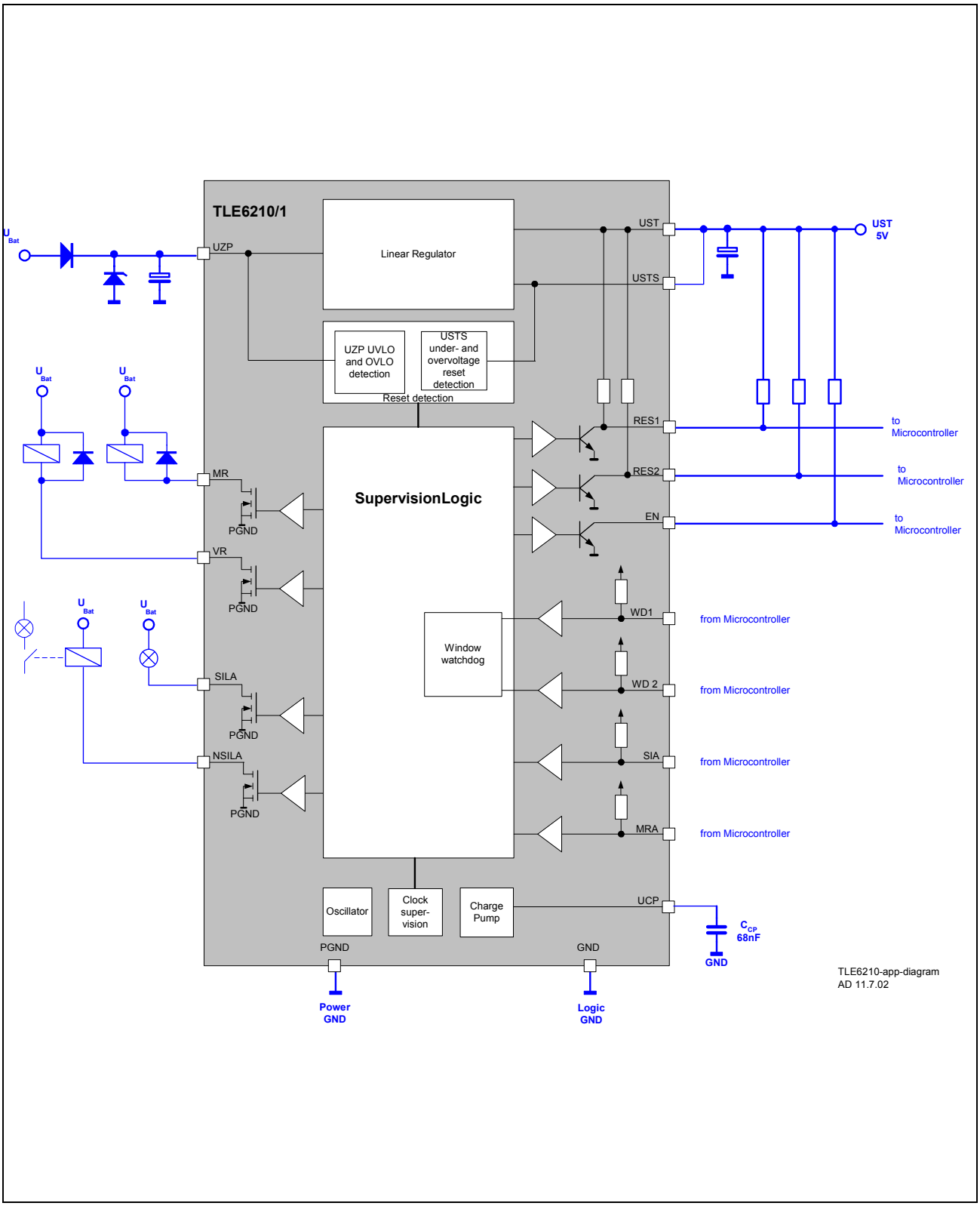
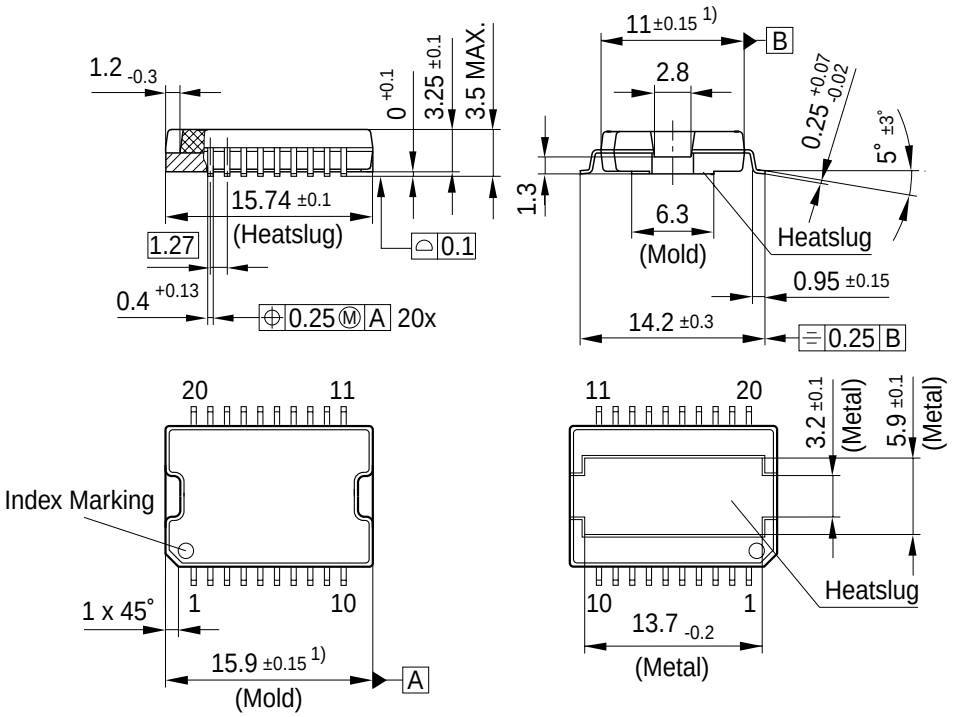


Figure 14 Application Diagram

6 Package Outlines

P-DSO-20-12
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS05791

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm

Version	Date	Major Changes
V0.0	2002-08	Advanced Information Data Sheet TLE 6210, TLE 6211 Device is a replacement of the TLE 5200/TLE 5201 with the following deviations form the specification from 1998-01-21. Devices are only available in the P-DSO-20-12 package or as bare dice The data sheet structure was changed and some chapters where moved. Parameter reference numbers are changed now: • Control input SIA: TLE 5200/01 1.x; TLE 6210/11 4.8.x • Control input MRA: 1.x; 4.7.x • Enable: 2.x; 4.5.x • Reset outputs: 3.x; 4.10.x • SILA/NSILA: 4.x; 4.8.x • VR: 5.x; 4.6.x • MR: 5.x; 4.7.x • Voltage supervision: 6.x; 4.9.x • Oscillator: 7.x; 4.2.x • Watchdog: 8.x; 4.11.x • Charge Pump: 9.x; 4.3.x • 5 V Regulator: 10.x; 4.4.x • General information: 10.x; 4.1.x Absolute Maximum Ratings: Digital I/Os (reference M6, M7, M8) changed to -0.5 to 7 V
V0.1	2001-11	Update truth table
V0.2	2002-04	increase error flag detection time t_{FSP} from 112 clock cycles to 120 clock cycles (parameter 4.11.8) Add of logic block diagram (figure 12) and watchdog timing diagrams (figure 5 to 10)

Revision History

Version	Date	Major Changes
V1.0	2002-07	Data sheet Remove pad / chip information from the datasheet ESD value SILA, MR, VR,UZP 4kV Update typ. value 4.3.3 Extend and correct block description at chapters 4.4; 4.6; 4.7; 4.8 Table 1: SILA function at overtemperature changed Table 2: timings as a function of t_{CLK} Figure 11, t3: corect timing Chapter 4.11: Extend description; add figure 12: Detection of watchdog edges Appplciation diagram: replace free wheeling zener diodes at MR and VR relay by normal diodes.
V1.1	2002-07	change device suffixes: bare dice: TLE621x C packaged: TLE621x G
V1.2	2002-08	Table 1 and text chapter 4.8: correct NSILA at overvoltage Change long term drift 4.4.6 to 10000h Add a more detailed description to figure 12.

Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

Characteristics show the deviation of parameter at the given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

Edition 2002-08

**Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
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